# A 0.8 mm² Sub-GHz GaAs HBT Power Amplifier for 5G Application Achieving 57.5% PAE and 28.5 dBm Maximum Linear Output Power

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**ABSTRACT** This paper presents a comprehensive design of a fully integrated multistage GaAs HBT power amplifier that achieves both linearity and high efficiency within a chip area of 0.855 mm² for 4G and 5G applications covering the lower frequency band of 700-800 MHz. A novel linearizer circuit is integrated to a dual stage class-AB PA to minimize the AM-PM (Amplitude Modulation-Phase Modulation) distortion generated by the parasitic capacitance at the PN-junction under low bias current condition. The linearized power amplifier is able to operate within a 100 MHz linear operating bandwidth (700-800 MHz) while meeting the adjacent channel leakage ratio (ACLR) specification for 4G and 5G application. The fully integrated PA achieves a wideband efficiency of 57.5% at 28.5 dBm output power. Observing a respective input and output return losses of less than 13 dB and 10 dB, the PA delivers a power gain within the range of 34.0-37.0 dB across the operating bandwidth while exhibiting an unconditional stability characteristic from DC up to 5 GHz. The proposed linearization method paves the way of reducing the complexity of linear and high efficiency PA design which is associated with complicated and high-power consumption linearization schemes.

**INDEX TERMS** Power amplifier, analog pre-distorter (APD), linearizer, Gallium–Arsenide (GaAs), hetero-junction bipolar transistor (HBT), multi stage, power added efficiency (PAE), phase, 4G, 5G, sub-GHz.

## I. INTRODUCTION

As the demand for high data rate, low latency and reliable wireless communication increases globally, extensive efforts have been taken in the standardization of the 4G and future 5G mobile systems which include newer frequency bands [1]. The lower frequency band in the region of 700-800 MHz is favorable for wider communication coverage which is inherited by its large wavelength characteristics [2]. The aim of transmitting large amounts of data is achievable through the implementation of advance and complex modulation techniques such as Orthogonal Division Frequency Multiplexing (ODFM) and Multiple Input Multiple Output (MIMO)

OFDM [3]–[8]. The ODFM/MIMO OFDM wireless systems which is realized using Fast Fourier Transform (FFT) technique, provides great immunity to fading in an instantaneous multipath signal environment [9]. However, high peak-to-average power ratio (PAPR) of the transmit signal degrades the system performance due to the nonlinear intermodulation distortions (IMD3) contributed by the Power Amplifier (PA). This imposes a serious challenge for the PA designer to meet both linearity and efficiency performances since high linearity is achieved at lower power whereas efficiency is highest at the peak power [10]–[15].

The linear power is measured in terms of Adjacent Channel Leakage Power Ratio (ACLR). For example, if the signal's PAPR is 7 dB, PA's maximum output power must be 35 dBm

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in order to meet the ACLR specification at output power of 28 dBm. This degrades its efficiency, $\eta$ as the relationship between backed off output power and efficiency are expressed as [16]:

For Class-A PA, efficiency is given by

$$\eta_{pbo-classA} = \frac{1}{2} \cdot \frac{P_{bo}}{P_{max}} \qquad (1)$$

For Class-B PA, efficiency is given by

$$\eta_{pbo-classB} = \frac{\pi}{4} \cdot \sqrt{\frac{P_{bo}}{P_{max}}} \qquad (2)$$

where $P_{bo}$ and $P_{max}$ represent backed off output power and maximum output power level respectively. For example, if a PA is transmitting WCDMA signal with PAPR of 7 dB, the resultant efficiency at $P_{bo}$ of 28 dBm ($P_{max} = 35$ dBm) is 9.9% and 35% in the event the PA is operating in class-A or class-B mode respectively. These values are not favorable for battery operated mobile devices.

The efficiency of the amplifier can be optimized through the waveform shaping of the voltage and current by minimizing the overlap between the two waveforms. This will reduce the power dissipation in the transistor [17]. Additional factor that causes efficiency degradation is the mismatch in the fundamental, 2nd harmonic and 3rd harmonic reactance due to highly volatile narrowband matching. Hence, extensive output matching optimization is required to achieve optimum performances.

The solution to improve $\eta$ at backed off output power is either to reduce the back-off level by reducing the $P_{max}$ (smaller device size) or to introduce efficiency enhancement techniques. Reducing the backed off level will result the PA to fail ACLR specifications. Therefore, linearization techniques need to be implemented to curb this issue. As it implies, efficiency enhancement techniques regulate in improving the efficiency of a linear PA, whereas linearization techniques improve the linearity of a highly efficient non-linear PA.

The dynamic bias configuration is one of the efficiency enhancement techniques implied to improve the PAE at backed off output power [18], [19], where an integrated detector is used to track the envelope of the RF input signal and varies the bias point of the PA accordingly. The adaptation of the highlighted integration at low output power results in a low current consumption that in turn improves the PAE. Research work has also prioritized in improving the inter-stage matching network between the driver and main amplifier to determine the optimum trade-off between linearity and PAE [20]. However, it is a challenging task in adapting this technique for multiband operation, where usually the optimum trade-off falls to be narrow band. An alternative solution is the implementation of transistor resizing technique to further enhance the efficiency and linearity at the average low power region [20]. The proposed method requires complex two-chip solution which is not favorable for low cost mass implementation. In the effort to reduce the cost, implementing the PA on a CMOS platform has

been explored [22], [23]. The Floating Bulk technique is introduced to minimize the power losses and enhance the PAE of the cascode Class-E power amplifier [24]. The proposed method is limited to cascode PA topology and exhibits narrowband characteristics.

Independent harmonic control circuit using the characteristic of a quarter-wavelength microstrip line has been proposed as matching element to achieve high efficiency performance in [25]. Peak output power of 47.2 dBm, drain efficiency of 70.2% and power gain of 10.2 dB was achieved at 5.8 GHz using GaN HEMT. However, performance is limited to narrowband.

Recently, envelope tracking power amplifier (ETPA) is continuously gaining popularity to improve the efficiency of linear PA. This technique utilizes the supply modulation method where the supply voltage of the PA is modulated respective to the RF input drive voltage while sustaining a constant load resistance. As a result, the efficiency at low output power increases. However, the stringent requirement in the linear output power favors GaAs HBT as the PA instead of other technologies [26]. Therefore, to fully realize ETPA, dual chip solution is often required, which serves to be a burden in context of cost, complexity and size. Linear ET PA with simple correction circuit (SCC) is proposed in [27], whereby the AM-AM and AM-PM nonlinearity which is contributed by supply voltage is minimized. However, the efficiency achieved is on the lower side due to low breakdown voltage of CMOS process.

In order to curb the disadvantages, attempt on single chip implementation using SiGe BiCMOS process [28] and fully CMOS process [29], [30] has been explored. Efficiency and linearity using CMOS process is inferior due to the higher substrate losses and low breakdown voltage [31]. Among the critical component is the inductor where high quality on-chip inductors are preferred for high frequency operation for RFIC solution in CMOS [32], [33]. An un-even bias scheme, which consists of a programmable gain amplifier biased at Class C and a power stage biased at Class AB is able to improve the efficiency and linearity of the CMOS PA in low power operating region [34]. However, the resulting linear output power is still low as compared to GaAs HBT.

On the other hand, the analog pre-distortion (APD) and digital re-distortion (DPD) techniques focuses in improving the linear output power of non-liner PA. In both methods, a signal pre-distorter is placed at the input of the PA to alter the non-linear transfer function's magnitude and phase of the PA. The difference between APD and DPD lies in the design of the pre-distorter where the latter generates the aforementioned non-linear responses with the aid of a DSP processor [35]–[38]. However, the complexity in integration, resulting in larger chip area and dual fabrication process serves to be the prime disadvantages. The DPD chip which uses a high-speed DAC (Digital to Analog Converter) has been implemented with DSP/FPGA chips on CMOS process, while the PA has been designed on an HBT process. Hence this function is implemented utilizing two different chips.
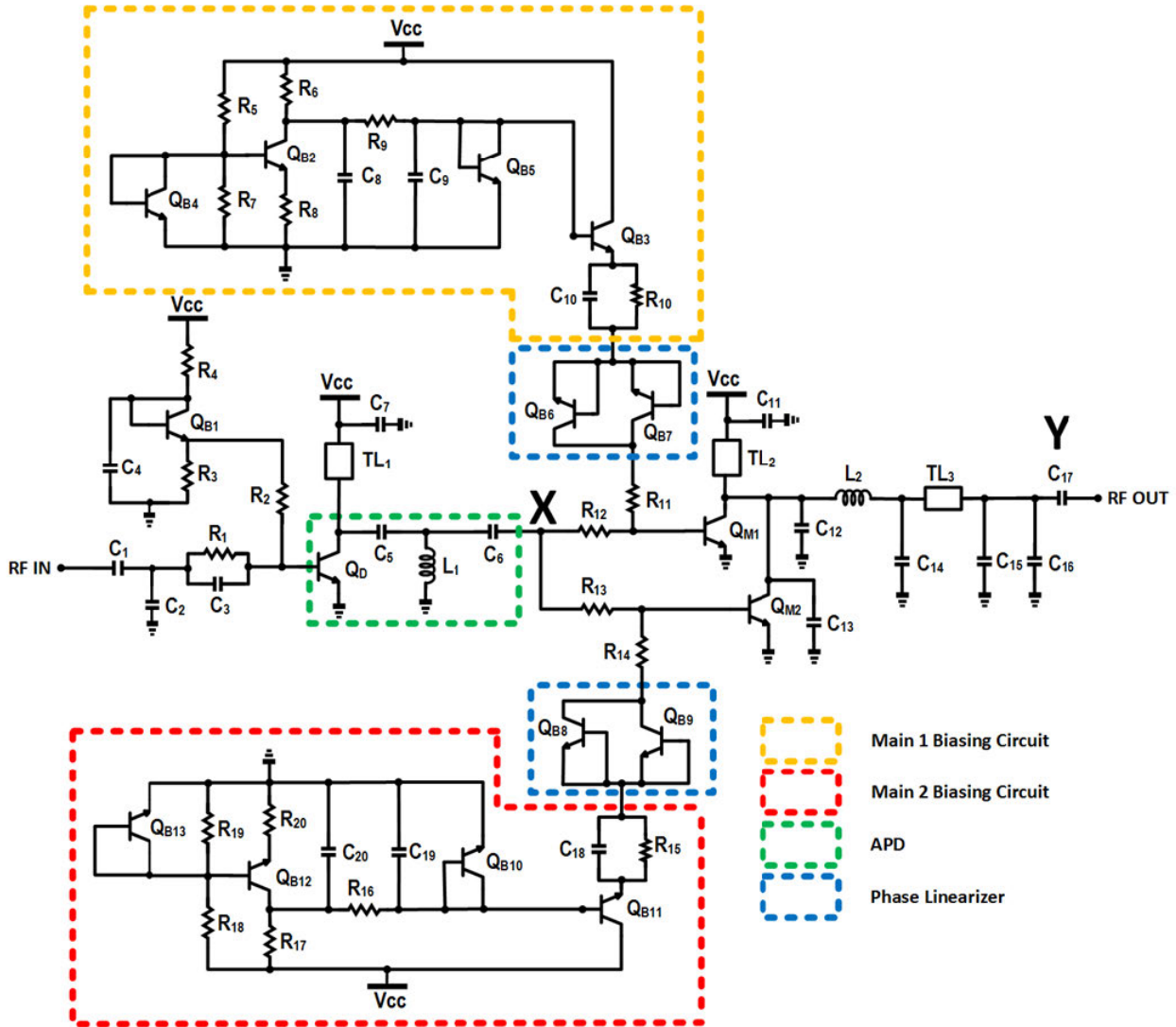
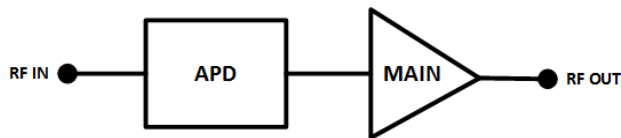**FIGURE 1.** Schematic diagram of the proposed PA.



**FIGURE 2.** IMD3 cancellation analysis.

In contrary, APD offers a simple solution of integrating additional active devices, usually within the same process at the input of the power amplifier [39]–[43]. Passive elements are alternately utilized as a pre-distorter, to linearize a non-linear class-E PA [44]. In [45], APD is introduced at the input matching network to enable optimum third order nonlinear cancellation in order to improve the OIP3 of a Quarter Watt gain block amplifier. The proposed circuit technique is limited for lower power applications and ineffective to improve the linearity at higher or peak power levels.

In this paper, a novel technique is introduced to improve the linearity of a PA at reduced back off level by integrating an analog pre-distorter and phase linearizer block at the input of a class-AB amplifier. The integrated solution minimizes the phase distortion which arises due to the parasitic capacitance of the HBT PN-junction. In this single chip solution, the total chip area consumption is 0.85 mm$^2$.The outline of this work is organized as follows. In Section 2, the design of high power and high efficiency PA is explained. The design methodology and theory of operation of the Analog Pre-Distorter and phase linearization is elaborated in Section 3, while Section 4 highlights the validation result of the PA. Finally, the conclusion is drawn in Section 5.

## II. HIGH POWER AND HIGH EFFICIENCY PA DESIGN

Fig. 1 illustrates the schematic of the proposed LTE PA. The PA consists of 3 blocks, which are the APD, phase linearizer and two parallel connected main amplifiers. Each main
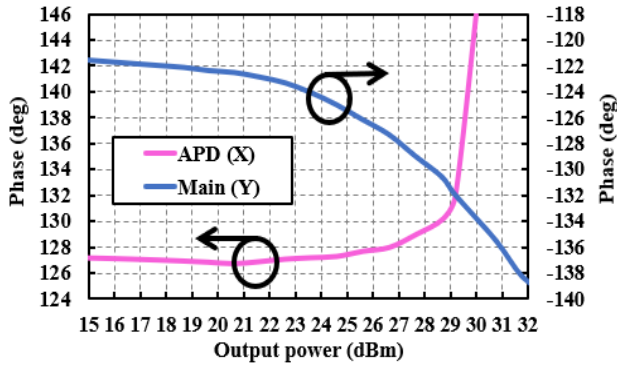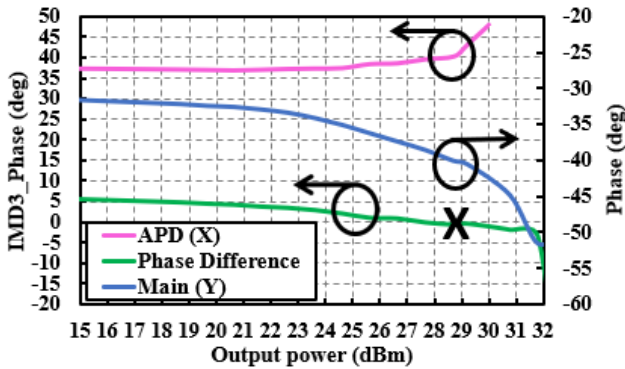
(a). Simulated AM-PM response of the main amplifier and APD at 750 MHz.
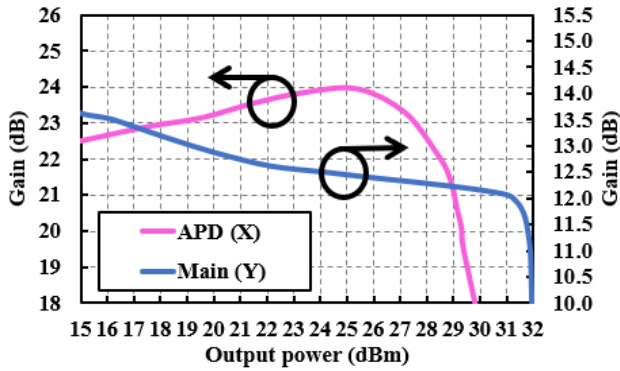


(b). Simulated AM-AM response of the main amplifier and APD at 750 MHz.

**FIGURE 3.** (a) Simulated AM-PM response of the main amplifier and APD at 750 MHz. (b). Simulated AM-AM response of the main amplifier and APD at 750 MHz.
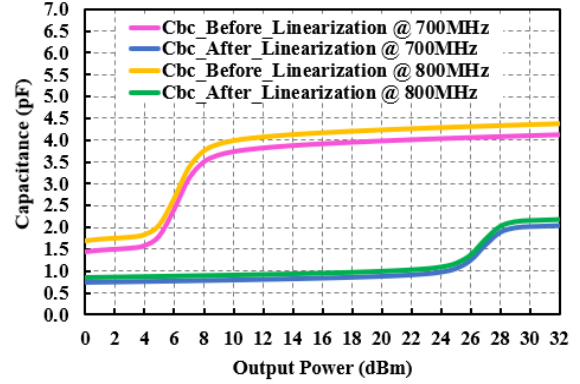


**FIGURE 4.** Simulated IMD3 response of the main amplifier and APD at 750 MHz.



**FIGURE 5.** $C_{bc}$ response before and after linearization at 700 MHz and 800 MHz.

delivers maximum output power. The width, w of $TL_1$, $TL_2$ and $TL_3$ are determined from (3) to (5):

$$Z_T = \frac{377}{\sqrt{\varepsilon_{eff}}} \left[ \frac{w}{d} + 1.98 \left( \frac{w}{d} \right)^{0.172} \right]^{-1} \quad (3)$$

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \left[ 1 + \frac{1}{\sqrt{1 + \frac{10d}{w}}} \right] \quad (4)$$

$$Z_T = \sqrt{Z_L Z_{out}} \quad (5)$$

where $Z_L$ is equals to 50 Ω, $Z_{out}$ is the output impedance of the main amplifier, $\varepsilon_r$ is the dielectric constant of the GaAs substrate and $d$ represents the substrate thickness. To determine the output matching's capacitor value:

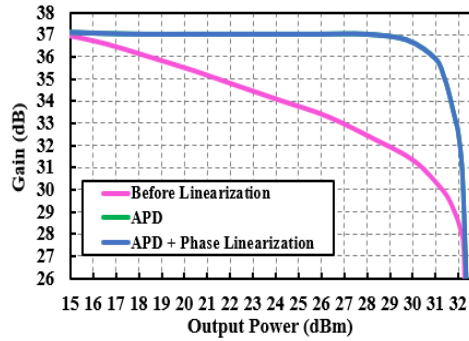$$C_{T1}, C_{T2} = \frac{1}{Z_T \omega} \sqrt{\frac{1 - cos\theta}{1 + cos\theta}} \quad (6)$$

where,

$$C_{T1} = C_{14} \quad (7)$$
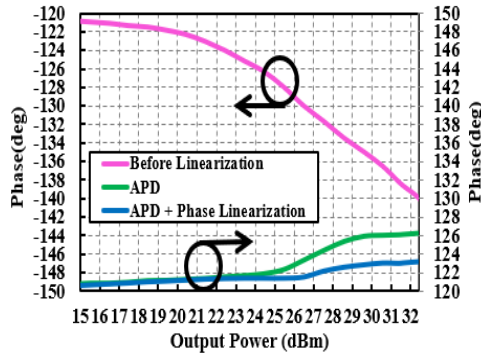$$C_{T2} = C_{15}//C_{16} \quad (8)$$

A parallel combination of $C_{15}$ and $C_{16}$ is desired to reduce the Equivalent Series Resistance (ESR) inherited in the capacitor.
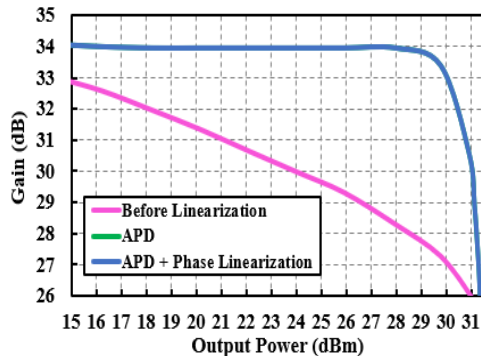
### B. BIAS CIRCUIT DESIGN
In order to provide a stable biasing platform for the main amplifiers, a base-voltage stabilizer architecture is proposed to bias them up as shown in Fig. 1. In this bias configuration, an increase in the $V_{be}$ of the transistor $Q_{B2}/Q_{B12}$ due to the variations in supply voltage $V_{CC}$ is compensated by the voltage drop across the resistor, $R_6/R_{17}$. Hence, the voltage delivered to the base-emitter junction of $Q_{B3}/Q_{B11}$ becomes insensitive to the changes in the input current of $Q_{B2}/Q_{B12}$. This circuit therefore provides a stable biasing condition for the both main amplifiers $Q_{M1}$ and $Q_{M2}.Q_{B2}/Q_{B12}$ is biased through a voltage division network of resistor $R_5/R_{18}$ and $R_7/R_{19}$. The dependency of $Q_{B2}/Q_{B12}$ to $V_{be}$ due to its collector current is reduced by integrating the voltage degeneration resistor, $R_8/R_{20}.Q_{B4}/Q_{B13}$ and $Q_{B5}/Q_{B10}$ serve to be diodes

amplifier has its own phase linearizer circuit to reduce the phase distortion. Both main amplifiers are biased in deep class-AB mode. Parallel base ballast resistor and capacitor, RC is used for electrical and thermal stability.

### A. OUTPUT MATCHING NETWORK DESIGN
Referring to Fig. 1, $C_{12}$ and $C_{13}$ are the second harmonic termination components. The PI network, which consists of Transmission line $TL_3$, $C_{14}$, $C_{15}$ and $C_{16}$, ensures the PA

(a). Simulated AM-AM profile at 700 MHz.



(b). Simulated AM-PM profile at 700 MHz.



(c). Simulated AM-AM profile at 800 MHz.



(d). Simulated AM-PM profile at 800 MHz.

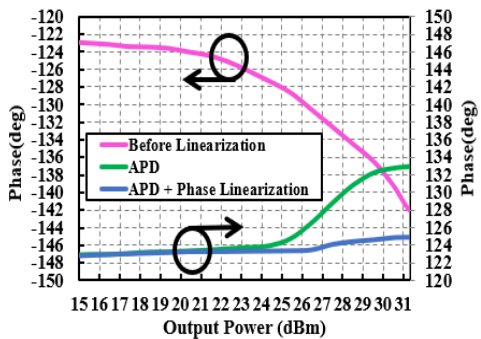**FIGURE 6.** (a) Simulated AM-AM profile at 700 MHz. (b). Simulated AM-PM profile at 700 MHz. (c). Simulated AM-AM profile at 800 MHz. (d). Simulated AM-PM profile at 800 MHz.

outlining a consistent biasing profile across different temperature condition. $R_9/R_{16}$, $C_8/C_{20}$ and $C_9/C_{19}$ acts as a low pass filter to protect the biasing circuit from the influence of higher frequency components.



(a)



(b)
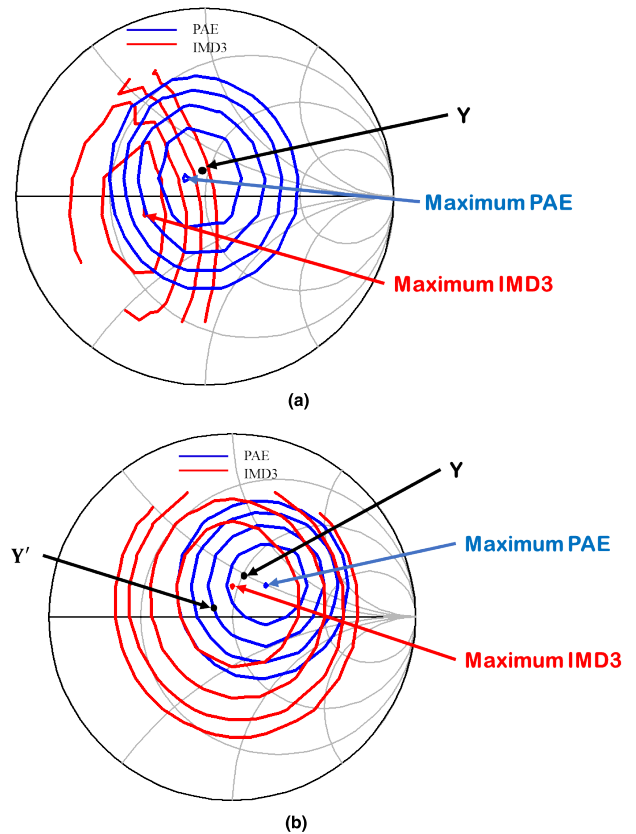
**FIGURE 7.** Load pull simulation result of the PA at output power of 28 dBm. (a) The IMD3 and PAE contour before linearization (b) IMD3 and PAE contour after linearization. The PAE contour is plotted in 1% step whereas the IMD3 contour is plotted in 2dB step.

## III. LINEARIZATION SCHEME

The low supply voltage headroom of the main amplifier tends to result in an early gain compression much earlier from maximum saturated power. This is due to the rise of the third order intermodulation distortion (IMD3) component as the output power increases, thus significantly degrading the ACLR performance [46]. The APD linearization scheme is only able to resolve this issue for narrowband. This is due to the sensitivity in the AM-PM cancellation. Albeit narrowband, it's a preferred solution for its low cost. To improve the APD performance, an additional phase linearizer is added after the APD system to minimize the phase distortion across bandwidth. This is illustrated in Fig. 1. The principle of operation of the proposed linearization scheme is explained below.

### A. ANALOG PRE-DISTORTION LINEARIZER
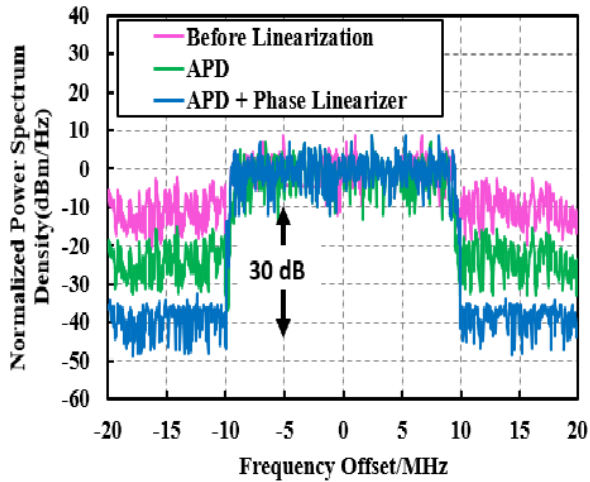
The APD operation can be explained with the aid of the following analysis that utilizes power series.

The general form of power series for the Analog Pre-Distorter (APD) architecture described in Fig. 2 is given from (9) to (15).

### B. INTERMEDIATE MATCHING NETWORK DESIGN

The T network in the APD, which consist of $C_5$, $L_1$ and $C_6$ in Fig. 1 is used to generate the opposite AM-AM and

(a). Simulated spectrum mask profile before linearization, with APD and with APD + Phase Linearizer at 700 MHz.
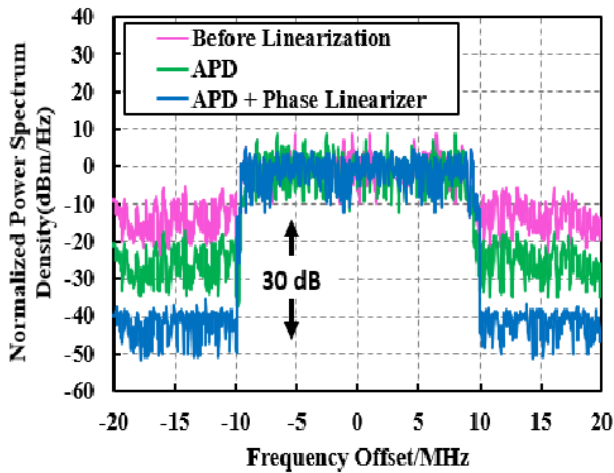


(b). Simulated spectrum mask profile before linearization, with APD and with APD + Phase Linearizer at 800 MHz

**FIGURE 8.** (a). Simulated spectrum mask profile before linearization, with APD and with APD + Phase Linearizer at 700 MHz. (b). Simulated spectrum mask profile before linearization, with APD and with APD + Phase Linearizer at 800 MHz.

AM-PM response. Driver size $Q_D$ and $TL_1$ ensures more than 20 dB gain is delivered. Fig. 3(a) illustrates AM-PM response of the main amplifier and APD, whereas Fig. 3(b) depicts the AM-AM response of the main amplifier and APD across corresponding output power. The phase response of the APD refers to location X whereas the phase response of the main amplifier refers to location Y in Fig. 1.

$$v_o = G'_{v0} + G'_{v1}v_{PD} + G'_{v2}v_{PD}^2 + G'_{v3}v_{PD}^3 + G'_{v4}v_{PD}^4$$
$$+ G'_{v5}v_{PD}^5 + \dots \quad (9)$$

$$v_{PD} = M_0 + M_1 v_i + M_2 v_i^2 + M_3 v_i^3 + M_4 v_i^4 + M_5 v_i^5 + \dots \quad (10)$$

whereby $G'_v$ and $M$ denotes the gain of the PA and APD respectively.
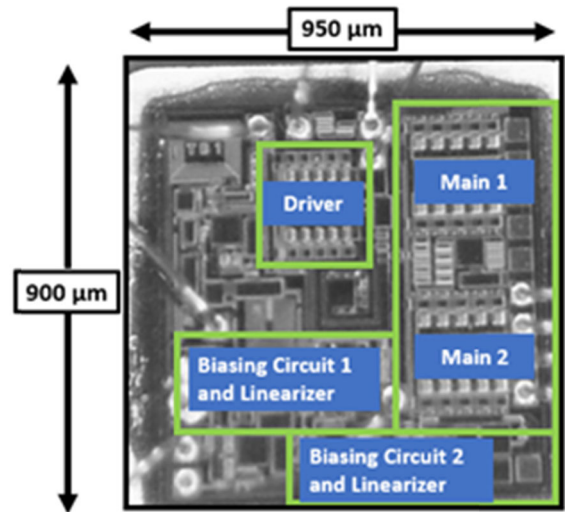


**FIGURE 9.** Photomicrograph of the fabricated PA.
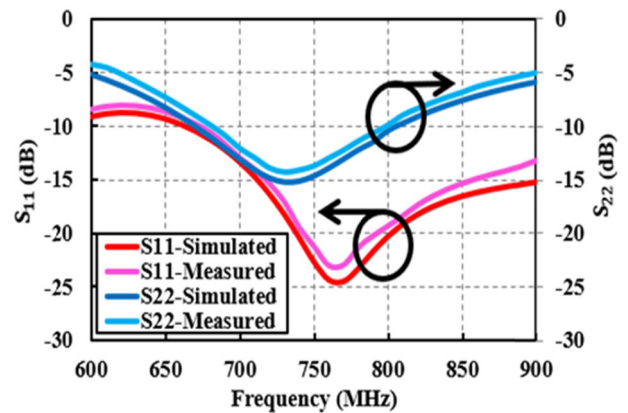


(a). Simulated and measured $S_{11}$ and $S_{22}$ of the PA with a supply voltage of 3.3 V.
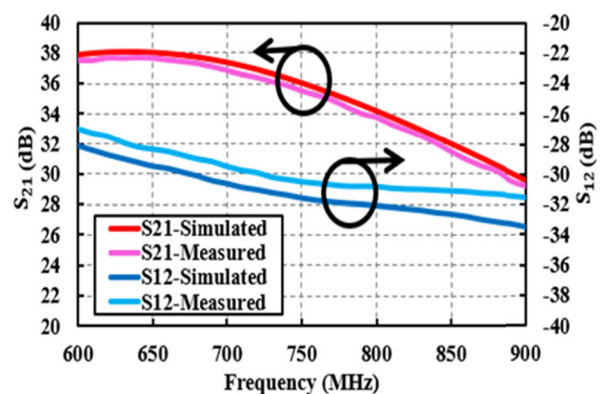


(b). Simulated and measured $S_{21}$ and $S_{12}$ of the PA with a supply voltage of 3.3 V.

**FIGURE 10.** (a). Simulated and measured $S_{11}$ and $S_{22}$ of the PA with a supply voltage of 3.3 V. (b). Simulated and measured $S_{21}$ and $S_{12}$ of the PA with a supply voltage of 3.3 V.

Taking the fundamental and the third order components into the analysis:

$$v_o = G'_{v1}\left[M_1 v_i + M_3 v_i^3\right] + G'_{v3}\left[M_1 v_i + M_3 v_i^3\right]^3 \quad (11)$$

**FIGURE 11.** PA has K-Factor >1 from DC up to 5 GHz.



(a). Simulated and measured gain at 700 MHz.



(b). Simulated and measured gain at 750 MHz



(c). Simulated and measured gain at 800 MHz.

**FIGURE 12.** (a). Simulated and measured gain at 700 MHz. (b). Simulated and measured gain at 750 MHz. (c). Simulated and measured gain at 800 MHz.

(11) is further elaborated:

$$v_o = G'_{v1}M_1 v_i + \left[ G'_{v1}M_3 + G'_{v3}M_1^3 \right] v_i^3$$

$$+ G'_{v3}M_3[3M_1^2 v_i^5 + M_1 M_3 v_i^6$$

$$+ 2M_1 M_3 v_i^7 + M_3^2 v_i^8] \quad (12)$$
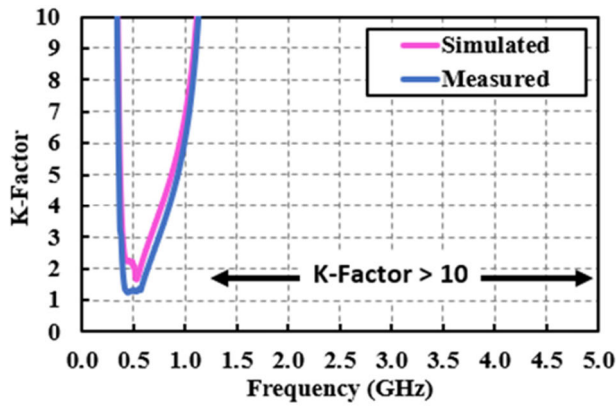
Cancellation of the source of IMD3 which is the third order component in (12),

$$v_o = G'_{v1}M_3 + G'_{v3}M_1^3 = 0 \quad (13)$$

$$M_3 = \frac{-G'_{v3}M_1^3}{G'_{v1}} \quad (14)$$

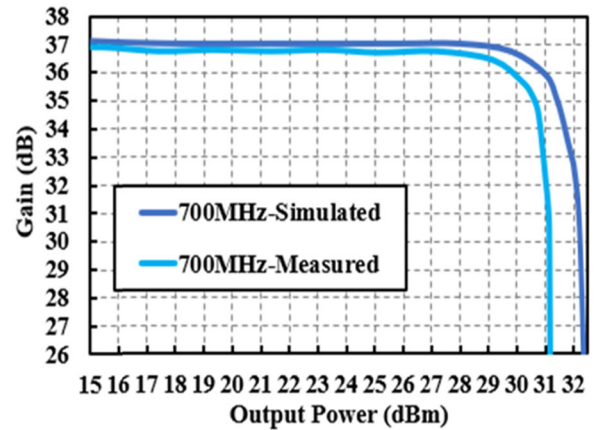(14) is further normalized in terms of the first order linear gain, $G'_{v1}/M_1^3$:

$$M_3 = -G'_{v3} \quad (15)$$

(15) [47] shows that the APD needs to generate third order component which has an opposite response respective to the third order component generated by the main amplifier to suppress the spectral growth. The cancellation can be achieved if the APD generates an opposite response to the main amplifier's response across its fundamental output power [48], [49]. This is characterized in terms of AM-AM and AM-PM response of the system.

With reference to Fig. 3(a) and 3(b), the APD and main amplifier indeed exhibit opposite amplitude and phase response with optimum cancellation at output power of 28.5 to 29.2 dBm whereby the phase differences is close to 0°. The IMD3 phase plot is shown in Fig. 4, depicting the optimum cancellation as described in [47].

Additionally, Fig. 5 illustrates the $C_{bc}$ improvement contributed by the proposed linearization scheme at 700 MHz and 800 MHz.

$C_5$, $L_1$ and $C_6$ are InterStage Matching Network implemented using the $\pi$ network topology. These components are essential to define the AM-AM and AM-PM characteristics

of the APD. The values of $C_5$, $L_1$ and $C_6$ are determined from the following equations:

$$C_5 = \left( \omega_0 R_1 \sqrt{N-1} \right)^{-1} \quad (16)$$
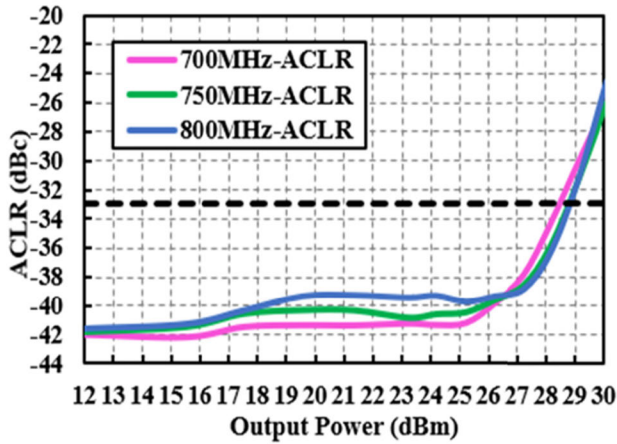
FIGURE 13. Measured ACLR plot across output power.
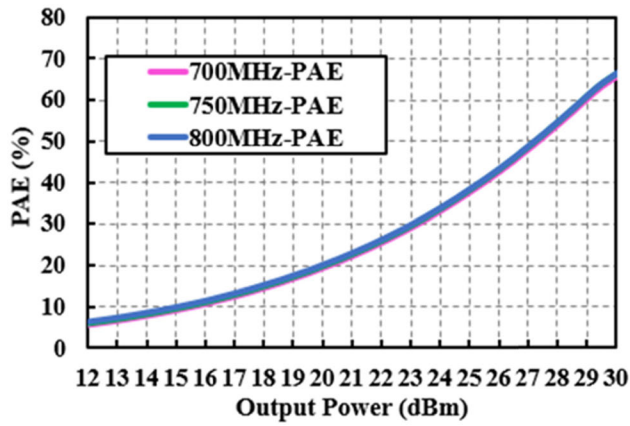


FIGURE 14. Measured PAE across output power.
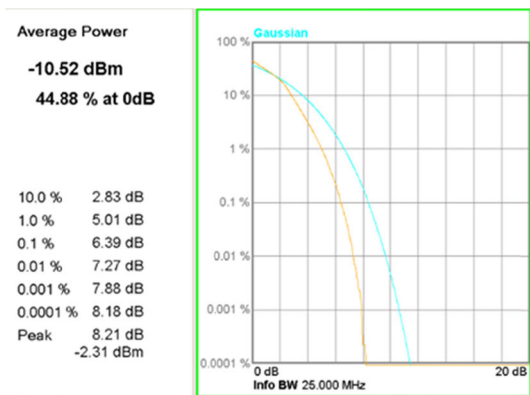


FIGURE 15. PAPR of 20MHz LTE 16 QAM signal.



FIGURE 16. Measured spectrum plot at 750 MHz.
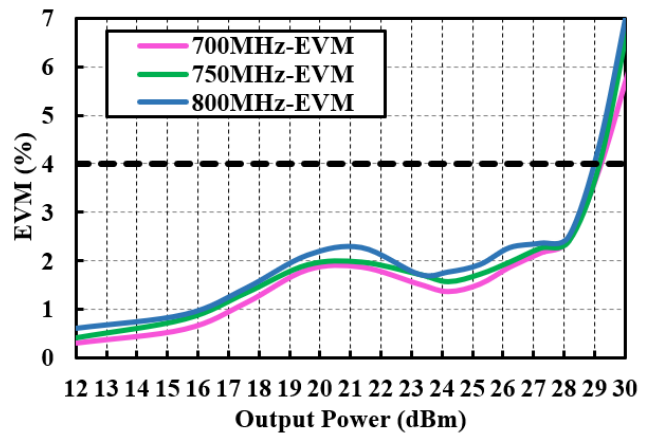


FIGURE 17. Measured EVM plot across output power.
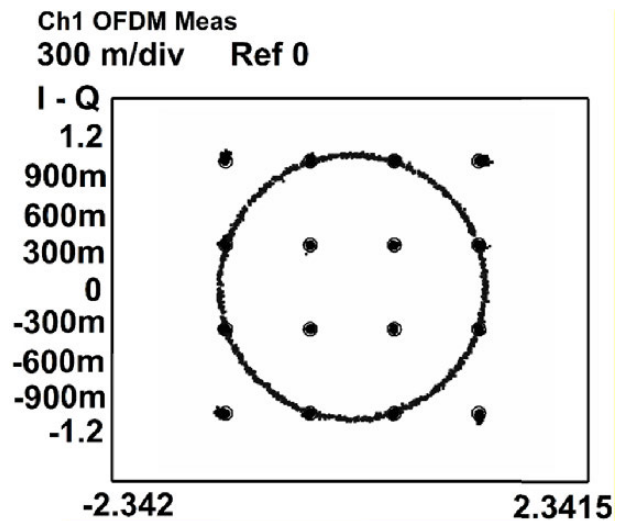


FIGURE 18. Measured EVM constellation plot at 28.5dBm at 750MHz.

$$L_1 = \frac{NR_1}{\omega_0 \left( \sqrt{N-1} + \sqrt{\frac{N}{M} - 1} \right)} \quad (17)$$

$$C_6 = \left( \omega_0 R_2 \sqrt{\frac{N}{M} - 1} \right)^{-1} \quad (18)$$

$$M = \frac{R_2}{R_1} \quad (19)$$

where $\omega_o$ is the operating frequency, $R_1$ is the load resistance of amplifier $Q_D$, $R_2$ is the input resistance of the main amplifiers ($Q_{M1}$ and $Q_{M2}$) and $N = 1.2$ is a constant.

## C. LINEARIZER CIRCUIT DESIGN

The spectral re-growth in HBT is mainly contributed by its base-collector parasitic capacitance $C_{bc}$ [50], [51]. In order to reduce the growth catering for linear transmission, this work proposes the utilization of base-collector diodes. The reverse bias capacitance $C_{bc-reversebias}$ present in an HBT transistor is expressed as follows [52]:

$$C_{bc-reversebias} = \frac{C_{bc0}}{\left(1 + \frac{V_{CB}}{\phi_0}\right)^{n_c}} \qquad (20)$$

where $C_{bco}$ is the collector-base capacitance when $V_{cb} = 0$, $\phi_0$ is the collector-base junction built in voltage and $n_c$ is the grading coefficient of the collector-base junction. If the collector-base junction is forward biased, an opposite output phase response as compared to reverse bias profile is generated. The forward biased collector-base capacitance, $C_{bc-forwardbias}$ for HBT transistor is represented as:

$$C_{bc-forwardbias} = \frac{C_{bc0}}{\left(1 - \frac{V_{CB}}{\phi_0}\right)^{n_c}} \qquad (21)$$

Therefore, to minimize the phase distortion, forward biased base-collector diodes are integrated at the base of the main amplifier.

In order to ensure an optimum linearization takes place, the final stage main amplifier has been split into two devices and be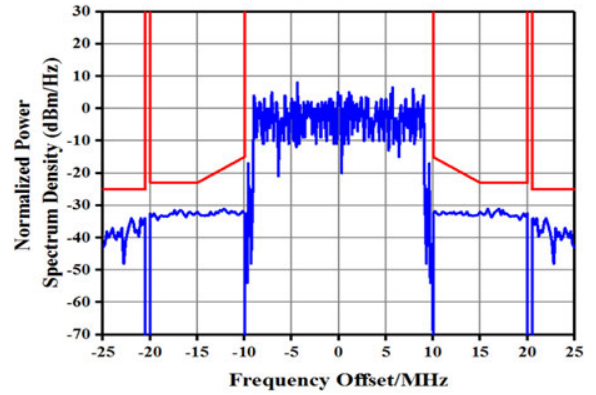en incorporated with individual phase linearizer as depicted in Fig. 1. The improvement achieved through the APD and linearization scheme is represented in the Amplitude-Amplitude (AM-AM) and Amplitude-Phase (AM-PM) modulation results as illustrated in Fig. 6(a) - 6 (d). Fig. 6(a) and 6(c) describes the AM-AM response characteristics prior to APD linearization and with the implementation of the APD and Phase Linearization, whereas Fig. 6(b) and 6(d) describes the AM-PM characteristics. Referring to Fig. 6(a) and Fig. 6(c), the AM-AM responses improves with the amplitude linearization which is incorporated with the APD scheme. However, the AM-AM response does not vary with implementation of the Phase Linearization circuity.

The purpose of phase linearizer is to ensure linearity specification is achieved across 700 to 800 MHz which encapsulates LTE Band 12, 13, 14, 17, 20, 27, 28, 29, 44, 67, 68 and 85 and 5G Band which is n28. As quantified in [53], an AM-PM distortion of 5° or more results in gain compression degradation of 1 dB or more. The effectiveness of the linearizer is verified through the AM-PM profile as represented in Fig. 6(b) and Fig. 6(d) which exhibits a phase deviation of around 2° at 700 and 800 MHz. In order to confirm an effective APD process takes place, a load pull simulation has been performed as shown in Fig. 7. With reference to location Y in the schematic in Fig. 1, the location of the impedance for both optimum IMD3 point and optimum PAE point with respect to location Y in the Smith chart is analyzed. Prior linearization, the optimum IMD3 contour is located almost 8 dB

**TABLE 1.** Performance summary of the PA.

| Results | |
|---|---|
| Technology | 2 um InGaP/GaAs HBT |
| Supply voltage | 3.3 V |
| Frequency | 700-800 MHz |
| Mode | Multiband LTE (Band 12, 13, 14, 17, 20, 27, 28, 29, 44, 67, 68 and 85) 5G (Band n28) |
| Max Linear output Power @ ACLR -33 dBc (tested using LTE 16QAM 20MHz signal, PAPR 8.21 dB) | 28.5 dBm |
| PAE | 57.5% |
| Gain | Min: 33.6 dB @ 800 MHz Max: 36.7 dB @ 700 MHz |
| S11 | <-13dB (700-800 MHz) |
| S22 | <-10dB (700-800 MHz) |
| Stability | Unconditionally Stable (DC – 5 GHz) |

away from Y, exhibiting the poor linearity of the PA as shown in Figure 7(a). Integration of the proposed linearizer circuit shifts the optimum IMD3 contour to location Y. In addition, the distance between optimum PAE and optimum IMD3 point has been reduced. As illustrated in Fig. 7(a) and (b) load pull contours, the optimum impedance point for IMD3 prior linearization located in the capacitive region whereas the after-linearization takes place, the optimum impedance point moves to the inductive region. This is achieved through optimizing the T matching network in the APD as well as the size of the diodes. The size of the diodes determines the phase of the base-collector capacitances at the optimum impedance in-order to achieve high linearity performances. As described in the load pull contours in Fig. 7(b), $Y'$ shows the linearity improvement achieved with the implementation of only the optimized diode linearization topology, without the APD.

Fig. 8(a) and Fig. 8(b) further confirms and validates the effectiveness of the proposed APD and linearizer through the representation of the Adjacent Channel Leakage Ratio (ACLR) profile prior linearization, with APD only implementation and with APD + Phase linearizer. The side lobes reduce 30 dB after implementation of APD + phase linearizer for both 700 and 800 MHz, as a result of the AM-AM and AM-PM cancellation, thus meeting multiband LTE 4G and 5G specification.

## IV. MEASUREMENT RESULTS

Fig. 9 illustrates the photomicrograph of the proposed PA designed with 2 $\mu$m InGaP/GaAs HBT process. The chip area consumption is 0.855 mm², encapsulating the class-AB main amplifiers, APD and the phase linearizer. The supply voltage headroom of the LTE PA is 3.3 V.

The simulated and measured S-parameters of the proposed PA are shown in Fig. 10(a) and Fig. 10(b). The scattering parameters $S_{11}$ and $S_{22}$ are well matched for 100 MHz bandwidth operation (700-800 MHz), with a gain $S_{21}$ of more than

**TABLE 2.** Performance comparison with recent reported works.

| Work | Operating Frequency [GHz] | Bandwidth (MHz) | Supply Voltage [V] | Gain [dB] | Maximum Linear Output Power [dBm] | Signal | PAPR [dB] | PAE [%] @ max linear power. |
|---|---|---|---|---|---|---|---|---|
| 22 | 1.75 | 300 | 3.4 | 10.0 | 24.2 | WCDMA 3.84 MHz | 3.3 | 30.2 |
| 33 | 2.4 | - | 3.3 | 37.0 | 18.5 | WLAN 64 QAM 20 MHz | - | 14 |
| 54 | 1.9 | 60 | 4.5 | - | 20.0 | WCDMA 3.84 MHz | 3.3 | 40.0 |
| 55 | 0.82-0.92 | 100 | 3.6 | 26.6 | 26 | LTE 16 QAM 10 MHz | 7.5 | 23-25.3 |
| 56 | 0.88 | - | 5.0 | 30.0 | 25.6 | LTE 10 MHz | 8.1 | 18.8 |
| 57 | 1.9 | 10 | 3.6 | - | 23.8 | LTE 16 QAM 10 MHz | 7.5 | 24.0 |
| 58 | 0.8 | 5 | 3.6 | 22.8 | 23.5 | LTE 16 QAM 5 MHz | 7.0 | 43.0 |
| 59 | 1.85 | 10 | 4.0 | 14.2 | 27.5 | LTE 16 QAM 10 MHz | 7.5 | 42.4 |
| This work | 0.7-0.8 | 100 | 3.3 | 34.0-37.0 | 28.5 | LTE 16 QAM 20 MHz | 8.2 | 57.5 |

30 dB across the highlighted band. A low $S_{11}$ betokens the APD does not generate a severe input mismatch loss at the desired operating frequency.

The K-factor plot is illustrated in Fig. 11. From DC up to 5 GHz, the K-Factor is more than 1, which represents an unconditionally stable condition.

The power gain across the output power plot of the PA is shown in Fig. 12(a)-Fig. 12(c), which measures up to a maximum output power of 31.0 dBm, or 1.3 W. The 1dB compression point of the PA is observed to be 29.8 dBm at 750 MHz.

Fig. 13 and Fig. 14 illustrates the corresponding measured ACLR and PAE performances across the operating frequency, where the PA meets the LTE specification of -33 dBc at output power of 28.5 dBm. At maximum linear output power of 28.5 dBm, the PA is able to achieve a PAE of 57.5% across 100 MHz bandwidth.

The PA is tested using the LTE 16QAM signal with bandwidth of 20MHz and PAPR of 8.21 dB. The PAPR of the tested signal is shown in Fig. 15.

The measured spectrum mask plots at maximum linear output power of 28.5 dBm is depicted in Fig. 16, which clearly indicates the performance is within specification.

The EVM performance across output power of the PA is illustrated in Fig. 17. The measured EVM results meet the specifications of below 4.0 % at maximum linear output power which is 28.5 dBm as defined in the LTE 3GPP specification.

The EVM constellation plot is depicted in Fig. 18, whereby the EVM is measured at 2.34 % at 28.5 dBm output power at 750 MHz.

Table 1 tabulates the proposed PA's measured performance summary. In Table 2, the performance comparison of the PA with other recent reported works is presented.

## V. CONCLUSION
A novel linearization methodology for high efficiency sub-GHz power amplifier is presented. The integrated APD and phase linearizer provides a significant improvement in the ACLR at low backed-off output power from the 1dB compression point. This enables the PA to maintain higher efficiency at linear operating region. The proposed linearizer circuit does not jeopardize the input return loss, gain and stability of the PA, which are critical in ensuring an efficient operation of the transmitter. At the output power of 28.5 dBm, PA delivers 57.5% PAE, meeting the ACLR specifications. With a chip area of 0.855 mm², the proposed design that encapsulates 13 sub-GHz operating bands has reduced design cost and saves board space significantly. The results highlight the potential application of the proposed PA in a handset transmitter system, which favors low voltage headroom operation, thus prolonging the battery life.

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