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A Sliding-Mode Controlled Single-Phase Grid-Connected Quasi-Z-Source NPC Inverter With Double-Line Frequency Ripple Suppression

SERTAC BAYHAN[1], (Senior Member, IEEE), AND HASAN KOMURCUGIL[2], (Senior Member, IEEE)
[1]Qatar Environment and Energy Research Institute, Hamad Bin Khalifa University, Doha, Qatar
[2]Department of Computer Engineering, Eastern Mediterranean University, Famagusta, 996628 Mersin, Turkey

Corresponding author: Sertac Bayhan (sbayhan@hbku.edu.qa)

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ABSTRACT In this paper, double-line frequency (2ω) ripple suppression and SMC with time-invariant (fixed) switching frequency methods are proposed for single-phase grid-connected three-level neutral-point-clamped quasi-Z-source inverters. The 2ω ripple suppression method is based on the 180° phase difference existing between the 2ω ripple components of the capacitor and inductor voltages in the dc-side. Hence, when these components are added in the closed-loop, a phase cancellation occurs so that the inductor current reference can be generated without 2ω ripple component. In this case, the actual inductor current, which is forced to track its reference, has no 2ω ripple component. In addition, the grid current control is achieved via sliding mode control (SMC). Unlike the existing SMC methods, the proposed SMC achieves fixed switching frequency which is made possible by eliminating the discontinuities in the sliding surface function using a boundary layer. The proposed ripple suppression method together with the SMC method offers many advantages such as fast dynamic response, zero grid current error, simple implementation, robustness to parameter variations and fixed switching frequency. The effectiveness of the proposed control method is verified experimentally under steady-state and transient conditions.

INDEX TERMS Neutral-point clamped (NPC) inverter, quasi-Z-source network, sliding mode control (SMC), proportional-resonant (PR) control.

I. INTRODUCTION

Voltage source inverters are widely utilized in grid-connected systems for injecting power obtained from renewable energy sources (e.g. fuel cells, solar energy, wind energy, etc.) into the grid. Although traditional two-level (2L) inverters offer satisfactory performance regarding the steady-state and dynamic responses, their performance may be degraded in high-power applications leading to high voltage stress and waveform distortions which affect the overall efficiency. In the last two decades, multilevel inverters (MIs) have received considerable attention from the researchers and industry due to their prominent features such as high efficiency, excellent harmonic performance, high reliability, low semiconductor voltage stress and ability to work with low switching frequency [1]–[4]. The effort of the researchers and industry has led to rapid development of different multilevel inverter topologies such as cascaded multilevel [3], neutral point clamped (NPC) [4], flying capacitor (FC) [5] and Packed-U-Cell (PUC) [6] inverters. Even though MIs offer many advantages, they suffer from major drawbacks such as the implementation complexity and high cost due to the high number of switches, capacitors, and diodes employed in a typical n-level inverter.

On the other hand, alternative inverter topologies such as Z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) are also proposed to be utilized in grid-connected systems. These inverter topologies, which contain an impedance

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source (ZS) network between the dc input and inverter, have the ability to boost (or buck) the dc voltage produced by a photovoltaic (PV) panel to the desired level at the output of ZS network by applying the shoot-through states to the inverter [7]–[9]. The consequence of using shoot-through states also eliminates the requirement for dead-times which is essential for traditional 2L inverters.

The attractive features of NPC and ZS network based inverters are combined in a single topology [10]–[16]. The topology introduced in [10] and [11] employs ZSI and requires two dc sources. However, the discontinuous input current, which arises in the ZSI topology, may have an adverse effect on the dc input source. As a remedy to the discontinuous input current, the neutral-point-clamped quasi-Z-source inverter (NPC-qZSI) topology has been proposed [12]–[16]. The NPC-qZSI topology not only offers continuous input current, but also provides wide input voltage operation range, shoot-through immunity, twice lower semiconductor voltage stress, good performance at reasonably low switching frequency and ability to work with one dc input voltage source. In spite of these attractive features, the single-phase inverter topologies suffer from inherent double-line frequency (2ω) ripple existing on the ZS network capacitor voltages and inductor currents which have adverse effects on the lifetime and efficiency of the photovoltaic (PV) array utilized to supply input voltage to the system. Therefore, these 2ω ripples have to be minimized or at least restricted to an engineering tolerant range. With the aim of minimizing or eliminating these ripples, passive [17], active [18], [19], modulation [20] and closed-loop [21] based suppression techniques are proposed. The passive suppression technique requires large inductances and capacitors which increase the inverter size, weight, and cost. The active suppression technique requires extra semiconductor switches which not only increases the cost, but also worsens the system's reliability. On the other hand, modulation and closed-loop based suppression techniques offer better solution for suppressing 2ω ripple without increasing the size and cost of the inverter. Also, these techniques do not worsen the reliability of the entire system since no additional switching device is required.

In this paper, a new closed-loop based 2ω ripple suppression method is proposed for a single-phase grid-connected three-level (3L) NPC-qZSI. The idea behind the proposed suppression method is based on generating the inductor current reference without 2ω ripple and then, forcing the actual inductor current to track its reference using an appropriate closed-loop control. If the actual inductor current tracks its reference properly, it implies that the actual inductor current will be. The 2ω ripple free inductor current reference generation is based on the phase cancellation in the closed-loop due to the fact that the 2ω ripple components of capacitor and inductor voltages in the ZS network have inherent opposite phase (180° phase difference). In order to achieve such phase cancellation, the 2ω ripples of inductor and capacitor voltages should be added inside the closed-loop. In [14], the control of dc-side variables (capacitor voltages and inductor currents) is achieved by using proportional-integral (PI) controllers. In NPC-qZSI topology, all inductor currents are equal to each other (see next Section) in the steady-state. Also, the capacitor voltages converge to two different dc levels in the steady-state. This means that there are three variables which should be controlled in the dc-side. Hence, if the 2ω ripple of capacitor voltage is added with 2ω ripple of inductor voltage (after it is multiplied by a gain), they cancel each other so that no 2ω component occurs in the resultant signal. Thereafter, this signal together with the desired capacitor voltage references can be used to generate the inductor current reference by using a PI controller which does not produce the 2ω component in the inductor current reference. Hence, no 2ω ripple component appears in the actual inductor current provided that the inductor current tracks its reference.

In the literature, there are only a few papers which discuss the control of grid-connected 3L-NPC-qZSI with LCL filter [15], [16]. The control strategy proposed in [15] achieves the control of dc- and ac-side variables by using proportional-integral-derivative (PID) and proportional-resonant (PR) controller, respectively. However, there is no 2ω ripple suppression methodology in dc-side control. Also, the proposed control strategy has not been validated experimentally. On the other hand, a three-phase grid-connected 3L-NPC-qZSI topology has been tested experimentally in [16] where no specific control method was described for the ac-side.

Sliding mode control (SMC) method has been recognized as one of the popular and powerful control tool in wide range of industrial applications (manipulators, robots, spacecraft, automotive control, and power converters) due to its distinguished features such as fast dynamic response, robustness against disturbances and variations in the system parameters, and implementation simplicity [22]. Its popularity comes from the robustness feature which eliminates the burden of the necessity of system parameters required for accurate modeling in most applications. In spite of these attractive features, the SMC method suffers from the undesired oscillations (called chattering) existing in the state variables due to unmodelled dynamics and switching time delays. Chattering results in low control accuracy, losses and time-varying switching frequency in power converter applications. Since chattering is the major obstacle in the practical implementation of SMC in power converter applications, its effects should be mitigated to acceptable level [23]. So far, the SMC with these attractive features has not been considered in the control of grid-connected 3L-NPC-qZSI.

In this paper, the SMC method with fixed switching frequency is proposed to control the ac-side grid current of a grid-connected 3L-NPC-qZSI. Unlike the SMC methods presented in [24]–[26], the SMC method proposed in this study offers fixed switching frequency. The fixed switching frequency can be achieved if the discontinuities in the sliding surface function are reduced (or eliminated) by a smoothing operation. The smoothing operation which is performed by passing the sliding surface function through a boundary layer

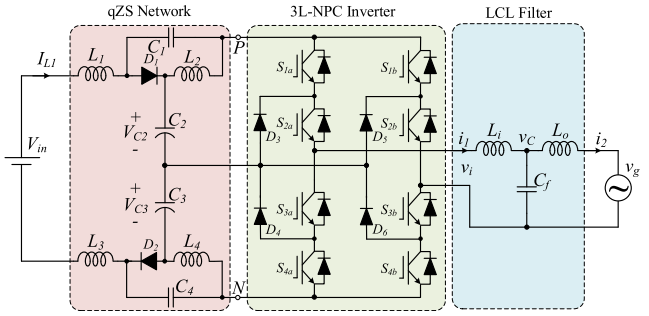


FIGURE 1. Single-phase grid-connected NPC-qZSI with LCL filter.

alleviates the chattering [22]. On the other hand, unlike the control method in [27] where a PI controller is employed in the ac-side for controlling the grid current, the grid current control in this study is based on using PR control which yields perfect tracking. The theoretical considerations and feasibility of proposed control method are validated by the experimental investigations.

II. MODELING OF THREE-LEVEL NPC-QZSI

The single-phase 3L-NPC-qZSI containing the ZS network, three-level NPC inverter, *LCL* filter, and grid is shown in Fig. 1 [14]. The ZS network currents and voltages contain dc and 2ω ripple components as follows

$$I_{L1} = \bar{I}_{L1} + \tilde{i}_{L1} \quad , I_{L2} = \bar{I}_{L2} + \tilde{l}_{L2} \tag{1}$$

$$I_{L3} = \bar{I}_{L3} + \tilde{i}_{L3} \quad , I_{L4} = \bar{I}_{L4} + \tilde{l}_{L4} \tag{2}$$

$$V_{C1} = \bar{V}_{C1} + \tilde{v}_{C1} \quad , V_{C2} = \bar{V}_{C2} + \tilde{v}_{C2} \tag{3}$$

$$V_{C3} = \bar{V}_{C3} + \tilde{v}_{C3} \quad , V_{C4} = \bar{V}_{C4} + \tilde{v}_{C4} \tag{4}$$

The complete mathematical model of the 3L-NPC-qZSI depends on the switching states of the NPC inverter. Two switching states are available which are referred to as shoot-through (ST) state and non-shoot-through (NST) state. The equivalent model of the entire system in each switching state is depicted in Fig. 2. The inductor voltages in the ZS network can be written easily if the capacitors and inductors in the ZS network are considered to be identical ($L_1 = L_3, L_2 = L_4, C_1 = C_4, C_2 = C_3$). In the NST state, where the NPC inverter is represented as a current source, the inductor voltages and capacitor currents can be written from Fig. 2(a) as follows

$$L_{13}\frac{dI_{L13}}{dt} = {}_{in} - V_{C2} - V_{C3} \tag{5}$$

$$L_2\frac{dI_{L2}}{dt} = -V_{C1}, \quad L_4\frac{dI_{L4}}{dt} = -V_{C4} \tag{6}$$

$$C_1\frac{dV_{C1}}{dt} = I_{L2} - I_o \tag{7}$$

$$C_2\frac{dV_{C2}}{dt} = C_3\frac{dV_{C3}}{dt} = I_{L13} - I_o \tag{8}$$

$$C_4\frac{dV_{C4}}{dt} = I_{L4} - I_o \tag{9}$$

On the other hand, the NPC inverter is represented as short circuit in the ST state as shown in Fig. 2(b). In this

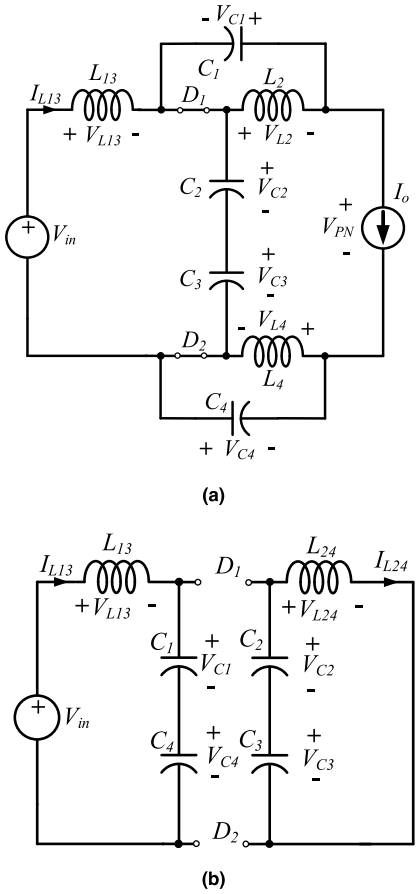


FIGURE 2. Model of qZS network. (a) in NST state; (b) in ST state [13].

state, the inductor voltages and capacitor currents can be expressed as

$$L_{13}\frac{dI_{L13}}{dt} = V_{in} + V_{C1} + V_{C4} \tag{10}$$

$$L_{24}\frac{dI_{L24}}{dt} = V_{C2} + V_{C3} \tag{11}$$

$$C_1\frac{dV_{C1}}{dt} = C_4\frac{dV_{C4}}{dt} = -I_{L13} \tag{12}$$

$$C_2\frac{dV_{C2}}{dt} = C_3\frac{dV_{C3}}{dt} = -I_{L24} \tag{13}$$

In (5) and (10), the inductor voltage V_{L13} is equal to $V_{L13} = V_{L1} + V_{L3}$. Similarly, V_{L24} in (11) is $V_{L24} = V_{L2} + V_{L4}$. In the steady-state, the dc components of the inductor voltages should be zero. Hence, using equations (5), (6), (10), and (11), the dc components of inductor voltages can be expressed as

$$\bar{V}_{L1} = T_{ST}\left(\frac{V_{in} + \bar{V}_{C1} + \bar{V}_{C4}}{2}\right) + T_{NST}\left(\frac{V_{in} - \bar{V}_{C2} - \bar{V}_{C3}}{2}\right) = 0 \tag{14}$$

$$\bar{V}_{L2} = T_{ST}\left(\frac{\bar{V}_{C2} + \bar{V}_{C3}}{2}\right) + T_{NST}\left(-\bar{V}_{C1}\right) = 0 \tag{15}$$

$$\bar{V}_{L3} = T_{ST}\left(\frac{V_{in}+\bar{V}_{C1}+\bar{V}_{C4}}{2}\right) + T_{NST}\left(\frac{V_{in}-\bar{V}_{C2}-\bar{V}_{C3}}{2}\right) = 0 \quad (16)$$

$$\bar{V}_{L4} = T_{ST}\left(\frac{\bar{V}_{C2}+\bar{V}_{C3}}{2}\right) + T_{NST}\left(-\bar{V}_{C4}\right) = 0 \quad (17)$$

In (14)-(17), T_{ST} and T_{NST} represent ST and NST periods, respectively. The dc components of capacitor voltages can be solved from (14)-(17) in terms of V_{in} and shoot-through duty-cycle as follows

$$\bar{V}_{C1}=\bar{V}_{C4}=\frac{D_{ST}V_{in}}{2-4D_{ST}},\ \bar{V}_{C2}=\bar{V}_{C3}=\frac{V_{in}(1-D_{ST})}{2-4D_{ST}} \quad (18)$$

where $D_{ST} = T_{ST}/T$ denotes the shoot-through duty cycle and $T = T_{ST} + T_{NST}$. Applying Kirchhoff's voltage law to Fig. 1, one can obtain the dc component of V_{PN} as follows

$$\bar{V}_{PN} = \bar{V}_{C1} + \bar{V}_{C2} + \bar{V}_{C3} + \bar{V}_{C4} \quad (19)$$

Since the boost factor is defined as the ratio between the dc-link and dc input voltages, it can be written as

$$B = \frac{\bar{V}_{PN}}{V_{in}} = \frac{1}{1-2D_{ST}} \quad (20)$$

Similarly, the dc components of the capacitor currents should be zero in the steady-state. Therefore, using (7)-(9), (12) and (13), the following equation can be obtained

$$\bar{I}_{L1} = \bar{I}_{L2} = \bar{I}_{L3} = \bar{I}_{L4} = \frac{(1-D_{ST})\bar{I}_o}{(1-2D_{ST})} \quad (21)$$

The differential equations regarding 2ω ripple components can be written as

$$L_1\frac{d\tilde{i}_{L1}}{dt} = L_3\frac{d\tilde{i}_{L3}}{dt} = \frac{(\tilde{v}_{C1}+\tilde{v}_{C4})D_{ST}-(\tilde{v}_{C2}+\tilde{v}_{C3})(1-D_{ST})}{2} \quad (22)$$

$$L_2\frac{d\tilde{i}_{L2}}{dt} = \frac{(\tilde{v}_{C2}+\tilde{v}_{C3})D_{ST}-\tilde{v}_{C1}(1-D_{ST})}{2} \quad (23)$$

$$L_4\frac{d\tilde{i}_{L4}}{dt} = \frac{(\tilde{v}_{C2}+\tilde{v}_{C3})D_{ST}-\tilde{v}_{C4}(1-D_{ST})}{2} \quad (24)$$

$$C_1\frac{d\tilde{v}_{C1}}{dt} = -\tilde{i}_{L1}D_{ST} + \left(\tilde{i}_{L2}-\tilde{i}_o\right)(1-D_{ST}) \quad (25)$$

$$C_2\frac{d\tilde{v}_{C2}}{dt} = -\tilde{i}_{L2}D_{ST} + \left(\tilde{i}_{L1}-\tilde{i}_o\right)(1-D_{ST}) \quad (26)$$

$$C_3\frac{d\tilde{v}_{C3}}{dt} = -\tilde{i}_{L4}D_{ST} + \left(\tilde{i}_{L3}-\tilde{i}_o\right)(1-D_{ST}) \quad (27)$$

$$C_4\frac{d\tilde{v}_{C4}}{dt} = -\tilde{i}_{L3}D_{ST} + \left(\tilde{i}_{L4}-\tilde{i}_o\right)(1-D_{ST}) \quad (28)$$

From (22)-(28), it can be deduced that $\tilde{v}_{C1} = \tilde{v}_{C2} = \tilde{v}_{C3} = \tilde{v}_{C4}$ and $\tilde{i}_{L1} = \tilde{i}_{L2} = \tilde{i}_{L3} = \tilde{i}_{L4}$. This means that 2ω ripple components of all capacitor voltages are equal to each other with the same amplitude and phase shift. Similarly, all inductor currents have equal 2ω ripple components with the same phase shift. Hence, the differential equations

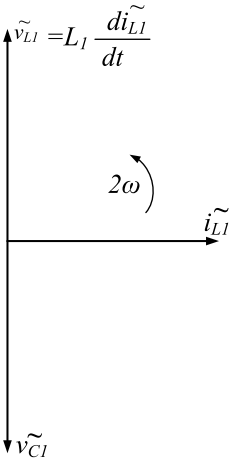


FIGURE 3. Phasor diagram of $\tilde{v}_{C1}$, $\tilde{i}_{L1}$, and $\tilde{v}_{L1}$.

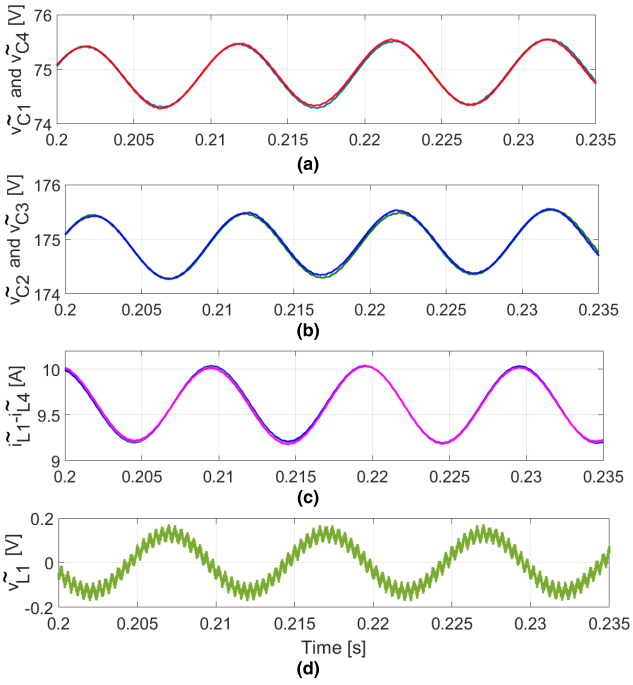


FIGURE 4. The 2ω ripple components of: (a), (b) capacitor voltages, (c) inductor currents, (d) inductor voltage.

regarding these components can be written in the simplified form as follows

$$L_1\frac{d\tilde{i}_{L1}}{dt} = (2D_{ST}-1)\tilde{v}_{C1} \quad (29)$$

$$C_1\frac{d\tilde{v}_{C1}}{dt} = (1-2D_{ST})\tilde{i}_{L1} - (1-D_{ST})\tilde{i}_o \quad (30)$$

Equations (29) and (30) are the same as the equations derived for single-phase 2L-qZSI in [17]. The phasor diagram of (29) for $D_{ST} < 0.5$ is depicted in Fig. 3. Clearly, there is 180° phase difference between $\tilde{v}_{L1}$ and $\tilde{v}_{C1}$.

The simulated 2ω ripple components of all capacitor voltages, all inductor currents and inductor voltage are shown in Fig. 4. The phase relationship between these components agrees well with the phasors illustrated in Fig. 3.

According to the phasor diagram, $\tilde{v}_{L1}$ leads $\tilde{i}_{L1}$ by 90°, $\tilde{i}_{L1}$, leads $\tilde{v}_{C1}$ by 90° and $\tilde{v}_{L1}$ leads $\tilde{v}_{C1}$ by 180°. In other words, the phase difference between $\tilde{v}_{L1}$ and $\tilde{v}_{C1}$ is 180°. Comparing Figs. 3 and 4, one can see that the phase relationship between the 2ω ripple components in Fig. 4 is in good agreement with the phase relationship in the phasor diagram. In addition, the 2ω ripple components of the capacitor voltages have equal amplitudes and phase shifts ($\tilde{v}_{C1} = \tilde{v}_{C2} = \tilde{v}_{C3} = \tilde{v}_{C4}$) as determined theoretically. Similarly, the 2ω ripple components of inductor currents also have equal amplitudes and phase shifts $\left(\tilde{i}_{L1} = \tilde{i}_{L2} = \tilde{i}_{L3} = \tilde{i}_{L4}\right)$. The proposed 2ω ripple suppression method which is described in the next section is based on the phase relationship between $\tilde{v}_{C1}$ and $\tilde{v}_{L1}$.

III. CONTROL STRATEGY

In order to be able to control the entire system shown in Fig. 1, both dc- and ac-sides should be controlled simultaneously. The former is achieved by controlling the inductor currents and capacitor voltages in the ZS network. In such a case, the desired D_{ST} can be generated and applied to the inverter successfully. On the other hand, the current injected to the grid should also be controlled in the ac-side. These control strategies are described in the following sub-sections.

A. CONTROL OF QZS NETWORK WITH 2ω RIPPLE SUPPRESSION

The ZS network has eight variables to be controlled. According to the theoretical results obtained in Section II, we have $\bar{I}_{L1} = \bar{I}_{L2} = \bar{I}_{L3} = \bar{I}_{L4}$, $\bar{V}_{C1} = \bar{V}_{C4}$, and $\bar{V}_{C2} = \bar{V}_{C3}$. Therefore, when the control of I_{L1}, V_{C2} and V_{C3} are achieved successfully, the control of other dc variables is achieved automatically. In this case, three references $\left(I^*_{L1}, V^*_{C2} \text{ and } V^*_{C3}\right)$ are needed. While V^*_{C2} and V^*_{C3} can be set to a desired constant value, the value of I^*_{L1} is determined by regulating V_{C2} and V_{C3} using PI controller. The inputs of these PI controllers are $V^*_{C2} - V_{C2}$ and $V^*_{C3} - V_{C3}$, respectively. The outputs of these PI controllers are added together to form I^*_{L1}. In this case, I^*_{L1} contains 2ω ripple which is propagated from V_{C2} and V_{C3}. Under such control scheme, I_{L1} involves 2ω ripple component too since it tracks I^*_{L1}.

In order to suppress 2ω ripple in I_{L1}, it is required to produce I^*_{L1} without 2ω ripple. If I^*_{L1} does not contain 2ω ripple, then I_{L1} will track I^*_{L1} with no 2ω ripple. It is obvious from Figs. 3 and 4 that $\tilde{v}_{L1}$ and $\tilde{v}_{C1}$ have 180° phase difference. The main idea behind the proposed ripple suppression method is to cancel the 2ω ripple in the signals $\left(V^*_{C2} - V_{C2} \text{ and } V^*_{C3} - V_{C3}\right)$ at the PI inputs before it propagates to the PI output which produces I^*_{L1}. Therefore, the effect of 2ω ripple can be suppressed if $K_\omega \tilde{v}_{L1}$ is added to the signals at the PI inputs as follows

$$\begin{aligned} I^*_{L1} = {} & K_{p1}\left[V^*_{C2} - (V_{C2} + K_\omega \tilde{v}_{L1})\right] \\ & + K_{i1}\int \left[V^*_{C2} - (V_{C2} + K_\omega \tilde{v}_{L1})\right] dt \\ & + K_{p1}\left[V^*_{C3} - (V_{C3} + K_\omega \tilde{v}_{L1})\right] \\ & + K_{i1}\int \left[V^*_{C3} - (V_{C3} + K_\omega \tilde{v}_{L1})\right] dt \end{aligned} \quad (31)$$

where K_{p1} and K_{i1} denote proportional and integral gains and K_ω is the gain used to adjust the level of ripple cancellation. The equation which generates $1 - D_{ST}$ is shown below

$$1 - D_{ST} = K_{p2}\left(I^*_{L1} - I_{L1}\right) + K_{i2}\int \left(I^*_{L1} - I_{L1}\right) dt \quad (32)$$

where K_{p2} and K_{i2} denote proportional and integral gains, respectively. In (31), $\tilde{v}_{L1}$ is obtained by measuring V_{L1} and averaging it. The block diagram for generating I^*_{L1} using conventional method without 2ω ripple suppression and the proposed method with 2ω ripple suppression is shown in Fig. 5. It is clear from Fig. 5(a) that the error signals ($e_{V_{C2}}$ and $e_{V_{C3}}$) at the PI inputs and the reference inductor current (I^*_{L1}) contain 2ω ripple. However, when $K_\omega \tilde{v}_{L1}$ term is added with the capacitor voltages (V_{C2} and V_{C3}), no 2ω ripple occurs in the resultant waveform due to the phase cancellation between $\tilde{v}_{C1}$ and $\tilde{v}_{L1}$ as shown in Fig. 5(b). It should be mentioned that the gain K_ω should be adjusted to the appropriate value so as to achieve the perfect cancellation.

Fig. 6 shows the simulated error voltages ($e_{V_{C2}}$ and $e_{V_{C3}}$) at the PI inputs and actual and reference inductor currents (I_{L1} and I^*_{L1}) generated without and with the proposed 2ω ripple suppression method. It is evident from Fig. 6(a) that 2ω ripple occurs in the error voltages at the PI inputs which propagates to the output and hence, generating I^*_{L1} with 2ω ripple when the suppression method is disabled. Since, I_{L1} tracks I^*_{L1} , then I_{L1} also contains 2ω ripple. However, when the 2ω ripple suppression method is activated, the error voltages do not contain 2ω ripple which in turn avoids the propagation of 2ω ripple to the output as shown in Fig. 6(b). In this case, both I^*_{L1} and I_{L1} do not contain 2ω ripple.

B. SMC OF NPC INVERTER WITH FIXED SWITCHING FREQUENCY

In ac-side, the current injected to the grid should be controlled such that it tracks its reference and in phase with the grid voltage. However, achieving these control objectives is a challenging task due to the damping requirement which complicates the controller design. Damping requirement, which arises due to the LCL filter, can be satisfied either by passive damping methods or active damping methods. While passive damping is achieved by connecting a small resistor to LCL filter components, active damping is performed via an appropriate control strategy. It is worth noting that passive damping methods are not preferred anymore since they cause additional power losses which degrade the performance of the system. On the other hand, active damping methods are widely utilized at the expense of increased controller complexity. However, they do not cause additional power losses.

In this study, SMC is proposed to achieve the grid current control in the ac-side. Let the sliding surface function be defined as

$$\sigma = \alpha x_1 + \frac{dx_1}{dt} \quad (33)$$

where α is the sliding coefficient which should be always positive, x_1 is the capacitor voltage error and dx_1/dt is the

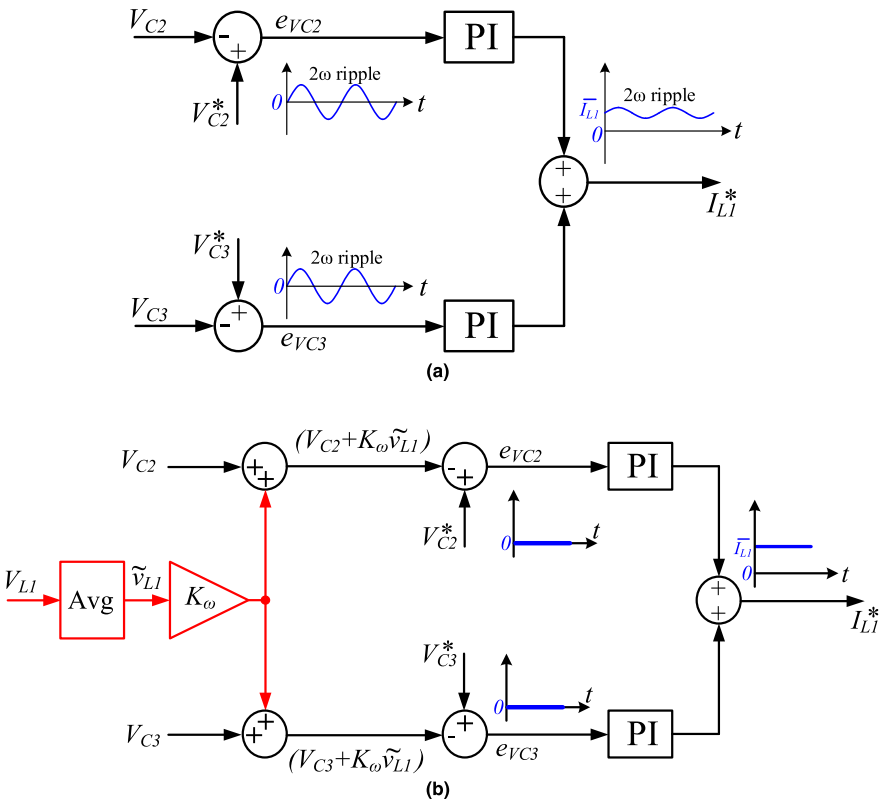


FIGURE 5. Block diagram for generating I^*_{L1}: (a) Conventional method without 2ω ripple suppression, (b) Proposed method with 2ω ripple suppression.

rate of change of capacitor voltage error defined as

$$x_1 = v_c - v_c^* \quad , \quad \frac{dx_1}{dt} = \frac{dv_c}{dt} - \frac{dv_c^*}{dt} \tag{34}$$

The main idea behind SMC is to direct the state trajectory toward a predefined sliding (switching) line and guarantee the movement of the state trajectory on the sliding line until they reach origin ($x_1 = 0, dx_1/dt = 0$) . When the system is in the sliding mode, the sliding surface function is zero ($\sigma = 0$). In this case, equation (33) reduces to

$$\frac{dx_1}{dt} = -\alpha x_1 \tag{35}$$

Equation (35) is a first-order differential equation which converges to zero for $\alpha > 0$. Achieving $x_1 = 0$ and $dx_1/dt = 0$ means that the actual capacitor voltage tracks its reference. It is worth noting that during the convergence period, x_1 depends neither on the system parameters nor the disturbance, but depends only on the sliding coefficient α. In this case, the order of the controlled system is reduced by one leading to simplification in the design and decoupling of the state variable dynamics.

Occurence of the sliding mode can be guaranteed if the existence conditions are satisfied. Generally, existence conditions are derived from the sliding surface function and its derivative which should have opposite signs around the sliding line. The sliding mode is stable if the following condition holds

$$\sigma \frac{d\sigma}{dt} < 0 \tag{36}$$

In order to derive the existence conditions and prove the stability of the sliding mode, a discontinuous switching law should be selected which drives the sliding surface function to zero. Although the system remains stable during the sliding mode, undesired oscillations (called chattering) exist in the state variables with finite frequency and amplitute due to the unmodelled dynamics. One common approach to reduce the effects of chattering is to replace the discontinuous switching law (u) with a hysteresis function. In this case, the state trajectory is forced to move within the band resulting in less chattering and thus, less switching frequency. The level of chattering and switching frequency are inversely proportional with the value of the band. Even though this approach reduces chattering, the switching frequency remains time-varying which is not desired in many applications.

As a remedy to the time-varying switching frequency, the control discontinuity neighboring the sliding surface function in the sliding mode should be smoothed out. A boundary layer with thickness Φ is used to perform the smoothing operation [22]. The control input interpolation within the boundary layer is shown in Fig. 7. It should be noted that the control law in the control input is replaced by σ/Φ. As a consequence of smoothing, the control input becomes

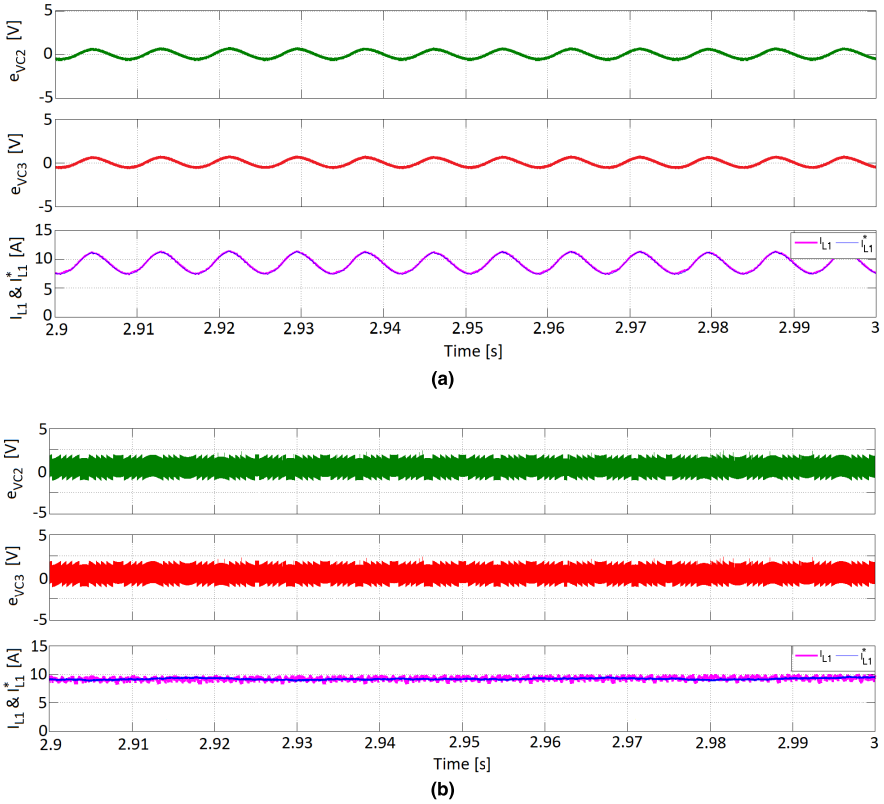


FIGURE 6. Error voltages at the PI inputs, actual and reference inductor currents when; (a) 2ω ripple suppression is disabled, (b) 2ω ripple suppression is enabled.

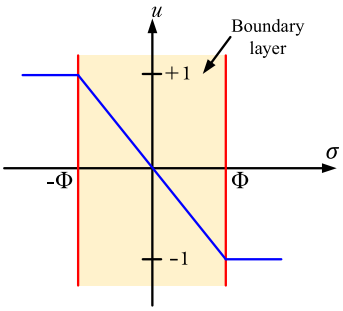


FIGURE 7. Control input within the boundary layer.

continuous within the boundary layer which results in no chattering. The pulse width modulation (PWM) signals can be produced by comparing σ/Φ with a triangular carrier signal having a constant frequency. In this case, the switching frequency of the inverter will always be constant. The operation of the system in ac-side is described by the following differential equations

$$L_i \frac{di_1}{dt} + r_i i_1 = v_i - v_c \tag{37}$$

$$L_o \frac{di_2}{dt} + r_o i_2 = v_c - v_g \tag{38}$$

$$C_f \frac{dv_c}{dt} = i_1 - i_2 \tag{39}$$

where r_i and r_o denote the resistance of the filter inductances, v_i, v_c, v_g are the inverter output, capacitor, and grid voltages, respectively. The expression for σ/Φ can be obtained by making use of (34) and (39) in (33) as follows

$$\frac{\sigma}{\Phi} = \frac{\alpha x_1}{\Phi} + \frac{\Delta i_C}{\Phi C_f} \tag{40}$$

where $\Delta i_C = i_C - i_C^*$ is an error in the capacitor current and i_C^* is the capacitor current reference. Since $\Delta i_C = \Delta i_1 - \Delta i_2$, then (40) can be written as

$$\frac{\sigma}{\Phi} = \frac{\alpha x_1}{\Phi} + \frac{(\Delta i_1 - \Delta i_2)}{\Phi C_f} \tag{41}$$

Now, assuming that the capacitor ripple current $(\Delta i_1 - \Delta i_2)$ is much greater than the sliding coefficient multiplied by the capacitor voltage error capacitor and ripple current Δi_2 is very small and negligible (since the current Δi_2 is assumed to flow through the capacitor and its average value through L_o), (41) can be approximated as

$$\frac{\sigma}{\Phi} \cong \frac{\Delta i_2}{\Phi C_f} \tag{42}$$

Since $\Delta i_2 = \Delta v_{Li} \Delta t / L_i$ and the maximum possible value of Δi_2 occurs when the control input is zero, then (42) reduces to

$$\frac{\sigma}{\Phi} \cong \frac{\bar{V}_{pn}}{\Phi L_i C_f} \tag{43}$$

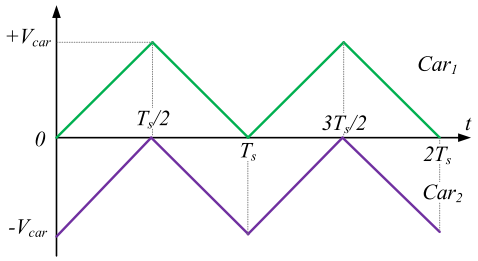


FIGURE 8. Level shifted carrier signals.

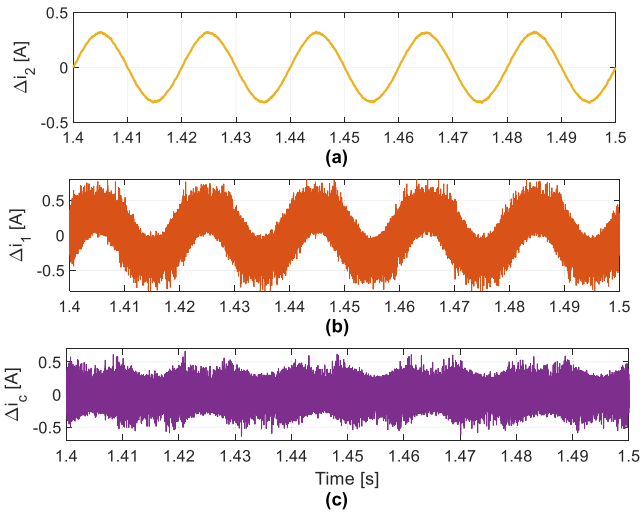


FIGURE 9. Simulated responses of Δi_1, Δi_2 and Δi_C.

The gate signals of the switches in NPC-qZSI are produced by using the level shifted carrier signals shown in Fig. 8.

The magnitude of the carrier slope can be written as follows

$$|\text{ Slope }_{Car1}| = 2V_{car}f_c \tag{44}$$

where V_{car} is the amplitude and f_c is the frequency of the carrier signals. In order to generate these PWM signals, the following condition should hold

$$\left(\frac{\bar{V}_{pn}}{2\Phi L_i C_f} \cong \frac{\sigma}{2\Phi}\right) < \left(\left|\text{Slope}_{Car1}\right| = 2V_{car}f_c\right) \tag{45}$$

Hence, the lower boundary of Φ can be obtained as

$$\Phi > \frac{\bar{V}_{pn}}{4L_i C_f V_{car} f_c} \tag{46}$$

The simulated responses of $\Delta i_1, \Delta i_2$ and Δi_C are shown in Fig. 9. Comparing the ripple currents in Fig. 9, one can easily see that the magnitude of the ripple in i_1 and i_C are close to each other which implies that the ripple in i_2 is negligible.

In order to compute σ, measurements of the inductor currents (i_1, i_2) and capacitor voltage (v_c) are essential. Also, the reference capacitor voltage (v_c^*) is needed. As mentioned before, the control objective in the ac-side is to control grid

TABLE 1. System and control parameters.

Description and Symbol	Value
Input DC voltage (V_{in})	200V
qZS network inductances ($L_1 - L_4$)	0.5mH
qZS network capacitances ($C_1 - C_4$)	470μF
LCL filter inductances (L_i , L_o)	1.5mH, 0.5mH
LCL filter inductor resistances, (r_i , r_o)	0.1Ω , 0.05Ω
LCL filter capacitance (C_f)	22μF
Grid voltage amplitude (V_g)	220Vrms
Proportional Gains (K_{p1} , K_{p2} , K_p)	1.72 , 1.2, 5
Integral Gains (K_{i1} , K_{i2} , K_r)	3.03 , 2.1, 1000
Ripple control gain (K_w)	20
Sliding coefficient (α)	30000
Cut-off frequency (ω_c)	1 rad/s
Carrier amplitude (V_{car})	1V
Carrier frequency (f_c)	2.5kHz

current i_2 such that i_2 becomes in phase with the grid voltage $\left(v_g = V_g \sin(\omega t)\right)$ and tracks its reference defined by

$$i_2^* = I_2^* \sin(\omega t) \tag{47}$$

In order to produce v_c^*, a proportional-resonant (PR) controller is utilized which processes the grid current error $\left(i_2^* - i_2\right)$ applied to its input. PR controllers are widely used in the regulation of ac signals due to their excellent tracking performance. The transfer function of the PR controller used in this study is given by

$$G_{PR}(s) = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{48}$$

where ω_c is the cut-off frequency, ω is the resonant frequency, K_p and K_r are proportional and resonant gains, respectively.

IV. EXPERIMENTAL VERIFICATION

The effectiveness and correct operation of the proposed control strategy have been verified by experimental results obtained from a 2.5kW prototype where the controller is implemented using an OPAL-RT OP5600 real-time platform. The complete block diagram involving the dc- and ac-side controls together with the PWM generation scheme is shown Fig. 10. The photograph of the testbed is given in Fig. 11. The system and control parameters listed in Table 1. The values of ZS network and *LCL* filter are chosen according to their availability in the laboratory.

Fig. 12 shows the steady-state responses of V_{PN}, V_{C1-C4}, I_{L1}, i_1, i_2 and v_g when the ripple suppression technique is disabled. The voltage and current references for this operation are $V_{C2}^* = V_{C3}^* = 175$V and $I_2^* = 10$A. Clearly, the capacitor voltages V_{C2} and V_{C3} track their references. Ignoring the 2ω ripple components of capacitor voltages and substituting $\bar{V}_{C2} = \bar{V}_{C3} = 175\ V$ and $V_{in} = 200$V into the second

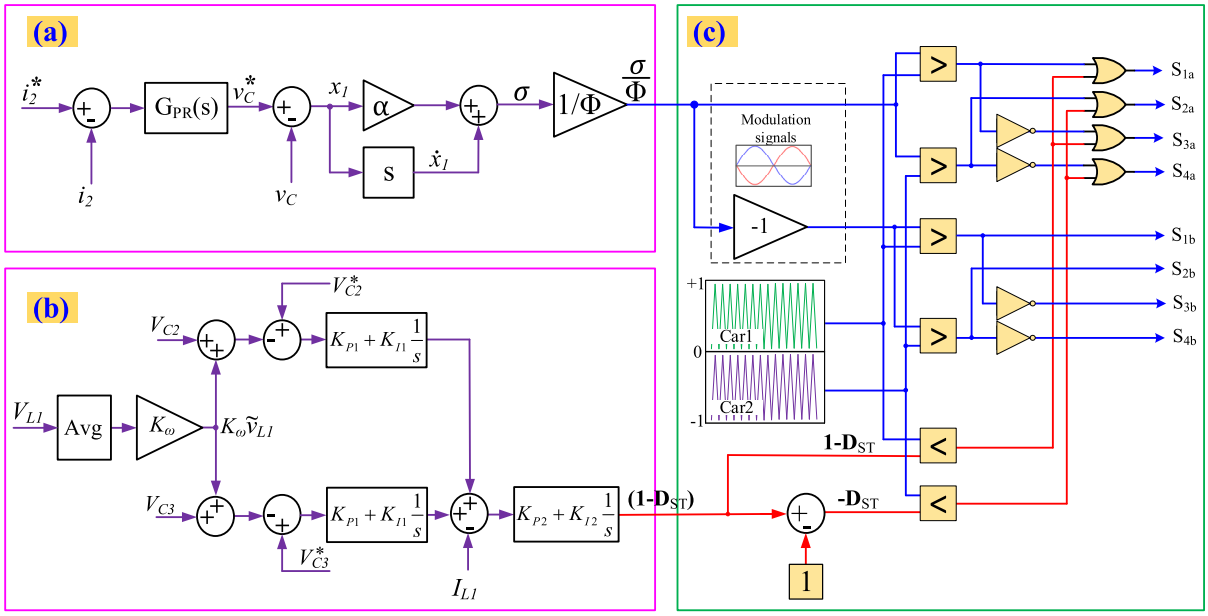


FIGURE 10. Block diagram of the proposed control method together with the switching logic. (a) ac-side control with SMC, (b) dc-side control, (c) Switching logic.

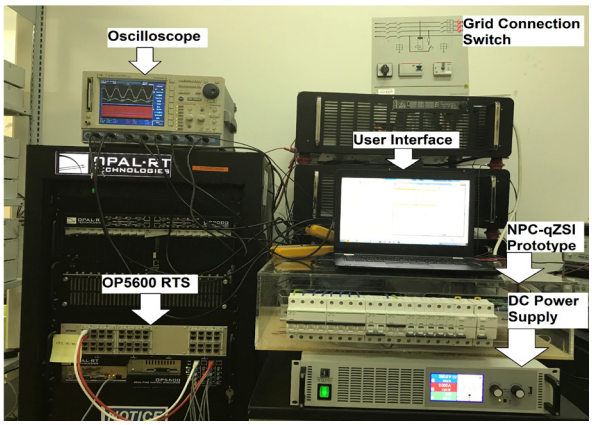


FIGURE 11. Experimental testbed.

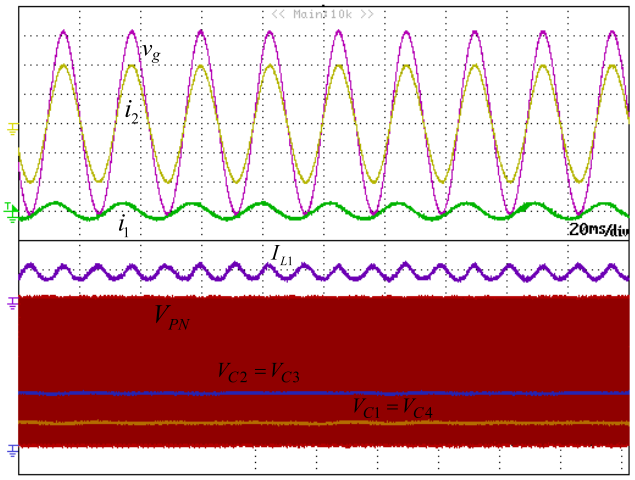
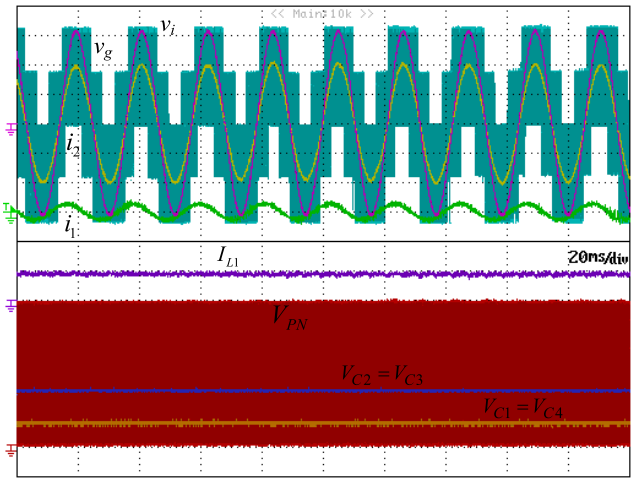


FIGURE 12. Steady-state responses of dc- and ac-side variables when the ripple suppression technique is disabled. V_{PN}(100V/div), V_{C1-C4}(100V/div), I_{L1}(10A/div), i_1(20A/div), i_2(5A/div), v_g(100V/div).

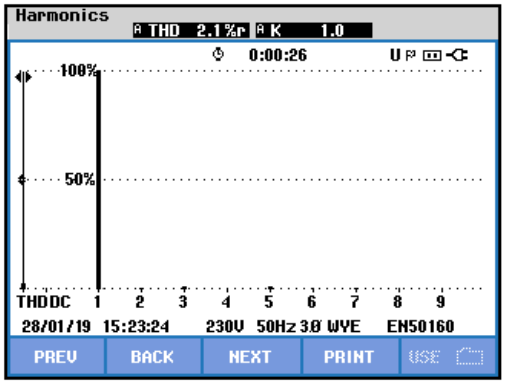
equation of (18), one obtains the value of shoot-through duty cycle as $D_{ST} = 0.3$.

Now, substituting $V_{in} = 200$V and $D_{ST} = 0.3$ into the first equation of (18) and solving for the capacitor voltages, one finds the theoretical values of other capacitor voltages as $\bar{V}_{C1} = \bar{V}_{C4} = 75\ V$. In this case, the theoretical value of V_{PN} can be obtained from (19) as 500V. It is evident from Fig. 10 that $\bar{V}_{C1} = \bar{V}_{C4} = 75\ V$, $\bar{V}_{C2} = \bar{V}_{C3} = 175\ V$ and $V_{PN} = 500$V. This means that the experimental results are in good agreement with the theoretical results derived in (18). Also, the grid current i_2 attains the maximum value of 10A which reveals that it tracks its reference $i_2^* = 10\sin(\omega t)$ successfully. Another important feature of the proposed control strategy is that there is no need to employ a special active damping method for damping the resonance due to the LCL filter. The capacitor voltage feedback involved in the sliding surface function has an inherent damping effect. Close inspection to the inductor current I_{L1} reveals that it contains 2ω ripple. Such ripple in dc-side is not desired in practice since it reduces the lifetime and efficiency of the photovoltaic (PV) array used to generate dc input voltage V_{in}.

Fig. 13 shows the steady-state responses of V_{PN}, V_{C1-C4}, I_{L1}, i_1, i_2, v_g and spectrum of the grid current when the ripple suppression technique is enabled. The reference signals are the same as in Fig. 12. Comparing Fig. 12 and 13(a), one can see that I_{L1} does not contain 2ω ripple. Furthermore, as a consequence of 2ω ripple suppression, the fluctuations in the dc capacitor voltages are also reduced. On the other hand, the total harmonic distortion (THD) of the grid current



(a)



(b)

FIGURE 13. Steady-state responses of dc- and ac-side variables when the ripple suppression technique is enabled. (a) V_{PN}(100V/div), V_{C1-C4}(100V/div), I_{L1}(10A/div), i_1(20A/div), i_2(5A/div), v_g(100V/div); (b) Spectrum of i_2.

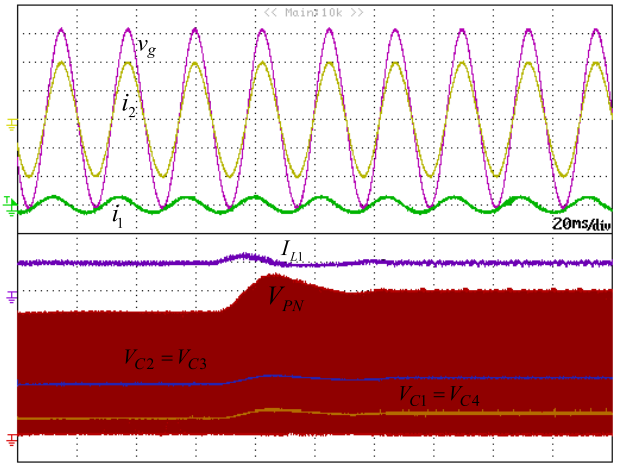


FIGURE 14. Dynamic responses of dc- and ac-side variables for an abrupt change in $V^*_{C2}=V^*_{C3}$ from 150V to 175V. (V_{Pv}(100V/div), V_{C-c4}(100V/div), I_{l1}(10A/div), i_1(20A/div)i_2(5A/div), v_g(100V/div)).

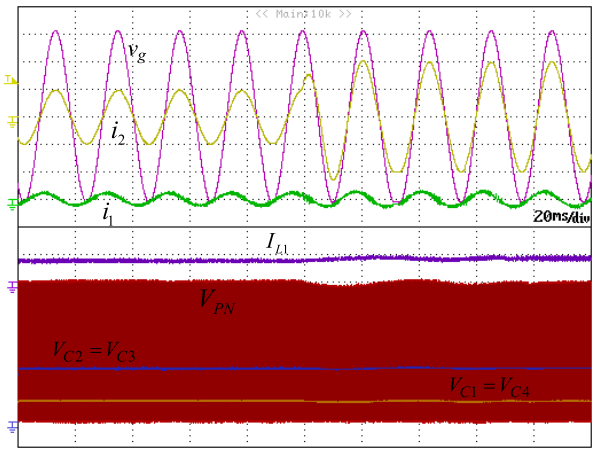


FIGURE 15. Dynamic responses of dc- and ac-side variables for an abrupt change in I^*_2 from 5A to 10A. (V_{PN} (100V/div), $V_{(c1-c4}$(100V/div), I_{L1}(10A/div), i_1(20A/div), i_2(5A/div), v_g(100V/div)).

is measured to be 2.1% as shown in Fig. 13(b). The harmonic components are negligibly small.

Fig. 14 shows the dynamic responses of V_{PN}, V_{C1-C4}, I_{L1}, i_1, i_2 and v_g for an abrupt change in capacitor voltage reference $\left(V^*_{C2}=V^*_{C3}\right)$ from 150V to 175V when the 2ω ripple suppression method is enabled. It is worth noting that with $V^*_{C2}=V^*_{C3}=150$V and $V_{in}=200$V, the value of D_{ST} is computed to be 0.25 which means that the values of V_{C1} and V_{C4} should be 50V. Hence, under this operating condition, V_{PN} should be 400V. Again, all of these theoretical computations are in good agreement with the experimental results shown in Fig. 14 before the reference change occurs. It is important noting that there is no change in the output power when the value of $V^*_{C2}=V^*_{C3}$ is changed. This means that I_{L1} should converge to the same value after the transients die out. Also, no change occurs in the ac-side variables.

Fig. 15 shows the dynamic responses of V_{PN}, V_{C1-C4}, I_{L1}, i_1, i_2 and v_g for an abrupt change in I^*_2 from 5A to 10A. It is obvious that the dc voltages are almost not affected from this step change. However, the dc inductor current converges to its new value in order to achieve the desired power change due to the change in I^*_2. It can be seen that the amplitude of grid current converges to the reference amplitude (10A) successfully which is an indicator that the proposed controller performs good tracking. Also, it is worth noting that no oscillations exhibit in the grid current which means that proposed SMC provides good damping as well.

Fig. 16 shows steady-state responses of I_{L1}, I^*_{L1}, σ/Φ, and D_{ST} obtained without and with 2ω ripple suppression method. Initially, the system is operated without the ripple suppression method. As can be seen from Fig. 15, both I_{L1} and I^*_{L1} contain 2ω ripple components. The modulating signal σ/Φ is a continuous sinusoidal signal which involves no switching ripples. The shoot through signal D_{ST} is a constant which is around 0.3. However, when the ripple suppression method is enabled, the 2ω ripples in I_{L1} and I^*_{L1} are cancelled out. The activation of the ripple suppression method does not have any effect on σ/Φ and D_{ST}.

The experimental efficiency of the system is also investigated. From Fig. 15, where the grid current amplitude is 10A, the efficiency is calculated to be around 90%.

TABLE 2. Comparisons of five 2ω ripple suppression methods with the proposed ripple suppression method.

Comparison Category	[17]	[18]	[19]	[20]	[21]	Proposed 2ω Ripple Suppression
Inverter topology	Cascaded multilevel-qZSI	2L-qZSI	2L-qZSI	2L-qZSI	2L-qZSI	3L-NPC-qZSI
Type of 2ω ripple suppression	Passive	Active	Active	Modulation	Closed-loop	Closed-loop
Number of additional switching devices	None	2	2	None	None	None
Number of additional passive elements	None	2	2	None	None	None
Number of required sensors for 2ω ripple suppression	None	3	4	1	3	1
Required calculations/operations	None	- DFT - Other operations	- DFT - αβ/dq	LPF & Resonant controller	LPF	Averaging
Number of required gains	None	3	1	2	2	1
Size of impedance network elements for efficient 2ω ripple suppression	Very large	Small	Small	Small	Small	Small

TABLE 3. Comparisons of five SMC based control methods with the proposed SMC method.

Comparison Category	[24]	[25]	[26]	[27]	[28]	Proposed SMC
Inverter topology	1-ph 2L inverter	1-ph 2L inverter	3-ph 2L inverter	1-ph 2L-qZSI	3-ph 2L-qZSI	1-ph 3L-NPC-qZSI
Type of coupling	*LCL* filter	*LCL* filter	*LCL* filter	*L* filter	*L* filter	*LCL* filter
Operation mode	Grid-connected	Grid-connected	Grid-connected	Grid-connected	Standalone	Grid-connected
Switching frequency	Time-invariant	Time-varying	Time-varying	Time-invariant	Time-invariant	Time-invariant
Chattering suppression	Not available	Partially available	Not available	Not available	Partially available	Available
Resonance damping	Inherent	Inherent	Inherent	Not applicable	Not applicable	Inherent
Number of required sensors to control i_2	4	3	4	8	6	2
Steady-state error in i_2	Does not exist due to the use of PR	Exists due to the parameter variations	Does not exist due to the use of PR	Exists due to the use of PI	Does not exist due to the use of PR	Does not exist due to the use of PR

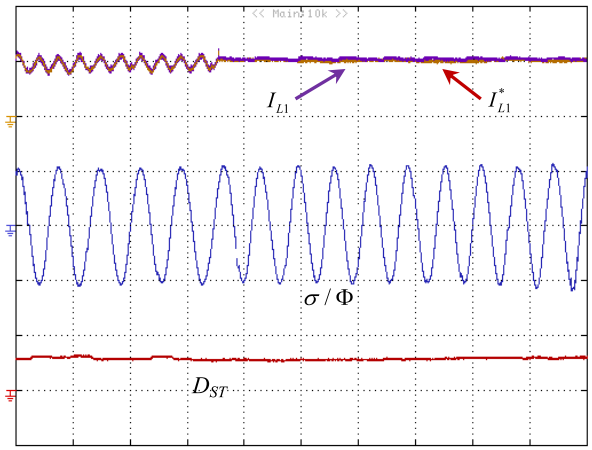


FIGURE 16. Steady-state responses of I_{L1} (10A/div), I^*_{L1} (10A/div), σ/Φ(0.75V/div) and D_{ST}(0.5V/div) obtained without and with 2ω ripple suppression.

The proposed control method (2ω ripple suppression in I_{L1} and fixed switching frequency based SMC in ac-side) is compared with the existing methods. Table 2 shows the comparison of five ripple suppression methods presented in [17]–[21] with the proposed ripple suppression method. It can be seen from Table 2 that the proposed ripple suppression method offers many advantages in terms of number of required sensors, required calculations (or operations) and number of required gains. While existing methods require discrete Fourier transform (DFT), low pass filter (LPF), $\alpha\beta$/dq transformation, and some trigonometric calculations, the proposed method needs an averaging only. Also, unlike the methods presented in [18] and [19], the proposed ripple suppression method does not need any additional switching devices and additional passive elements.

On the other hand, a comparison of proposed SMC method with the existing SMC methods presented in [24]–[28] is given in Table 3. The proposed SMC method with boundary layer reduces the chattering in the discontinuous control signal which in turn makes it a continuous control signal suitable for the comparison process with the triangular carrier signal to achieve the time-invariant switching frequency operation. Moreover, the proposed SMC method needs lesser sensors

than the SMC methods in [24]–[28]. Unlike, the SMC methods in [25] and [27], the proposed SMC eliminates the steady-state error in i_2.

V. CONCLUSION

In this paper, 2ω ripple suppression and SMC with time-invariant switching frequency methods are proposed for a single-phase grid-connected 3L-NPC-qZSI. The proposed ripple suppression method is based on canceling the 2ω ripple components of capacitor and inductor voltages at the PI controller inputs which are used to generate the reference inductor current needed in the dc-side. The main reason behind this ripple cancellation comes from the fact that there is 180° phase difference between the 2ω ripple components of capacitor and inductor voltages. It is shown that ripple cancellation can be achieved when these ripple components are added and processed by PI controllers which produce the reference inductor current without 2ω ripple. In this case, if the actual inductor current tracks the generated reference, then there will be no 2ω ripple in the actual inductor current. In addition, the grid current control is achieved using SMC which achieves time-invariant switching frequency. The discontinuity in the sliding surface function is eliminated by using boundary layer method. The proposed ripple suppression method together with the SMC strategy offers many advantages such as fast dynamic response, zero grid current error, simple implementation, robustness to parameter variations and time-invariant switching frequency. The effectiveness of the proposed method is verified experimentally under steady-state and transient conditions.

REFERENCES

[1] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*. Hoboken, NJ, USA: Wiley, 2014.

[2] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] M. Malinowski, K. Gopakumar, J. Rodríguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[5] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, Jan. 2007.

[6] Y. Ounejjar, K. Al-Haddad, and L.-A. Gregoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1294–1306, Apr. 2011.

[7] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[8] J. Anderson and F. Z. Peng, "Four quasi-Z-source inverters," in *Proc. 39th IEEE Annu. Power Electron. Spec. Conf. (PES)*, Jun. 2008, pp. 2743–2749.

[9] Y. Liu, H. Abu-Rub, and B. Ge, "Z-source\/quasi-Z-source inverters: Derived networks, modulations, controls, and emerging applications to photovoltaic conversion," *IEEE Trans. Ind. Mag.*, vol. 8, no. 4, pp. 32–44, Dec. 2014.

[10] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, "Three-level Z-source inverters using a single LC impedance network," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 706–711, Mar. 2007.

[11] M. Stempfle, S. Bintz, J. Wölfle, and J. Roth-Stielow, "Adaptive closed-loop state control system for a three-level neutral-point-clamped Z-source inverter," *IET Elect. Syst. Transp.*, vol. 6, no. 1, pp. 12–19, Mar. 2016.

[12] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, "Single phase three-level neutral-point-clamped quasi-Z-source inverter," *IET Power Electron.*, vol. 8, no. 1, pp. 1–10, 2015.

[13] S. Bayhan, P. Kakosimos, H. Abu-Rub, and J. Rodriguez, "Model predictive control of five-level H-bridge neutral-point-clamped qZS inverter," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2016, pp. 5971–5976.

[14] S. Bayhan, H. Komurcugil, H. Abu-Rub, and Y. Liu, "A Lyapunov stability theorem based control strategy for single-phase neutral-paint-clamped quasi-impedance source inverter with LCL filter," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2018, pp. 3695–3699.

[15] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, and F. Blaabjerg, "Single-phase 3L PR controlled qZS inverter connected to the distorted grid," in *Proc. 10th Int. Conf. Compat., Power Electron. Power Eng. (CPEPOWERENG)*, Jun./Jul. 2016, pp. 234–239.

[16] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and T. Jalakas, "Three-level three-phase quasi-Z-source neutral-point-clamped inverter with novel modulation technique for photovoltaic application," *Electr. Power Syst. Res.*, vol. 130, pp. 10–21, Jan. 2016.

[17] D. Sun, B. Ge, X. Yan, D. Bi, H. Zhang, Y. Liu, H. Abu-Rub, L. Ben-Brahim, and F. Z. Peng, "Modeling, impedance design, and efficiency analysis of quasi-Z source module in cascaded multilevel photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 11, pp. 6108–6117, Nov. 2014.

[18] B. Ge, Y. Liu, H. Abu-Rub, R. S. Balog, F. Z. Peng, H. Sun, and X. Li, "An active filter method to eliminate DC-side low-frequency power for a single-phase quasi-Z-source inverter," *IEEE Trans. Ind. Elect.*, vol. 63, no. 8, pp. 4838–4848, Aug. 2016.

[19] Y. Liu, B. Ge, H. Abu-Rub, H. Sun, F. Z. Peng, and Y. Xue, "Model predictive direct power control for active power decoupled single-phase quasi-Z-source inverter," *IEEE Trans. Ind. Informat.*, vol. 12, no. 4, pp. 1550–1559, Aug. 2016.

[20] Y. Zhou, H. Li, and H. Li, "A single-phase PV quasi-Z-source inverter with reduced capacitance using modified modulation and double-frequency ripple suppression control," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2166–2173, Mar. 2016.

[21] B. Ge, Y. Liu, H. Abu-Rub, R. S. Balog, F. Z. Peng, S. McConnell, and X. Li, "Current ripple damping control to minimize impedance network for single-phase quasi-Z source inverter system," *IEEE Trans. Ind. Informat.*, vol. 12, no. 3, pp. 1043–1054, Jun. 2016.

[22] J.-J. Slotine and W. Li, *Applied Nonlinear Control*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1991.

[23] V. Utkin, J. Guldner, and J. Shi, *Sliding Mode Control in Electro-Mechanical Systems*, 2nd ed. Boca Raton, FL, USA: CRC Press, 2009.

[24] X. Hao, X. Yang, T. Liu, L. Huang, and W. Chen, "A sliding-mode controller with multiresonant sliding surface for single-phase grid-connected VSI with an LCL filter," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2259–2268, May 2013.

[25] H. Komurcugil, S. Ozdemir, I. Sefa, N. Altin, and O. Kukrer, "Sliding-mode control for single-phase grid-connected LCL-filtered VSI with double-band hysteresis scheme," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 864–873, Feb. 2016.

[26] N. Altin, S. Ozdemir, H. Komurcugil, and I. Sefa, "Sliding-mode control in natural frame with reduced number of sensors for three-phase grid-tied LCL-interfaced inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2903–2913, Apr. 2019.

[27] U. K. Shinde, S. G. Kadwane, S. P. Gawande, M. J. B. Reddy, and D. K. Mohanta, "Sliding mode control of single-phase grid-connected quasi-Z-source inverter," *IEEE Access*, vol. 5, pp. 10232–10240, 2017.

[28] B. Xu and X. Ran, "Sliding mode control for three-phase quasi-Z-source inverter," *IEEE Access*, vol. 6, pp. 60318–60328, 2018.

SERTAC BAYHAN (M'14–SM'18) received the M.Sc. and Ph.D. degrees in electrical engineering from Gazi University, Ankara, Turkey, in 2008 and 2012, respectively, where he did his undergraduate studies and graduated as a valedictorian.

In 2008, he joined the Electronics and Automation Engineering Department, Gazi University, as a Lecturer, where he was promoted to the position of Assistant Professor and Associate Professor, in 2013 and 2017, respectively. From 2014 to 2018, he also worked at Texas A&M University at Qatar as an Associate Research Scientist. He is currently with the Qatar Environment and Energy Research Institute (QEERI), Hamad Bin Khalifa University, Doha, Qatar, as a Scientist. His research interests lie in the areas of advanced control of PV systems, microgrids, and smart grid applications. He has led several international projects with collaborators from all over the world. He has authored 150 high-impact journals and conference papers. He is the coauthor of two books and three book chapters. Because of the visibility of his research, he has been elected as the Chair of the IES Power Electronics Technical Committee. He currently serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and a Guest Editor for the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS.

HASAN KOMURCUGIL (S'94–M'99–SM'12) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Eastern Mediterranean University (EMU), Famagusta, North Cyprus, Turkey, in 1989, 1991, and 1998, respectively. In 1998, he joined the Computer Engineering Department, EMU, as an Assistant Professor, where he was promoted to the position of Associate Professor and Professor, in 2002 and 2008, respectively. From 2004 to 2010, he was the Head of the Computer Engineering Department, EMU. In 2010, he played an active role in preparing the department's first self-study report for the use of Accreditation Board for Engineering and Technology. From 2010 to 2019, he has served as the Board Member of Higher Education, Planning, Evaluation, Accreditation, and Coordination Council (YODAK) North Cyprus. He is currently a full-time Professor with the Computer Engineering Department, EMU. His research interests include power electronics and innovative control methods for power converters. He was a recipient of the Best Presentation Recognitions at the 41st and 42nd Annual Conferences of the IEEE Industrial Electronics Society, in 2015 and 2016, respectively. He was a corresponding Guest Associate Editor for Emerging Electric Machines and Drives for Smart Energy Conversion in the IEEE TRANSACTIONS ON ENERGY CONVERSION. He is currently a Guest Editor of the Identification and Observation Informatics for Energy Generation, Conversion, and Applications and Recent Advances on Sliding Mode Control and its Applications in Modern Industrial Systems in the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS. Also, he is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS.