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Discontinuous PWM Strategy for Neutral Point Clamped Three-Level Inverter to Achieve Multiple Control Objectives

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ABSTRACT In order to reduce switching loss of neutral-point clamped (NPC) three-level inverter (TLI), a switching loss minimized discontinuous PWM (SLMDPWM) strategy is proposed firstly. There are DC offset and AC ripple on the neutral-point (NP) voltage when SLMDPWM is used, which causes an appearance of low frequency harmonics (LFHs) in the output voltage. Aiming at this drawback, reduced LFHs (RLFHs) method is then proposed. While using RLFHs, the self-equilibrium ability of NP voltage is thus lost. So, active neutral-point voltage control (ANPVC) is also proposed. The performances of NPC TLI with the proposed DPWM and other DPWMs are compared by simulation and experimental results. The results show that switching loss, LFHs can be reduced significantly and the NP voltage can be controlled within an allowable range. Therefore, the multiple control objectives of reduced switching loss, no LFHs and allowable NP voltage are achieved.

INDEX TERMS Neutral-point clamped three-level inverter, discontinuous modulation strategy, neutral-point voltage, switching loss.

I. INTRODUCTION

Neutral-point (NP) clamped (NPC) three-level inverters (TLI) are more and more widely used because of some advantages over the conventional two-level inverter, such as reduced total harmonic distortion (THD), reduced voltage stress across switching devices, and higher inversion efficiency. The NPC TLI is widely used in many applications such as photovoltaic, wind turbine, and railway electrical traction drive systems [1]–[5]. In order to achieve better performances of NPC TLI, the following requirements for well-established PWM strategies should be satisfied.

i) Ensure the NP voltage balance, or NP voltage offset can be controlled within an acceptable range. Since there is unbalance NP voltage inevitably in some application, the good PWM strategies must have some tolerance ability of unbalance NP voltage.

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ii) Reduce the harmonics as much as possible even under unbalanced NP voltage, especially low frequency harmonics (LFHs) should be removed.

iii) Reduce switching loss to achieve higher efficiency.

One critical issue of NPC TLI is the potential unbalanced NP voltage. There are two components on NP voltage when unbalanced capacitor voltage takes place, which are (a) DC offset and (b) AC ripple [6], [7]. The unbalanced NP voltage deteriorates the three phase currents when open loop voltage control is used. On the other hand, a closed loop current control can improve the current quality but may aggravate the unbalanced NP voltage. Therefore, stable and reliable operation of the NPC TLI in practice application demands well NP voltage control ability.

Several PWM strategies have been reported to solve the NP voltage unbalance problem of NPC TLI, which are generally classified into space vector PWM (SVPWM) and carrier based PWM (CBPWM) schemes. For SVPWM scheme [8], [9], NP voltage control is achieved by adjusting the

ratio of dwell times of redundant small vectors during each control cycle. However, which are considerably complex to be implemented. The NP voltage control under CBPWM is to inject an appropriate zero sequence voltage (ZSV) to the reference voltages. Several CBPWM schemes to control the NP voltage have been reported in the literatures [10]–[16]. However, the NP voltage control ability of SVPWM and CBPWM are dependent on load power factor (PF) and modulation index.

In [7], the mechanism of self-equilibrium is studied. When there is DC offset on NP voltage, even-order harmonics are generated at the ac-side. These harmonic currents (mainly second and fourth) can contribute to the NP current under the influence of a non-perfect PI current controller, which appears as ''self-equilibrium'' effect. The self-equilibrium is very important in some PWM strategies without active NP voltage control (ANPVC). Therefore, if the LFHs are removed from the output voltage, the self-equilibrium ability is lost. Then ANPVC must be provided.

In order to achieve the higher efficiency and reduce the bulk of cooling system, the loss produced by TLI should be considered in some applications. Discontinuous PWM (DPWM) has superiority in reducing loss. In [17], [18], four space vector based DPWM strategies for TLI are presented, namely, DPWM I-IV. In these DPWM strategies, two phase legs have switching actions while the other one phase is clamped to the positive bus (PB) or negative bus (NB) within one control cycle. Compared with continuous PWM strategies, DPWM can reduce switching loss by arranging the discontinuous intervals appropriately. The main difference of DPWM I-IV is the distribution of discontinuous intervals, as shown in Table 1, which makes DPWM I-IV suitable for loads with different power factor, respectively.

TABLE 1. Clamping interval for phase A under different DPWM.

DPWM I	DPWM II	DPWM III	DPWM IV
$\pi/3<\omega t<2\pi/3$	$\pi/2<\omega t<5\pi/6$	$\pi/6<\omega t<\pi/2$	$\pi/6<\omega t<\pi/3$, $2\pi/3<\omega t<5\pi/6$

Although switching loss can be reduced effectively by using DPWM, but there are few studies on NP voltage control based on the background of DPWM. There is larger DC offset and AC ripple on NP voltage under DPWM, which results in more LFHs. In [19], a DPWM method using two different offsets for the NP voltage ripple reduction is proposed, and the effectiveness of the proposed DPWM method is verified by the simulation and the experiment. But the unexpected switching action will appear when different clamping modes switch. To overcome this shortcoming, the modified DPWM with improved PWM sequence is proposed in [20]. In [21], a hybrid modulation strategy is proposed, and hysteresis control is adopted to switch between the two PWM strategies. But the switching loss reduction ability is weakened due to CBPWM being used in some region. In [22], by abandoning the vector with larger common mode voltage based on the space vector diagram, appropriate clamping mode is selected to control NP voltage for NPC TLI. For these DPWM methods, NP voltage is well controlled. However, the switching losses are not optimized.

As stated above, larger DC offset and AC ripple on NP voltage will result in more LFHs, so the reduced LFHs method must be considered under DPWM. However, due to the elimination of LFHs, the self-equilibrium ability of NP voltage is also weakened. To control NP voltage within allowable range, ANPVC is also required.

In this paper, multiple control objectives for NPC TLI are considered. Firstly, a switching loss minimized discontinuous PWM (SLMDPWM) strategy is proposed, which can reduce switching losses as much as possible. While SLMDPWM is applied alone, it found that there are DC offset and AC ripple on NP voltage, which causes LFHs in the output line-to-line voltage. Then, to reduce LFHs, RLFHs is applied. But a new problem is then caused. The self-equilibrium ability is lost, which makes the NP voltage rapidly shift. Therefore, ANPVC is proposed based on the background of DPWM. With that, the multiple control objectives is achieved, which makes the NPC TLI operate with high performances in practice.

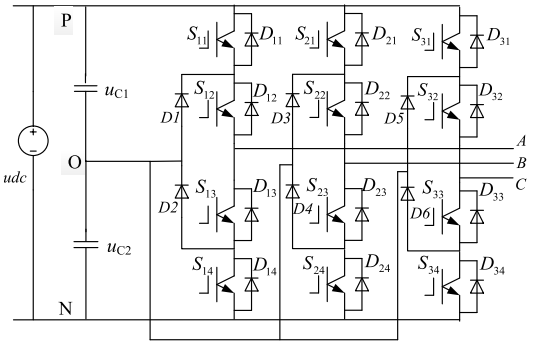


FIGURE 1. The topology of NPC TLI.

II. NPC 3LI AND ITS PWM MODEL

The topology of the NPC TLI is shown in Fig. 1. Each phase consists of four switching devices and two clamping diodes. The NP is selected as a reference point. When the NP voltage is balance, $u_{C1} = u_{C2} = u_{dc}/2$ is satisfied. When S_{X1}(X = 1, 2 or 3) and S_{X2} are on, the output voltage is $u_{C1} = u_{dc}/2$, denoted by P level. When S_{X2} and S_{X3} are on, the output voltage is zero, denoted by O level. When S_{X3} and S_{X4} are on, the output voltage is $-u_{C2} = -u_{dc}/2$, denoted by N level. u_A, u_B, u_C denote the phase voltage; i_A, i_B, i_C denote the output current; C_1 and C_2 denote the upper and lower capacitance.

DPWM can effectively reduce switching loss, which can be realized by clamping a certain phase to the PB, NB or NP. DPWM can be implemented either based on SVPWM through redundant vector assignment or CBPWM through ZSV injection. These two implementations are the same in essential. But the calculation process based on CBPWM can be greatly simplified. The three-phase voltages can be

rearranged as follow:

$$\begin{cases} u_{\max} = \max(u_A, u_B, u_C) \\ u_{\mathrm{mid}} = \mathrm{mid}(u_A, u_B, u_C) \\ u_{\min} = \min(u_A, u_B, u_C) \end{cases} \tag{1}$$

Only the phase corresponding to $u_{\min}$ can be clamped to the NB, the clamping method is named as DPWM_NB and the ZSV is:

$$u_{\mathrm{com\_NB}} = -u_{dc}/2 - u_{\min} \tag{2}$$

Only the phase corresponding to $u_{\max}$ can be clamped to the PB, the clamping method is named as DPWM_PB and the ZSV is:

$$u_{\mathrm{com\_PB}} = u_{dc}/2 - u_{\max} \tag{3}$$

The traditional DPWM I-IV can be achieved by the combination of DPWM_PB and DPWM_NB as shown in Table 2.

TABLE 2. Combination rules for traditional DPWM I-IV.

ωt∈	[0, π/6]	[π/6, π/3]	[π/3, π/2]	[π/2, 2π/3]
DPWM I	DPWM_PB	DPWM_NB	DPWM_NB	DPWM_PB
DPWM II	DPWM_PB	DPWM_PB	DPWM_NB	DPWM_NB
DPWM III	DPWM_NB	DPWM_NB	DPWM_PB	DPWM_PB
DPWM IV	DPWM_NB	DPWM_PB	DPWM_PB	DPWM_NB

On the other hand, when any one phase is clamped to the NP, the clamping method is named as DPWM_NP. This clamping mode is beneficial to switching losses reduction under some conditions, but the applicability is limited by the other two phase voltage. The ZSV for DPWM_NP can be calculated as:

$$\begin{cases} u_{\mathrm{com\_NP1}} = -u_{\max}, & \text{Clamp } u_{\max} \text{ to NP} \\ u_{\mathrm{com\_NP2}} = -u_{\mathrm{mid}}, & \text{Clamp } u_{\mathrm{mid}} \text{ to NP} \\ u_{\mathrm{com\_NP3}} = -u_{\min}, & \text{Clamp } u_{\min} \text{ to NP} \end{cases} \tag{4}$$

The $u'_{\max}, u'_{\mathrm{mid}}, u'_{\min}$ denote the three phase after ZSV injected, one of them is equal $u_{\mathrm{dc}}/2$, 0 or $-u_{\mathrm{dc}}/2$ to clamp corresponding phase to PB, NP or NB.

$$\begin{cases} u'_{\max} = u_{\max} + u_{\mathrm{com}} \\ u'_{\mathrm{mid}} = u_{\mathrm{mid}} + u_{\mathrm{com}} \\ u'_{\min} = u_{\min} + u_{\mathrm{com}} \end{cases} \tag{5}$$

In fact, the condition given below for any clamping mode must be satisfied

$$\begin{cases} u'_{\max} \le u_{dc}/2 \\ u'_{\min} \ge -u_{dc}/2 \end{cases} \tag{6}$$

The duty ratios of u'_X can be calculated as:

$$\begin{cases} d'_{X,P} = 2u'_X/u_{dc}, \\ d'_{X,O} = 1 - 2u'_X/u_{dc} \quad (u'_X \ge 0) \\ d'_{X,N} = 0 \end{cases} \tag{7}$$

$$\begin{cases} d'_{X,P} = 0, \\ d'_{X,O} = 1 + 2u'_X/u_{dc} \quad (u'_X < 0) \\ d'_{X,N} = -2u'_X/u_{dc} \end{cases} \tag{8}$$

III. SLMDPWM

In Section 2, the three clamping modes for NPC TLI and their carrier-based realization are revealed. But which specific clamping mode should be chosen to reduce switching loss as much as possible? This issue will be discussed in this section. Generally, switching action is not wanted in the phase with maximum current. The traditional DPWM I-IV often does not meet this requirement with the variation of modulation index m and power factor angle φ.

In this paper, a new DPWM, i.e. SLMDPWM is proposed, in which the relationship between phase voltage and current is considered with the variation of m and φ to minimize switching loss. The three-phase currents can be rearranged as:

$$\begin{cases} i_{\max} = \max(|i_A|, |i_B|, |i_C|) \\ i_{\mathrm{mid}} = \mathrm{mid}(|i_A|, |i_B|, |i_C|) \\ i_{\min} = \min(|i_A|, |i_B|, |i_C|) \end{cases} \tag{9}$$

In this Section, $u_{\mathrm{i,max}}$denotes voltage of the phase corresponding to $i_{\max}$; $u_{\mathrm{i,mid}}$ denotes voltage of the phase corresponding to i_{mid}; $u_{\mathrm{i,min}}$ denotes voltage of the phase corresponding to $i_{\min}$.

Case1: If $u_{\mathrm{i,max}} = u_{\max}$ or $u_{\min}$, which means that $i_{\max}$ takes place in the phase corresponding to $u_{\max}$ or $u_{\min}$, so DPWM_PB or DPWM_NB should be used to clamp the corresponding phase to PB or NB.

Case 2: If $u_{\mathrm{i,max}} = u_{\mathrm{mid}}$, which means that $i_{\max}$ takes place in the phase corresponding to u_{mid}, so DPWM_NP should be used to clamp this phase to NP. However, over-modulation may be occurred in the phase corresponding to $u_{\max}$ or $u_{\min}$. If over-modulation does happen, $u_{\mathrm{i,mid}} = u_{\min}$ or $u_{\max}$ should be further judged to determine the clamping mode.

The above two conditions can achieve the maximum reduction of switching losses, but the adjusted phase voltage must meet (6). When Case 2 is used, if $u'_{\max} > u_{dc}/2$ or $u'_{\min} < -u_{dc}/2$ takes place, the phase corresponding to u_{mid} cannot be clamped NP otherwise. So, the phase corresponding to i_{mid} should have no switching action in order to reduce switching loss as much as possible. So the clamping state should be reselected between DPWM_PB and DPWM_NB. The rules for SLMDPWM can be stated as follows.

Rule 1: The phase corresponding to $i_{\max}$ can be clamped to PB, NB or NP to ensure that there is no switching action in the phase corresponding to $i_{\max}$.
Rule 2: If Rule 1 cannot be satisfied, the phase corresponding to i_{mid} should have no switching action in order to reduce switching losses.

The flow chart of SLMDPWM based on CBPWM is shown in Fig. 2.

While $m = 0.8$ and $\varphi = 5\pi/12$, the corresponding modulation waves are shown in Fig. 3. The detailed description of stages 1, 2, and 3 are conducted as follows and the other stages of 4 to 10 can be analyzed similarly.

Stage 1: phase B is corresponding to $i_{\max}$ and u_{mid}. If phase B is clamped to NP, over modulation will occur in phase A.

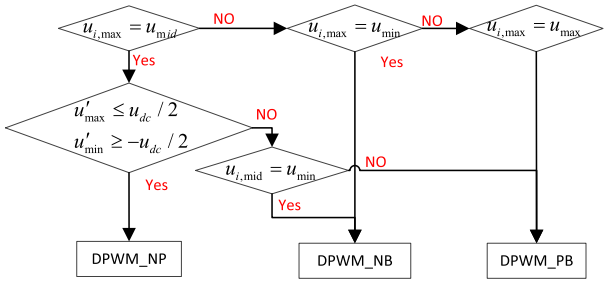


FIGURE 2. The flow chart of SLMDPWM based on CBPWM.

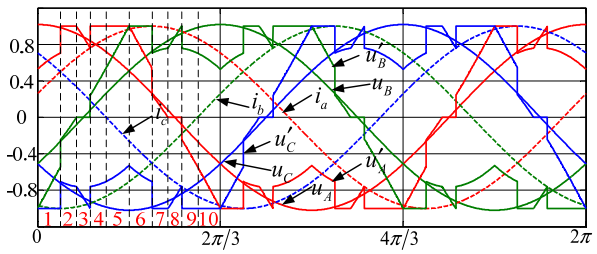


FIGURE 3. The modulation waves for SLMDPWM under $m = 0.8$, $\varphi = 5\pi/12$.

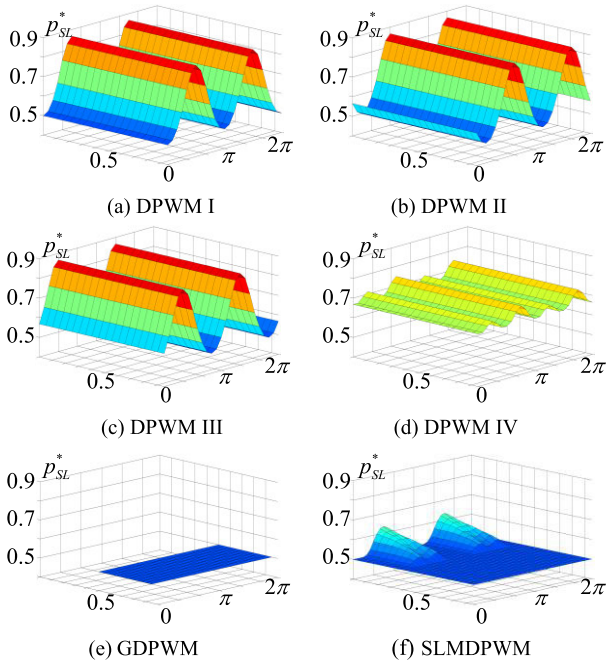


FIGURE 4. Simulation results: P^*_{SL} with respect to m and φ under different PWM strategies.

So phase C corresponding to i_{mid} and $u_{\min}$ should be clamped to NB. Rule 2 is followed in this interval.

Stage 2: phase B is corresponding to $i_{\max}$ and u_{mid}. If phase B is clamped to NP, over modulation will occur in phase A. So phase A corresponding to i_{mid} and $u_{\max}$ should be clamped to PB. Rule 2 is also followed in this interval.

Stage 3: phase B corresponding to $i_{\max}$ and u_{mid} should be clamped to NP. Rule 1 is followed in this interval.

The conduction losses for different DPWMs are approximately equal while the switching losses are quite different from each other. So for the loss analysis, the switching losses are significant and the conduction loss can be neglected. The average switching losses in a fundamental period with variation of m and φ for DPWM I-IV, GDPWM [23] and SLMDPWM can be calculated. Let the switching losses under 7 segments SVPWM as base value, the switching losses under DPWM I-IV, GDPWM and the SLMDPWM can be normalized as following:

$$P^*_{SL} = P_{SL}/P_{SL\_SVPWM} \tag{10}$$

P^*_{SL} with variation of m and φ for different PWM strategies are shown in Fig. 4. It can be seen that the switching losses reduction ability under DPWM I-IV is influenced by specific φ. The switching losses only can be reduced about 13% in worst condition and about 50% in best condition under DPWM I-III. DPWM IV cannot reduce switching loss to half of that under SVPWM, however, when PF is low, its switching losses reduction ability is better than that under DPWM I-III. The switching losses can be reduced about 37% in worst condition and about 50% in best condition under SLMDPWM. The worst condition for SLMDPWM is that $m = 1$ and $\varphi = \pi/2$ or $3\pi/2$. In fact, there is about 85% of region in which the switching losses can be reduced about 50% compared to SVPWM.

It should be noted that P^*_{SL} under GDPWM just has a half region to reduce switching loss about 50%, it is because that GDPWM is only effective when $m < 0.5$ [23]. So SLMDPWM can be seen as an extension of GDPWM.

IV. LFHs CAUSED BY UNBALANCED NP VOLTAGE

The NP voltage is affected when level O is outputted. The average NP current i_{NP} in one carrier cycle can be expressed as

$$i_{NP} = i_A d_{A0} + i_B d_{B0} + i_C d_{C0} \tag{11}$$

When the carrier frequency is significantly higher than the fundamental frequency, the NP voltage change Δu_{NP} can be expressed as:

$$\Delta u_{NP} = \frac{1}{C_1 + C_2} \int i_{NP} dt \tag{12}$$

In the interval $\omega t \in [0, 2\pi]$, the ripple amplitude Δu_{NP_FV} can be expressed as the difference between the maximum NP voltage and the minimum NP voltage:

$$\Delta u_{NP\_FV} = \frac{I_m}{4\pi f (C_1 + C_2)} \Delta u_{NPn} \tag{13}$$

where Δu_{NPn} is the NP voltage ripple factor, which is related to m and φ. It can be used to evaluate the NP voltage ripple under different PWM strategies. Δu_{NPn} for SVPWM, DPWM I-IV and SLMDPWM with the variation of m and φ are given in Fig. 5. The maximum ripple on NP voltage under DPWM I-IV appears when $m = 0.5$ and $\varphi = 0$, approximately.

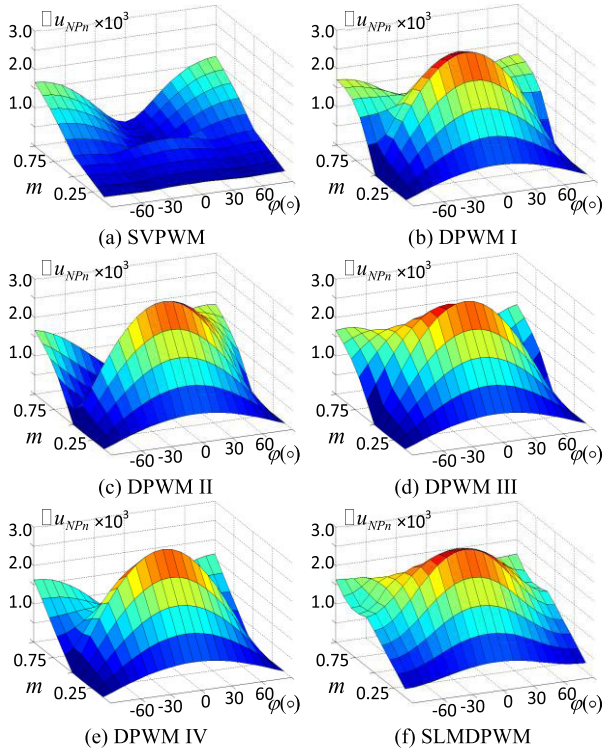


FIGURE 5. Simulation results: Δu_{NPn} with respect to m and φ under different PWM strategies.

And the ripple on NP voltage under SLMDPWM is not higher than that of DPWM I-IV.

When the NP voltage is shifted by Δu_{NP}, the voltages across upper and lower capacitor become $u'_{C1} = u_{dc}/2 - \Delta u_{NP}$ and $u'_{C2} = u_{dc}/2 + \Delta u_{NP}$. Then, the NP should not be taken as the reference point. Taking NB as the reference point, if the duty ratios of every phase are not compensated, the output voltage $\tilde{u}'_X$ of the phase corresponding to $\tilde{u}'_X$ referenced to NB can be expressed as:

$$\tilde{u}'_X = (1 - 2|u'_X|/u_{dc})\Delta u_{NP} + u'_X + u_{dc}/2 \tag{14}$$

So, the line-to-line voltage $\tilde{u}'_{AB}$ can be expressed as:

$$\tilde{u}'_{AB} = u'_A - u'_B + 2(|u'_A| - |u'_B|)\Delta u_{NP}/u_{dc} = u'_{AB} - \Delta u_{AB} \tag{15}$$

When the NP voltage is shifted by Δu_{NP}, it can be seen that the line-to-line voltage is changed. It is very complex to analyze $\tilde{u}'_{AB}$ in this case. Omitting the tedious analysis process, the following conclusions can be drawn.

Fourier analysis shows that there are even-order LFHs in the output line-to-line voltage when there is DC offset on NP voltage and there are odd-order LFHs when there is AC ripple on NP voltage. In fact, the DC offset and AC ripple on NP voltage take place simultaneously, so there are odd-order and even-order LFHs in the output line-to-line voltage. Even-order harmonic voltages will cause even-order harmonic currents, which will favor the self-equilibrium of the NP voltage [7]. However, LFHs are not desired in the output line-to-line voltage, whether even- or odd-order LFHs. Therefore, there are two considerations must be taken into account.

(1) In order to eliminate LFHs in the output line-to-line voltage, which are caused by DC offsets and AC ripples on the NP voltage, the improved PWM strategy must be studied;

(2) While even-order LFHs are removed from the output line-to-line voltage by the improved PWM strategy, the self-equilibrium ability of the NP voltage is thus weakened. Therefore, ANPVC must be provided.

V. RLFHs FOR DPWM UNDER UNBALANCED NP VOLTAGE

From analysis given in Section IV, when the NP voltage is shifted, there are odd-order and even-order LFHs in the output line-to-line voltage if the duty ratios of every phase are not compensated. When the NB is selected as the reference point, considering the maximum utilization of DC bus voltage, the phase voltage is modified as:

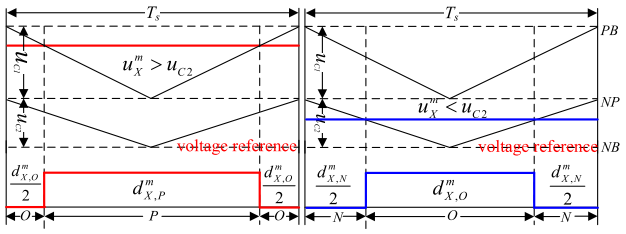
$$u^m_X = u_X + u_{dc}/2 + u_{\text{mid}}/2 \tag{16}$$

Then the duty ratios for u^m_X can be calculated as

$$\begin{cases} d^m_{X,P} = (u^m_X - u_{C2})/u_{C1} \\ d^m_{X,O} = 1 - d^m_{X,P} \\ d^m_{X,N} = 0 \end{cases} \quad (u^m_X \geq u_{C2})$$

$$\begin{cases} d^m_{X,P} = 0 \\ d^m_{X,O} = u^m_X/u_{C2} \\ d^m_{X,N} = 1 - d^m_{X,O} \end{cases} \quad (u^m_X < u_{C2}) \tag{17}$$

When the NP voltage is shifted, the modulation methods are shown in Fig. 6. After modified three-phase voltages u^m_A, u^m_B, u^m_C are arranged according to (1). The phase corresponding to $u^m_{\max}$, $u^m_{\min}$ and u^m_{mid} can be clamped to PB, NB and NP under DPWM_PB, DPWM_NB and DPWM_NP, respectively, where $u_{dc} - u^m_{\max}$, $-u^m_{\min}$ and $u_{C2} - u^m_{\text{mid}}$ correspond to the ZSVs.



(a) $u^m_X > u_{C2}$ (b) $u^m_X < u_{C2}$

FIGURE 6. The modulation method under unbalanced NP voltage.

Take DPWM_PB as an example, the three phases voltages with ZSV injected can be rewritten as:

$$\begin{cases} u'^m_{\max} = u^m_{\max} + u_{dc} - u^m_{\max} = u_{dc} \\ u'^m_{\text{mid}} = u^m_{\text{mid}} + u_{dc} - u^m_{\max} = u_{dc} + u^m_{\text{mid}} - u^m_{\max} \\ u'^m_{\min} = u^m_{\min} + u_{dc} - u^m_{\max} = u_{dc} + u^m_{\min} - u^m_{\max} \end{cases} \tag{18}$$

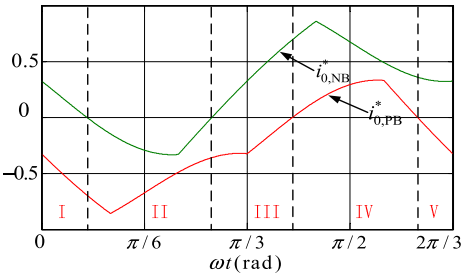


FIGURE 7. $i^*_{0,PB}$ and $i^*_{0,NB}$ in $\omega t \in [0, 2\pi/3]$ when $m = 0.9$ and $\varphi = \pi/3$.

Combining (17), the modified duty ratios can be acquired. Take $u'^m_{\max} = u_{dc}, u'^m_{\text{mid}} > u_{C2}, u'^m_{\text{mid}} < u_{C2}$ as an example, the modified duty ratios can be acquired as:

$$\begin{aligned}
&d'^m_{\max,P} = 1, \quad d'^m_{\max,O} = 0, \quad d'^m_{\max,N} = 0 \\
&d'^m_{\text{mid},P} = \frac{u_{dc} + u_{\text{mid}} - u_{\max} - u_{C2}}{u_{C1}}, \\
&d'^m_{\text{mid},O} = 1 - d'^m_{\text{mid},P}, \quad d'^m_{\text{mid},N} = 0 \\
&d'^m_{\min,P} = 0, \quad d'^m_{\min,O} = \frac{u_{dc} + u_{\min} - u_{\max}}{u_{C2}}, \\
&d'^m_{\min,N} = 1 - d'^m_{\min,O}
\end{aligned} \tag{19}$$

Then, the line-to-line voltage can be obtained as:

$$\begin{aligned}
&u'^m_{\max} - u'^m_{\text{mid}} \\
&\quad = (d'^m_{\max,P} - d'^m_{\text{mid},P})u_{dc} + (d'^m_{\max,O} - d'^m_{\text{mid},O})u_{C2} \\
&\qquad +(d'^m_{\max,N} - d'^m_{\text{mid},N})0 \\
&\quad = u_{\max} - u_{\text{mid}} \\
&u'^m_{\text{mid}} - u'^m_{\min} \\
&\quad = (d'^m_{\text{mid},P} - d'^m_{\min,P})u_{dc} + (d'^m_{\text{mid},O} - d'^m_{\min,O})u_{C2} \\
&\qquad +(d'^m_{\text{mid},N} - d'^m_{\min,N})0 \\
&\quad = u_{\text{mid}} - u_{\min}
\end{aligned} \tag{20}$$

From (20), it can be seen that the line-to-line voltage remains the same although NP voltage is shifted. That means the LFHs is removed from the output line-to-line voltage.

The same conclusions can be drawn while DPWM_NB or DPWM_NP is applied. Therefore, after modifying duty ratios, the LFHs caused by unbalanced NP voltage can be eliminated in theory.

VI. ACTIVE NP VOLTAGE CONTROL FOR SLMDPWM

When RLFHs is used, the even-order LFHs are removed from the output line-to-line voltage. And the self-equilibrium ability of NP voltage is thus weakened. The NP voltage will be shifted rapidly. Therefore, ANPVC is needed, and it is also implemented based on the background of DPWM. The positive direction of NP current is defined as flowing from the NP. Therefore, the positive NP current make NP voltage decrease and the negative NP current make NP voltage increase.

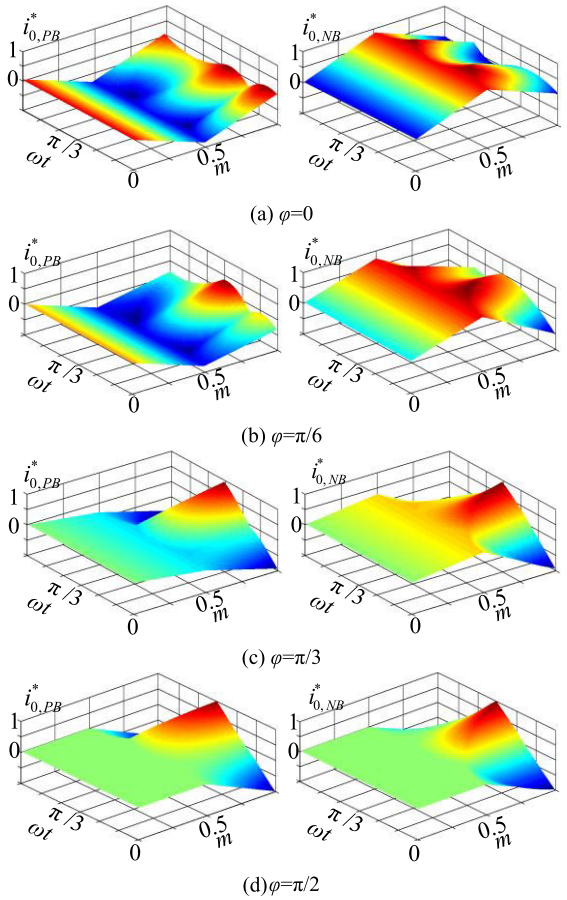


FIGURE 8. $i^*_{0,PB}$ and $i^*_{0,NB}$ in $\omega t \in [0, 2\pi/3]$ under different φ and $m \in [0, 1]$.

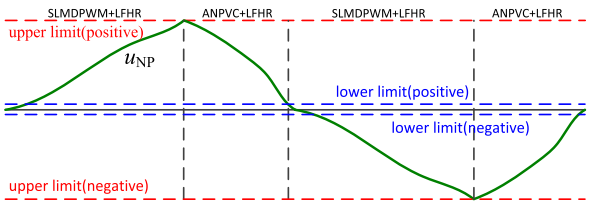


FIGURE 9. The hysteresis control logic for the ANPVC.

The average NP current in one control cycle can be expressed as:

$$i_0 = \sum_{X=a,b,c} i_X d'_{X,O} = I_m \sum_{X=a,b,c} i_X d'_{X,O} = T_s I_m i^*_0 \tag{21}$$

where, i^*_0 denotes the per-unit average value of NP current, and the real average value i_0 can be obtained by multiplying i^*_0 with I_m. The $i^*_{0,PB}$, $i^*_{0,NP}$ and $i^*_{0,NB}$ denote the per unit value of NP current under DPWM_PB, DPWM_NP and DPWM_NB modes.

When $m < 0.5$, the NP current is relative simple. ANPVC for DPWM can be achieved by choosing DPWM_PB or DPWM_NB properly according to the active power handled TLI.

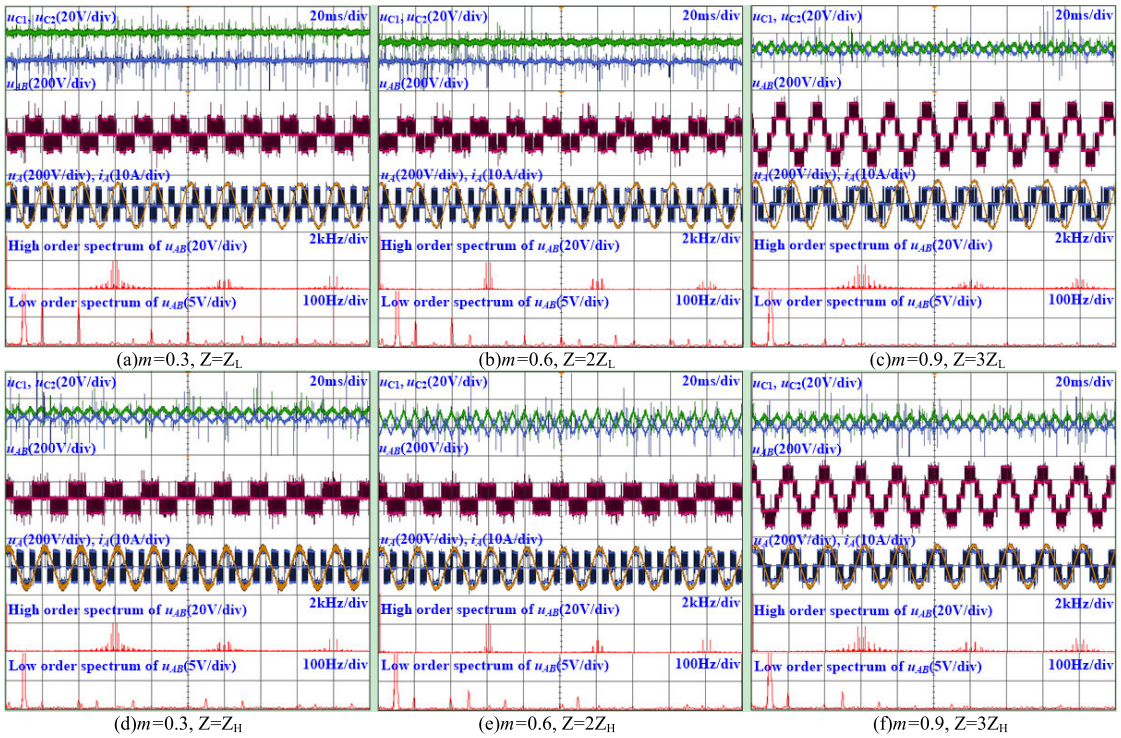


FIGURE 10. The steady-state experimental results for DPWM I under different m and φ.

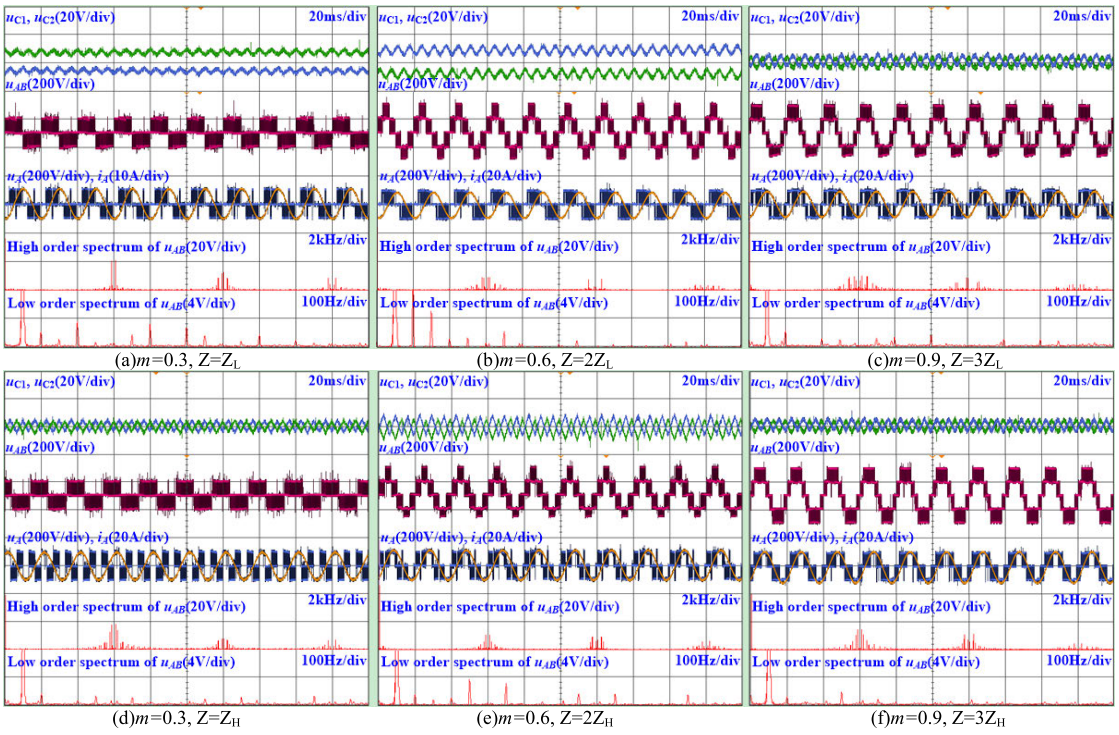
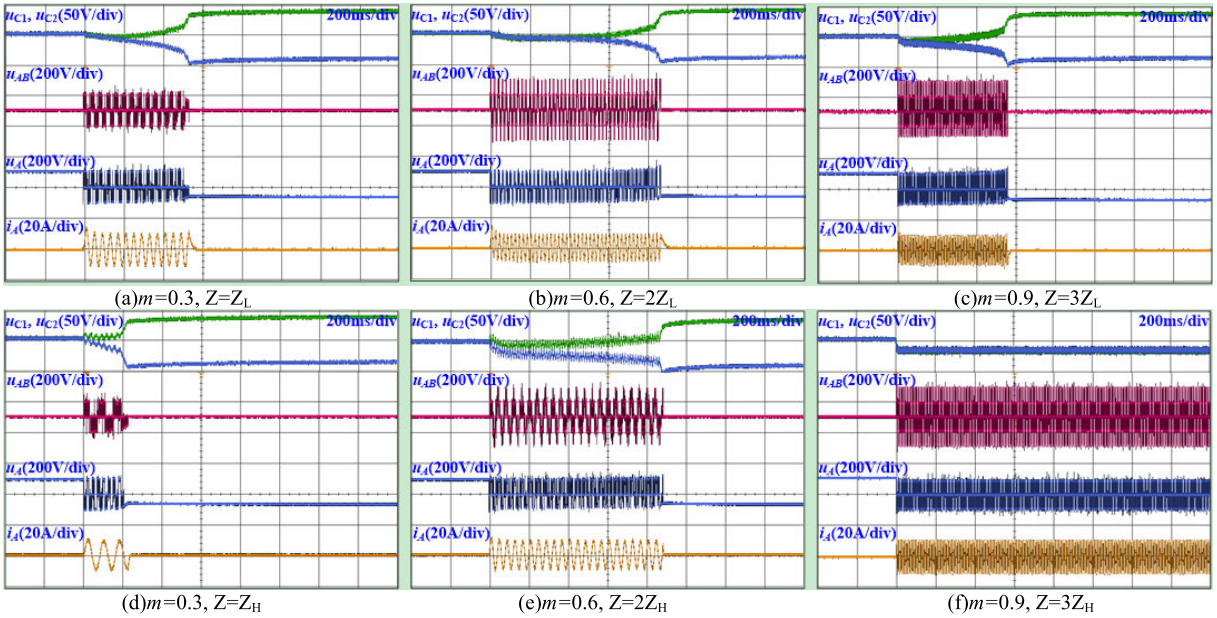


FIGURE 11. The steady-state experimental results for SLMDPWM under different m and φ.

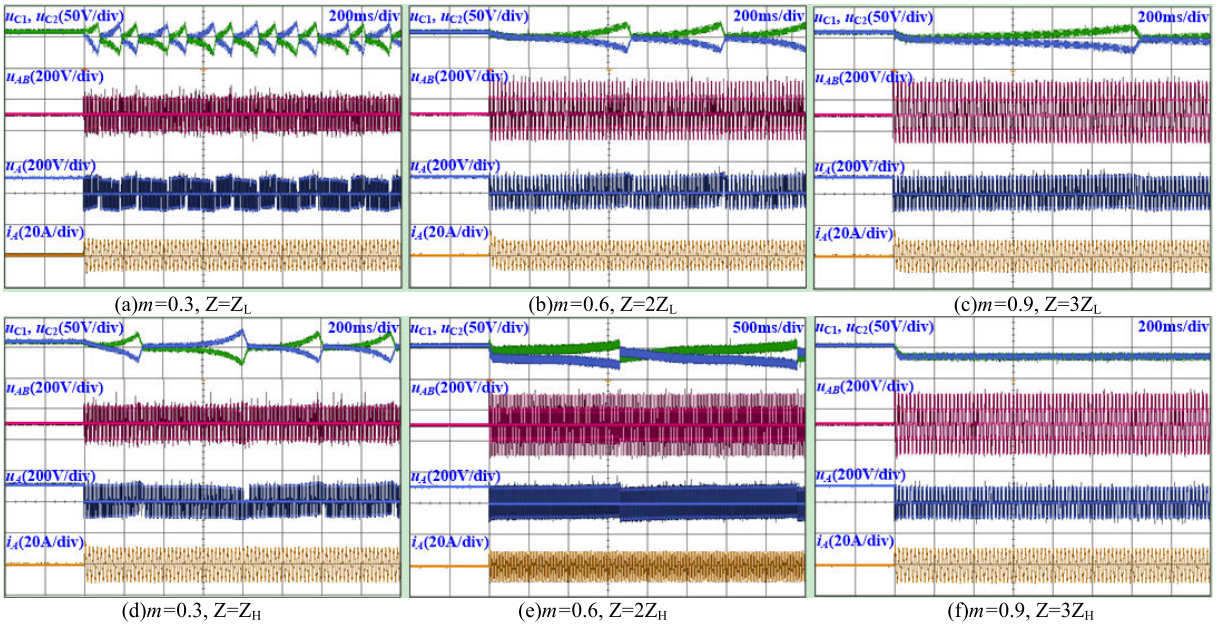
When $m > 0.5$, DPWM_PB or DPWM_NB should be used. Fig. 7 shows the curves of $i^*_{0,\mathrm{PB}}$ and $i^*_{0,\mathrm{NB}}$ in $\omega t \in [0, 2\pi/3]$ when $m = 0.9$ and $\varphi = \pi/3$. $i^*_{0,\mathrm{PB}}$ and $i^*_{0,\mathrm{NB}}$ in the intervals of $\omega t \in [2\pi/3, 4\pi/3]$ and $\omega t \in [4\pi/3, 2\pi]$ are similar. When $\varphi = 0, \pi/6, \pi/3$ and $\pi/2$, the $i^*_{0,\mathrm{PB}}$ and $i^*_{0,\mathrm{NB}}$ for $m \in [0, 1]$ are shown in Fig. 8. When $t_1 > 2\pi/3\omega$,



(a)m=0.3, Z=Z_L (b)m=0.6, Z=2Z_L (c)m=0.9, Z=3Z_L

(d)m=0.3, Z=Z_H (e)m=0.6, Z=2Z_H (f)m=0.9, Z=3Z_H

FIGURE 12. The experimental results of start process for SLMDPWM with RLFHs but without ANPVC under different m and φ.



(a)m=0.3, Z=Z_L (b)m=0.6, Z=2Z_L (c)m=0.9, Z=3Z_L

(d)m=0.3, Z=Z_H (e)m=0.6, Z=2Z_H (f)m=0.9, Z=3Z_H

FIGURE 13. The experimental results of start process for SLMDPWM with RLFHs and ANPVC under different m and φ.

the integral of $i^*_{0,\mathrm{PB}}$ and $i^*_{0,\mathrm{NB}}$ satisfy with:

$$\begin{cases} \int_0^{t_1} i^*_{0,\mathrm{PB}} dt > 0, & \text{when } \cos\varphi{>}0 \\ \int_0^{t_1} i^*_{0,\mathrm{NB}} dt < 0, & \text{when } \cos\varphi{>}0 \\ \int_0^{t_1} i^*_{0,\mathrm{PB}} dt < 0, & \text{when } \cos\varphi < 0 \\ \int_0^{t_1} i^*_{0,\mathrm{NB}} dt > 0, & \text{when } \cos\varphi < 0 \end{cases} \tag{22}$$

(22) means that the NP voltage can be adjusted by using DPWM_PB or DPWM_NB if the time of every clamping mode is long enough. So, ANPVC can be simply acquired as:

$$\begin{cases} \text{DPWM\_PB is used}, & \Delta u_{NP} > 0, \cos\varphi > 0 \\ \text{DPWM\_NB is used}, & \Delta u_{NP} < 0, \cos\varphi > 0 \\ \text{DPWM\_NP is used}, & \Delta u_{NP} < 0, \cos\varphi < 0 \\ \text{DPWM\_PB is used}, & \Delta u_{NP} > 0, \cos\varphi < 0 \end{cases} \tag{23}$$

To achieve ANPVC, NP voltage hysteresis control logic is adopted to switch between SLMDPWM and ANPVC, as shown in Fig. 9. The hysteresis threshold is determined

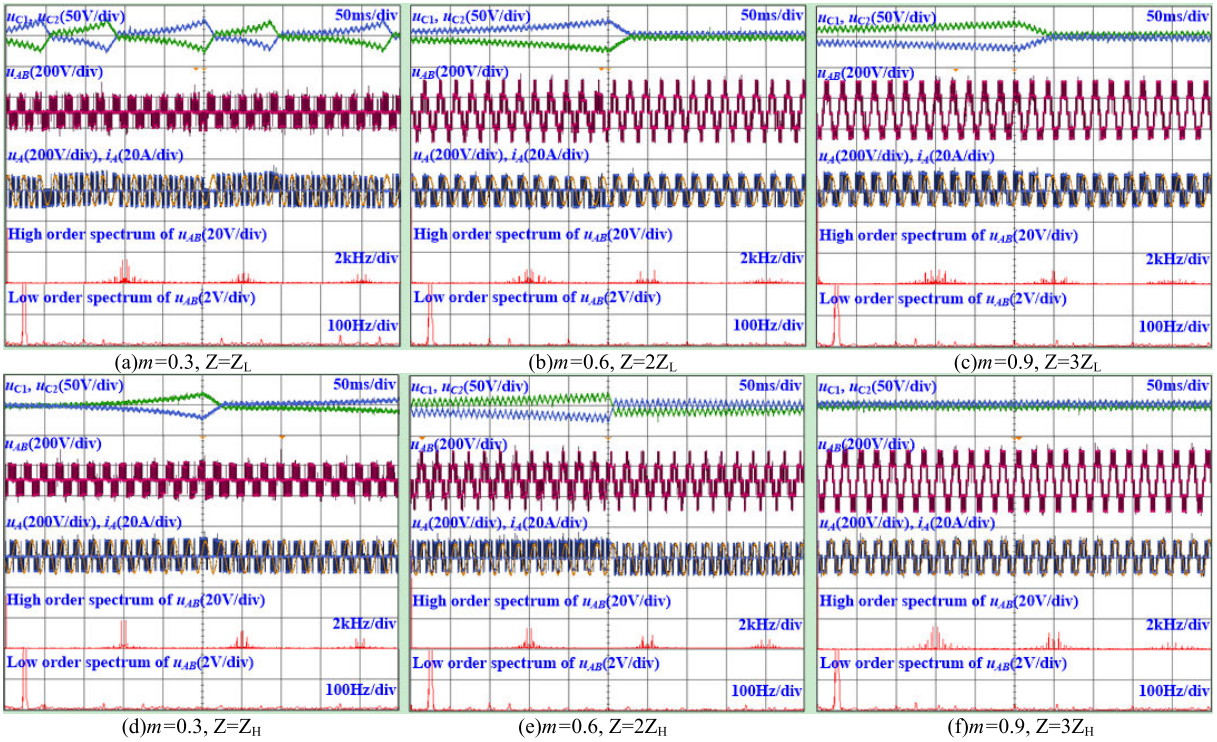


FIGURE 14. The steady state experimental results for SLMDPWM with RLFHs and ANPVC under different m and φ.

by the allowable shifted NP voltage. When the NP voltage reaches the allowable upper limit, ANPVC is active until the NP voltage is lower than the predefined lower limit. The controller switches between the two operations modes to generate the corresponding PWM sequences.

VII. EXPERIMENTS

The feasibility of the proposed method in this paper has been verified through experiments. The system parameters are listed in Table 3. Because of modulation strategy is focused on, open-loop control is applied in the experiments for fair comparison to avoid the potential effect by control loop.

TABLE 3. Parameters of the system.

parameter	value
dc-link voltage	200V
upper and lower dc-link capacitor	1000μF
resistive-inductive load for high pf (Z_H)	$2.8e^{j6.4^\circ}\Omega$
resistive-inductive load for low pf (Z_L)	$2.8e^{j83.6^\circ}\Omega$
switching frequency	6000Hz
fundamental frequency	50Hz

A. EXPERIMENTS FOR SLMDPWM

The steady-state experimental results of DPWM I and SLMDPWM under different m and φ are shown in Figs. 10 and 11, respectively. From the phase voltage of u_A, it found that it is clamped to PB and NB alternately, and the clamping interval is constant for DPWM I although under different conditions, but that is quite different for SLMDPWM. For SLMDPWM, besides PB and NB, u_A may be also clamped to NP, and the clamping interval is variable. As shown in Fig. 11, Rule 1 is satisfied for most conditions, and u_A corresponding to peak phase current is just clamped to PB, NB or PB, which can reduce switching losses as much as possible. But in Fig. 11(c), Rule 2 is satisfied, and u_A corresponding to peak phase current cannot be clamped to NP, that is because over-modulation will result in with the increase of m.

Moreover, as shown in Figs. 10 and 11, there are AC ripple and DC offset on NP voltage, and abundant LFHs in output line-to-line voltage, especially under low m and low PF, which are consistent with the theoretical analysis. When the DC offset is dominated on NP voltage, LFHs are mainly even-order harmonics; when the AC ripple is dominated on NP voltage, LFHs are mainly odd-order harmonics. Comparing to DPWM I, the AC ripple becomes larger and the spectrum characteristics are relatively worse under SLMDPWM. Although its performances are not fine, the NPC TLI can work continuously.

B. EXPERIMENTS FOR SLMDPWM WITH RLFHS AND ANPVC

The experimental results for SLMDPWM with RLFHs but without ANPVC are shown in Fig. 12. It can be seen that the NP voltage is gradually shifted during the start process. When the NP voltage offset protection is triggered, the NPC

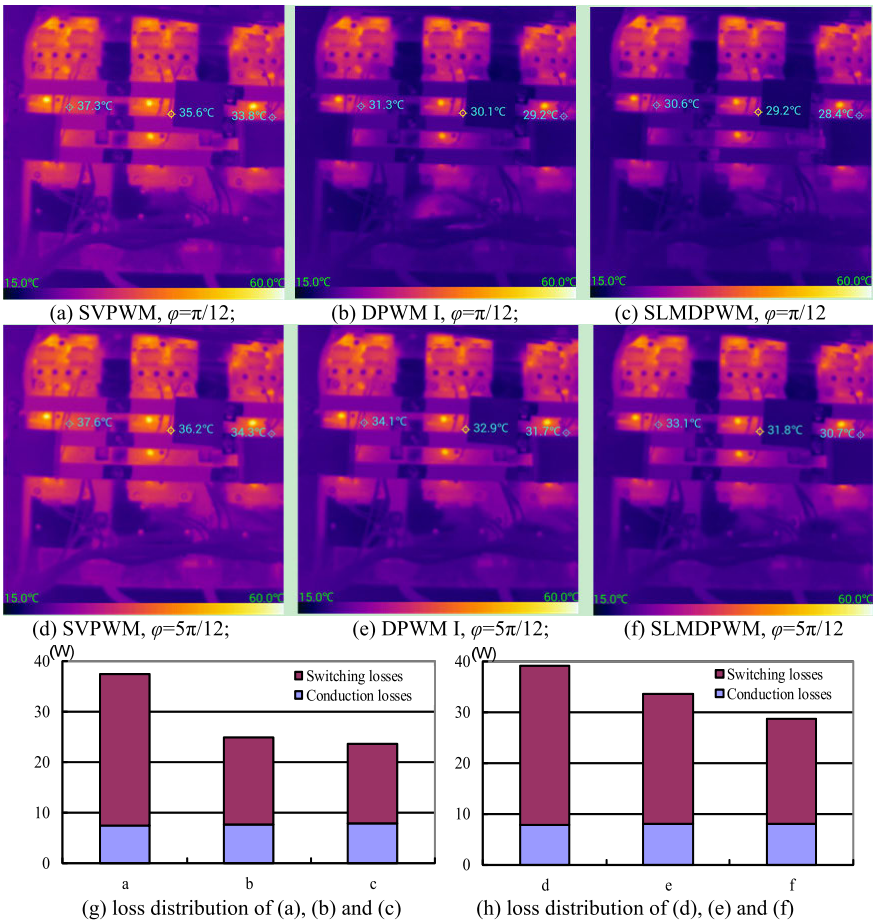


FIGURE 15. The infrared thermal images and loss distribution under different PWM strategies.

TLI stops working. It indicates that SLMDPWM only with RLFHs cannot be used in practice, which is consistent with the theoretical analysis.

When the $m = 0.9$, $\varphi = 6.4°$, there is no obvious shift on NP voltage although SLMDPWM with RLFHs is used. That is because very small even-order harmonic current is sufficient to ensure self-equilibrium in this case. But this mechanism may be unstable and ANPVC is still needed.

The experimental results for SLMDPWM with RLFHs and ANPVC are shown in Fig. 13. It can be seen that NP voltage is always gradually shifted, and the shifting speed is related to the operation conditions. When the offset reaches the upper limit, ANPVC is intervened to quickly recover NP voltage. The process is repeated and the NP voltage can be controlled within an acceptable range.

The steady state experimental results for SLMDPWM with RLFHs and ANPVC are shown in Fig. 14. By comparing the spectrum of output line-to-line voltage u_{AB} shown in Figs. 11 and 14, it can be seen that LFHs are effectively reduced in Fig. 14. Moreover, from Fig. 14, it found that the ANPVC process is short, so SLMDPWM is applied most of the time. That means the low switching losses can be obtained almost the same with that only using SLMDPWM.

C. TEMPERATURE RISING FOR DIFFERENT PWM STRATEGIES

At the same environmental temperature and cooling condition, the infrared thermal images for different PWM strategies including SVPWM, DPWM I and SLMDPWM after two hours operation are shown in Fig. 15, where the results under the conditions of $m = 0.8$ and 10A rms phase current for $\varphi = \pi/12$ and $5\pi/12$ are given, respectively. Regardless of $\varphi = \pi/12$ and $\varphi = 5\pi/12$, arranged in descending order of the temperature rising, SVPWM, DPWM I and SLMDPWM are listed. It indicates that SLMDPWM can effectively reduce switching losses and temperature rising of the system.

From the experimental results, it can be seen that:

(1) While SLMDPWM is applied, there are AC ripple and DC offset on NP voltage, which causes LFHs.

(2) If SLMDPWM with RLFHs is used, since the even-order LFHs are removed from output line-to-line voltage, the self-equilibrium capability of NP voltage is weakened. The NP voltage is rapidly shifted and the NPC TLI cannot work continuously.

(3) When SLMDPWM with LFHR and ANPVC is used, the TLI can work continuously; the LFHs are reduced

TABLE 4. Comparisons of different DPWMs.

	DPWMI-IV	SLMDPWM	SLMDPWM+RLFHs	SLMDPWM+RLFHs+ANPVC
reduction of switching loss	low	high	high	almost to SLMDPWM
self-equilibrium of the NP voltage	yes	yes	no	no
low frequency harmonics	yes	yes	no	no
active NP voltage control	no	no	no	yes
long time operation ability	yes	yes	no	yes

significantly. And the offset on NP voltage is limited within allowable range.

(4) The switching loss reduction ability of SLMDPWM with LFHR and ANPVC is prior to the traditional DPWM.

Finally, the comparisons of different DPWMs are listed in Table 4. It can be seen that the proposed SLMDPWM with RLFHs and ANPVC can achieve multiple control objectives, which makes NPC TLI possessing more practical performances.

VIII. CONCLUSION

In this paper, SLMDPWM is proposed to reduce switching losses of NPC TLI as much as possible. But there are DC offset and AC ripple on NP voltage, which causes LFHs in the output line-to-line voltage. So, RLFHs method is proposed to suppress LFHs. However, the self-equilibrium capability of NP voltage is then weakened. The NP voltage is rapidly shifted and the TLI cannot work continuously. Thus, ANPVC is also proposed to control NP voltage. With that, the NP voltage can be controlled within an allowable range, but there are no LFHs in the output line-to-line voltage. Finally, multiple control objectives are achieved. The proposed method may be very suitable for the applications where switching losses and harmonics are strictly required.

REFERENCES

[1] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] H. Aburub, J. Holtz, and J. Rodriguez, "Medium-voltage multilevel converters-state of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron*, vol. 57, no. 8, pp. 2581–2596, Dec. 2010.

[4] W. Chen, H. Sun, X. Gu, and C. Xia, "Synchronized space-vector PWM for three-level VSI with lower harmonic distortion and switching frequency," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6428–6441, Sep. 2015.

[5] C. Xia, X. Gu, T. Shi, and Y. Yan, "Neutral-point potential balancing of three-level inverters in direct-driven wind energy conversion system," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 18–29, Apr. 2011.

[6] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1582–1588, Dec. 2005.

[7] J. Shen, S. Schröder, R. Rösner, and S. El-Barbari, "A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3084–3095, Nov. 2011.

[8] S. Busquets-Monge, J. D. Ortega, J. Bordonau, J. A. Beristain, and J. Rocabert, "Closed-loop control of a three-phase neutral-point-clamped inverter using an optimized virtual-vector-based pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 2061–2071, May 2008.

[9] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Nearest-vector modulation strategies with minimum amplitude of low-frequency neutral-point voltage oscillations for the neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4485–4499, Oct. 2013.

[10] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2262–2271, Jul. 2010.

[11] J. Shen, S. Schroder, B. Duro, and R. Roesner, "A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 138–148, Jan./Feb. 2013.

[12] S. Sangwong wanich, "Double-carrier-based modulation theory of three-level inverters and a new discontinuous PWM for neutral-point voltage balancing," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Oct. 2012, pp. 4961–4966.

[13] R. Maheshwari, S. Munk-Nielsen, and S. Busquets-Monge, "Design of neutral-point voltage controller of a three-level NPC inverter with small DC-link capacitors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1861–1871, May 2013.

[14] P. Chaturvedi, S. Jain, and P. Agarwal, "Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 613–624, Feb. 2014.

[15] J. Lyu, W. Hu, F. Wu, K. Yao, and J. Wu, "Variable modulation offset SPWM control to balance the neutral-point voltage for three-level inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7181–7192, Dec. 2015.

[16] J.-S. Lee and K.-B. Lee, "Time-offset injection method for neutral-point AC ripple voltage reduction in a three-level inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1931–1941, Mar. 2016.

[17] C. Xia, G. Zhang, Y. Yan, X. Gu, T. N. Shi, and X. N. He, "Discontinuous space vector PWM strategy of neutral-point-clamped three-level inverters for output current ripple reduction," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5109–5121, Jul. 2017.

[18] A. R. Beig, S. Kanukollu, K. A. Hosani, and A. Dekka, "Space-vector-based synchronized three-level discontinuous PWM for medium-voltage high-power VSI," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 3891–3901, Aug. 2014.

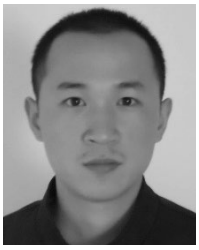
[19] J.-S. Lee, S. Yoo, and K.-B. Lee, "Novel discontinuous PWM method of a three-level inverter for neutral-point voltage ripple reduction," *IEEE Trans. Ind. Electron*, vol. 63, no. 6, pp. 3344–3354, Jun. 2016.

[20] W. Jiang, L. Li, J. Wang, M. Ma, F. Zhai, and J. Li, "A novel discontinuous PWM strategy to control neutral point voltage for neutral point clamped three-level inverter with improved PWM sequence," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9329–9341, Sep. 2019.

[21] W. Jiang, Y. Gao, J. Wang, and L. Wang, "A hybrid modulation strategy with reduced switching losses and neutral point potential balance for three-level NPC inverter," *J. Elect. Eng. Technol.*, vol. 12, no. 2, pp. 738–750, Mar. 2017.

[22] J. Wang, F. Zhai, J. Wang, W. Jiang, J. Li, L. Li, and X. Huang, "A novel discontinuous modulation strategy with reduced common-mode voltage and removed DC offset on neutral-point voltage for neutral-point-clamped three-level converter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7637–7649, Aug. 2019.

[23] S. Bhattacharya, D. Mascarella, and G. Joos, "Space-vector-based generalized discontinuous pulsewidth modulation for three-level inverters operating at lower modulation indices," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 912–924, Jun. 2017.



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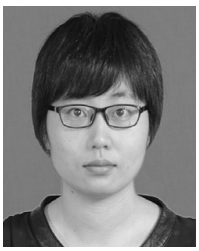

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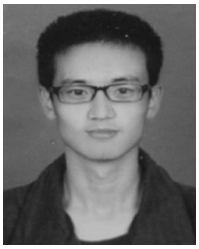

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