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A Seizure-Based Power Reduction SoC for Wearable EEG in Epilepsy

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ABSTRACT Epilepsy is one of the most common serious brain disorders affecting 1% of the world population. Epileptic seizure events are caused by abnormal excessive neuronal activity in the brain, which may be associated with behavioural changes that severely affect the patients' quality of life. These events are manifested as abnormal activity in electroencephalography (EEG) recordings of individuals with epilepsy. This paper presents the on-chip implementation of an algorithm that, operating on the principle of data selection applied to seizures, would be able to reduce the power consumption of EEG devices, and consequently their size, thereby significantly increasing their usability. In order to reduce the power consumed by the on-chip implementation of the algorithm, mathematical approximations have been carried out to allow for an analog implementation, resulting in the power consumed by the system to be negligible in comparison to other blocks in an EEG device. The system has been fabricated in a 0.18 μm CMOS process, consumes 1.14 μW from a 1.25 V supply and achieves a sensitivity of 98.5% while only selecting 52.5% of the EEG data for transmission.

INDEX TERMS Seizure, epilepsy, electroencephalography (EEG), System-on-Chip (SoC), seizure detection.

I. INTRODUCTION

Epilepsy is a serious neurological condition affecting more than 1% of the world population. It is characterized by seizure episodes resulting from abnormal brain activity that affects quality of life of patients. Recurring seizures can result in reduced activities related to the patient's work, educational and social life [1]. Despite the significant consequences of epilepsy, almost 25% of patients are misdiagnosed [2].

The diagnosis of epilepsy often involves the use of electroencephalography (EEG) to monitor the brain activity of patients. Seizures can be infrequent events, occuring in the space of weeks or months, and about two-thirds of patients have between 1 and 12 seizures a year [3]. Long-term EEG monitoring is therefore desirable in order to capture epileptic traces and to increase the diagnostic yield [4]. Continuous EEG recordings carried out in hospital settings are costly and the secluded setup reduces the patient exposure to seizure provoking factors that may have otherwise resulted in seizures being recorded. Recordings can be carried out in a home setting using Ambulatory EEG (AEEG) units. However, AEEG units in their current form have a number of shortcomings [5], [6], including their bulkiness, heaviness (over 500 g) and short battery lifetime (less than 3 days).

The creation of truly Wearable EEG (WEEG) systems would allow for the long term monitoring of patients in the comfort of their natural environment. By monitoring patients in their own environment, as opposed to a clinical setup, patients can be exposed to stimuli that would provoke the seizure activity under investigation.

The WEEG system must maintain key features including wireless connectivity, miniature size, light-weight and low power consumption, while complying with medical regulatory standards such as those provided by the International Federation of Clinical Neurophysiology (IFCN) [7] and International Electrotechnical Commission (IEC) [8] to ensure the clinical-grade gathering of EEG signals and patient safety. Wireless connectivity of the WEEG system to a base station (e.g. mobile phone or tablet) is desirable to avoid long wired connections that may limit patient movement during the monitoring period. The WEEG system ergonomics and wireless connectivity features are also important from a privacy standpoint, since wearing a larger device with long wires may make apparent the user's health condition. Low-power operation of

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the WEEG system is essential in order to achieve long-term monitoring, without interruption, from miniature batteries limited by the mentioned size and weight considerations. Extending the battery lifetime through low-power operation of the WEEG system would also mitigate the inconvenience and risks associated with recharging or replacement of batteries by untrained users.

The WEEG system architecture would at least contain an Instrumentation Amplifier (IA), Analog to Digital Converter (ADC) and a transmitter [9]. A power analysis carried out in [10] for a 32 channel EEG system using state-of-the-art IAs, ADCs and transmitter modules revealed that due to the continuous transmission of raw EEG signals, the power consumed by the transmitter would account for 97% of the total power consumption of the EEG system. In the context of epilepsy monitoring, a number of recently published works, focusing on treatment rather than diagnosis, targeted a reduction on the communication cost by detecting seizures locally. A reduction of 14× in system power consumption has been achieved in the work of [11]. This system transmits feature-vectors, rather than raw EEG signals, and seizure detection is performed in the software domain using the extracted features. Feature Extraction (FE) is carried out in the seizure detection System-on-Chip (SoC) of [12] by deriving the spectral energy distribution of the input EEG signal prior to the classification stage. The SoC utilizes a Non-Linear Support Vector Machine (NLSVM) classifier to perform the patient-specific seizure classification, while consuming 19.6 μW/channel (FE + classification). The implantable seizure detection system of [13] is designed based on counters that detect high frequency activity while consuming 1.5 μW/channel. The system uses parameters that must be tuned specifically to each patient. An implantable seizure detector utilizing signal entropy and frequency spectrum based feature extraction together with a Linear Least Square (LLS) classifier has been reported in [14]. The SoC requires patient-specific training and achieves a power consumption figure of 162.31 μW/channel. The patient-specific and implantable seizure detector of [15] uses the line length feature to discriminate between seizures and background activity, subsequent to compressive sensing and digitization stages, while performing seizure classification using a thresholding scheme. The SoC consumes 0.85 μW/channel. Seizure events are detected in the implantable seizure counting system of [16] by deriving the input signal energy in different frequency bands. A lookup table is also generated during a patient-specific training phase, and is used to match the measured energy values with the probability of seizure occurrence. The power consumed by the seizure detector is 0.45 μW/channel. All these patient-specific approaches to detect seizure occurence ([11]–[16]) focus on the real-time treatment of epilepsy through closed-loop instantaneous seizure suppression and symptom alleviation. Patient-specific approaches can be utilized in systems intended for epilepsy treatment since patients requiring such systems have already been diagnosed with epilepsy and therefore the gathered EEG data, which is known to contain seizure activity, can be used for training the seizure detection algorithms.

This paper presents a scalable EEG data selection SoC targeting a different aspect of epilepsy, which is the diagnosis stage, for which the previously mentioned approaches are unsuitable. The mentioned seizure detection systems require a training phase using patient-specific EEG data containing marked seizure events, which may be available during the post-diagnosis stage. Such patient-specific data is, however, not readily available during the diagnosis stage.

The system presented in this paper reduces the amount of data to be transmitted by a WEEG device by continuously selecting sections of EEG data containing *likely* seizure activity. In other words, the system aims not to '*lose*' seizure related sections of recorded signal that are important for the neurologist to see to make a diagnosis; whilst at the same time still reducing the amount of data that needs to be transmitted in order to significantly reduce the overall power consumed by the WEEG device. Note that reviewing raw and relevant EEG data is currently considered to be important for neurologists during the diagnostic process. As an illustration, a survey of neurologists, carried out in [5], revealed that the majority of respondents would not trust systems performing 'automated diagnosis', i.e. systems that would automatically mark clinical events without the intervention of neurologists during the diagnosis stage. In contrast, a large portion of the surveyed neurologists were in favour of systems that would reduce the amount of EEG data presented to them. It is also important to note that the process of manually reviewing raw EEG data by neurologists is time consuming, taking approximately 2 h per 24 h of recordings [17]. Hence, this approach, has the advantages of simultaneously reducing the power of the EEG system, but also the amount of time required by neurologists to review the transmitted EEG data, since it still gives them access to the clinically relevant seizure information, whilst eliminating large amounts of recorded brain signal that has nothing diagnostically important in them. Furthermore, because of its very low power consumption, the system presented in this paper could also be used in the WEEG system in combination with others which focus on selecting other relevant but also, in some cases, important diagnostic biomarkers, such as interictal spikes [10].

The remainder of this paper has been organised as follows. The concept of data selection in WEEG devices and epilepsy monitoring has been explained in Section II. This is followed by Section III, in which the system architecture together with the circuits blocks used in the system have been presented. The front-end and control circuitry are discussed in Section IV. Subsequently, measurement and performance results of the fabricated chip have been presented in Section V.

II. SEIZURE SELECTION

The complexity of the data selection system should be kept to a minimum to allow for the power consumed by this stage to remain negligible compared to the other blocks in the WEEG

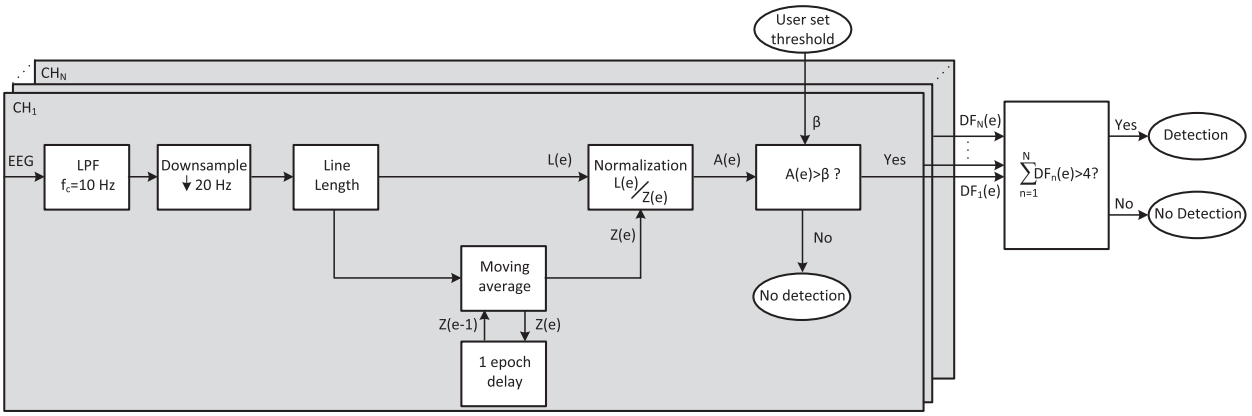

FIGURE 1. Overview of data selection algorithm.

unit. The system presented in this work utilizes the algorithm proposed in [18], as a foundation. The algorithm operates based on the concept of discontinuous recording [5], in which sections of raw EEG data containing clinically interesting events are selected while background EEG is discarded. The main operation of the algorithm has been illustrated in Fig. 1. The EEG input to each channel of the algorithm is initially high pass filtered with a cutoff frequency of 0.16 Hz. The following decimation block includes a third order low pass filter to strongly attenuate the signal frequency components above 10 Hz and allow for downsampling the input signal to 20 Hz, while avoiding distortion resulting from aliasing. The downsampled signal is used during the line length feature extraction in the form of 2 s non-overlapping windows of EEG data. The mentioned windows of data are hereon referred to as 'epochs'. The line length is calculated over each epoch as

$$L(e) = \sum_{k=1}^{S} |x(k-1) - x(k)| \tag{1}$$

where e is the epoch number being processed and $L(e)$, x, k and S are the line length calculated within the epoch, downsampled signal, sample number and total number of samples in the epoch, respectively. Signal normalization is performed in the next stage of the algorithm to correct for changes in signal amplitude between different patients or due to the quality of the electrodes. Normalization is performed using the median decaying memory calculated as

$$z(e) = (1-\lambda) \times \text{median}\{L(e-1) \ldots L(e-B_1)\} + \lambda \times z(e-1) \tag{2}$$

where $z(e)$ represents the estimated background activity calculated for the current epoch. The number of epochs used in the median calculation (searching window) is B_1 and λ is a decay constant which controls the effect of previously derived values of z.

A start-up time of 2 min was chosen for the algorithm in the work of [18] to allow for the background estimate $z(e)$ to reach the same range of values as $L(e)$, during which the median is derived using all available epochs and $\lambda = 0.92$. The value of λ is increased to 0.99 after the initial 2 min period to reduce the effect of erroneous values of the median calculation likely caused by seizure events [18]. The normalization estimate is calculated over a 120 s period and therefore $B_1 = 60$ for 2 s epochs.

Hardware implementations of median filters, not specifically designed for processing EEG signals, have been previously reported in the literature and proven to be power hungry. A 3 input median filter has been proposed in [19] consuming 14 mW and the work of [20] reports a 9 input median circuit consuming 1.25 mW. Since in (2), the median operation is performed on the input signal and its time-shifted copies, the required delay elements (60 in the case of (2)) would only add to the hardware implementation complexity and power consumption. Due to the limited power budget for the algorithm hardware implementation in this work, a moving average filter was used to estimate the background activity instead of the median decaying memory. The moving average (MAV) is calculated as

$$MAV(e) = \frac{1}{B_2} \sum_{i=0}^{B_2-1} L(e-i) \tag{3}$$

where B_2 is the window length of the filter and which was set to 60, similar to B_1 in the median decaying memory calculation of (2). For $B_2 \gg 1$, the moving average of (3) can be approximated in the less computationally expensive recursive form, that was used in this work to estimate the backgroud activity ($z(e)$) as in (4) [21].

$$z(e) = \frac{B_2 - 1}{B_2} \times z(e-1) + \frac{L(e)}{B_2}. \tag{4}$$

It should be noted that equation (4) is specific to processing discrete time signals. Considering the epoch duration of 2 s (f_s = 500 mHz), the transfer function of the moving average corresponds to a single-pole recursive low pass filter with a cutoff frequency (f_c) of 1.3 mHz calculated using (5), allowing for a continuous time analog domain approximation

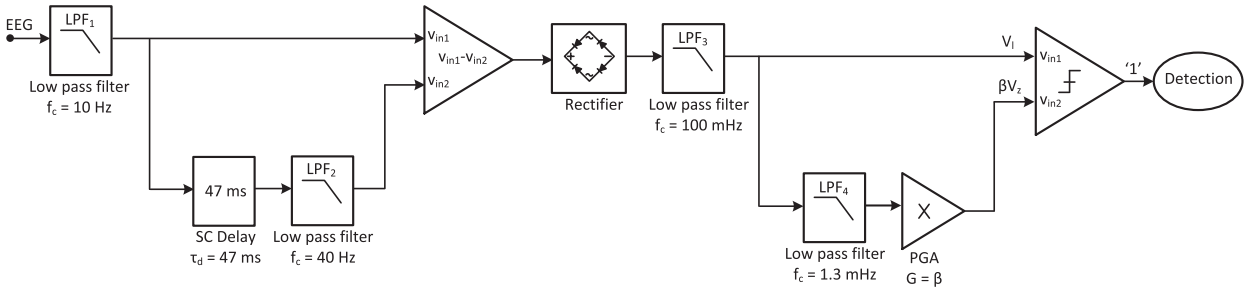

FIGURE 2. System-level implementation of the data selection algorithm.

which was used in the hardware implementation, shown later in Section III.

$$f_c = \frac{-f_s}{2\pi} \ln\left(\frac{B_2 - 1}{B_2}\right). \tag{5}$$

The normalization stage is completed by dividing the output of the line length calculation by the background estimate as:

$$A(e) = L(e)/z(e). \tag{6}$$

A detection flag for the channel being analysed (represented by $DF_n(e)$ in Fig. 1) will be set to '1' if the normalized feature $A(e)$ is greater than a user set threshold (β). Candidate seizure events are selected using a multichannel approach and therefore, a section of EEG data is selected for containing likely seizure activity only if the number of channels with a detection of '1' is higher than a threshold of 4 (chosen empirically).

III. SYSTEM ARCHITECTURE

The system level implementation of the algorithm is shown in Fig. 2. An initial low-pass filtering stage strongly attenuates the signal frequency components above 10 Hz to ensure that the signal can be subsequently sampled during the line length feature calculation at a reasonable sampling rate. The filter was created by cascading three first order G_mC low-pass filters with cutoff frequencies of 21 Hz, achieved by a biasing current of 200 pA for each filter OTA and an integrated capacitance of 20 pF.

The line length equation of (1) was implemented by subtracting the original signal from a delayed copy of itself, followed by a rectifier and integrator. The delay line was created by cascading six of the delay cells proposed in [22], each consisting of two SC stages and controlled by complementary clock signals. The delay cells were clocked at 128 Hz with a duty cycle of 50%, resulting in an overall delay of 47 ms for the six cascaded delay cells. A single stage G_mC low-pass filter with a cutoff frequency of 40 Hz, placed after the delay circuit, effectively attenuates the distortion resulting from the clock signal frequency component and its harmonics. As shown in Fig. 3a, the subtractor circuit utilizes quasi-infinite resistors (M_{R2-R3}) and capacitors (C_{1-2}) to block the DC offset resulting from the previous circuitry. The circuit

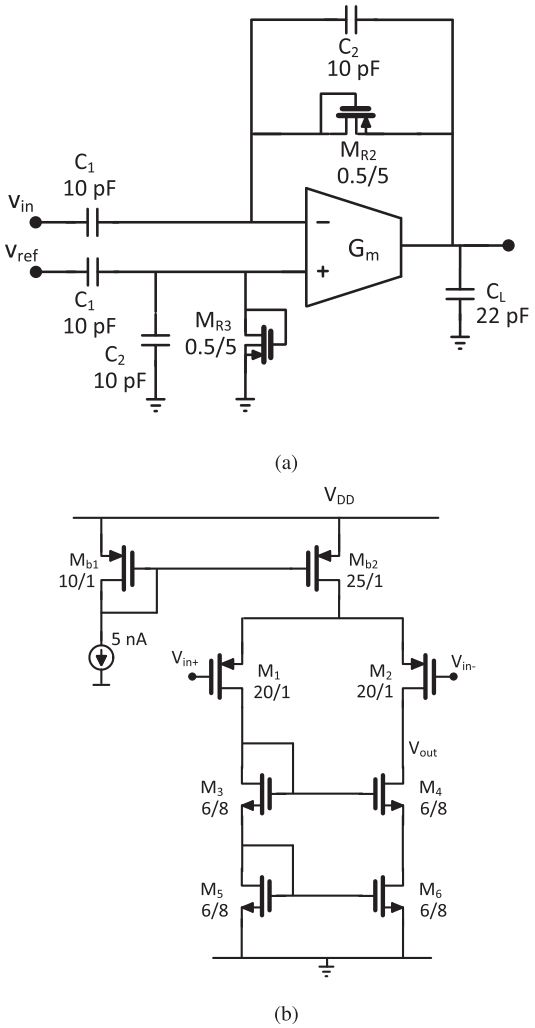

FIGURE 3. Subtractor circuit to subtract the low-pass filtered input signal from a delayed copy of itself (a) subtractor top-level design (b) OTA circuit.

was designed to have a gain ($-C_1/C_2$) of -1 by choosing a capacitance of 10 pF for both C_1 and C_2. The negative sign is of no consequence since the subtractor output is subsequently passed through a full-wave rectifier. A PMOS input stage was used in the subtractor OTA (Fig. 3b) to reduce the effect of low frequency noise on the subtractor output. The biasing current of the OTA was set to 12.5 nA, and cascoded devices ($M_3 - M_6$) were used to maintain the DC operating point.

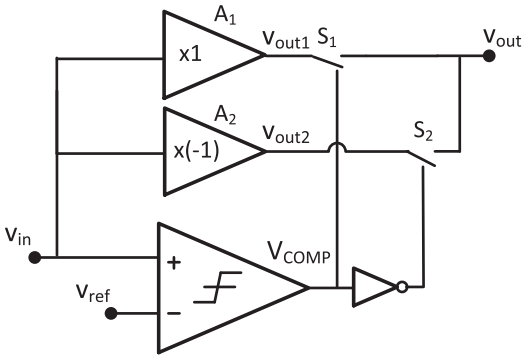

FIGURE 4. Rectifier circuit topology. The input signal is passed through an amplifier (A_1 or A_2) based on the comparison result against V_{ref}.

The design of the full-wave rectification stage was influenced by the concept proposed in [23], in which comparison results of the input signal (V_{in}) against a DC reference voltage (V_{ref}) is used to discriminate between the positive and negative signal polarities (see Fig. 4). A low impedance path is provided to the outputs of the non-inverting and inverting amplifiers (A_1 and A_2) upon selection based on the comparator output, through the switches (S_1 and S_2) which were implemented using minimum sized NMOS devices. The following SC low-pass filter, implemented based on the work of [24], effectively integrates the rectified signal to approximate the line length behaviour.

The low-pass filter clock frequency was set to 128 Hz with a duty cycle of 4% to achieve a filter cutoff frequency of 100 mHz.

The transfer function of the recursive moving average of (4) results in a filter with a cut off frequency of 1.3 mHz. The low-pass filter of [24], was also used to approximate the moving average filter using a 128 Hz clock with a duty cycle of 0.5%. A Programmable Gain Amplifier (PGA) behaving as a multiplier was implemented using the Operational Transconductance Amplifier (OTA) based amplifier topology of [25], to apply the user-set threshold values (β) to the background estimate. The PGA consists of two OTAs and the gain of the amplifier represents the user set threshold values. The gain of the amplifier is set, by the ratio of the biasing currents of the two OTAs, to achieve a desired system performance after deciding on the specific tradeoff between sensitivity and amount of data reduction.

A comparator detects the time periods for which the line length output V_L is greater than the modulated background estimate (βV_Z). As can be seen in Fig. 5a, three pre-amplification stages ($A_1 - A_3$) were used prior to the dynamic latch for an output offset cancellation scheme (OOS) implementation to reduce the effect of the comparator offset [26]. Due to the low speed requirement of the comparator, the devices in the pre-amplifiers shown in Fig. 5b were biased in the weak inversion region. Current injecting devices ($M_{i1} - M_{i2}$) were used to increase the transconductance of the input transistors compared to the diode connected load transistors ($g_{m1} > g_{m3}$), resulting in a moderate gain of 5.5 for each of

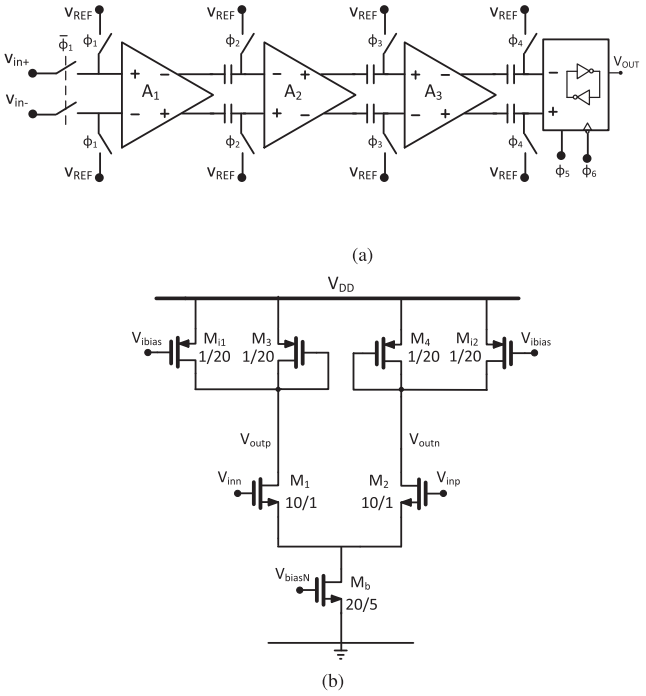

FIGURE 5. Comparator producing the system output detection flag (a) top-level architecture (b) pre-amplifier schematic.

the pre-amplifiers. The comparator output was sampled in 2 s intervals to create the effect of non-overlapping epochs inline with the epoch duration of the data selection algorithm.

IV. SYSTEM FRONT END AND CONTROL CIRCUITRY

The IA, which was designed based on the topology reported in [27], achieves a mid-band gain of 37 dB and input referred noise of 4 μV_{rms} integrated from 0.5-100 Hz. A proportional to absolute temperature current generation circuit was used to draw a reference current of 366 nA from the 1.25 V power supply. The currents required by the circuits in the data selection system were generated using scaled copies of the reference current. An 8b counter circuit using JK flip-flops followed by D flip-flops and combinational digital logic was used to scale-down a 32.6 KHz clock provided by an off-chip oscillator and to generate the low duty cycle pulses required for the circuits in the system.

V. FABRICATION AND TESTING

A. CHIP FABRICATION

The chip was fabricated in a 0.18 μm, tripple well 6 metal AMS CMOS technology. The chip padring was split into the two separate padrings to isolate sensitive analog circuitry from the noisy digital stages. The chip micrograph is shown in Fig. 6. The active area consumed by the seizure selection system is 1.48 mm^2.

B. EXPERIMENTAL RESULTS

A National Instruments NI USB-6259 data acquisition board (DAQ) was used to feed the input signals to the chip and to gather the output results and intermediate test-points.

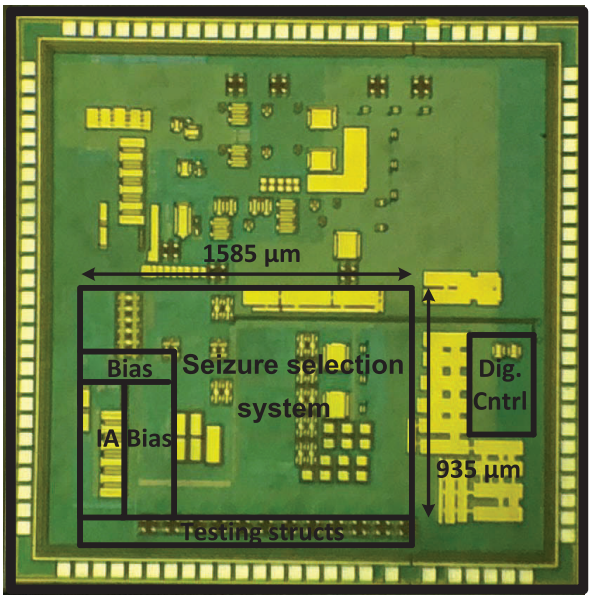

FIGURE 6. Micograph of fabricated chip.

The DAQ board introduces a capacitive load of 15 pF to its analog input signals and the implemented circuits generally have a low driving ability not suitable for driving the off-chip load. Single stage analog buffer circuits with a biasing current of 40 μA, provided through a separate 1.8 V supply and ground pad, were placed on-chip after the analog test-points for testing purposes. A digital buffer was also placed at the decision flag output.

The EEG dataset used for testing the system performance contains over 168 h of recordings from 21 patients and 34 marked seizure events from the Epilepsy Society (UK), Freiburg University Hospital (Germany) and Katholieke Universiteit Leuven (Belgium) [28], [29]. A summary of the dataset is provided in Table 1 together with the number of events per patient. The 16 channels used for testing the system performance are chosen as the channels common to all recordings in the dataset and are: C3, C4, CZ, F3, F4, FZ, F7, F8, FP1, FP2, O1, O2, T3, T4, T5, and T6.

A 700 s trace of EEG data from patient 5 (channel C3), shown in Fig. 7, includes a marked seizure event (from 341 s to 416 s time marks) and has been used to illustrate the system behaviour. The modelled and measured line length signal (V_L) and background estimate output (V_Z) in response to the input data trace is presented in Fig. 8a and Fig. 8b respectively. It can be seen that the measured signals (solid) are inline with the shape of the modelled (dashed) results. The system detection flag output (V_{DF}) is also shown in Fig. 8c.

The indices used to report the system performance are sensitivity and specificity. In order to distinguish between the number of seizure events correctly identified by the system and the number of identified seizure epochs, two variants of sensitivity have been used which are event sensitivity and epoch sensitivity. Event sensitivity is calculated as

$$\text{Event Sensitivity} = \frac{TP_{ev}}{TP_{ev} + FN_{ev}} \times 100\% \qquad (7)$$

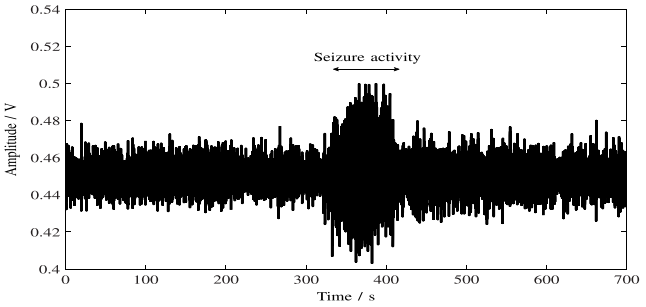

FIGURE 7. A 700 s section of EEG containing a seizure event with a duration of 75 s (from 341 s to 416 s time marks).

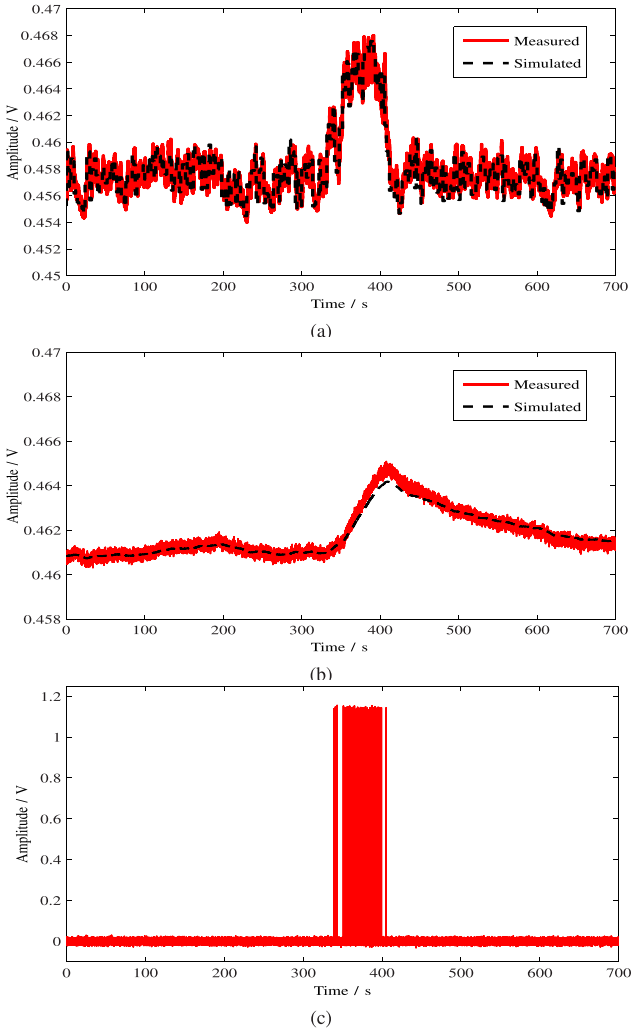

FIGURE 8. System outputs in response to the input EEG trace (a) Line length calculation (V_L) (b) Output of moving average approximation (V_Z) (c) Detection flag output.

where TP_{ev} is the number of True Positives and is equal to the number of correctly identified seizure events. The number of seizure events that have not been identified by the system has been considered as False Negatives (FN_{ev}). The calculation of epoch sensitivity follows the general form of (7), as

$$\text{Epoch Sensitivity} = \frac{TP_{ep}}{TP_{ep} + FN_{ep}} \times 100\% \qquad (8)$$

TABLE 1. Dataset used for testing the system performance.

Patient	Age at test	Gender	Marked seizure events	Seizure duration (s)	Recording duration
1	33	Female	3	293	34:02:07
2	53	Female	1	118	02:20:50
3	56	Female	7	827	66:59:38
4	41	Female	5	2029	19:54:17
5	35	Male	1	75	10:45:20
6	35	Male	1	102	12:04:50
7	60	Male	1	45	03:23:44
8	33	Male	1	97	04:08:57
9	23	Female	1	38	01:08:00
10	34	Male	0	0	02:00:11
11	Unknown	Male	0	0	04:00:22
12	22	Female	1	94	00:49:59
13	35	Female	6	109	00:31:55
14	46	Female	1	148	00:06:12
15	Unknown	Unknown	3	98	00:26:42
16	Unknown	Female	2	85	00:21:39
17	47	Female	0	0	02:00:11
18	45	Female	0	0	00:46:19
19	43	Male	0	0	00:15:15
10	47	Male	0	0	02:00:11
21	28	Female	0	0	02:00:11
Total	-	-	34	4158	168:57:31

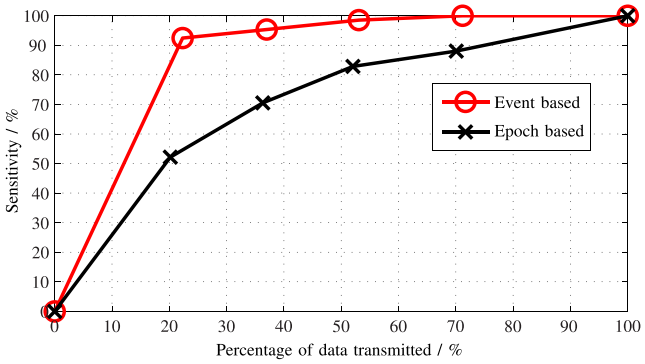

FIGURE 9. System performance tradeoff curve.

TABLE 2. System performance summary.

CMOS Process	0.18 μm	
Area	1.48 mm^2	
Supply Voltage	1.25 V	
Sensitivity	98.5%	
Fraction of data transmitted	52.5%	
Current consumption (nA)	LPF_1	2
	SC delay line	622
	LPF_2	5
	Subtractor	32
	Rectifier	172
	LPF_3	5
	LPF_4	5
	PGA (β = 1.1)	56
	Comparator	5.5
	Digital circuitry	5
	Total	910

where TP_{ep} and FN_{ep} are the number of correctly detected seizure epochs and incorrectly rejected seizure epochs respectively.

Considering the 75 s seizure event of Fig. 7 and the epoch duration of 2 s used in this work, a single detection by the system during any of the 37 epochs will result in an event sensitivity of 100%. However, to achieve an epoch sensitivity of 100%, the system must correctly identify all present epochs as seizure epochs resulting in 37 detections. The detection flag output (Fig. 8c) indicates that the system is able to identify the seizure event (event sensitivty of 100%) while correctly detecting 29 out of the 37 seizure epochs present, resulting in an epoch sensitivity of 78.3%.

When testing the system performance on data obtained from patients during long recording periods, where the duration of seizure events is insignificant compared to the overall duration of the recordings, the percentage of data transmitted is very close to 100% − specificity [18]. The specificity of the system is calculated using (9), where TN_{ep} and FP_{ep} are the number of correctly rejected non-seizure epochs (True Negatives) and the number of incorrectly detected non-seizure epochs (False Positives) respectively.

$$\text{Specificity} = \frac{TN_{ep}}{TN_{ep} + FP_{ep}} \times 100\% \tag{9}$$

In order to keep the duration of the measurement process across the dataset of Table 1 reasonable, the values of the sensitivity and percentage of data transmitted indices were calculated and averaged across all epochs using four threshold (β) values of 0.9, 1.1, 1.3 and 1.5. The system performance tradeoff curve is shown in Fig. 9. It can be seen that the system is able to achieve an epoch sensitivity of 82.8% and an event sensitivity of 98.5% for a percentage of data transmitted of 52.5%. In comparison, for the same percentage of data transmitted, the mathematical model of the

TABLE 3. Comparison with published works.

	Verma [11] JSSC 2010	Bin Atlaf [12] TBCAS 2016	Mirzaei [13] TBCAS 2013	Chen [14] JSSC 2014	Shoaran [15] TCAS 2015	Do Valle [16] TBCAS 2016	Imtiaz [30] Access 2019	This work
Signal	Wearable EEG	Wearable EEG	Implantable EEG	Implantable EEG	Implantable EEG	Implantable EEG	Wearable EEG	Wearable EEG
Application	Epilepsy management	Epilepsy management	Epilepsy management	Epilepsy management	Epilepsy management	Epilepsy management	Epilepsy diagnosis	Epilepsy diagnosis
Technology (μm)	0.18	0.18	0.13	0.18	0.18	0.18	0.18	0.18
Supply (V)	1	1	-	1.8	0.8	0.9	1.8	1.25
Patient specificity	-	○	○	○	○	○	×	×
Seizure detection	-	95.1%	100%	92%	100%	98.5%	97%	98.5%
Power (μW/Ch)	48.1	19.6	1.5	162.3	0.85	0.45	23	1.14

data selection algorithm achieves an event sensitivity of 100% and epoch sensitivity of 85%. The difference in the results is due to the mathematical approximations carried out in the original algorithm in order to aid the analog implementation.

The performance metrics must be considered in the context of the system aim, namely power reduction for a WEEG unit to aid with the diagnosis of epilepsy. It is expected that performance results achieved for the system event sensitivity will be higher than that of epoch sensitivity since it is easier to detect a single seizure event as opposed to detecting all seizure epochs. Event sensitivity is an important metric for real-time treatment systems that require a seizure event to be detected to allow for focal treatment and prevent seizure progression. However, epoch sensitivity is also an essential metric for the system of this work since a higher number for this metric would indicate that a larger percentage of interesting EEG data has been successfully selected for transmission, resulting in increased accuracy in the diagnosis.

A summary of the chip performance is shown in Table 2. The fabricated chip consumes 910 nA from a 1.25 V supply resulting in a power consumption figure of 1.14 μW. A comparison of this work with other published seizure detection SoCs has been shown in Table III. It should be noted that the previously published seizure detection systems mentioned in Table 3 require patient-specific training and the EEG data required to train these systems on a patient-by-patient basis is already marked as corresponding to seizure or non-seizure. This training data may be available once a patient is diagnosed with epilepsy, however, such data is not readily available during the diagnosis stage, rendering the mentioned systems unsuitable for use during this stage, unlike the system proposed in this paper. It is also difficult to directly compare the performance of the system presented in this paper, which is intended to aid the diagnosis of epilepsy, with works that focus on the real-time treatment (management) aspect of epilepsy and are designed based on different requirements. For example, the delay in seizure detection (latency) is an important metric in seizure detectors operating in real-time [31], but not so in the proposed system as the transmitted sections of data will ultimately be reviewed by a neurologist after being gathered, and not in real time. Instead, the ability of the system to identify the entire duration of seizure events (epoch sensitivity), in addition to the ability of the system to identify the occurrence of seizures (event sensitivity), are important performance indices in a system intended to be used to aid the diagnosis of epilepsy. Furthermore, the selection of false positives by the proposed system does not affect the overall EEG analysis as it is the neurologist, and not the presented system, who makes the final decision on the clinical relevance of the transmitted sections of data and rejects incorrect features. This is unlike systems performing seizure event quantification, where any false detections result in the overall result to be fundamentally incorrect, resulting in a very low false positive rate requirement. The SoC proposed in [30], which is a fully digital on-chip implementation of the algorithm of [18] and also operates based on the concept of discontinuous recording, can aid neurologists in the diagnosis stage of epilepsy. However, the power figure of 23 μW reported for the SoC of [30] is almost 23 times larger than the power consumed by the SoC presented in this paper, which is 1.14 μW.

To put numbers into context, assuming a conventional wireless EEG unit (32 channels) with no data reduction and created using an array of 32 IAs, ADCs and a single transmitter module based on previously reported low-power works with power consumption figures of 1.62 μW [31], 200 nW ([32]) and 2.112 mW ([33]), respectively, will result in a overall power consumption of 2.171 mW for the EEG system. Including an array of 32 data selection stages in the EEG system will result in an added power figure of 36.5 μW while effectively reducing the power consumed by the transmitter by a factor of 2 (for a data reduction of 50%), resulting in a reduced overall power consumption figure of 1.15 mW for the EEG system. This power figure translates to over 213 h ($\sim$ 9 days) of operation from a miniature battery typically used in hearing aids [34]. The achieved power savings could also be capitalized on by using the system proposed in this work in combination with other data reduction stages that select inter-ictal sections of EEG data, such as [10], to obtain a complete WEEG system for the purpose of epilepsy diagnosis.

VI. CONCLUSION

This paper presented the design and experimental results for a low-power seizure focused power reduction SoC. The mapping of the mathematical model of the seizure selection algorithm to an analog-based SoC, together with the hardware design procedure and implementation are discussed. The analog based seizure selection circuitry are implemented using a 0.18 μm CMOS process. A power analysis presented as part of this paper shows the potential of the power reduction SoC in extending the battery lifetime of a EEG system to over 9 days of operation. The seizure focused power reduction SoC, which is tested with over 168 hours of EEG data from 21 patients and 34 marked seizure events, is able achieve a sensitivity of 98.5% while selecting 52.5% of the EEG data for transmission and consuming 1.14 μW.

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