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Single Event Transient Study of pMOS Transistors in 65 nm Technology With and Without a Deep n+ Well Under Particle Striking

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ABSTRACT In triple-well PMOSFET transistor, a deep n+ well (DNW) is a process used to isolate the substrate noise, which can lead to changes in effect of single event transient (SET). In outer space, collision of cosmic energetic particles with sensitive nodes of integrated circuits can generate electron-hole pairs. The probability of recombination of electrons and holes is different, which results in transient changes of sensitive nodes' state. Transient potential change is transmitted to the output terminal, that is, a single event transient. In this paper, measured SET effect characteristics of PMOSFET transistors in 65 nm process are performed with heavy particle experiments. Compared with triple-well PMOSFET transistor, the experimental data show that the average of SET pulse width in double-well PMOSFET is increased by 19.4% (Ge linear energy transfer (LET) = 37.4 MeV·cm2/mg) and 14.4% (Ti LET = 22.2 MeV·cm^2/mg). The data show that a triple-well PMOSFET transistor is better for SET, which is be appropriate for radiation hardened integrated circuits (ICs) design.

INDEX TERMS Particle, deep n+ well (DNW), PN junction.

I. INTRODUCTION

Along with the wide application of electronic equipments in aerospace field, research on single-event effects of electronic equipments has gained an increasing important. One of the principal reasons for the dominance of CMOS technology in today's semiconductor industry is the scalability of MOSFETs. When the process is scaled down to deep submicron dimension, SETs have been becoming a key source of logical errors in ICs in outer space [1]. The physical mechanisms of charge motion of SET has been verified, the charge diffusion or charge drift of sensitive nodes, and amplification effect of parasitic bipolar transistors are main mechanisms of SET in a bulk CMOS technology. Nevertheless, the experimental characterization of SET pulses of the PMOS transistor is still rarely reported up to now. Because of microstructures of the lattices, variation of energy states of impurities and the inherent non- instantaneity and nature of SET pulse, SET pulse mitigation has always been a challenging task in the field of reliability of ICs in space [2]–[6].

The physical mechanisms of charge motion on SET have been extensively studied in MOSFET transistors, which are expressed by the mobility of electrons and holes, etc. Our previous work has also simulated the physical mechanism of charge motion [5]. Electrical characteristics of charge motion on SET are controlled by charge concentration gradient, electric field, and amplification effect of parasitic bipolar transistor, which are expressed by current and voltage. While most of the results come from NMOSFET transistors, PMOSFET transistors are rarely studied. As ICs are designed with deep submicron process, the effects of space particles on ICs have attracted the attention of scientists [7]–[13]. Due to space particles striking, charges generated by striking accumulate at the sensitive nodes of logic circuits leading to SETs. In order to quantify the effect of particles on PMOS transistors, more studies on PMOS transistors need to be investigated from heavy ion experiments.

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Because DNW technology can isolate substrate noise, DNW technology is widely used in ICs design. Due to the heavy doping of DNW, it is easy to adjust the threshold voltage. In semiconductor physics, the V_{TH} of a PMOSFET transistor is usually defined as the gate voltage for which the oxide-silicon interface is "as much p-type as the substrate is n-type." It can be proved that

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{OX}} \quad (1\text{-}1)$$

$$\Phi_F = \frac{(kT)}{q} \ln(\frac{N_{sub}}{n_i}) \quad (1\text{-}2)$$

where Φ_{MS} is the difference between the work functions of the poly-silicon gate and the n-type silicon substrate, q is the electron charge, N_{sub} is the doping concentration of the n-type substrate, Q_{dep} is the charge in the depletion region, and C_{ox} is the gate oxide capacitance per unit area. From pn junction theory,

$$Q_{dep} = \sqrt{4q\varepsilon_{si}\,|\Phi_F|\,N_{sub}} \quad (1\text{-}3)$$

where ε_{si} denotes the dielectric constant of silicon. As dimension is scaled down, a phenomenon observed in scaled transistors is the dependence of the threshold voltage on the channel length. Transistors with different lengths yield lower V_{TH} as L decreases. This is because the depletion regions associated with the source and drain junctions protrude into the channel area considerably, thereby reducing the immobile charge that must be imaged by the charge on the gate [14]. DNW technology is also widely used in storage circuits [15]. However, when these circuits are used in space electronic equipments, electronic equipments are exposed to the radiation of space particles. Particle radiation effects on these equipments have become an important research focus. In our previous works, the quantitative characterization of single-event multiple cell transients was studied in a fully customized SRAM with DNW in 65nm process. The experimental data show that this SRAM is very sensitive to single-event multiple cell upsets, the DNW technology is not as good as the double-well CMOS technology [15]. Because sources and drains of several transistors share the same area, the pulse quenching on SETs in this SRAM with DNW becomes more significant than that in the double-well CMOS technology [15]–[19]. However, the quantitative characterization of the effect on SET in 65 nm PMOSFET transistor with DNW has not yet been performed with heavy particle experiments. In order to quantify the SET effect of PMOSFET transistor with DNW in 65 nm process, two types of PMOS transistor experimental chips were manufactured by 65 nm domestic double-well CMOS technology and triple-well CMOS technology. In order to measure the SET pulse width and number, The P-hit cell and chain, designed by Gadlage *et al.* [10] and Hamad *et al.* [11], were introduced in our experiments. In this paper, Ti (LET = 22.2 MeV·cm2/mg) and Ge (LET = 37.4 MeV·cm2/mg) are represented by Ti and Ge.

Sentaurus TCAD from Synopsys is the most popular software for device emulation. In this paper, electrical characteristics charge motion of SET in 65nm PMOSFET transistor is further interpreted by a mixed-mode numerical emulation. The experiments of energy particles Ge and Ti are used to judge the SET effect of DNW [9], [13], [15], [20], [21].

II. DEVICE STRUCTURE AND I-V CURVE

In this paper, an inverter was used to simulate the pulse of SET production process. The PMOSFET was modeled with three dimensional digital models and the NMOSFET was modeled with a SPICE model [10], [20], [22], [23]. Both the double-well PMOSFET transistor and the triple-well PMOSFET transistor were investigated. The n-well contact, gate and source of PMOSFET transistor was connected to high voltage level ("1"), the drain of PMOSFET transistor was connected the drain of NMOSFET transistor , the p-well contact and source of NMOSFET transistor was connected to GND ("0") , the gate of NMOSFET transistor was connected to high voltage level ("1")in the simulation.

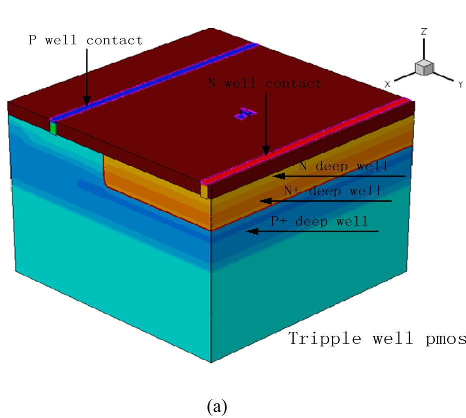
Sentaurus TCAD from Synopsys was used in the research to model the device and execute the simulations [21]. The domestic 65nm double-well PMOSFET transistor and triple-well PMOSFET transistor were modeled. According to the design rule from the foundry, the DNW is buried in the substrate and under the n-well, which is used to form triple-well PMOS transistor. In this paper, angular effects are not discussed, although their importance is apparent in problems concerning charged particle interactions with semiconductors [24]–[26]. Heavy ion strike was taken as perpendicular to the drain of the PMOSFET transistor [21]. Figure 1(a) represents the three dimensional view of the triple-well PMOSFET transistor, Figure 1(b) represents the cross-section view of the triple-well PMOSFET transistor.

Correspondingly, the structure of double-well PMOSFET transistor without the DNW is similar to that of triple-well PMOSFET, Figure 2(a) represents the three dimensional view of the double-well PMO-SFET transistor, Figure 2(b) represents the cross-section view of the double-well PMOSFET transistor.

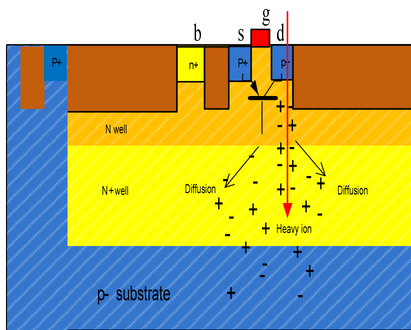
65nm double-well PMOSFET transistor and triple-well PMOSFET transistor were calibrated based on the SMIC65 PDK [16]. Fig.3 shows the I-V characteristic curves of the triple-well PMOSFET transistor. The W/L ratio of the triple well and double-well PMOSFET transistor are 0.065/0.2μm in the TCAD model and the W/L ratio of the NMOSFET transistor is 0.065/0.2μm in the SPICE model.

Fig.4 shows the I-V characteristic curves of the double-well PMOSFET transistor.

Heavy particle striking was simulated with a cylinder of electron-hole pairs. Along the axis of the cylinder, the linear energy transfer value was an invariant. The height of the cylinder was 5μm, the radius of the cylinder was 0.07μm [15], [20]–[22]. Ge's range is 30.5μm, Ti's range is 40μm. The charge deposited by the incident particles were modeled using a Gaussian radial profile.

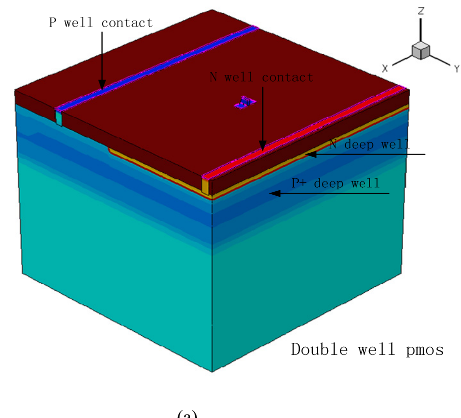


(a)

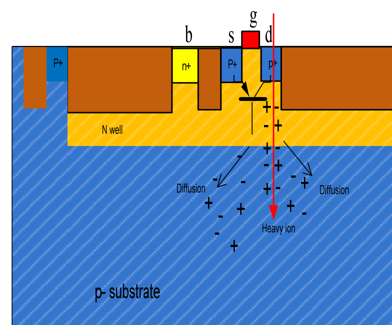


(b)

FIGURE 1. Triple-well PMOSFET: (a) three dimensional view and (b) cross-section view.



(a)



(b)

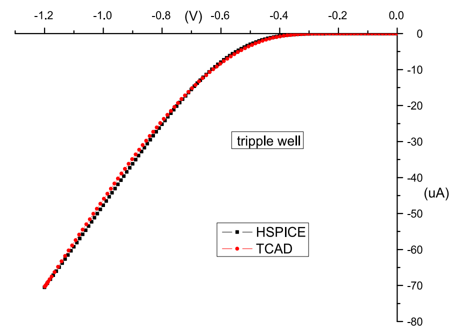
FIGURE 2. Double-well PMOSFET: (a) three dimensional view and (b) cross-section view.

III. SIMULATION RESULTS AND QUANTITATIVE CHARACTERIZATION

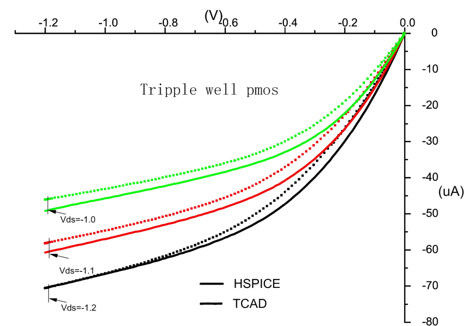
Heavy particle striking is illustrated in Fig, 5. Heavy particle strikes the drain of double-well PMOSFET in a normal strike, numerous generated electron-hole pairs are generated along the cylinder [20]. The drain collect the generated holes making a SET pulse appear at the output of the inverter [20]. Electron-hole pairs generated by striking diffuse in the n-well and DNW at the same probability, the generated electrons are prevented from entering the substrate by PN junctions, which is located between the p-substrate and the n-well or DNW, the excess electrons lead to a decrease potential of n-well, but the n-well potential is still higher than source potential and drain potential shown in Fig.6. In Fig. 6, "after" means to measure the potential distribution at a certain time after a particle striking. This is a qualitative description of the potential distribution at that time. The parasitic bipolar junction transistor consisting of source-n-well-drain is harder to turn on and the bipolar amplification effect is insignificant in PMOSFET transistor [27], [28].

As shown in Fig.7 (a), when a particle with a LET of 37Mev struck a triple-well PMOS transistor, single event transient (SET) was simulated. As shown in Fig.7 (b), the simulation results showed that the maximum current appeared at 0.22ns when the striking time was 0.2ns and the LET was 37Mev.

As shown in Fig.8, a triple-well PMOS transistor and a double-well PMOS transistor were simulated when particle -s



(a)



(b)

FIGURE 3. Triple-well PMOSFET: (a) I_d-V_g curves and (b) I_d-V_d curves.

with LETs struck. In integrated circuits, the larger the pulse width, the harder it is to shield. The simulation results showed that the pulse widths of a triple-well PMOS transistor were

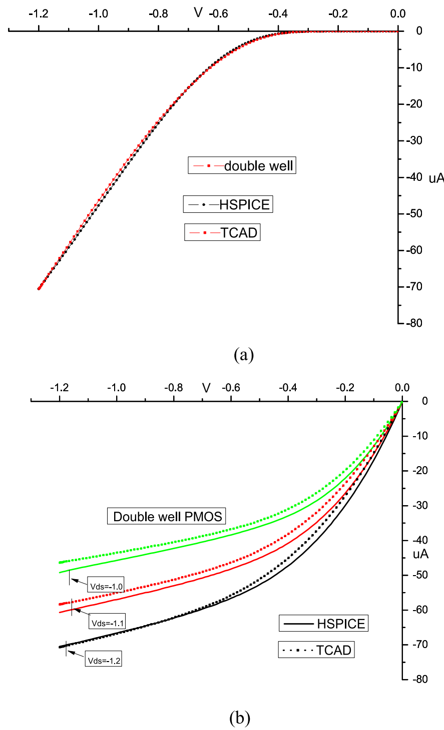


FIGURE 4. Double-well PMOSFET: (a) I_d-V_g curves and (b)I_d- V_d curves.

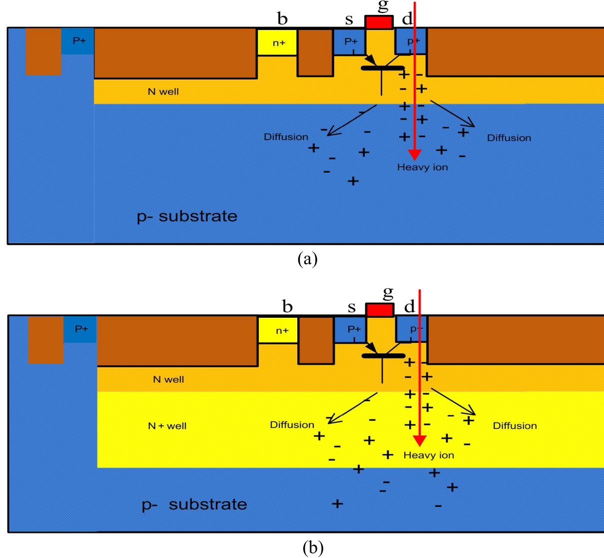


FIGURE 5. Cross sections of particle striking for two types of PMOSFET transistor: (a) double-well PMOSFET transistor and (b) triple-well PMOSFET transistor.

narrower than those of a double-well PMOS transistor, which was advantageous in integrated circuits. In this simulation, LETs of [20], [30], [37], [40] Mev were used. Two LETs of [22.2, 37.4] Mev were used in the experiment.

Gadlage is credited with designing the measuring circuit of SET pulse shown in Fig .9, the circuit consists of the P-hit cell and chain [10]. These measurement topology structures

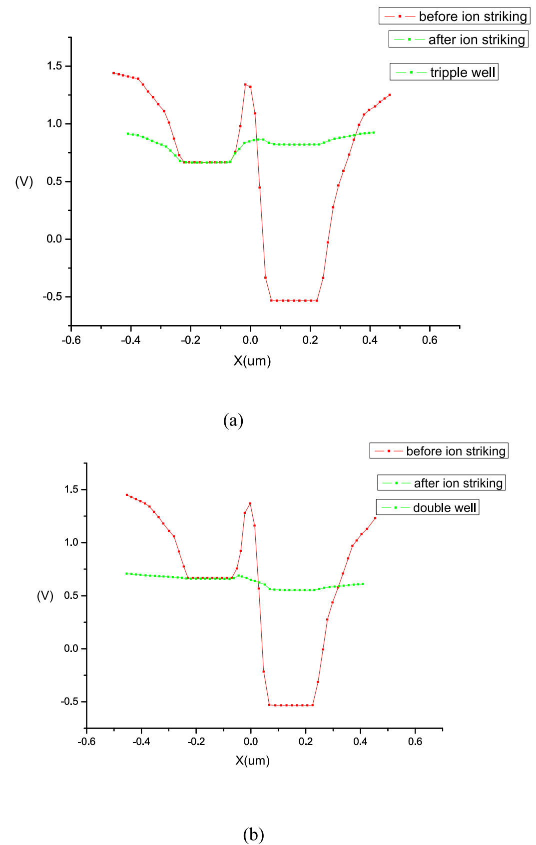


FIGURE 6. Potential distribution of PMOSFET transistor along X-axis. (a) Potential distribution of triple-well PMOSFET transistor along X-axis before particle striking and after 10 ps of particle striking. (b) Potential distribution of double-well PMOSFET transistor along X-axis before particle striking and after 10 ps of particle striking.

were introduced into this experiment. "101" or "010" pulse of SET pulse may produced off-state NMOSFET transistor in inverter cell or off-state PMOSFET transistor in the NOR cell in this chain. However, the NOR cell shield the "101" SET pulse produced in NMOSFET transistor, which cannot travel through the chain. Therefore, just only the "010" SET pulse produced in PMOSFET transistor in the NOR can travel through the transmission chain and captured by the monitoring circuit. Narasimham is credited with designing the monitoring circuit [29]. In the monitoring circuit, four chains of short 200-stage P-hit were in turn connected to an OR logic cell, which was connected to the SET pulse monitoring system [10].

The two types of PMOS experimental chips were irradiated using two heavy particles: Ti and Ge. The measurements were carried out at the HI-13 Tandem Accelerator in the China Institute of Atomic Energy, Beijing. The particle flow density was $1*10^7$ions/cm^2. the width and numbers of pulses were recorded. Experimental data were recorded in time, the experimental data were saved for subsequent processing.

The cross-sections of captured single event transients in the double-well PMOSFET transistor and triple-well PMOS-FET transistor are shown in Fig. 10 at Ge and Ti exposure.

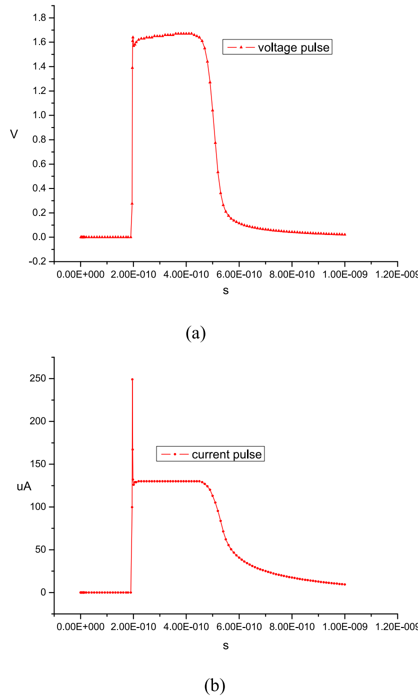


FIGURE 7. Simulated pulse on SET: (a) voltage pulse and (b) current pulse.

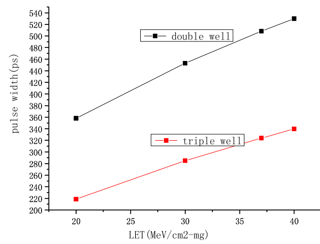


FIGURE 8. Pulse width of a triple well PMOS vs pulse width of a double well PMOS.

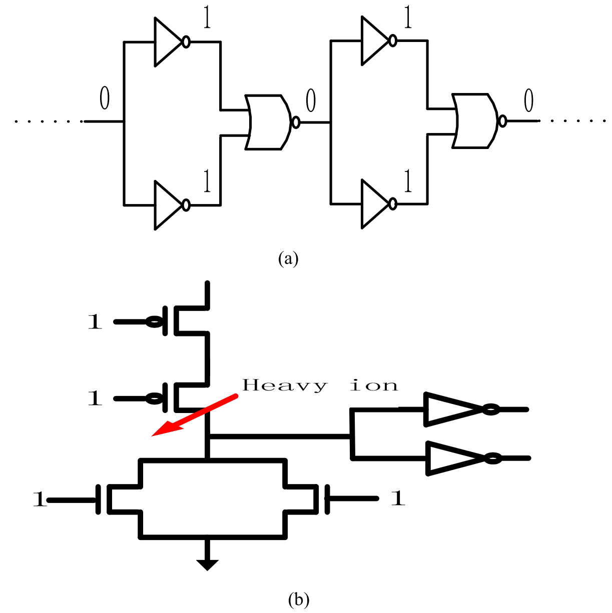


FIGURE 9. P-hit chain (a) and P-hit cell (b).

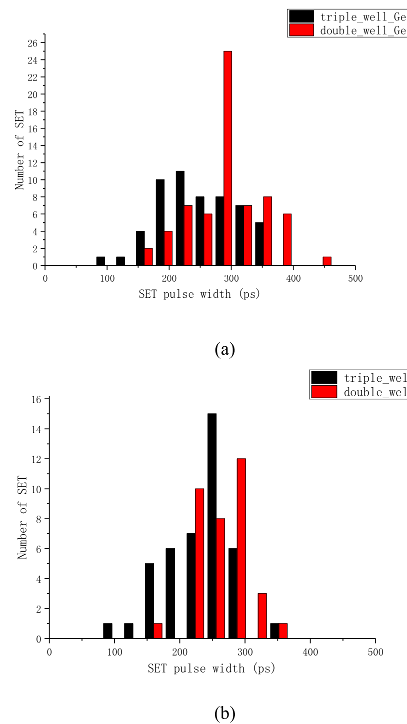


FIGURE 10. Triple well vs double well (a) at Ge(LET = 37.4 MeV·cm^2/mg) irradiation and (b) at Ti (LET = 22.2 MeV·cm^2/mg) irradiation.

Compared with double-well PMOSFET transistor, Fig. 10(a) shows that cross section of the total single event transient at Ge exposure decreases significantly in triple-well PMOSFET transistor. At the larger pulse widths, the numbers of monitored SET decreases significantly in a triple-well PMOSFET transistor. The comparison of SET cross-sections in two types of PMOSFET transistor under Ti irradiation is also shown in Fig.10 (b). At the smaller pulse widths, the number of monitored SETs increases slightly in the triple-well PMOSFET transistor. At the larger pulse widths, the number of monitored SET decreases slightly in a triple-well PMOSFET transistor. Compared with the double-well PMOS transistor, the triple-well PMOS transistor has larger carrier recombination rate, so the pulse width is narrower and the spread of the pulse width is a slight increase. In integrated circuits, the larger the pulse width, the harder it is to shield, and as a result that a triple-well PMOS is better than a double-well PMOS. The experimental chip without DNW generated 66 and 35 single event transients under the radiation of Ge and Ti, respectively. The experimental chip with DNW generated 55 and 42 single event transients under the radiation of Ge and Ti, respectively. The overall cross-section of the SETs of a PMOS is 0.000744cm^2.

The minimum, average, maximum and ±1 standard deviation of SET pulse width in the two types of PMOSFET transistor are indicated in Fig. 11 [18]. Two types of PMOS transistor were irradiated by Ge, the average pulse width

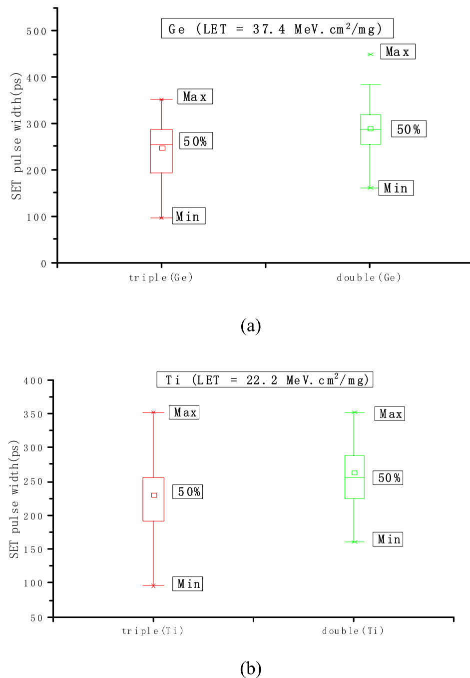


FIGURE 11. **Minimum, average, maximum, ±1 standard deviation of SET pulses in double-well PMOSFET transistor and triple-well PMOSFET transistor (a) at Ge(LET = 37.4 MeV·cm^2/mg) irradiation and (b) at Ti(LET = 22.2 MeV·cm^2/mg) irradiation.**

of 290.9ps was calculated in double-well PMOSFET transistor, the average pulse width of 243.6ps was calculated in triple-well PMOSFET transistor, the difference was 47.3ps. Two types of PMOS transistor were irradiated by Ti, the average pulse width of 230.1ps was calculated in triple-well PMOSFET transistor, the average pulse width of 263.3ps was calculated in double-well PMOSFET transistor, the difference was 33.2ps [15]. The measuring results of radiation showed that the average pulse width were increased by19.4% (Ge exposure) and 14.44% (Ti exposure) in double-well PMOSFET transistor compared with that in triple-well PMOSFET transistor.

The results of radiation experiments show that for single event transient, the pulse width of a triple-well PMOSFET transistor is narrower than that of a double-well PMOSFET transistor, and as a result that a triple-well PMOS is better than a double-well PMOS in integrated circuits. A triple well PMOSFET transistor may be suitable for the design of ICs for space environments.

IV. CONCLUSION

In this paper, the simulation results and experimental characteristics of the SET effect of PMOSFET transistor with and without DNW in 65 nm process are investigated in heavy particle experiments. The data show that the average pulse width is increased by19.4% (Ge exposure) and 14.44% (Ti exposure) in the double-well PMOSFET transistor compared with that in the triple-well PMOSFET transistor. Research has proved that a triple-well PMOSFET technology has the natural advantage in the design for radiation hardened integrated circuits and may be used in the design of integrated circuits in radiation environments. Referring to other studies, the next step is to do further specific experiments on 40nm and 28nm process for quantitative characterization [30].

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