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An Investigation of Electric Field and Breakdown Voltage Models for a Deep Trench Superjunction SiC VDMOS

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ABSTRACT The theoretical analysis of breakdown model for a deep trench superjunction (DT-SJ) SiC VDMOS is presented in this paper. The vertical electric field distribution is derived by the electric field decomposition. Then, a fitting dependence of the critical electric field on the doping concentration for the device is obtained, based on which, the model of breakdown voltage is given for the DT-SJ SiC VDMOS. Analytical results are compared with simulative results with the same thicknesses of drift region from 8 μm to 16 μm and the doping concentrations from 4×10^{16} cm^{-3} to 8×10^{16} cm^{-3}. It is numerically demonstrated that the errors between model and simulation are less than 3% when N pillar and P pillar have the same width of 1μm.

INDEX TERMS Silicon carbide, electric field, breakdown voltage, model.

I. INTRODUCTION

Nowadays, Silicon Carbide (SiC) power devices have been increasingly applied to many new and emerging fields, such as hybrid and pure electric vehicles, intelligent power system, industrial control, defense and aerospace, due to their merits of comprehensive performances of higher voltage, higher temperature, higher power density, and more excellent thermal conductivity, compared with traditional Silicon and GaAs power devices [1]–[4]. Extensive researches have been carried out on SiC power devices to obtain better and better performance in the aspect of the breakdown voltage (BV), the specific on resistance ($R_{on,sp}$), the maximum gate oxide electric field ($E_{max,ox}$), and the gate charge (Q_g), etc [5]–[10].

Vertical Double-diffused MOSFET (VDMOS) is one of the mostly used power device due to its merits of high input impedance, fast switching, easily driven, etc. However, the conventional SiC VDMOS (C SiC VDMOS) suffers from gate oxide reliability under high electric field, low mobility in inversion, and the trade-off between BV and $R_{on,sp}$. Some structures and technologies have been widely investigated to reduce the gate oxide field for the SiC VDMOS [11]–[21]. Besides, in order to alleviate the trade-off between BV and $R_{on,sp}$, several technologies, which are widely used in silicon power device such as the trench structure and SJ [22], have been introduced into SiC VDMOS [23], [24]. Trench structure is favorable in reducing $R_{on,sp}$ with the elimination of JFET effect and the shortening of transverse dimensions. SJ can reduce $R_{on,sp}$ and increase BV simultaneously [25]–[27], and is one of the most promising technologies for SiC power device [28]. Compared with the trench technology, the studies of SiC devices with the superjunction (SJ) principle are not as sufficient. In 2003, a 400-V SiC lateral SJ diode was reported to be fabricated for the first time [29]. In 2008, L. C. Yu and K. Sheng developed the models of the electric field distribution for the SiC SJ

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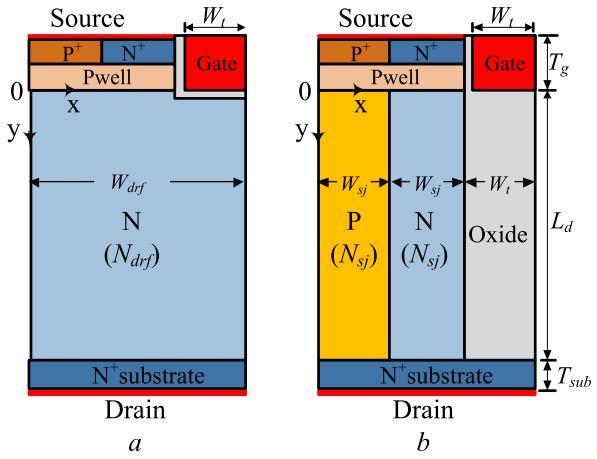

FIGURE 1. Cross section of structures of SiC VDMOS. (a) C SiC VDMOS, (b) DT-SJ SiC VDMOS.

devices [30]. The models were the type of piecewise function, based on which the BV and $R_{on,sp}$ were calculated. In 2012, 5-20 kV SiC SJ diodes were reported by simulation, and the best trade-off between BV and $R_{on,sp}$ were obtained with structure parameters [31]. In 2014, Ryoji Kosugi et al. presented the first experimental demonstration of SiC SJ structure by multi-epitaxial growth, and a BV of 1545 V with a $R_{on,sp}$ of 1.06 mΩ·cm^2 were measured [32]. In 2016, a SiC Schottky diode with partial SJ region processed by two groups of implantations was developed, and a BV of 1350V and a $R_{on,sp}$ of 0.92 mΩ·cm^2 were achieved [33]. In 2017, T. Masuda et al. reported that the 0.97 mΩ·cm^2/820 V SiC SJ V-Groove Trench MOSFET had been fabricated [34]. Since the SJ can improve the trade-off relationship between BV and $R_{on,sp}$, more studies of the structures and models for the SiC SJ devices are being still expected.

The research on the structure of a novel DT-SJ SiC VDMOS has been done in the authors' previous work, but the models of electric field and BV have not been involved [24]. Therefore, this paper continues to focus on the analysis and modeling of the electric field and BV based on the previous work. To begin with, the structure of DT-SJ SiC VDMOS is briefly presented. Then, the analytical distribution of the vertical electric field along the border of P pillar is obtained by the electric field decomposition method. Thirdly, with a fitting dependence of the SiC critical field ($E_{C,SiC}$) and the doping concentration of the N/P pillars, the theoretical model of the BV is thus obtained. Finally, comparisons between the models and simulations are made to verify the accuracy of the proposed models.

II. DEVICE STRUCTURE AND THE MODEL OF THE VERTICAL ELECTRIC FIELD

A. DEVICE STRUCTURE

DT-SJ SiC VDMOS is illustrated as Fig. 1. Compared with the C SiC VDMOS, one of the major distinguishing structure features is the deep trench (DT), which extends to the drain

TABLE 1. The parameters for the DT-SJ SiC VDMOS.

Parameter	Value
Half-cell width	3 μm
Thickness of gate, T_g	1.55 μm
Thickness of gate oxide, T_{ox}	0.05 μm
Thickness of drift region, L_d	8-16 μm
Thickness of N+ substrate, T_{sub}	1 μm
Width of N/P-pillars, W_{sj}	1 μm
Width of gate oxide, W_t	1 μm
N/P-pillar concentration, N_{sj}	(4-8)×10^{16} cm^{-3}

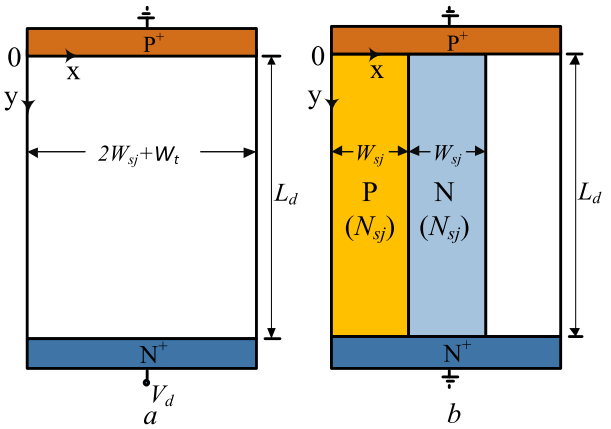

FIGURE 2. Structure decomposition for electric field analysis (a) PIN structure with drain voltage V_d, (b) SJ without voltage bias.

N+ region. The DT can alleviate the restricted dependence of the Gauss' law on the interface of gate oxide and the curvature effect on the corner of the gate, producing a small $E_{max,ox}$. The DT can also lead to a low Q_g. Another feature for the DT-SJ SiC VDMOS is the SJ in the drift region. The lateral depletion effect between the P and N pillars leads to a heavier doping for the full depletion; thus, a lower $R_{on,sp}$ and a higher $E_{C,SiC}$ are obtained. The optimized field distribution from the SJ structure and the enhanced $E_{C,SiC}$ result in a higher BV for the DT-SJ SiC VDMOS [24].

The key parameters for the DT-SJ SiC VDMOS are defined and listed as Table 1. Sentaurus TCAD is used in the simulations. While making the simulations, SRH, AUGER, OkutoCrowell are used as recombination models, and DopingDependence, HighFieldSaturation and Enormal are used as mobility models.

B. MODEL OF THE VERTICAL ELECTRIC FIELD

Based on the SJ principle, the non-balances of the charges at the bottom of P pillar and at top of N pillar form the highest electric fields at the points [35]. Considering the breakdown characteristic, the electric field $E(0, y)$ along the left edge of the pillar P is derived. The DT-SJ structure can be decomposed into a PIN diode with reverse bias voltage of V_d as shown in Fig. 2.(a), and a SJ structure with zero bias voltage as shown in Fig. 2.(b) , respectively.

For the PIN structure, the electric field is uniformly distributed with biased voltage of V_d, then the electric field is calculated as:

$$E_{PIN} = \frac{V_d}{L_d} \tag{1}$$

It is assumed that both P and N pillars have the same width W_{sj} and the doping concentration N_{sj} for analysis. P and N pillars are fully depleted. The electric potential in SJ satisfies the following 2-dimension Poisson equation:

$$\frac{\partial^2 \phi_{sj}(x,y)}{\partial x^2} + \frac{\partial^2 \phi_{sj}(x,y)}{\partial y^2} = -\frac{qN_{sj}}{\varepsilon_{SiC}} \quad 0 \le y \le L_d, \quad 0 \le x \le W_{sj} \tag{2}$$

where ε_{SiC} is the permittivity of SiC, and q is the electron charge. The boundary condition of the Eq. (2) is:

$$\begin{cases} \left.\dfrac{\partial \phi_{sj}(x,y)}{\partial x}\right|_{x=0} = 0 \\ \left.\dfrac{\partial \phi_{sj}(x,y)}{\partial x}\right|_{x=W_{sj}} = -\dfrac{2[\phi_{sj}(W_{sj},y) - qN_{sj}W_{sj}^2/2\varepsilon_{SiC}]}{W_{sj}} \\ \phi_{sj}(0,0) = 0 \\ \phi_{sj}(0,L_d) = 0 \end{cases} \tag{3}$$

Solving Eq. (2) and Eq. (3), $E_{sj}(0, y)$ is derived as:

$$E_{sj}(0,y) = -\frac{\partial \phi_{sj}(0,y)}{\partial y} = \frac{qTN_{sj}}{\varepsilon_{SiC}} \cdot \frac{\cosh(\frac{y}{T}) - \cosh(\frac{L_d - y}{T})}{\sinh(\frac{L_d}{T})} \tag{4}$$

where T is equal to $W_{sj}/\sqrt{2}$.

According to superposition principle, $E(0, y) = E_{PIN} + E_{sj}(0, y)$, the electric field $E(0, y)$ is obtained as:

$$\mathrm{E}(0,y) = \frac{V_d}{L_d} + \frac{qTN_{sj}}{\varepsilon_{SiC}} \cdot \frac{\cosh\left(\frac{L_d}{T}\right) - \cosh\left(\frac{L_d - y}{T}\right)}{\sinh\left(\frac{L_d}{T}\right)} \tag{5}$$

Assuming that when $E(0, L_d)$ reaches to $E_{C,SiC}$, breakdown occurs, and BV related with N_{sj}, L_d and W_{sj} for the DT-SJ SiC VDMOS can be obtained.

C. COMPARISONS BETWEEN THEORETICAL AND SIMULATED ELECTRIC FIELD DISTRIBUTIONS

Both the theoretical and simulated electric fields are simultaneously shown in the Fig. 3 with a L_d of 12 μm and a N_{sj} of 6×10^{16} cm^{-3}. The drain voltage V_d varies from 600 V to 2000 V. As the theoretical analysis, the maximum electric field $E(0, y)$ locates at $y = L_d$ and the electric fields keep almost constants in the middle of the SJ region. It is clear that the theoretical electric fields highly agree with the simulated results and there is a little discrepancies within the scope of $\pm5\%$ in all cases. The electric fields with different lengths of drift region on the condition of the fixed N_{sj} of 6×10^{16}cm^{-3} are also shown in Fig. 4. The theoretical and simulated results also match well. Besides, the dependence of the electric field with doping concentration on the same L_d of 12 μm and V_d of 1800 V is also shown as Fig. 5. Adding the N_{sj} from 4×10^{16} cm^{-3} to 8×10^{16} cm^{-3}, the results from Eq. (5) always match well with the simulative results.

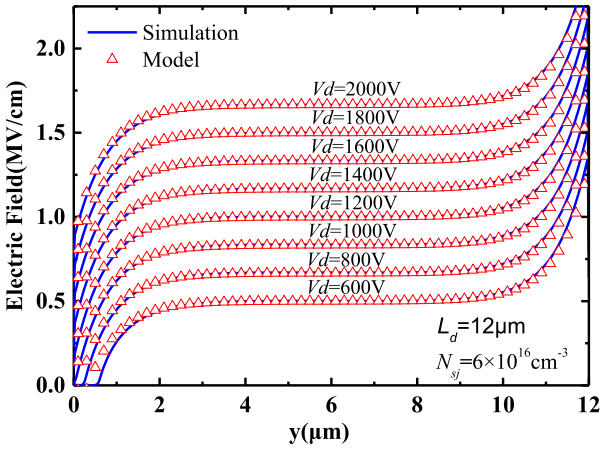

FIGURE 3. Distribution of electric field under different drain voltage with fixed L_d = 12 μm and N_{sj} = 6 × 10^{16} cm^{-3}.

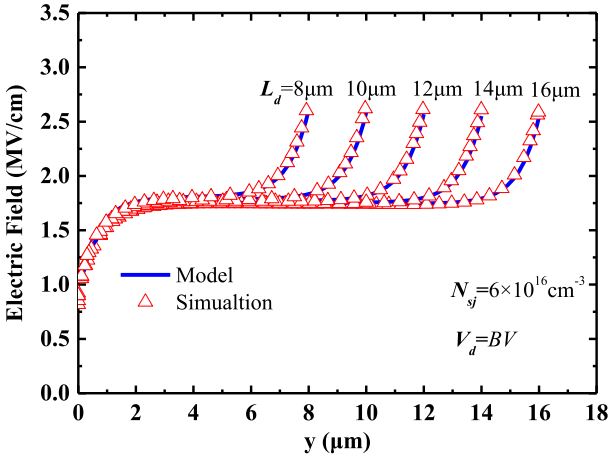

FIGURE 4. Distributions of electric fields with different L_d.

In a word, the relative errors between theoretical and simulated electric fields under different geometrical parameters are within the scope of $\pm5\%$, which show that the derived analytical electric field model for DT-SJ SiC VDMOS is usable.

III. MODEL OF THE BREAKDOWN VOLTAGE

For power devices, once the electric field at any position reaches the critical field, breakdown occurs. Based on the above analysis, the electric field peak is $E(0, L_d)$, which means that when $E(0, L_d)$ increases to $E_{C,SiC}$, the breakdown happens in the DT-SJ SiC VDMOS. By integral of the electric field E from 0 to L_d, BV is obtained as:

$$BV = L_d\left[E_{C,SiC} - \frac{qTN_{sj}}{\varepsilon_{SiC}} \cdot \frac{\cosh(\frac{L_d}{T}) - 1}{\sinh(\frac{L_d}{T})}\right] \tag{6}$$

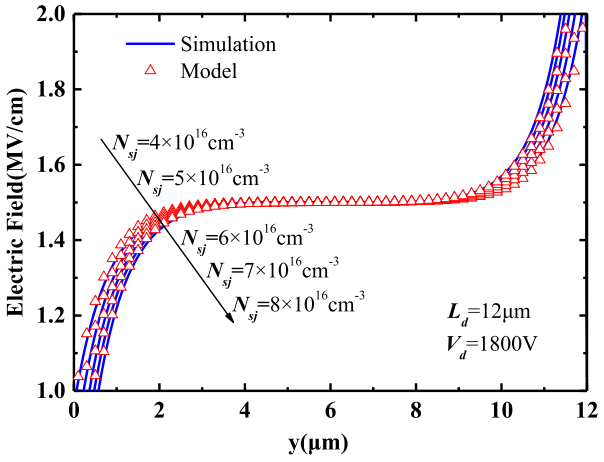

FIGURE 5. Distributions of electric fields with different N_{sj} concentration.

Obviously, the model of $E_{C,SiC}$ is the key point to the calculation of BV. A critical electric field model for SiC device had been derived by A. O. Konstantinov [36]:

$$E_{C,SiC} = \frac{2.49 \times 10^6}{1 - 0.25 \log_{10}(N_{sj}/10^{16})} \tag{7}$$

Eq. (7) is obtained based on the epitaxial p-n diodes, in which, the interreaction between the positive charges and the negative charges is totally in the vertical direction. In SJ device, there is lateral interreaction between the two types of charges in P/N pillars. With the consideration of assisted depletion effect in SJ structure, the expression of the critical electric in Eq. (7) need to be modified. Two additional constants, a and b, as shown in the following Eq. (8), are introduced to reflect the lateral depletion between the N pillar and the P pillar in the SJ structure.

$$E_{C,SiC} = \frac{2.49 \times 10^6}{1 - a log_{10}\left(bN_{sj}/10^{16}\right)} \tag{8}$$

Here, two amendatory factors, a and b, are estimated by two steps. At the first step, factors a and b are coarsely determined by massive simulation with a W_{sj} of 1μm and a L_d of 12 μm, and $a \approx 0.45$ and $b \approx 0.2$ are then found. In the second step, factors a and b are finely determined by simulation with very small step, as shown in Figs. 6 (a) and (b). Ultimately, $a = 0.45$ and $b = 0.19$ are determined with constraint of maximum relative error between theoretical and simulated results less than 3%.

Based on Eq. (8), BV model for the DT-SJ SiC VDMOS is obtained as Eq. (9).

$$BV = L_d \left[\frac{2.49 \times 10^6}{1 - 0.45 log_{10}\left(0.19N_{sj}/10^{16}\right)} - \frac{qTN_{sj}}{\varepsilon_{SiC}} \cdot \frac{\cosh\left(\frac{L_d}{T}\right) - 1}{\sinh\left(\frac{L_d}{T}\right)} \right] \tag{9}$$

The simulative results and theoretical results of BV are compared as shown in Fig. 7. The theoretical results from

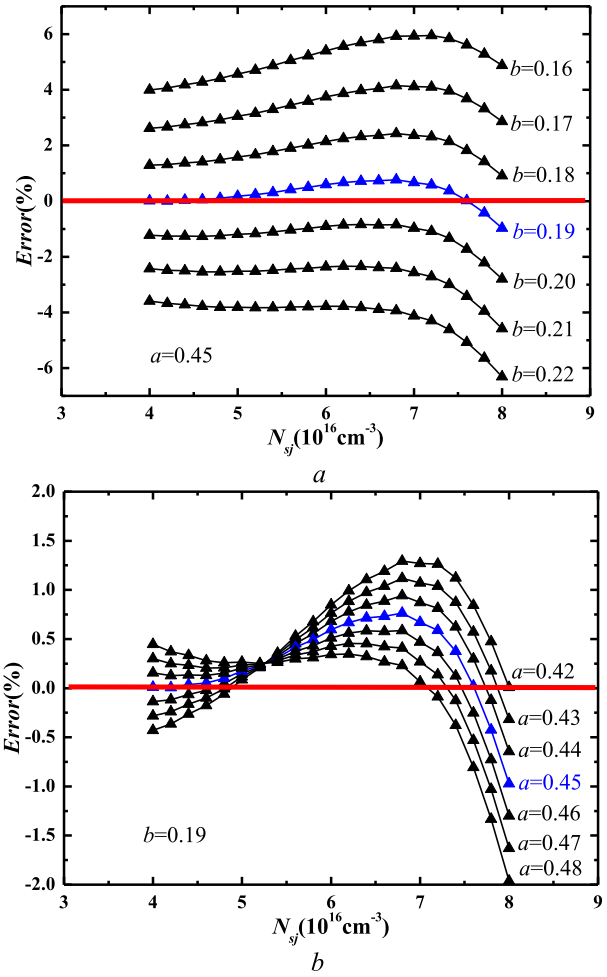

FIGURE 6. BV relative errors between model and simulation. $L_d = 12$ μm. $W_{sj} = 1$ μm. (a) with different b , (b) with different a.

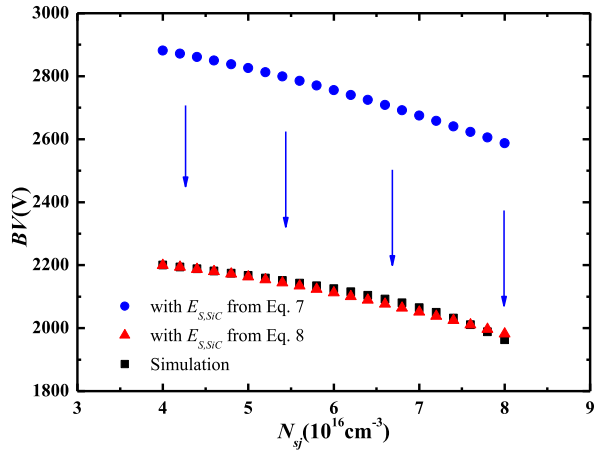

FIGURE 7. BVs between model and simulation with different N/P pillar doping concentrations N_{sj}. $L_d = 12$ μm. $W_{sj} = 1$ μm.

Eqs. (7) and (8) are both given with a W_{sj} of 1μm and a L_d of 12 μm. It is obvious that the proposed BV model of Eq. (9) matches better with the simulative results, and the relative

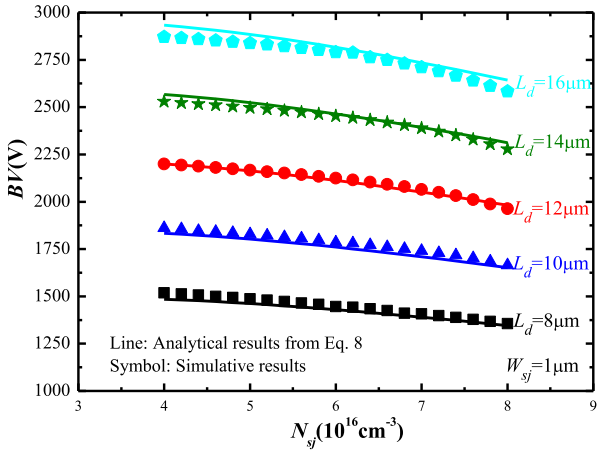

FIGURE 8. BVs between model and simulation with different thicknesses of drift region L_d. $W_{sj} = 1$ μm.

errors are less than 3% with doping concentration range from 4×10^{16} cm^{-3} to 8×10^{16} cm^{-3}.

Eq. 9 is verified in comparison with the simulative results while L_d varies from 8 μm to 16 μm. As shown in Fig. 8, under all the used conditions, the relative errors are all less than 3%.

IV. CONCLUSION

The model of the vertical electric field is derived for the DT-SJ SiC VDMOS. By fitting the critical field of the SiC SJ structure, the theoretical model of the BV is thus obtained. Extensive simulations validate the models of the electric field and BV, which will be beneficial for quantitative prediction of the breakdown characteristic of the SJ SiC device.

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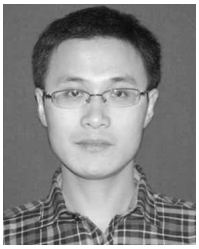

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