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Conceptual Design of Switch Network Unit for CFETR Coil Power Supply Systems

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ABSTRACT The China Fusion Engineering Test Reactor (CFETR) device is a milestone in the roadmap for the utilizing of fusion energy in China, whose final goal of plasma current is up to 10.02 MA. As the key system to generate a high enough voltage (20 kV) required for gas breakdown and plasma initiation, the Switch Network Unit (SNU) should have the ability to transfer 80 kA direct current by inserting resistor (0.25 Ω) to the superconducting coil circuit in 12 milliseconds. SNU topologies applied in other fusion devices are mostly based on the utilization of oscillation zero-point circuit, or combination of mechanical switch and semiconductor switch and so on, which bring stricter requirements for the components in the circuit and raise the cost due to the series and parallel connection of multiple devices if used in 80 kA/ 20 kV application. Based on the combination of solid-state switch (SSS) and auxiliary capacitor, this paper proposes a novel hybrid switch scheme. The SSS consists of insulated gate bipolar transistors (IGBT) group and thyristors group connected in series. The combination of added auxiliary capacitor and SSS can significantly reduce the number of series-connected IGBTs. This paper introduces the operation principle, design methods and simulation analysis of proposed scheme in detail. Coinciding with the analysis, the simulation results of SNU demonstrates the feasibility and reliability of the proposed scheme, which suggests its promising applications in fast switches with tens of kilovolts and hundreds of kilo-amperes.

INDEX TERMS CFETR, switch network unit, hybrid switch, auxiliary capacitor.

I. INTRODUCTION

The China Fusion Engineering Test Reactor (CFETR) is an indispensable fusion device to realize commercial power generation of fusion energy in China, one option of which is superconducting machine [1], [2]. Fig. 1 shows the simplified configuration of superconducting coil (SC) power supply circuit of CFETR. The switch network unit (SNU) is connected in series with the SC. It is used to generate a high enough voltage required for breakdown and plasma initiation by inserting discharge resistors in series with the coil [3]. In CFETR, the SNU is rated for up to 80 kA/20 kV, and the voltage should be established within 12 ms. The SNU is similar to DC circuit breakers (DCCB) in high voltage direct

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current (HVDC) transmission network and is also a highpower DC switch. In order to ensure the safe operation of the HVDC network, a variety of DC circuit breaker schemes have been proposed [4]–[6]. The difference between SNU and DCCB is that SNU transfers current to discharge resistor, while DCCB transfers current to arrester and removes it.

Generally, the SNU adopts a hybrid switch scheme with three branches: by-pass switch (BPS), solid-state switch (SSS) and discharge resistor (DR) as shown in Fig. 1 The BPS usually is a mechanical switch, carries current in the steady state and transfers it to SSS. The SSS operates in the pulse mode and is capable of transferring the current to DR. To this end, the SSS can be composed of IGBT or integrated gate commutated thyristor (IGCT) or thyristor switch equipped with pre-charge oscillation zero point circuit, as reported in [3], [4], [7]. The DR is used to generate



FIGURE 1. Simplified circuit schematic of superconducting coil power supply of CFETR (PMS: protective make switch, SNU: Switch network unit, BPS: by-pass switch, SSS: solid-state switch, DR: discharge resistor, SC: superconducting coil, FDU: fast discharge unit).

voltage required for breakdown and plasma initiation after current transferred to it.

The SNU is widely used in fusion experimental devices, such as EAST, JT-60SA, ITER and so on. Due to the various operation conditions and rate parameters of the devices, various SNU topologies are adopted. In EAST, the required current and voltage parameters of SNU are 15 kA and 2.4 kV which are not extremely high. Its BPS and SSS are integrated into one whole, consisting of thyristors with pre-charge oscillation zero point circuit and discharge resistor [8], [9]. In JT-60SA, the SNU, which is rated at 20 kA/5 kV, is a hybrid switch based on mechanical breaker and integrated gate-commutated thyristor (IGCT) [7], [10]. The hybrid switch scheme combines the advantages of low conduction loss of mechanical switch and fast turn-off performance of semiconductor switch, making it the first choice for high-power applications. In ITER, the SNU also adopts a hybrid switch scheme based on mechanical switch and thyristor. Unlike the scheme mentioned in JT-60SA, ITER SNU adopts an ingenious three-step commutation scheme to realize the quick transfer of current from mechanical switches to discharge resistors, with the high rated parameters (45 kA/10 kV) [3]. As for SNU of CFETR, its rated parameters are up to 80 kA/20 kV and the voltage must be established within 12 ms. Existing topologies are hard to realize these design goals. Thus, this paper proposes a novel hybrid switch scheme, which is based on the combination of solid-state switch and auxiliary capacitor. In addition, the operation principle, design methods and simulation results of SNU are also discussed in detail. Table 1 shows the parameters comparison of various SNUs of typical fusion experimental devices.

II. SNU OPERATION PRINCIPLE

Fig. 2 shows the simplified schematic diagram of CFETR SNU. It is a hybrid switch scheme, which mainly consists of four branches: by-pass switch (BPS), solid-state switch (SSS), auxiliary capacitor (AC) and discharge resistor (DR). The BPS branch is composed of a fast open switch (FOS), a fast isolation switch (FIS) and an IGBT group (S_1). Both FOS and FIS are mechanical switches that have much lower

TABLE 1. Parameters comparison of various snus of fusion devices.

Fusion Devices	Rated current	Rated voltage	Topology
EAST	15 kA	2.4 kV	thyristors with pre-charge oscillation zero point circuit.
JT-60SA	20 kA	5.0 kV	mechanical breaker and IGCT.
ITER	45 kA	10.0 kV	mechanical switch and thyristors with pre-charge oscillation zero point circuit.
CFETR	80 kA	20.0 kV	combination of solid-state switch and auxiliary capacitor.



FIGURE 2. Simplified circuit diagram of SNU of CFETR (BPS: by-pass switch, FOS: fast open switch, FIS: fast isolation switch, S_1 : an IGBT group, SSS: solid-state switch, S_2 : an IGBT group, S_3 : a thyristor group, AC: auxiliary capacitor, DR: discharge resistor.)

conduction loss compared with semiconductor switches. Thus, the conduction losses of SNU can keep at a lower level for the current flows through FOS and FIS during the steady state. S₁ consists of multi-IGBTs and aims to reliably transfer rated current 80 kA from BPS branch to SSS branch. Similarly, the SSS branch mainly consists of an IGBT group (S₂) and a thyristor group (S₃) connected in series, and is used to transfer current to auxiliary capacitor and discharge resistor. The AC can slow down the voltage rise rate to ensure the reliable turn-off of S₃. The DR (0.25 Ω) provides a high enough voltage (20 kV) needed for plasma initiation after the 80 kA current transferred to it.

Once SNU receives the action command, FOS opens and the current transfers to S_1 . Until the contacts of FOS reach a sufficient opening distance, S_1 turns off and the current starts to commutate from BPS to SSS. Then, the FIS opens without current and the FOS recloses. This allows the voltage across the BPS to be sustained by the FIS during subsequent processes, and can protect S_1 from overvoltage. Subsequently, S_2 turns off and the current transfers to AC branch and DR branch. As the capacitor is charged, the capacitor voltage rises and the current is gradually transferred to DR branch. When the current of 80 kA is completely transferred to the DR (discharge resistor, 0.25 Ω), the voltage (20 kV) is established. Moreover, before the thyristors of S_3 are turned off, the voltage across the SSS is withstood by S_2 . After the thyristors are turned off, the voltage is shared by S_2 and S_3 .

III. DESIGN METHODS OF SNU

A. BPS

Unlike most BPS of hybrid switch, the proposed BPS in SNU for CFETR adds a parallel semiconductor switch, S₁. The purpose of adding S_1 is to realize the quick commutation of current from BPS to SSS. In order to undertake high voltage and current, the SSS has to use a large number of semiconductor switches in series and parallel. This is followed by a large stray inductance and a high conduction voltage drop. However, the arc voltage generated by a conventional mechanical switch is usually only about tens of volts [11]. That is not enough for the quick commutation. Therefore, S₁, a group of IGBTs, is added and connected in parallel with FOS. For S_1 , there is no need to connect several IGBTs in series since the voltage applied to S_1 is much lower than its rated voltage when the current transfers to SSS branch. In addition, in order to reduce stray inductance of BPS as much as possible and improve the reliability of turning S_1 on, S_1 should be installed very close to FOS, so FOS can quickly transfer current to S₁ at low arc voltage.

Finally, the main requirements for FOS and FIS can be deduced as listed as follows: (1) both should be able to withstand 80 kA continuous direct current; (2) FOS has the ability to generate enough arc voltage to commutate current to S_1 in 3 ms; (3) FIS should open in 2 ms without current, according to that the 20 kV of SNU should be established in 12 ms as mentioned above; (4) FIS must quickly restore the insulating properties (< 3 ms).

B. SSS and C_{AC}

The SSS consists of IGBT group (S₂) and thyristors group (S₃) connected in series. When the SSS receives turn-off signal, S₂ will firstly turn off. Then S₃ starts the reverse recovery process, which usually takes about 200 μ s [12]. During this process, the voltage is withstood by S₂. After S₃ is turned off, the voltage across SNU is shared by S₂ and S₃. Compared with the schemes that only use IGBTs in SSS, this scheme reduces the number of series-connected IGBTs and further reduce the difficulty of realizing the dynamic voltage balancing of IGBTs connected in series. In addition, since the price of thyristors is lower than that of IGBT, the manufacturing cost of SSS will also decrease.

In order to ensure reliable turn-off of S_3 , an AC is connected in parallel with SSS. The key point, to realize the reliable turn-off of S_3 , is that the voltage of snubber capacitor of S_2 must be greater than that of AC during the reverse recovery process of thyristors. The snubber capacitor of S_2 is the total equivalent value of the capacitor of RCD snubber circuits of IGBTs, which is shown in Fig. 3. The RCD snubber circuit is used to protect the IGBT from transient overvoltage, which is usually caused by the inevitable stray inductance in the circuit. In fact, after IGBTs of S_2 turns off, the current will be firstly commutated to their RCD snubber circuits and then to



FIGURE 3. RCD snubber circuit of IGBT.



FIGURE 4. Equivalent circuit of current transfer process from SSS snubber circuit to AC.

the AC branch. After this commutation process, the thyristors of S_3 begin their reverse recovery process, during which the thyristors cannot withstand forward voltages.

Base on the equivalent circuit as shown in Fig. 4, the process of current transferring from snubber circuit to AC is discussed here. From this, the range of total snubber capacitor and AC can be deduced and obtained. In Fig. 4, C_{St} is the total equivalent snubber capacitor of S₂, C_{AC} is capacitance of the AC, R_{DR} is resistance of the DR, L_{S1} and L_{S2} are the stray inductance of the SSS branch and the AC branch, respectively.

During the short commutation process between snubber circuit and AC, current change rate can be considered to be linear. Assuming that the commutation process starts at t = 0 and end at $t = \tau$, the voltage of C_{St} at $t = \tau$ is shown as following equation:

$$U_{C_{\mathrm{St}}}(\tau) = \frac{1}{C_{\mathrm{St}}} \int_0^\tau i_1(t) dt = \frac{1}{C_{\mathrm{St}}} \int_0^\tau \left(\mathbf{I} - \frac{\mathbf{I}t}{\tau} \right) dt = \frac{\mathbf{I}\tau}{2C_{\mathrm{St}}}$$
(1)

where, I is the total current through SNU (refer to rated 80 kA here), so $I = i_1 + i_2 + i_3$. The voltage of each branch is equal as shown in (2).

$$U_{\rm C_{St}} + L_{\rm S1} \frac{di_1}{dt} = U_{\rm C_{AC}} + L_{\rm S2} \frac{di_2}{dt} = R_{\rm DR} i_3$$
(2)

According to (2), i_3 and i_2 at $t = \tau$ is equal as shown in (3) and (4).

$$i_{3}(\tau) = \frac{U_{C_{St}}(\tau) + L_{S1}\frac{di_{1}}{dt}}{R_{DR}} = \frac{I\tau}{2R_{DR}C_{St}} - \frac{L_{S1}I}{R_{DR}\tau}$$
(3)

$$i_2(\tau) = I - i_1(\tau) - i_3(\tau) = I - \frac{1\tau}{2R_{DR}C_{St}} + \frac{L_{S1}I}{R_{DR}\tau}$$
 (4)

 TABLE 2. Part parameter of SNU equivalent circuit.

Symbol	Parameters	Values
Ι	Rated current	80 kA
L_{S1}	Stray inductance of SSS branch	10 µH
L_{S2}	Stray inductance of AC branch	10 µH
$R_{ m DR}$	Discharge resistance	0.25 Ω

Based on (4) a nd considering the current change rate as a constant, the di_2/dt and the voltage of C_{AC} at $t = \tau$ can be obtained as shown in (5) and (6).

$$\frac{di_2}{dt} = \frac{i_2(\tau)}{\tau} = \frac{I}{\tau} - \frac{I}{2R_{DR}C_S} + \frac{L_{S1}I}{R_{DR}\tau^2}$$
(5)

$$U_{C_{AC}}(\tau) = \frac{1}{C_{AC}} \int_{0}^{\tau} i_{2}(t) dt$$

= $\frac{I\tau}{2C_{AC}} - \frac{I\tau^{2}}{4C_{AC}C_{St}R_{DR}} + \frac{L_{S1}I}{2R_{DR}C_{AC}}$ (6)

Combining (1), (3)-(6), (7) can be obtained by solving (2).

$$\frac{I\tau}{2C_{St}} - \frac{L_{S1}I}{\tau} = \frac{I\tau}{2C_{AC}} - \frac{I\tau^2}{4C_{AC}C_{St}R_{DR}} + \frac{L_{S1}I}{2R_{DR}C_{AC}} + L_{S2}\left(\frac{I}{\tau} - \frac{I}{2R_{DR}C_S} + \frac{L_{S1}I}{R_{DR}\tau^2}\right)$$
(7)

Further, the relationship between τ and circuit parameters can be obtained by solving (7) as shown in (8).

$$\tau^{4} + 2R_{\rm DR} \left(C_{\rm AC} - C_{\rm St} \right) \tau^{3} + 2 \left(L_{\rm S2} C_{\rm AC} - L_{\rm S1} C_{\rm St} \right) \tau^{2} - 4R C_{\rm AC} C_{\rm St} \left(L_{\rm S1} + L_{\rm S2} \right) \tau - 4C_{\rm AC} C_{\rm St} L_{\rm S1} L_{\rm S2} = 0$$
(8)

After the current is transferred to C_{AC} , since the voltage of C_{St} is greater than the voltage of C_{AC} , C_{St} begins to discharge, and C_{AC} starts charging simultaneously. Ignoring the influence of L_{S2} , the voltage of C_{AC} after $t = \tau$ is as follows:

$$U_{\mathrm{C}_{\mathrm{AC}}}(t) = IR_{\mathrm{DR}} + \left(U_{\mathrm{C}_{\mathrm{AC}}}(\tau) - IR_{\mathrm{DR}}\right)e^{-t/R_{\mathrm{DR}}C_{\mathrm{AC}}}$$
(9)

Assuming the voltage of C_{St} remains constant in a short time, the time (Δt), required for the voltage of C_{AC} to be equal to the voltage of C_{St} , can be obtained as shown in (10).

$$\Delta t = R_{\rm DR} C_{\rm AC} \ln \left(\frac{U_{C_{\rm AC}}(\tau) - IR_{\rm DR}}{U_{C_{\rm St}}(\tau) - IR_{\rm DR}} \right)$$
(10)

In addition, to ensure reliable turn-off of the thyristors, Δt must be longer than the turn-off time (t_q) of the thyristors.

According to (1) and (8), when other parameters are as shown in Table 2, the voltage of C_{St} at $t = \tau$ versus various C_{St} and C_{AC} is shown in Fig. 5. According to (1), (8), (9) and (10), Δt versus various C_{St} and C_{AC} is shown in Fig. 6. Indicated from Fig. 5 and Fig. 6, both the voltage of C_{St} at $t = \tau$ and the Δt decrease with the C_{St} . The voltage of C_{St} at $t = \tau$ increasing means the larger number of series-connected IGBT in S₂. Therefore, a compromise is required between the number of series-connected IGBTs and Δt . Moreover, increasing C_{AC} can lower the voltage of C_{St} at $t = \tau$ and



FIGURE 5. Voltage of C_{St} versus various C_{St} and C_{AC}.



FIGURE 6. Δt versus various C_{St} and C_{AC} .

TABLE 3. Main parameters of semiconductor switches.

Parameters	IGBT	Thyristors
Туре	5SNA 3000K452300	KK _C 2700-45
Rated current (A)	3,000	2,786
Rated voltage (V)	4,500	4,500
Surge current (during 10 ms, kA)	21.0	36.8
Turn-off time (µs)	5.85	200

increase Δt . But considering the cost, the C_{AC} should take a suitable value, not the bigger the better.

Based on the IGBT of 5SNA 3000K452300 type and the thyristors of KK_C 2700-45 type, the values of C_{St} and C_{AC} in SNU of CFETR are analyzed in detail. Main parameters of semiconductor switches are given in Table 3 [12], [13]. According to the voltage level of C_{St} shown in Fig. 5, the number of series-connected IGBT should be at least 2. Considering a certain safety margin, the voltage of C_{St} should

FOS open S_1 turn on	S ₁ turn off SSS turn on	FIS open FOS close	S ₂ turn off	
$T_1 = 0.5 ms$	$T_2 = 3.0 \text{ ms}$	$T_3 = 3.5 \text{ ms}$	$T_4 = 5.0 \text{ ms}$	

FIGURE 7. Action sequence of SNU in simulation.

be less than 7,500 V, and the Δt should be larger than 300 μ s. Therefore, it is appropriate for C_{St} to take 1.5~1.7 mF and C_{AC} to take 4~5 mF.

In fact, the voltage balancing and the current sharing are two challenging issues in series and parallel switches. In SNU, these issues are mainly caused by the parameter deviations of switches and the stray parameters of the branches. In order to cope with uneven voltage distribution, the rated voltage of S_2 and S_3 should be 1.2 times greater than the actual voltage. Therefore, the IGBT series number of S2 and the thyristor series number of S_3 are 2 and 4, respectively. Due to the turn-on time of both IGBTs and thyristors is within 3 ms, the current should be kept below the surge current. The IGBT of 5SNA 3000K452300 type can still turn off a current of 19.0 kA after 5 ms and has been reported in [14]. Considering the uneven current distribution and a certain margin, the parallel number of IGBTs in this paper is set as 10. Thus, each IGBT only needs to turn off a current of ~ 8 kA, which is much smaller than 19.0 kA as mentioned. And this is beneficial to extend the life of IGBTs. In a similar way, the parallel number of thyristor KK_C 2700-45 type (as shown in Table 3) is 5 and each thyristor carries a current of ~ 16 kA (< 36.8 kA).

IV. RESULTS OF SIMULATION

The simulation of full model of SNU is carried out to verify the feasibility of the proposed scheme. The models of semiconductor switches used in the simulation are datasheetbased behavioral models. The rated current of the superconducting coil is 80 kA and is assumed to remain constant during whole commutation process. S₁ uses a 1 (series) × 10 (parallel) IGBTs group, S₂ uses a 2 (series) × 10 (parallel) IGBTs group and S₃ uses a 4 (series) × 5 (parallel) thyristors group. The other parameters used in the simulation are $R_{DR} =$ 0.25 Ω , $C_{AC} = 4$ mF, $C_{St} = 1.5$ mF, $L_{S1} = L_{S2} = 10 \mu$ H. The simulation is also carried out with the stray inductance (L_{S1} and L_{S2}) taking 20 μ H and other parameters unchanged. The action sequence of SNU in simulation is shown in Fig. 7.

The simulation results are given in Fig. 8 to Fig. 10. In the Fig. 8, the solid line and the dotted line indicate the current waveforms when $L_{S1} = L_{S2} = 10 \ \mu\text{H}$ and $L_{S1} = L_{S2} = 20 \ \mu\text{H}$, respectively. The current of FOS starts to decrease after 0.68 ms because a certain action delay is set. It can be seen that the current can be transferred to DR even if the stray inductance is 20 μ H. However, stray inductance also has a negative impact on the current commutation process, that is, the pulse current amplitude is increased. The voltage waveforms of SNU during commutation process at $L_{S1} = L_{S2} = 10 \ \mu\text{H}$ is as shown in Fig. 9.



FIGURE 8. Current waveforms of SNU during commutation process (solid line: $L_{S1} = L_{S2} = 10 \ \mu$ H, dotted line: $L_{S1} = L_{S2} = 20 \ \mu$ H).



FIGURE 9. Voltage waveforms of SNU during commutation process when $L_{S1} = L_{S2} = 10 \ \mu$ H.

It is worth mentioning that the voltage is initially undertaken by S_2 after S_2 is switched off. When the voltage of $C_{\rm AC}$ is greater than the voltage of $C_{\rm St}$, the voltage bore by S₃ begins to rise. Before this, the thyristors have completed the reverse recovery process and are turned off. The maximum voltage of S₂ in the simulation is 8,568 V. It's slightly higher than the calculation result (7,300 V) as shown in Fig. 5, which is the calculation error caused by the simplified calculation (assuming the current change rate during the short commutation process between snubber circuit and AC is linear, as mentioned in (1)). Although the maximum voltage of S_2 is within the acceptable range, to ensure reliability, C_{St} or the number of series-connected IGBTs in S2 should be increased appropriately. As shown in Fig. 10, the voltage of S_2 is up to 11,316 V which is larger than its rated voltage (9,000 V). From Fig. 9 and Fig. 10, it can be concluded that the voltage sharing between S_2 and S_3 is greatly affected by the stray inductance. The larger the stray inductance, the larger the voltage of S₂ and the more series number of IGBT.



FIGURE 10. Voltage waveforms of SNU during commutation process when $L_{S1} = L_{S2} = 20 \ \mu$ H.

In conclusion, the simulation results prove the feasibility of the proposed SNU scheme and the design methods. In addition, the current oscillation at time $3\sim5$ ms indicates the adverse effects of stray inductance. Thus, in practical engineering design and application, this inductance should be minimized to reduce overvoltage and snubber capacitance.

V. CONCLUSION

This paper presents the conceptual design of SNU for CFETR coil power supply systems. It is a novel hybrid switch based on mechanical switch, solid-state switch and auxiliary capacitor. The proposed design of solid-state switch not only can quickly transfer the current up to 80 kA, but also combines the advantages of IGBT and thyristors. The utilization of IGBT allows the switch to have the ability to actively turn off the current without a counterpulse circuit. Moreover, the combination of solid-state switch (SSS) and auxiliary capacitor reduces the number of series-connected IGBT. This not only helps to reduce costs, but also makes it easier to achieve voltage balancing of IGBTs. Moreover, the key issues associated with the proposed design, namely the reliable turn-off of thyristors and the selection of capacitors parameters, have been deeply analyzed. The simulation results have proved the feasibility of the proposed scheme.

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