IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received September 15, 2019, accepted September 24, 2019, date of publication October 1, 2019, date of current version October 15, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2944876

Analysis and Verification of a Novel Single-Photon Memristor

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This work was supported by the National Natural Science Foundation of China for the Youth under Project 11502224.

ABSTRACT This work reports a device based on single-photon memristor. In this paper, the equivalent circuit model of single-photon memristor was established, and we stimulated three distinctive signatures of general memristors by this model. Through the incident photon is absorbed, the device goes from the avalanche state to the quenching state, then back to the equilibrium state, and we obtained the experimental results. The results of three distinctive signatures of general memristors are verified by the test of the real single-photon memristor, which is fabricated with 0.18 μm CIS technology. On the basis of the memristive characteristics of this device, it can be applied in chaotic circuit integrated with single-photon memristor and neural network.

INDEX TERMS Single-photon memristor, memristive characteristics, avalanche.

I. INTRODUCTION

Memristor is a circuit device that represents the relationship between magnetic flux and charge. The resistance of a memristor, different from resistor, which be determined by the charge flowing through it. In 1971, Leon Chua reasoned from symmetry arguments that there should be a fourth fundamental element in nature [1], [2]. In 2008, researchers at Hewlett-Packard company made nano-memristor devices for the first time, which set off an upsurge in memristor research [3]. With the arrival of the post-Moore era, researchers had successively developed different memristive devices, such as Cu/SiO_2/Pt electrochemical metallization memristor [4], Au/SAM/Pd molecular junction and Pd/SAM/Pd molecular junction memristor [5], Au/ PEDOT:PSS/ Au memory device [6] photoelectric-motivated memristor [7] and so on.

Although the researcher had developed photoelectric-motivated memristor based on avalanche photo-diode [7], the actual measurement data currently has an error due to the error of the test system. Meanwhile, the frequency of the photoelectric-motivated memristor is out of control because the device is triggered by noise in the case of dark counting. For optimizing the actual measurement data and verifying the frequency characteristics of the photoelectric-motivated memristor, we analyzed and verified a new single-photon memristor based on single photon avalanche diodes (SPAD), which is fabricated with 0.18 μm CIS (CMOS image sensor) technology. Compared with avalanche photo-diode (APD), the single photon avalanche diode (SPAD) has higher quantum efficiency and the SPAD structure can reduce noise in the case of dark counting effectively, so the actual measurement data of novel memristor can be in good accordance with simulation results and the frequency of the single-photon memristor is in control because the device is triggered by single photon. Generally speaking, general memristive device has three special properties. Firstly, a distinctive signature of memristive device is a hysteresis loop. Secondly, the sidelobe area of hysteresis loop decreases with frequency increasing. Finally, when subject to a periodic stimulus, a memristive device typically behaves as a linear resistor in the limit of infinite frequency, and as a non-linear resistor in the limit of zero frequency [2]. In this paper, the equivalent circuit model of the single photon memristor was employed to verify that the proposed device has three distinctive signatures of general memristive device. And the simulation results of proposed memristive device are in good accordance with experiment measurements. On the other hand, CMOS image sensor technology has many advantages, such as low power consumption, fast speed, strong anti-interference ability and high integration. Most of the integrated devices are manufactured by CIS technology [8], [9], which has become the mainstream technology of large scale integrated devices. Therefore, a new single-photon memristor was proposed, which has a strong anti-interference ability and is accessible for large-scale

The associate editor coordinating the review of this manuscript and approving it for publication was Sun Junwei.

integration. This device also has a useful application prospect in both chaotic circuit [10]–[12] and neural network [13].

II. MODELING AND FINGERPRINTS OF SINGLE PHOTON MEMRISTOR

The novel memristive behavior is dominated by the photoelectric response of the single photon memristor. A single photon memristor is a common P+/N+/P-sub junction, operating in Geiger-mode.

When the single photon memristor is reversed biased, there is an electric field near the P-N junction, which distributes the electrons to n region and the holes to p region, in Figure 6d (1). If the incident photon (energy >1.1 eV in the case of silicon) is absorbed this moment, the electronic-hole pair is formed. Under the electrical field formed in the depletion layer, the electron can obtain enough field energy to collide with the crystal lattice and produce another electron-hole pair. This process leads to loss of kinetic energy, called impact ionization. Meanwhile, the secondary electrons can obtain energy again, and produce more electron-hole pairs, so the called ''avalanche''. Moreover, if the magnitude of the reverse-bias voltage is greater than the breakdown voltage, leading the number of electrons and holes to increasing, and electrons migrate to the cathode and holes migrate to the anode [14], [15]. The number of electrons and holes in the high-field region and the connected photocurrent rises exponentially in time. The greater above breakdown voltage the memristor is reversed biased, the fewer the rising time constant. Due to the presence of the rising number of electrons and holes or the rising current, this growth of current lasts for so long as the electric fields in the memristor are negligibly changed. During this process, the resistance of novel memristor is decreased by the formation of conductive filament, in Figure 6d (2) and (3).

However, if there is a series resistance in the memristor, the resistance's voltage rises gradually with the increase of the current, which reduces the voltage dropped in the electric field region, thus slowing down growth rate of the avalanche. Finally, the high-field voltage is reduced to the breakdown voltage, and the production and extraction rates are balanced in the breakdown voltage, thus the equilibrium state is formed. At this point, the current will not increase (or decrease), and the series resistance is provided a negative feedback function, which inclines to steady the vacillation of current level. For example, the vacillation of current come down leads to the decrease of series resistance's voltage and the equal increase of high-field region's voltage. This process in turn increases the impact ionization rate and leads current to back-flow.

However, the connection between a memristor and a low impedance power supply does not allow the detection of avalanche openings or closures, enabling the memristor to be ready to detect another photon. Closing the avalanche current is called quenching, and is realized by passive quenching circuit and gated detector operation. In a passive quenching circuit, the memristor is loaded on some bias above breakdown and then left open circuited. As long as the memristor is turned on, the memristor releases its capacitance until it no longer exceeds the breakdown voltage and the avalanche disappears. Particularly, to reprogram the memory unit, quenching process is required to erase conductive filaments from anode to cathode. A ballast resistance Rl in series with the single photon memristor makes up the simplest quenching circuit, implementing the so-called passively quenching circuit. During the quenching-reset process, the conductive filament nearby anode will be disintegrated in part and migrate back to the direction of depletion layer by discharging process of negative feedback circuit [15], [16], in Figure 6d (4). Using such a method, the single photon memristor can achieve the operations of ''write'' and ''erase'' under the existence of light.

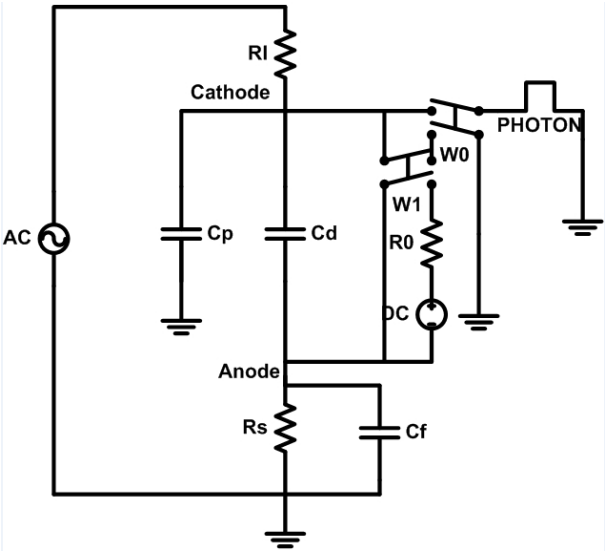

FIGURE 1. Schematic diagram of the single photon memristor model and passively quenching circuit with Cadence Spectra.

In order to carry out the performances of the proposed memristor, the equivalent circuit model of SPAD and passively quenching circuit given in Figure 1 is investigated. There are two switches W0 and W1. When optical pulse voltage has reached, the switch W0 is turned off. When supply voltage has exceeded breakdown voltage, the switch W1 is turned off. In other cases, the switch W0 and W1 will be turned on.

In the avalanche process, the population of electrons and holes in the high-field region and the associated photo-current grow exponentially in time. If the single photon memristor has been turned off by switch W0 and W1, it charges its own capacitance until it is above the breakdown voltage. With a time constant R_0C_s, we obtain

$$V_{ava}(t) = (V_s(t) - V_{bd})(1 - \exp(-\frac{t}{R_0C_s}))$$

$$I_{ava}(t) = C_f * \frac{dV_{ava}(t)}{dt} + \frac{V_{ava}(t)}{R_s}$$

As Figure 1 shows, there are electrical model of a SPAD. Cp and Cf are the P+/P-substrate and N+/P-substrate parasitic capacitances, respectively. Cd is the P+/N+ parasitic capacitance. R0 is internal resistance of a SPAD. DC is the

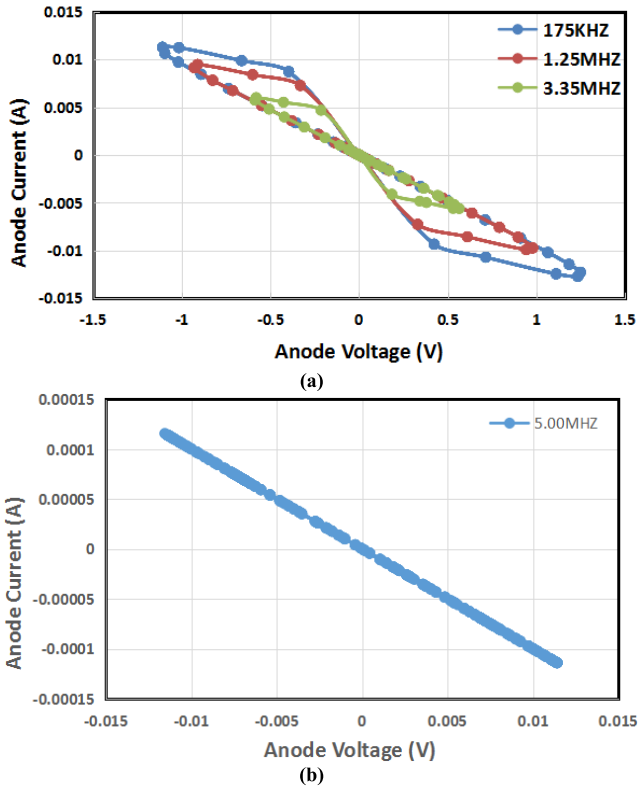

FIGURE 2. (a) The pinched hysteresis loop at different frequencies (b) the device behaves as a linear resistor at 5.00MHZ.

breakdown voltage Vbd of the device. Cs is total parasitic capacitance of SPAD. AC and PHOTON are supply voltage Vs and optical pulse, respectively.

TABLE 1. Model parameters for the simulated single photon memristor.

Symbol	Quantity	Value
AC(Vs)	applied reverse voltage	18.5 V
DC(Vbd)	breakdown voltage of SPAD	10.6 V
R_S	sampling resistor	100 Ω
R_L	quenching resistor	51 kΩ
R0	internal resistance of SPAD	267 Ω
C_d	P+/N+ parasitic capacitance	322fF
C_p	P+/P-substrate parasitic capacitances	500fF
C_f	N+/P-substrate parasitic capacitances	120fF
f	frequency of applied voltage	175 KHZ/1.25 MHZ/3.35 MHZ/5.00MHZ
V_{pulse}	pulse voltage of simulated photon	5 V
T_r/T_f	rise time/fall time of pulse voltage	10 ps/10 ps
T_w	pulse voltage width	2 ns
T	pulse voltage period	500ns

In a passive-quenching circuit, the single photon memristor is charged up to some bias above breakdown and then left open circuit. Once the single photon memristor has been turned on by switch W0 and W1, it discharges its own capacitance until it is no longer above the breakdown voltage, at which point the avalanche dies out. With a time constant $R_L C_s$, the model predicts that current exponential decays to zero and voltage to breakdown level [17]. On the basis of this proposition, we obtain

$$V_{que}(t) = (V_s(t) - V_{bd})(-\exp(-\frac{t - T_Q}{R_L C_s}))$$
$$I_{que}(t) = C_f * \frac{dV_{que}(t)}{dt} + \frac{V_{que}(t)}{R_s}$$

As Figure 1 shows, there are electrical model of a passively quenching circuit. Rl and Rs are ballast resistance and sampling resistance, respectively. Tq equals avalanche time. The model parameters for the simulated single photon memristor are shown in Table 1. Here internal resistance R0 value of SPAD and the value of breakdown voltage Vbd were obtained through measured current-voltage curve of reversed biased SPAD. In order to let the high-field voltage reduce to the breakdown voltage and form an equilibrium state, the value of ballast resistance Rl should be more 100 times than internal resistance R0 value of a SPAD, so Rl equals 51KΩ. These simulations took conventionally available values of capacitive load of the materials as inputs, as well as the independently calibrated thicknesses from the device fabrication. The optical pulse width is 2ns because the avalanche state of this device last for nanoseconds order of magnitude.

According to simulation data, the current-voltage correlation of a novel memristor is obtained on the basis of passively quenching readout circuit. The variations of the pinched hysteresis loop at different frequencies are shown in Figure 2. It is observed that the sidelobe area of hysteresis loop decreases with frequency increasing, in Figure 2(a). Meanwhile, the single photon memristor behaves as a linear resistor at 5.0 MHZ, in Figure 2(b).

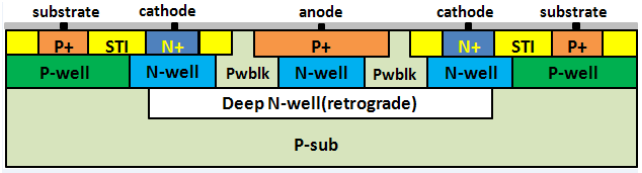

FIGURE 3. The cross section of the designed SPAD.

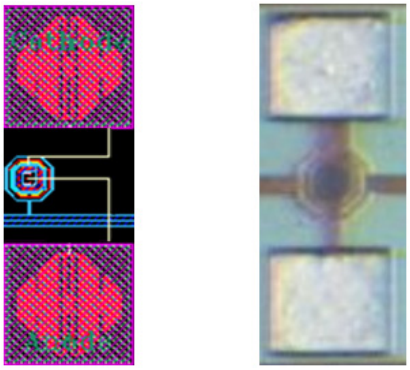

FIGURE 4. The layout of the designed octagon SPAD and Micro-photograph of the SPAD.

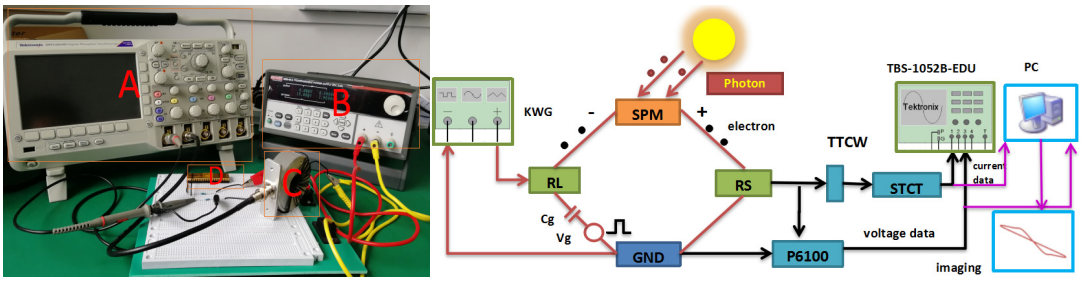

FIGURE 5. (a) Test platform of the single photon memristor with its quenching circuits (b) the diagrammatic sketch of test platform.

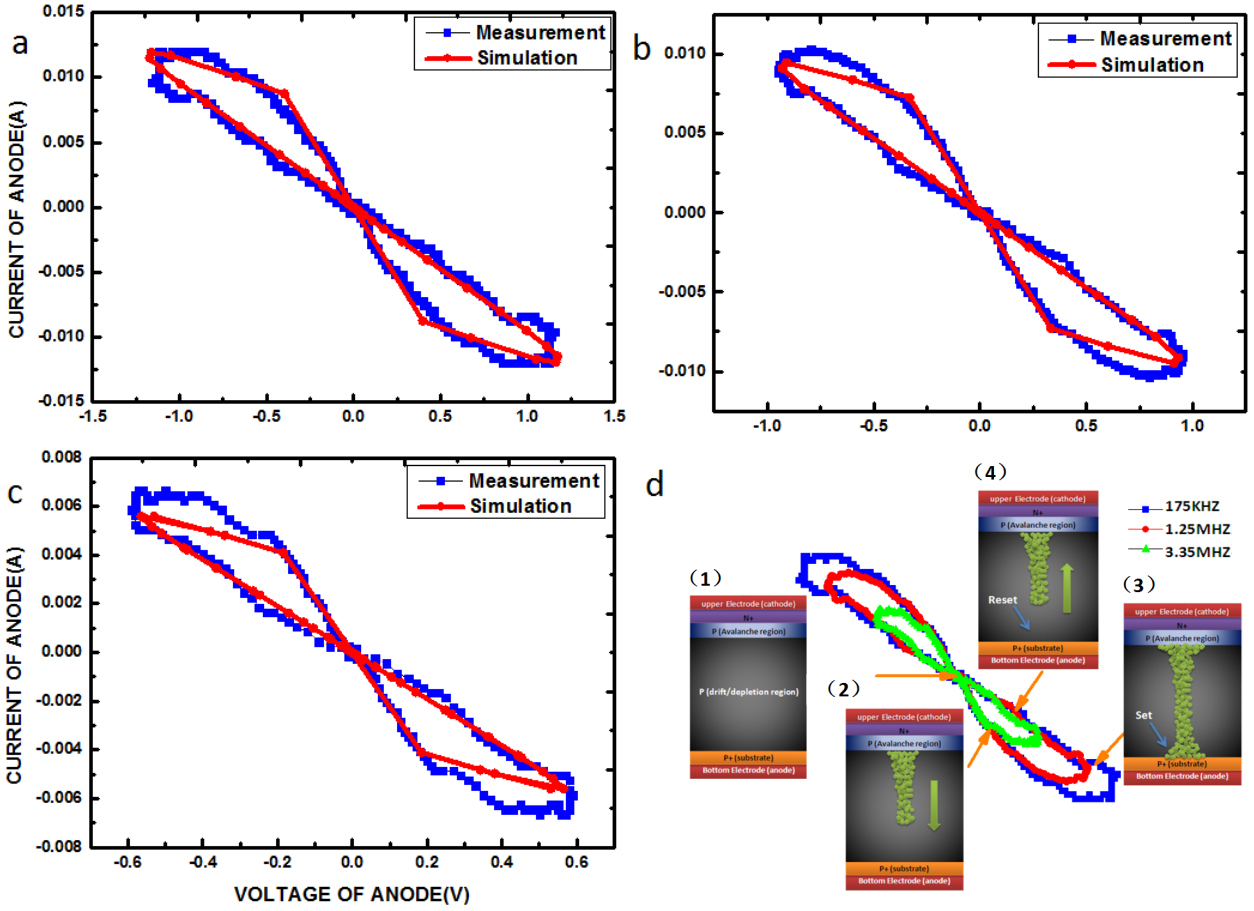

FIGURE 6. Simulation results are in accordance with experiment data at 175KHZ (a), 1.25MHZ (b) and 3.35MHZ (c) frequencies. (d) Hysteresis loop of the tested single-photon memristor at different frequencies. Inset: the working principle sketch of single-photon memristor.

III. DEVICE FABRICATION AND EXPERIMENTAL VERIFICATION

As can be seen in Figure 3, the SPAD consists of a P+ /N-well junction and a circular virtual guard-ring which is made out of lightly doped Pwblk. A planar and shallow P+ /N-well junction is used to define the active region for photon detection where charge multiplication occurs. The space charge region is achieved by diffusing the curved edge of the P+ implant into a surrounding Pwblk ring, so as to reduce electrical filed non-uniformities which can cause premature edge breakdown. Another N type well is implanted with a deep N-well doping profile. The upward diffuse of doped atoms in the deep wafer improves the active region's ability of collecting charges. Note that the STI delimits the SPAD, while the Pwblk guard ring ensures that the electric field is maximized in the center of the device [18]. Moreover, all the non-active areas of SPAD are covered with the metal layers to avoid lighting, which can cause higher noise probability.

A 0.18 μm CIS technology has been selected for manufacturing the SPAD. The layout and micro-photograph of the designed octagon SPAD are shown in Figure 4. A diameter of P+/N-well junction of SPAD is 8μm. The total diameter of the designed octagon SPAD is 25μm. The total area of the fabricated chip is 70μm*210μm. The oscilloscope (module A, TBS-1052B-EDU) was mainly used for pulse waveform display and pulse waveform data extraction. The passively quenching circuit of the SPAD (module D) was driven by using Keysight waveform generator (module B, KWG).

The electrical measurements were conducted using a straight-through current transformer (module C, STCT) for current measurements and a probe P6100 for voltage measurements in Figure 5(a) and (b), respectively. In various applications, it is necessary to control high-sensitivity single photon memristor under gated detector operation. In the case of single photon memristor, the task is much simpler: the amplitude of gated pulse VG is slightly higher than the excess bias voltage VE, which allows the memristor to switch from turning off (at voltage $Vs < Vbd$) to turning on (at the operating voltage $Vs + VG = Vbd + VE$). If the memristor is turned off a long time enough before it is put into operation, the trapped carrier is almost empty and does not interfere with the following measurement. Note that Cg (Cg $>>$ Cd + Cs) should be high enough in order to minimize the relative loss in pulse amplitude [19].

Electrical bias was applied to the upper electrode and ballast resistance Rl, while the bottom electrode and resistance Rs was grounded. We have measured on voltage and current of device, which can achieve high and low resistance state. The experimental results of the proposed memristor are in accordance with theoretical and simulation analysis at different frequencies, as shown in Figure 6. Note that ten turns coiling windings (TTCW) are employed due to 1:10 attenuation of the current transformer.

IV. CONCLUSION

In this paper, we have verified that the proposed device has three distinctive signatures of general memristors. Firstly, we can obtain hysteresis loop of single-photon memristor. Secondly, according to simulation and experiment results, the sidelobe area of hysteresis loop decreases with frequency increasing. Finally, when subject to a periodic stimulus, a novel memristor typically behaves as a linear resistor in the limit of infinite frequency. Meanwhile, we derive an advantage in memristor yield, which can be steadily integrated on a silicon-based chip. The single photon memristor can be applied for chaotic circuit. Our results can be leveraged for further investigation of switching dynamics for chaotic circuit and open unforeseen perspectives for single photon memristor in future application.

ACKNOWLEDGMENT

The author would like to thank HU Xin of Zhengzhou Shengda University of Economics, Business & Management, for English writing.

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