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Theory and Design of Impedance Matching Network Utilizing a Lossy On-Chip Transformer

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ABSTRACT In this paper, we present a study on a transformer-based impedance matching network. We use a simplified transformer model comprising two magnetically coupled coils, which are driven by a source and terminated by a load. The formulae of the load and the source impedance for conjugate matching of both sides of the transformer are presented, and a figure of merit is proposed for the evaluation of the power transfer efficiency of the transformer under conjugate matching conditions. Analytical expressions are provided for constructing the widely used transformer network consisting of a resistive load and a parallel tuning capacitor. To verify the proposed work, we examined various on-chip transformers implemented in 0.18 μm CMOS technology. Simulation and measurement results for a matching network synthesized using the aforementioned analytical expressions corresponded well with the result of analysis for operating frequencies up to 72% of the self-resonant frequency of the transformer. The presented results confirm that the proposed analytical formulae based on the simplified transformer model are useful for the design and optimization of transformer-based impedance matching networks in the microwave and millimeter-wave regimes.

INDEX TERMS CMOS technology, impedance matching, power efficiency, transformers.

I. INTRODUCTION

At present, numerous radio frequency integrated circuit (RFIC) designs are being implemented with transformers for various purposes such as impedance matching, impedance transformation, and signal conversion between single-ended and differential signals in various frequency bands ranging from the radio frequency (RF) to terahertz regimes. Transformers are used in many applications, including power amplifiers, low-noise amplifiers, voltage-controlled oscillators, mixers, and power-combining circuits [1]–[9]. Therefore, many studies have been published on modeling and analyzing transformers, new transformer structures, and new methods for enhancing transformer efficiency [10]–[15]. However, most of these studies are not only complex but also application-specific, making it difficult to directly apply the proposed techniques to the practical design of a highly efficient transformer.

In particular, when we use a transformer for a specific purpose such as impedance transformation or signal balancing, the transformer should be optimally designed to provide maximum power transfer from the source to the load. It is well known that the input and output ports of a transformer should be simultaneously conjugate matched to the source and load impedances [16]. The general solution of the load and the source to the simultaneous conjugate match for a two-port network using Z-parameters was presented originally in [17], or recently in [18]. However, little analytical details can be seen for specific structures used in RF circuit design such as the impedance matching network consisting of a lossy transformer and a shunt tuning capacitor for calculating the optimum source and load impedances. Relevant work on synthesizing lossless impedance matching networks was given in [19] which gave the detailed analysis and synthesis of the lossless matching network based on the transmission phase shift from a given source to a load. Nevertheless, the work did not cover the impedance matching network using a lossy transformer.

Considerable effort has been devoted to optimizing the efficiency of transformers. In [20], the authors presented formulae for a series load (a resistor in series with a capacitor)

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for achieving the maximum efficiency. However, they cannot be extended to a transformer-based matching network with a resistive load in parallel with a capacitor, which is widely used in RFICs [21]–[24]. In the wireless power transfer (WPT) field, an inductive power link involves a load with a parallel tuning capacitor; the load resonates with the inductive part of the transformer [25]. Although optimum load equations have been proposed, the assumptions made for deriving them render them impractical for a typical transformer. In addition, these studies have not considered impedance matching at the source, which is as important as impedance matching at the load for power transfer from the source to the load. Based on the work in [17], a comprehensive solution of the load and the source for inductively coupled coils for the wireless power transfer application was presented in [26]. However, it did not cover the transformer-based impedance matching network with a shunt tuning capacitor which has been widely used in RFIC design.

In this study, we developed a systematic approach to the design and analysis of a transformer-based impedance matching network. We derived general conditions for the source and load from the characteristic parameters of the transformer for optimal power transfer. For a simplified transformer model involving two magnetically coupled coils, analytical equations were derived for simultaneous conjugate matching, and the transformer parameters were extracted from Z-parameters. On the basis of an analysis of the maximum power transfer condition, the product of the coupling coefficient k and the quality factors of the primary (Q_1) and secondary (Q_2) windings $k^2Q_1Q_2$ was used as a figure of merit to evaluate the quality of the transformer.

This paper consists of five sections. We present a detailed analysis of the impedance matching of the on-chip transformer based on two magnetically coupled coils in Section II. To demonstrate the validity and applicability of the derived equations for various transformer parameters, a typical 2:1 on-chip transformer designed in a 0.18 μm CMOS process was evaluated with the High Frequency Structure Simulator (HFSS). A comparison of the calculated values with the simulation results is presented in Section III to demonstrate the validity of the presented analysis. Next, in Section IV, we present a design for impedance matching with a transformer containing a parallel tuning capacitor at the load and source, along with an analysis of the impedance matching. In Section V, the fabrication of the on-chip transformer (mentioned in Section III) in a 0.18 μm CMOS process is discussed, and our works are compared with measurement results to verify the applicability of the proposed work on the on-chip transformer to RFIC design in the gigahertz regime. Finally, conclusions are provided in Section VI.

II. IMPEDANCE MATCHING FOR A GENERAL LOAD

A. LOW-FREQUENCY TRANSFORMER MODEL WITH TWO MAGNETICALLY COUPLED COILS

In a passive transformer, an input signal or input power from the source is transferred to the load by the magnetic coupling between two or more conductors, which are called windings. Notably, when we implement a winding transformer on a silicon substrate, the series resistance of each winding is quite significant because of the fabrication of the windings on relatively thin metal layers within back-end-of-the-line (BEOL) dielectric layers, and the skin effect in the metal windings in modern silicon technologies.

Several secondary effects, such as capacitive coupling and magnetic coupling to the substrate, lower the quality factor Q of each coil. For the accurate modeling of the on-chip transformer, an enormously large number of lumped-element parameters should be considered [27]. Therefore, this type of sophisticated modeling might not be quite appealing in the early stages of design optimization. Instead, we extracted the effective transformer parameters for the two magnetically coupled coils from Z-parameters, and the extracted parameters were then used in the derived analytical formulae to design a simultaneous conjugate matching network, which demonstrated a promising accuracy of the maximum power transfer by the frequency response up to 72 % of the self-resonant frequency (SRF) of the transformer within a percentage error of 10 %.

Typically, a transformer can be considered as two magnetically coupled coils, as shown in Fig. 1. In this simplified model, the transformer is characterized by only five parameters: the series resistances (R_1 and R_2), the inductances (L_1 and L_2) of the primary and secondary windings, and the coupling coefficient, which indicates the strength of the magnetic coupling between the two windings [27]. The turn ratio between the two windings is defined as $n = L_1/L_2$. It is noteworthy that the parasitic coupling capacitance between the two coils was neglected in this work since the complexity of the model and the analysis were considerably increased while the effect is marginal at the frequency of interest (below SRF) when it was considered. (Some of the effects of this coupling capacitance can be found in [28].) The simple low-frequency model has been widely used as a core circuit to characterize transformers in many studies (e.g., [10]–[15]) since the physical size of transformers is usually designed to be noticeably less than the guided wavelength at the operating frequency [27]. Therefore, it can reflect dominant physical phenomena occurring in a transformer with an inductance and magnetic coupling of the windings at operating frequencies

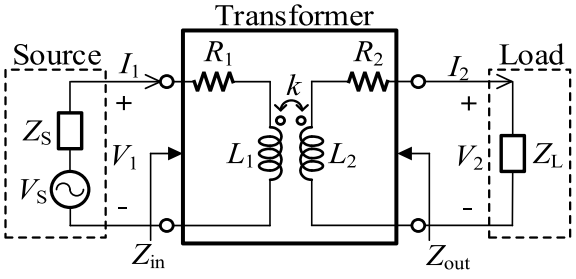

FIGURE 1. Low-frequency transformer model with two magnetically coupled coils with load and source terminations.

well below the SRF of the transformer. The validity of a low-frequency model is discussed in Section III.

B. IMPEDANCE MATCHING WITH TWO MAGNETICALLY COUPLED COILS

An important criterion that designers should consider when using a transformer is the amount of power delivered from the source to the load, especially in applications such as WPT [3], [25], and impedance transformation in power amplifiers [1], [2], [4], [21], [22], [29]. We can assess the efficiency of the network with regard to the power from the transducer power gain G_T, which is defined as the ratio of the power delivered to load P_L to the power available from source P_{avs} [16]:

$$G_T = \frac{P_L}{P_{avs}} = \frac{P_L}{P_{in}}\frac{P_{in}}{P_{avs}} = \eta(1-|\Gamma_s|^2), \tag{1}$$

where P_{in} is the input power delivered from the source to the network (including the transformer and load) and $\eta = P_L/P_{in}$ is the power efficiency (operating power gain) of the network [20]. Γ_S is the source reflection coefficient, and it is given by

$$\Gamma_S = \frac{Z_{in} - Z_S^*}{Z_{in} + Z_S}, \tag{2}$$

where Z_S and Z_{in} are the source and network impedances, respectively. Thus, impedance matching is important to obtain an optimal transducer power gain for a given passive network. On the source side, Z_{in} should be the conjugate of the source impedance: $Z_{in} = Z_S^*$. Similarly, the load impedance Z_L should be the conjugate of the output impedance Z_{out} on the load side: $Z_L = Z_{out}^*$. The former condition maximizes the power delivered from the source to the network when the source is given, and the latter condition maximizes the power delivered to the load when the source and transformer are given.

We can consider the transformer as a two-port network driven by a source and terminated by a load, as shown in Fig. 1. The transformer is modeled using two magnetically coupled inductors, and the load and the source impedances are given by

$$Z_L = R_L + jX_L \quad \text{and} \quad Z_S = R_S + jX_S, \tag{3}$$

where R_L and X_L are the equivalent series resistance and reactance of the load, respectively, while R_S and X_S are the equivalent series resistance and reactance of the source, respectively. The relationship between the input (V_1) and output (V_2) voltages for the input and output currents, given by I_1 and I_2, respectively, can be written as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} (R_1 + j\omega L_1) & -j\omega M \\ j\omega M & -(R_2 + j\omega L_2) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{4}$$

$$V_2 = Z_L I_2, \tag{5}$$

where ω is the angular frequency, and $M(= k(L_1L_2)^{1/2})$ is the mutual inductance between the primary inductor (L_1) and the secondary inductor (L_2). The quality factors Q_1 and Q_2 of the primary and secondary inductors are calculated as

$$Q_1 = \frac{\omega L_1}{R_1}; \quad Q_2 = \frac{\omega L_2}{R_2}. \tag{6}$$

As shown in Appendix A, simultaneous conjugate matching on both sides of the transformer can be achieved either when the transformer is ideal ($R_1 = R_2 = 0$) or when Z_S and Z_L satisfy the following conditions:

$$\begin{cases} X_L = -\omega L_2, X_S = -\omega L_1 & (7.1) \\ R_L = R_2\sqrt{1+k^2Q_1Q_2}, R_S = R_1\sqrt{1+k^2Q_1Q_2}. & (7.2) \end{cases}$$

The equations in (7) are the derivation of the general conjugate matching condition based on Z-parameters presented in [17] for the transformer model with the impedance matrix in (4).

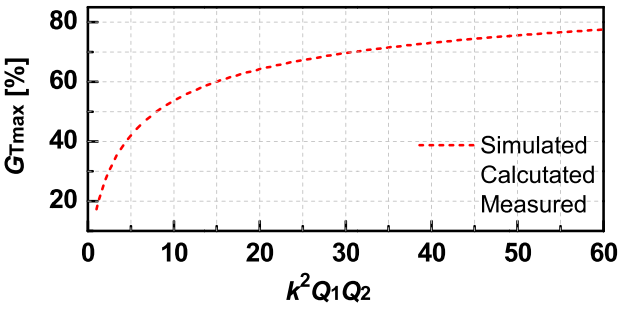

FIGURE 2. Maximum transducer power efficiency (G_{Tmax} [%]) versus $k^2Q_1Q_2$.

C. FIGURE OF MERIT FOR A TRANSFORMER, OBTAINED FROM THE TRANSDUCER POWER GAIN

Under the simultaneous conjugate matching conditions on both sides of the transformer, the maximum of the transducer power gain G_{Tmax} is calculated in Appendix B as

$$G_{T\,\max} = 1 - 2\frac{\sqrt{k^2Q_1Q_2+1}-1}{k^2Q_1Q_2}. \tag{8}$$

It is noteworthy that because the optimal transducer power gain in (8) is obtained under the condition $\Gamma_s = 0$, it eventually equals the optimal power efficiency derived in [20], which is presented in (1). Fig. 2 shows the maximum transducer power gain as a function of $k^2Q_1Q_2$. (The simulation and measurement setups are described in Sections III and V, respectively.) Clearly, G_{Tmax} increases rapidly as $k^2Q_1Q_2$ increases in the low-value region of the x-axis and saturates at a sufficiently large value. Therefore, $k^2Q_1Q_2$ is a reasonable candidate for the figure of merit, which can be used to assess the quality of the designed transformer.

For a given transformer, the load and source impedances calculated from (7) can be used for performing simultaneous conjugate matching for both source and load ($\Gamma_L = \Gamma_S = 0$), which would maximize the transducer power gain.

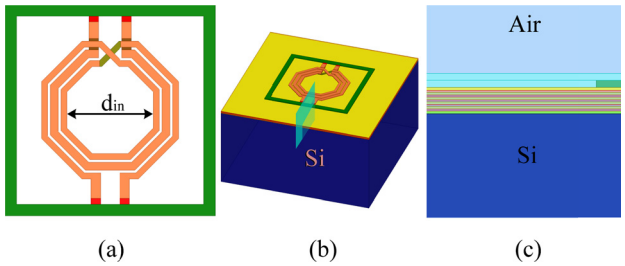

FIGURE 3. On-chip 2:1 transformer structure used for 3D electromagnetic simulation: (a) the front face, (b) a 3D view in HFSS, and (c) a side view of the layer stacks used in HFSS.

III. VERIFICATION OF THE PROPOSED ANALYSIS WITH AN ON-CHIP TRANSFORMER IN A 3D EM SIMULATION

In this section, we discuss the examination of a typical on-chip winding transformer (presented in Fig. 3) that is widely used for interstage matching in millimeter-wave circuits in silicon technologies [1], [2], [29]–[31]. In this study, an on-chip transformer was designed in a 0.18 μm CMOS process by using an 8.625 μm thick back-end-of-line (BEOL) stack and a 300 μm thick silicon substrate. The complex dielectric stacks from the BEOL process were simplified into 14 equivalent dielectric layers, each of which was calculated on the basis of a series capacitance approximation verified in previous works [2], [4], [32], [33]. The conductivity of the substrate was set to 10 S/m. An on-chip winding transformer with a side-coupled structure was implemented using a 2 μm ultra-thick metal. The primary winding inductor had one turn, and its width was set to 8 μm, while the secondary inductor had two turns and was 6 μm wide. The gap between two adjacent turns was set to 3 μm, and the inner diameter (d_{in}) of the octagonal winding inductor was 90 μm. In microwave inductor and transformer design, a definite return path is necessary to achieve good agreement between the HFSS simulation and measurements. Therefore, we placed ground tiles all over the area, which was modeled as a square ring around the transformer, as shown in Fig. 3.

We performed 3-D electromagnetic (EM) simulations with HFSS for the transformer design to attain its two-port Z-parameters. Subsequently, the parameters of the low-frequency transformer model R_1, R_2, L_1, L_2, and k were extracted as below (depicted in Fig. 4)

$$R_i = Re\{z_{ii}\}; \quad L_i = \frac{Im\{z_{ii}\}}{\omega}; \; k = \frac{\sqrt{Im\{z_{12}\} \times Im\{z_{21}\}}}{\sqrt{Im\{z_{11}\} \times Im\{z_{22}\}}} \tag{9}$$

where $i = \{1, 2\}$; z_{ij} with $i, j = \{1, 2\}$ is the element of the extracted Z-matrix.

The simulated SRF was 51.8 GHz for the designed 2:1 on-chip transformer. The effective inductance of the two windings increased rapidly near the SRF because of the resonance between the winding inductor and the parasitic capacitances seen from the winding inductor. When the operating frequency exceeded the SRF, the effective reactance of each inductor became capacitive.

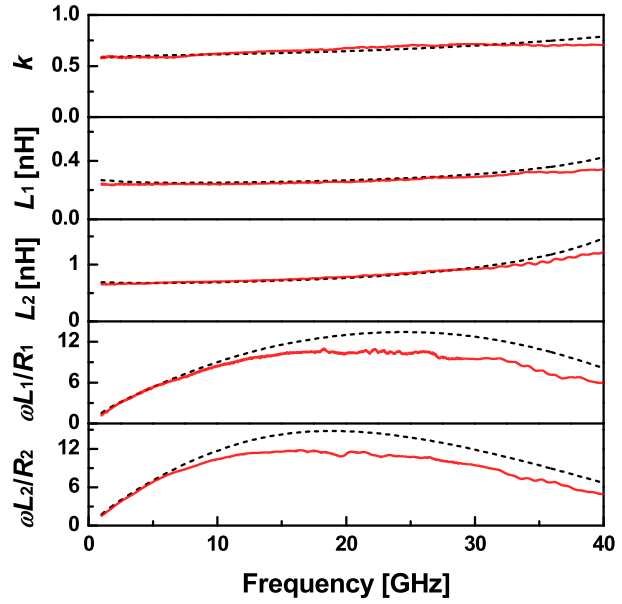

FIGURE 4. Simulated (dashed line) and measured (solid line) values of the effective parameters of the on-chip 2:1 transformer.

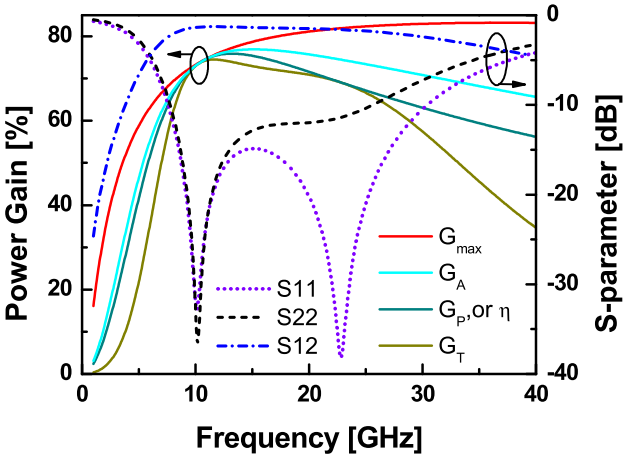

FIGURE 5. Simulation results for several power gains of the 2:1 transformer as a function of the operating frequency.

Fig. 5 shows the simulation results for various power gains of the on-chip transformer when the source and load impedances were conjugately matched at 10 GHz. The analytical expressions given in (7) were used to achieve simultaneous conjugate matching. Here, G_{Tmax} (or G_{max}) is the maximum transducer power gain with $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$; $G_A (= P_{avn}/P_{avs})$ is the available power gain, which is defined as the ratio of the power available from the transformer (P_{avn}, or the maximum power that can be delivered to the load) to the power available from the source; and $G_P (= P_L/P_{in})$ is the operating power gain (or the power efficiency η of the transformer in [20]) [16]. As evident, all the mentioned power gains had the same value when both source and load were simultaneously conjugate matched at 10 GHz. Fig. 5 presents the simulation results of the

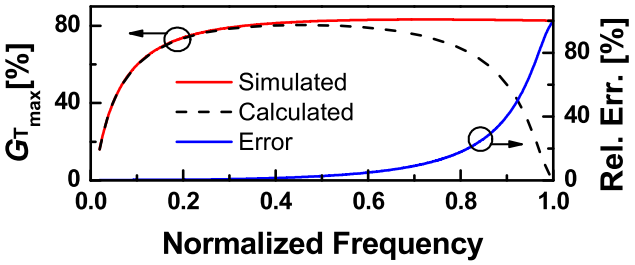

FIGURE 6. Plot of optimum power efficiency versus frequency for the 2:1 transformer with SRF = 51.8 GHz.

S-parameters. S_{11} on the source side and S_{22} on the load side were less than −30 dB, while S_{21} reached its maximum value at 10 GHz.

Fig. 6 shows a comparison between G_{Tmax} calculated from (8) (which is also the maximum power efficiency η_{max}) and G_{Tmax} simulated with Spectre ™; both parameters are plotted against the normalized frequency ($f_{nor} = f_o$/SRF) for SRF = 51.8 GHz. We determined the percentage error, defined as the difference between the simulated and calculated values divided by the simulated value, to quantify the limitation of the low-frequency model. At a relatively low frequency ($f_{nor} < 0.72$ or $f < 37.3$ GHz) compared with the SRF of the transformer, the calculated G_{Tmax} matched well with the simulated G_{Tmax} within an error of 10%.

It is quite encouraging that such a simple low-frequency model can provide promising results in a frequency range of around 72% of the SRF of the transformer coil. As the operating frequency approaches the SRF of a transformer, the parasitic coupling capacitances between the primary and the secondary windings and between them and the substrate start to play a vital role [27]. Furthermore, with an increase in the operating frequency, the mutual resistance associated with the eddy currents induced by the coupled magnetic flux of another inductor increases the power loss [34]–[36]. Therefore, the operating frequency of the on-chip transformer is typically chosen to be well below the SRF since the input and output impedances of the transformer change drastically around the SRF. Accordingly, the low-frequency model used in this study is acceptable for this typical case.

IV. TRANSFORMER MATCHING CONFIGURATION WITH A PARALLEL TUNING CAPACITOR

A. TRANSFORMER MATCHING NETWORK CONFIGURATIONS

Fig. 7(a) shows a compact lumped circuit model for a typical monolithic transformer derived from two magnetically coupled coils and intended for operation at a relatively low frequency compared with the SRF [27]. Aoki *et al.* transformed this low-frequency model into a T-model, and they used the T-model for investigating the power efficiency ($\eta = P_L/P_{in}$) as well as the power enhancement ratio (PER) of a typical transformer for impedance transformation [20]; they presented conditions for the optimal power efficiency of a

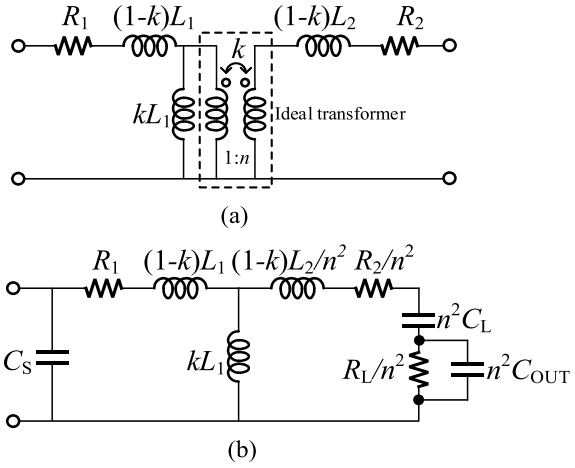

FIGURE 7. Impedance transformation in a transformer with a load, series tuning capacitors, and an extra tuning capacitor in parallel to the load.

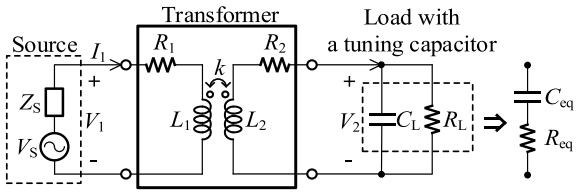

FIGURE 8. Configuration for impedance transformation in a transformer with a tuning capacitor in parallel with the load, and the series equivalent circuit of the configuration.

transformer network with three additional capacitors. Such a network is shown in Fig. 7(b). The series capacitor C_L in series with the load is tuned to maximize the transformer's power efficiency, and another capacitor C_{OUT} in parallel with the load is used to reduce the turn ratio n, which makes it possible to use a transformer with a reasonable turn ratio while keeping the PER unchanged. On the source side, a shunt capacitor C_S is added to adjust the input reactance to the desired value. More recently, a configuration with a tuning capacitor in parallel with the load has been widely used [21]–[24]; the configuration is shown in Fig. 8. In this configuration, the parallel capacitor can increase the efficiency of the transformer (if it is tuned to a proper value) as well as transform the equivalent series load resistance to $R_{eq}<R_L$, which relaxes the requirement for the turn ratio n. Moreover, when an active device is used as the load, the tuning capacitor can absorb uncalculated parasitic capacitances of the device.

Although this configuration with a parallel capacitor (Fig. 8) has been widely used in implementing a transformer-matching network, to the best of the authors' knowledge, no analytical design equations have been reported so far. Such equations must be readily applicable in the hand calculation at the early stage of design. It should be noted that the configuration in Fig. 8 is different from that in Fig. 7(b). When we transform the parallel network configuration (R_L in parallel with C_L or a tuning capacitor C_t) in Fig. 7 to

the series equivalent circuit (R_{eq} in series with C_{eq}), it is easy to confuse the parallel configuration (shown in Fig. 8) with its series counterpart (shown in Fig. 7b). Thus, the optimization conditions of the load with a parallel capacitor are different from those for the network presented in Fig. 8.

In the following, for a transformer network with a capacitor in parallel with a resistive load, we present design formulae that can be used for achieving optimum power efficiency by choosing the optimal parallel capacitor.

B. CALCULATION OF OPTIMAL LOAD AND SOURCE IMPEDANCES FOR A GIVEN TRANSFORMER

For the load impedance, given by $Z_L = R_L + jX_L$, in Fig. 7(b) (excluding C_{OUT}), the power efficiency (calculated in Appendix C) is given by

$$\eta = \frac{R_L}{(R_L + R_2) + R_1 \frac{(R_L+R_2)^2+(\omega L_2+X_L)^2}{(\omega M)^2}}. \tag{10}$$

If R_L is independent of $X_L(= -1/\omega C_L)$, η is maximized at $X_L = -\omega L_2$, which is identical to the condition presented in [20].

Let us consider the transformer with a load and a tuning capacitor ($C_L = C_t$) in parallel with the load, as shown in Fig. 8. The equivalent series reactance and resistance of the load are given by

$$R_{eq} = \frac{R_L}{1 + (\omega R_L C_t)^2}; \quad X_{eq} = -\frac{\omega R_L^2 C_t}{1 + (\omega R_L C_t)^2}. \tag{11}$$

By replacing the calculated values from (11) with the corresponding quantities in (10), the power efficiency can be expressed as a function of R_{eq} and X_{eq}. However, R_{eq} is a function of X_{eq} when C_t is tuned for fixed R_L. Therefore, we should not substitute X_{eq} with the aforementioned optimum value $(-\omega L_2)$ of X_L for maximizing η.

In order to calculate the value of C_t that maximizes η, we express η as follows:

$$\frac{P_{loss}}{P_L} = \frac{1}{\eta} - 1 = \frac{1 + (\omega R_L C_t)^2}{R_L} \times \left\{ R_2 + \frac{R_1}{(\omega M)^2} \left[\left(R_2 + \frac{R_L}{1 + (\omega R_L C_t)^2} \right)^2 + \left(\omega L_2 - \frac{\omega R_L^2 C_t}{1 + (\omega R_L C_t)^2} \right)^2 \right] \right\}, \tag{12}$$

where P_{loss} is the power dissipated in the transformer. The ratio P_{loss}/P_L should be minimized to maximize η.

By denoting $x = \omega R_L C_t$, this ratio can be expressed as

$$\frac{P_{loss}}{P_L} = ax^2 - 2bx + c, \tag{13}$$

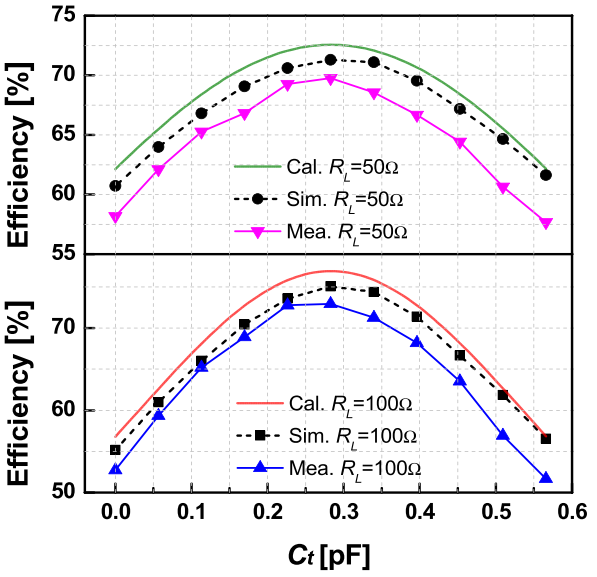

FIGURE 9. Plot of the power efficiency versus the value of the parallel tuning capacitor for the on-chip 2:1 transformer at 10 GHz.

where

$$a = \frac{R_2}{R_L} + \frac{R_1}{R_L}\frac{R_2^2 + (\omega L_2)^2}{(\omega M)^2}; \quad b = \frac{R_1 L_2}{\omega M^2}; \quad c = a + \frac{(2R_2 + R_L)R_1}{(\omega M)^2}. \tag{14}$$

Because $a > 0$, the ratio P_{loss}/P_L is minimized at $x = b/a$, where we can obtain the optimal parallel tuning capacitor (C_{topt}) as

$$C_{topt} = \frac{L_2}{R_2^2(1 + Q_2^2 + k^2 Q_1 Q_2)} \approx \frac{1}{(k^2+1)\,\omega^2 L_2}\Bigg|_{\substack{Q_1=Q_2 \\ Q_1Q_2(1+k^2)\gg 1}} \tag{15}$$

At this point, the maximum power efficiency is given by

$$\eta(C_{topt}) = \frac{1}{1 + c - \frac{b^2}{a}}. \tag{16}$$

As evident from (15), the optimum value of the parallel capacitor C_{topt} is less sensitive to the quality factors of the transformer if Q_1 is close to Q_2 and the product Q_1Q_2 (k^2+1) is sufficiently higher than unity. By applying C_{topt} in (15) to (11), we obtain X_{eqopt}, which differs from $-\omega L_2$ used in Fig. 7(b). Fig. 9 shows plots of the calculated and simulated efficiency versus C_t for two values of R_L at 10 GHz. Except for the tuning capacitor ($C_L = C_{topt}$) in parallel with the given load resistance R_L, the simulation setup was the same as before. Owing to the parasitic capacitor of the two windings, a peak discrepancy of around 2.5% was observed between the efficiency calculated from (15) and the simulated value. Interestingly, C_{topt} is not a function of R_L.

We can also obtain the same design formulae by using a different approach. When both source and load values are

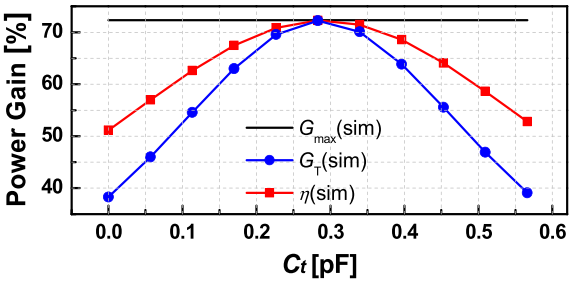

FIGURE 10. Plot of simulated power gains versus the value of the parallel tuning capacitor (Z_S is calculated from (7) and R_L is given by (18)).

set, it is desirable to find the impedance matching condition on both sides of the transformer so that the maximum transducer power gain, which is also the maximum power efficiency ($\eta_{max} = G_{Tmax}$) is obtained. The source and load impedances are given by (7) to achieve this condition. Therefore, the equivalent series resistance R_{eq} and equivalent series reactance X_{eq} should satisfy the conditions:

$$\begin{cases} R_{eq} = \dfrac{R_L}{1+(\omega R_L C_t)^2} = R_2\sqrt{1+k^2Q_1Q_2} \\ X_{eq} = -\dfrac{\omega R_L^2 C_t}{1+(\omega R_L C_t)^2} = -\omega L_2. \end{cases} \tag{17}$$

By solving these two equations, R_{Lopt} and C_{topt} are calculated as

$$\begin{cases} R_{Lopt} = R_2\sqrt{1+k^2Q_1Q_2}\left(1+\dfrac{Q_2^2}{1+k^2Q_1Q_2}\right) \\ C_{topt} = \dfrac{L_2}{R_2^2(1+Q_2^2+k^2Q_1Q_2)}. \end{cases} \tag{18}$$

Naturally, the optimum value of C_{topt} in (18) is the same as that in (15). Fig. 10 shows plots of the simulated power gains—G_{Tmax}, G_T, and the operating power gain (or power efficiency η)—around $C_t = C_{topt}$. In this verification, Z_S and R_L are chosen so that $\Gamma_S = \Gamma_L = 0$ at the optimum value C_{topt}, which is calculated using (18); Z_S is computed using (7) and (18) gives $R_L = R_{Lopt}$.

Similarly, if the source has the same structure, which means that the source consists of a resistor (R_{Sp}) in parallel with a tuning capacitor (C_{Sp}), the optimum values of parameters R_{Sp_opt} and C_{Sp_opt} to maximize the transducer power gain are given by

$$\begin{cases} R_{Sp\_opt} = R_1\sqrt{1+k^2Q_1Q_2}\left(1+\dfrac{Q_1^2}{1+k^2Q_1Q_2}\right) \\ C_{Sp\_opt} = \dfrac{L_1}{R_1^2(1+Q_1^2+k^2Q_1Q_2)}. \end{cases} \tag{19}$$

V. EXPERIMENTAL VERIFICATION

To demonstrate the validity of the proposed approach, we implemented various transformers with and without parallel capacitors in a 0.18 μm CMOS process. A reference transformer was also included to confirm the validity of the transformer model in HFSS, which is shown in Fig. 3 for

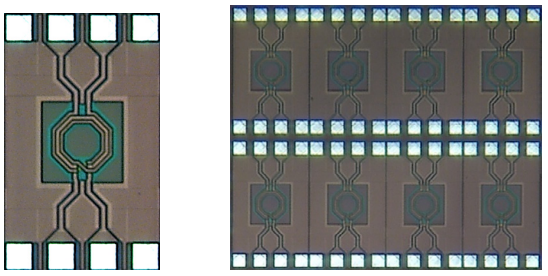

FIGURE 11. Photographs of the on-chip transformers fabricated in 0.18 μm CMOS technology: (a) the standalone 2:1 transformer, and (b) transformers with parallel tuning capacitors.

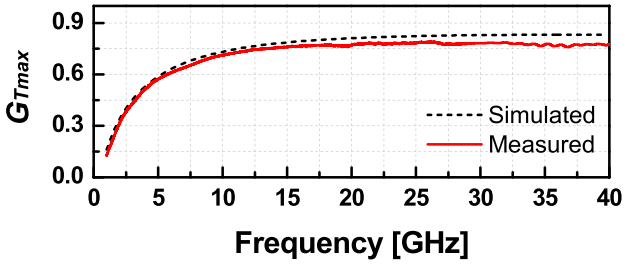

FIGURE 12. Plots of optimum power efficiency versus frequency for the on-chip 2:1 transformer.

$d_{in} = 9\mu$m. Fig. 11(a) presents a photograph of a fabricated transformer with two signal pads. The S-parameters of the transformer were measured and de-embedded from the pads and transmission lines that did not belong to the transformer. Parameters of the low-frequency model transformer—k, L_1, L_2, Q_1, and Q_2—were then extracted and compared with those extracted from the simulation, which are shown in Fig. 4. The maximum power gain (G_{Tmax}) was also extracted from the measured S-parameters; it is depicted in Fig. 2 along with plots of calculated and simulated values.

Fig. 4 shows that the measured inductances and coupling coefficients fit the simulation results quite well. By contrast, simulation results in the high-frequency region ($f > 7$ GHz) showed that the measured quality factors of the two coils were degraded. The optimistic loss consideration in the model, which does not hold true in a real environment, may cause this discrepancy. Specifically, the loss tangents of the dielectric materials depend on the frequency in the real case while they were assumed to be constants in HFSS which were extracted at low frequency region. In addition, the rough metal surfaces in the fabricated transformer could cause more loss at high-frequency region [37].

Because the maximum power gain is suppressed quickly when the product $k^2Q_1Q_2$ becomes large (as shown in Fig. 2), the G_{Tmax} extracted from measurements was still comparable to the simulated value (as shown in Fig. 12), regardless of the degradation of the measured quality factors Q_1 and Q_2 compared to those simulated (depicted in Fig. 4). In addition, in the high-frequency region (compared to the SRF), the parasitic capacitor also plays a role in the increase in G_{Tmax}, as shown in Fig. 6.

To verify the analysis proposed in section IV, we measured several fabricated transformers with parallel capacitors at the load; they are presented in Fig. 11(b). The S-parameters were de-embedded from the RF pads and extra transmission lines. Subsequently, power efficiencies for specific loads of 50 and 100 Ω were extracted (Fig. 9). The measured data indicated that the optimum C_t was the same for the two loads and that it deviated from the simulation value by around 20 fF (nearly 7%). The shift in the measured C_{topt} is because of the difference between the fabricated transformer and its model; this is shown by the extracted parameters in Fig. 4. Another reason could be that the nominal capacitance specified by the manufacturer was different from the actual value because of process variations. From the extracted parameters of the fabricated transformer, the optimum parallel load resistor R_{Lopt} was calculated to be 103 Ω by using (18). Therefore, the case of $R_L = 100\Omega$ still provided a higher power efficiency, which was confirmed by measurements when C_t was around its optimum value.

VI. CONCLUSION

We present a systematic analysis of and design formulae for an impedance matching network with a two-winding transformer. To develop design guidelines for the optimization of a transformer network, we investigated the role of the resistive and the reactive parts of the source and load in achieving the maximum power transfer. We present the design formulae, obtained from the aforementioned analysis, for the optimum source and load impedance of a given transformer for the case where a parallel tuning capacitor is used to achieve optimal power transfer in the transformer network. The validity of the proposed formulae was verified for a 2:1 on-chip transformer simulated and measured in a 0.18 μm CMOS process with a 3D EM simulator (HFSS). The results of the present study are widely applicable to various sectors in the fields of RFICs, WPT, and any transformer network operating below the transformer SRF.

APPENDIX A

From (4) and (5), we can obtain the input impedance as

$$Z_{in} = \frac{V_1}{I_1} = \left\{ R_1 + \frac{(\omega M)^2 (R_2 + R_L)}{(R_2 + R_L)^2 + (\omega L_2 + X_L)^2} \right\} + j \left\{ \omega L_1 - \frac{(\omega M)^2 (\omega L_2 + X_L)}{(R_2 + R_L)^2 + (\omega L_2 + X_L)^2} \right\}. \quad \text{(A1)}$$

Because the transformer is symmetric, Z_{out} can be derived from Z_{in} by replacing R_1, L_1, and Z_L with R_2, L_2, and Z_S, respectively, as follows:

$$Z_{out} = \left\{ R_2 + \frac{(\omega M)^2 (R_1 + R_S)}{(R_1 + R_S)^2 + (\omega L_1 + X_S)^2} \right\} + j \left\{ \omega L_2 - \frac{(\omega M)^2 (\omega L_1 + X_S)}{(R_1 + R_S)^2 + (\omega L_1 + X_S)^2} \right\}. \quad \text{(A2)}$$

If simultaneous conjugate matching conditions are met ($Z_S = Z_{in}^*$ and $Z_L = Z_{out}^*$), then we have

$$\begin{cases} R_L = R_2 + \dfrac{(\omega M)^2 (R_1 + R_S)}{(R_1 + R_S)^2 + (\omega L_1 + X_S)^2} \\ X_L = -\omega L_2 + \dfrac{(\omega M)^2 (\omega L_1 + X_S)}{(R_1 + R_S)^2 + (\omega L_1 + X_S)^2} \\ R_S = R_1 + \dfrac{(\omega M)^2 (R_2 + R_L)}{(R_2 + R_L)^2 + (\omega L_2 + X_L)^2} \\ X_S = -\omega L_1 + \dfrac{(\omega M)^2 (\omega L_2 + X_L)}{(R_2 + R_L)^2 + (\omega L_2 + X_L)^2}. \end{cases} \quad \text{(A3)}$$

If we express parameters as $r_L = R_L + R_2$, $x_L = X_L + \omega L_2$, $r_s = R_s + R_1$, and $x_s = X_s + \omega L_1$, then (A3) becomes

$$\begin{cases} r_L = 2R_2 + \dfrac{(\omega M)^2 r_S}{r_S^2 + x_S^2}, & \text{(A4.1)} \\ x_L = \dfrac{(\omega M)^2 x_S}{r_S^2 + x_S^2}, & \text{(A4.2)} \\ r_S = 2R_1 + \dfrac{(\omega M)^2 r_L}{r_L^2 + x_L^2}, & \text{(A4.3)} \\ x_S = \dfrac{(\omega M)^2 x_L}{r_L^2 + x_L^2}. & \text{(A4.4)} \end{cases}$$

Case 1: Consider $x_s \neq 0$ ($\Leftrightarrow x_L \neq 0$).
By replacing x_s in (A4.4) with (A4.2), we obtain

$$r_S^2 + x_S^2 = \frac{(\omega M)^4}{r_L^2 + x_L^2}. \quad \text{(A5)}$$

By using this expression for (A4.1) after replacing r_s in (A4.1) with that in (A4.3), we obtain

$$\begin{aligned} r_L &= 2R_2 + \frac{(\omega M)^2 \left(2R_1 + \frac{(\omega M)^2 r_L}{r_L^2 + x_L^2} \right)}{\frac{(\omega M)^4}{r_L^2 + x_L^2}} \\ &= 2R_2 + \frac{2R_1 \left(r_L^2 + x_L^2 \right)}{(\omega M)^2} + r_L \\ &\Rightarrow r_L^2 + x_L^2 = -\frac{R_2}{R_1} (\omega M)^2 . \end{aligned} \quad \text{(A6)}$$

Apparently, there is no solution for r_L and x_L that satisfies (A6), and therefore, the equations in (A3) have no solution.
Case 2: Consider $x_s = x_L = 0$. Therefore, (A4) becomes

$$\begin{cases} r_L = 2R_2 + \dfrac{(\omega M)^2}{r_S} \\ r_S = 2R_1 + \dfrac{(\omega M)^2}{r_L}. \end{cases}$$

$$\Rightarrow \begin{cases} r_L r_S = 2R_2 r_S + (\omega M)^2 \\ r_S r_L = 2R_1 r_L + (\omega M)^2 \end{cases} \Rightarrow r_S = r_L \frac{R_1}{R_2} \quad \text{(A7)}$$

By substituting this expression in the first expression in (A7), we obtain

$$r_L = 2R_2 + \frac{(\omega M)^2}{r_L \frac{R_1}{R_2}} \Rightarrow r_L^2 - 2R_2 r_L - \frac{R_2}{R_1} (\omega M)^2 = 0.$$

We know that $r_L = R_L + R_2$. By substituting this expression in the above equation, we can write

$$R_L^2 - R_2^2 - \frac{R_2}{R_1}(\omega M)^2 = 0 \Rightarrow R_L = R_2\sqrt{1 + \frac{(\omega M)^2}{R_1 R_2}} = R_2\sqrt{1 + k^2 Q_1 Q_2}.$$

Similarly,

$$R_S = R_1\sqrt{1 + k^2 Q_1 Q_2}.$$

From (A4), one can quickly point out that if $R_1 = R_2 = 0$ (an ideal transformer), then solutions for x_L and r_L in (A4.1) and (A4.2) automatically satisfy (A4.3) and (A4.4), respectively. This shows that when a transformer is ideal, a conjugate match on the source side leads to one on the load side. Intuitively, we can see that if the transformer is lossless, the transfer of the maximum power from the source to the network (including the transformer and load) implies that the maximum power is delivered to the load.

APPENDIX B

From (4) and (5), we can write

$$I_1 = \frac{(R_2 + R_L) + j(\omega L_2 + X_L)}{j\omega M} I_2. \tag{B1}$$

Under the condition $\Gamma_S = 0$, we can use (1) to obtain

$$G_T = \eta = \frac{P_L}{P_{avs}} = \frac{R_L |I_2|^2}{2P_{net}\left(Z_{in} = Z_s^*\right)} = \frac{R_L |I_2|^2}{R_{in} |I_1|^2 \left(Z_{in} = Z_s^*\right)} = \frac{R_L |I_2|^2}{R_S |I_1|^2}.$$

Using (7) along with the above formula and (B1), we can obtain

$$G_{T\max} = 1 - 2\frac{\sqrt{k^2 Q_1 Q_2 + 1} - 1}{k^2 Q_1 Q_2}. \tag{B2}$$

APPENDIX C

Because the mutual inductance is modeled as a pure imaginary value, the power loss in the transformer is the total resistive loss in the two windings expressed as

$$P_{loss} = (1/2)R_1 |I_1|^2 + (1/2)R_2 |I_2|^2.$$

The power consumed by the load is given by

$$P_L = (1/2)R_L |I_2|^2.$$

Using (B1), we can calculate the power efficiency as

$$\eta = \frac{P_L}{P_{net}} = \frac{P_L}{P_L + P_{loss}} = \frac{R_L |I_2|^2}{R_1 |I_1|^2 + R_2 |I_2|^2 + R_L |I_2|^2} = \frac{R_L}{(R_L + R_2) + R_1 \frac{(R_L + R_2)^2 + (\omega L_2 + X_L)^2}{(\omega M)^2}}. \tag{C1}$$

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