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Operations and Coordination of Dual-Functional DVR and Recloser in a Power Distribution System

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ABSTRACT Dynamic voltage restorers (DVRs) are devices that compensate for voltage sags/swells in power distribution systems effectively. However, the performance of DVRs may be easily endangered by large load-circuit currents. This work proposes a dual-functional DVR (DFDVR) that solves multiple problems by controlling the trigger angle of antiparallel thyristors, which are connected between the power converter and output filter. The DFDVR not only compensates for voltage fluctuation in the upstream grid but also limits fault current in the downstream grid. Moreover, the combined application of the DFDVR with a recloser is introduced. The DFDVR flexibly regulates the amplitude of the faulty current to coordinate the recloser. In addition, the coordination sequence diagrams of the DFDVR and the recloser under instantaneous and permanent faults are analyzed in detail. Simulations and experimental results verify the correctness and feasibility of the operations and coordination of the DFDVR and the recloser.

INDEX TERMS Dynamic voltage restorer, fault current limiting, recloser, switching sequence.

NOTATION

The following symbols are used in this paper:

u_S	Grid voltage;
u_{dvr}	Compensation voltage;
u_{Load}	Load voltage;
u_{Lf}	Filter voltage;
u_{dc}	DC-link voltage;
u_{sag}	Depth of voltage sag;
u_{VSI}	Output voltage of the inverter;
Δu	Fluctuation voltage;
u_{T2}	Secondary voltage of the series transformer;
u_{Smax}	Maximum withstand voltage of the series transformer;
u_{Cmax}	Maximum withstand voltage of the filter capacitor;
i_{fault}	Limiting fault current;
i_{Lim_min}	Minimum value of the limiting fault current;
i_{Lim_max}	Maximum value of the limiting fault current;
i_L	Rated current;
i_{T2}	Secondary current;
i_{th}	Threshold current value;
i_{Lf}	Current through the filter inductor;
i_{Cf}	Current through the filter capacitor;
Z_S	System impedance;
Z_{lim}	Current-limiting impedance;
Z_{Leq}	Equivalent impedance of the thyristor circuit;
R_{VSI}	Equivalent impedance of the inverter;
L_f	Filter inductance;
C_f	Filter capacitance;
C_{dc}	DC-link capacitance;
Q_{Lfmax}	Thermal limit of the filter inductor;
R_{Lf}	Resistance of the filter inductance;
φ_{Load}	Power factor of the load;
α	Firing angle of the thyristor;
σ	Conduction angle of the thyristor;
ω	Angular frequency;

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f_c Resonance frequency of the filter;
ρ Damping factor;
k Turns ratio of the series transformer;
γ Modulation depth.

I. INTRODUCTION

The grid voltage quality and service continuity of power supply encounter challenges given the high penetration of renewable energies [1], [2]. Among these challenges, voltage sags and swells are dominant disturbances that threaten the safety of sensitive loads [3]. The use of dynamic voltage restorers (DVRs) to improve voltage fluctuations has been widely investigated in recent years. A traditional DVR usually consists of a series transformer, a converter, a filter, a DC side capacitor, and an energy storage device [4], [5].

However, when short-circuit faults occur in the downstream grid, an unexpected high faulty current may easily damage the power converter of the DVR and threaten the safety of the grid. The DVR can protect itself through the short-circuit of the secondary side of the series transformer [6] (Fig.1 [a]). Nevertheless, this method cannot limit the fault current in the power distribution system. Thus, the high fault current may damage other power equipment (e.g., transformers and breakers).

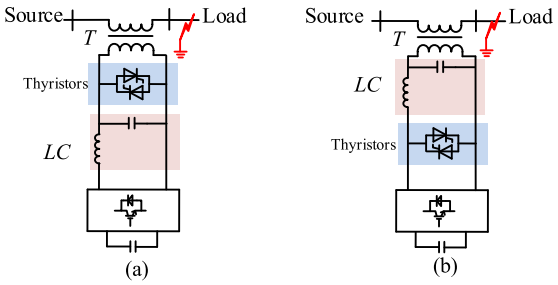

FIGURE 1. Antiparallel thyristor branches in different topologies: (a) traditional DVR system and (b) DFDVR system.

Numerous works have proposed the improvement of power grid safety by installing fault current limiters (FCLs) [7], [10]. Ideal FCLs must have the essential characteristics of low impedance during normal operation and high impedance during faults [11]. Solid-state and superconducting FCLs with these characteristics have been studied to achieve the desired performance [12]. By using the FCLs, the faulty current can be limited to a safe level before the first peak of the natural faulty current is reached. However, the probability of faults is less under this condition than under normal operations, and the use of FCLs is less efficient than that of other grid equipment. For example, short-circuit faults with considerable influence on the state grid in China occur less than 70 times annually [13]. Although FCLs are rarely used, they remain necessary for power grids in extreme cases.

In contrast to FCLs, DVRs almost continuously compensate for grid voltage. Thus, if the capability of DVRs to limit the fault current is similar to that of FCLs, then the use of DVRs in lieu of FCLs will be cost-efficient. A series compensator that limits fault currents while absorbing large energy from external energy storage during faults has been presented in [14]. The DVR can be controlled as a virtual impedance to limit the fault current [15], whereas the value of virtual *RL* or *L* impedance is difficult to set. The design and testing of UPFC–FCL can provide a reference for the design of dual-functional DVRs (DFDVR) [16]. A DFDVR with improved topology (as shown in Fig. 1[b]) was proposed in [17]. This DFDVR has two modes, namely, DVR and FCL modes.

In Fig.1, the major difference between conventional DVRs and DFDVRs is the installation location of antiparallel thyristors. In a conventional DVR, thyristors are installed between the transformer and the *LC* filter. By contrast, in a DFDVR, thyristors are installed between the terminal of the converter and the *LC* filter. Thus, the inductor in the *LC* filter is used as a filter inductor in the DVR mode and as a current-limiting inductor in the FCL mode.

Different topologies and optimal control strategies for DFDVRs [17]–[19] have been researched in the past few years; nevertheless, the operations and coordination of DFDVRs and reclosers, which have been widely used in power distribution system [20], [21], have been ignored. Therefore, the present work studies the coordination of DFDVRs and reclosers, and analyzes their coordination sequence during different faults to improve the understanding of the operation of DFDVRs in the power distribution system.

The remainder of this paper is organized as follows: The topology of the DFDVR and its operation principle (voltage compensation and faulty current limitation) are presented in Section II. The selection of parameters for the components of the DFDVR is proposed in Section III. The coordination sequence diagram between the DFDVR and the recloser during different fault types (instantaneous and permanent faults) is illustrated in Section IV. The simulations and experimental results for verifying the proposed scheme are introduced in Sections V and VI, respectively. Finally, the conclusion is presented in Section VII.

II. TOPOLOGY AND OPERATION OF THE DFDVR

In Fig. 2, the DFDVR used in this work includes a series transformer (*T*), an *LC* filter, a set of antiparallel thyristors (*S*), a cascaded multilevel voltage source inverter (VSI), and a

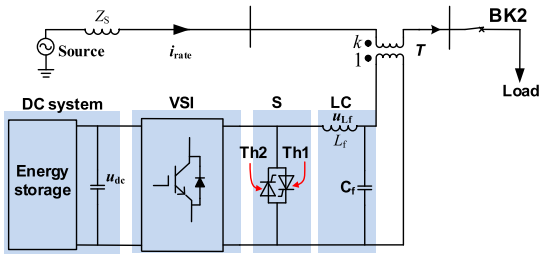

FIGURE 2. Topology of the DFDVR system.

DC-link system. The DFDVR system is installed between the source and the mechanical switch (BK2), which is equipped with the recloser. In contrast to the traditional DVRs reported in [5], [15], the new system adds the thyristors (S) between the VSI and the LC. The LC consists of L_f and C_f, and the turn ratio of the series transformer is k.

The working mode of the DFDVR system can be classified in accordance with functionality as voltage compensation (DVR mode) during normal operations and faulty current limit (FCL mode) during grid faults. Considering that the switching scheme between different modes has been analyzed in a previous study [17], the operation mechanism of the DFDVR is simply introduced in this paper for brevity.

A. VOLTAGE COMPENSATION MODE

The thyristors are turned off during normal operation, and the equivalent single-phase circuit is depicted in Fig. 3. The energy storage system provides the required power to compensate for voltage fluctuation (Δu) [22]. In the present work [18], the full-voltage compensation scheme, which injects suitable magnitude and phase, is adopted. The compensation voltage is expressed as

$$u_{\mathrm{dvr}} = -\Delta u = k(u_{\mathrm{VSI}} - u_{Lf}). \tag{1}$$

where u_{VSI} and u_{Lf} are the output voltage of the inverter and the filter voltage, respectively. Given that the DFDVR is composed of three single-phase inverters, each phase can be controlled independently, and unbalanced voltage is compensated easily. Moreover, the DFDVR not only compensates for voltage fluctuations or imbalances at the point of common coupling but also improves recovery after faults [23]. Thus, the DC-link voltage must be unaffected during the DVR or FCL mode given flexible function switching.

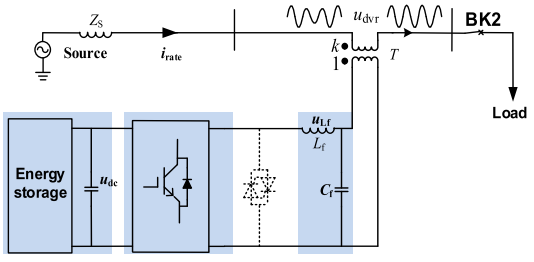

FIGURE 3. DFDVR in the DVR mode.

B. FCL MODE

The Insulated Gate Bipolar Transistors (IGBTs) of the VSI are all blocked when a short-circuit fault occurs at the load side. The antiparallel thyristors (S) are turned on, and then the operation mode of the DFDVR switches from the DVR mode to the FCL mode. The equivalent circuit of the DFDVR in the FCL mode is demonstrated in Fig. 4. Therefore, the DFDVR can be considered the FCL with thyristor-controlled impedances.

The thyristors and the LC filter are connected to the electric grid through the series transformer T as a series with high

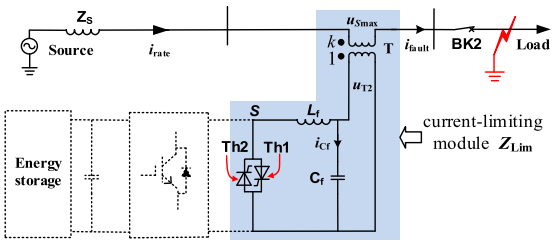

FIGURE 4. DFDVR in the FCL mode.

impedance to limit the faulty current. The leakage reactance and the resistance of the series transformer are negligible relative to high series impedance [19]. The current-limiting impedance in the FCL mode can be expressed as

$$|Z_{\mathrm{Lim}}| = k^2 \{|j\omega L_f| \,//\, |1/j\omega C_f|\} \approx k^2 |j\omega L_f|. \tag{2}$$

Thus, the limiting fault current i_{fault} can be defined as

$$i_{\mathrm{fault}} = \frac{u_S}{|Z_S + Z_{\mathrm{Lim}}|}, \tag{3}$$

where Z_S is the system impedance, and u_S is the supply voltage. For a nearby fault, $Z_{\mathrm{Lim}} >> Z_S$, and i_{fault} is mainly determined by Z_{Lim}. In Equation (2), considering the square of the turn ratio (k^2), Z_{lim} is a large value; thus, i_{fault} can be limited to an acceptable range. In the present work, the value of the fault current is limited to be 5–7 times that of the rated current; these values satisfy the requirement of relay protection in the power distribution system [18].

III. SWITCHING BEHAVIOR OF THE CURRENT-LIMITING MODULE

A. SWITCHING BEHAVIOR OF ANTIPARALLEL THYRISTORS

In Fig. 5, the antiparallel thyristors (S) act as a bidirectional switch (Thy-1 and Thy-2). u_{T2} is the secondary voltage of the transformer, and i_{Cf} is ignored. On the one hand, only Thy-1 functions when u_{T2} is in positive half-cycles. The firing angle of Thy-1 is α. i_{T2} reaches the maximum value when α is π. The turn-off phase angle of Thy-1 is $2\pi - \alpha$ based on symmetry theory. On the other hand, only Thy-2 functions when u_{T2} is in negative half-cycles. The firing angle of Thy-2 is $\pi + \alpha$. The turn-off phase angle of Thy-2 is $3\pi - \alpha$. The voltage and current waveforms of the antiparallel thyristors are exhibited in Fig. 5.

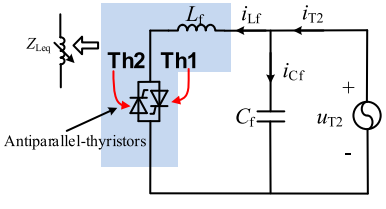

FIGURE 5. Equivalent circuit of the current-limiting module in the adjustment mode.

a) In Fig. 5(a), when $(2\pi - \alpha) < (\pi + \alpha), \alpha \in (\pi/2, \pi)$, i_{T2} is intermittent during one period. Thus, the conduction angle

$\beta = \pi - \alpha$. When $\alpha = \pi$, $\beta = 0$. The antiparallel thyristors are cut off at this time.

b) In Fig. 5(b), $(2\pi - \alpha) = (\pi + \alpha)$. At this time, $\alpha = \pi/2$. Thy-2 turns on when Thy-1 is off. i_{T2} is continuous during one period. Thus, the filter inductor is constantly in series with the line-through transformer.

c) In Fig. 5(c), $(2\pi - \alpha) > (\pi + \alpha)$, Thus, $\alpha \in (0, \pi/2)$. Although i_{T2} is continuous, it contains numerous DC components. The bias current is dangerous to the transformer and therefore must be avoided.

B. TRIGGER ANGLE CONTROL OF ANTIPARALLEL THYRISTORS

The current-limiting impedance is mainly determined by L_f and k, as presented in Equation (2). However, when L_f and k are very small, the current-limiting effect may not satisfy the requirement of relay protection. Thus, an effective approach based on controlling the trigger angle of the antiparallel thyristors to obtain variable impedance rather than fixed impedance is proposed. In Fig. 5, the general expression of the firing angle is

$$\omega t = \alpha + n\pi, \tag{4}$$

where $n = 0, 1, 2,....$ If R_{Lf} and i_{Cf} are ignored, i_{T2} through the filter inductor satisfies

$$L_f \frac{di_{T2}}{dt} = u_T \sin \omega t. \tag{5}$$

In Equation (5), i_{T2} is given as

$$i_{T2} = \frac{u_T}{\omega L_f}[\cos(\alpha + n\pi) - \cos(\omega t)]. \tag{6}$$

Through Fourier integral transform, i_{T2} can be rewritten as

$$i_{T2} = A_0 + \sum_{ki=1}^{\infty} [A_{ki} \cos(\alpha + n\pi) - B_{ki} \cos(\omega t)], \tag{7}$$

where $A_0 = \frac{1}{2\pi}\int_{T_0}^{T_0+2\pi} i_{T2} d\omega t$, $A_k = \frac{1}{\pi}\int_{T_0}^{T_0+2\pi} i_{T2} \cos(k\omega t) d\omega t$, and $B_k = \frac{1}{\pi}\int_{T_0}^{T_0+2\pi} i_{T2} \sin(k\omega t) d\omega t$. T_0 is the starting time.

In Equation (7), the Fourier decomposition of the fundamental current is expressed as

$$\begin{cases} A_1 = \frac{1}{\pi}\int_{\alpha}^{2\pi-\alpha} \frac{u_{T2}}{\omega L_f}(\cos\alpha - \cos\theta)\cos\theta d\theta \\ +\frac{1}{\pi}\int_{\pi+\alpha}^{3\pi-\alpha} \frac{u_{T2}}{\omega L_f}(\cos(\alpha+\pi) - \cos\theta)\cos\theta d\theta \\ B_1 = \frac{1}{\pi}\int_{\alpha}^{2\pi-\alpha} \frac{u_{T2}}{\omega L_f}(\cos\alpha - \cos\theta)\sin\theta d\theta \\ +\frac{1}{\pi}\int_{\pi+\alpha}^{3\pi-\alpha} \frac{u_{T2}}{\omega L_f}(\cos(\alpha+\pi) - \cos\theta)\sin\theta d\theta. \end{cases} \tag{8}$$

The following equation is obtained:

$$\begin{cases} A_1 = u_{T2} \cdot [2(\alpha - \pi) - \sin 2\alpha] / \pi\omega L_f \\ B_1 = 0. \end{cases} \tag{9}$$

In Equations (7) and (9), the instantaneous value of fundamental current can be expressed as

$$i_{T2} = A_1 \cos\omega t = \frac{u_{T2}}{\pi\omega L_f}[2(\pi - \alpha) + \sin 2\alpha]. \tag{10}$$

The equivalent impedance of the filter inductor is calculated as [24], [25]

$$Z_{Leq}(\alpha) = \frac{\pi\omega L_f}{2(\pi - \alpha) + \sin 2\alpha}. \tag{11}$$

Given that the filter capacitor is only several μF, its impedance Z_{cf} is ignored. In Equations (2) and (11), the current-limiting impedance can be expressed as

$$Z_{Lim}(\alpha) \approx k^2 Z_{Leq}(\alpha) = \frac{k^2\pi\omega L_f}{2(\pi - \alpha) + \sin 2\alpha}. \tag{12}$$

Selecting L_f on the basis of Equation (12) is easy. Highly complicated relationships exist among Z_{Lim}, k, and α, as expressed in Equation (12). When α is equal to $\pi/2$, $Z_{Lim} = k^2\omega L_f$, thereby indicating that the thyristor branch is in short circuit. When α is equal to π, Z_{Lim} tends to be infinite, thereby implying that the thyristors are disconnected. Thus, the value of α can be easily set to adjust the current-limiting impedance. The relationship among the current-limiting impedance (Z_{Lim}), transformer ratio ($1 \le k \le 10$), and trigger angle ($90° \le \alpha \le 115°$) is displayed in Fig. 7 to explain the change rule followed by Z_{Lim}. In Fig. 7, Z_{Lim} increases gradually with k and α.

C. DFDVR–RECLOSER COORDINATION ANALYSIS

To satisfy the current requirement of the recloser, the limited current must be larger than i_{th}, which is set to mi_{rate}. In Fig. 8, Curve-4 shows the current threshold curve of the over-current protection. In Equations (2) and (3), during the FCL mode, the minimum value of the limited current is given as

$$u_S/Z_{Lim}(\alpha) > i_{Lim\_min} = mi_{rate}. \tag{13}$$

The following equation is reduced on the basis of Equations (12) and (13):

$$\sin 2\alpha - 2\alpha = \frac{mi_{rate}k^2\pi\omega L_f}{u_s} - 2\pi. \tag{14}$$

In addition, the limited current must be smaller than the current setting value (i_{Lim_max}). This condition satisfies the basic safety requirements of equipment, such as *LC* filters, series transformers, and thyristors, in power distribution systems. On the basis of Equations (3) and (12), the maximum value of the limited current is expressed as

$$u_S/Z_{Lim}(\alpha) < i_{Lim\_max}. \tag{15}$$

In Fig. 8, Curve-5 shows the curve of the carrying maximum current of the limited current module. Based on Equations (13) and (15), the limited current must satisfy the following condition:

$$i_{Lim\_min} < i_{Lim}(\alpha) < i_{Lim\_max}. \tag{16}$$

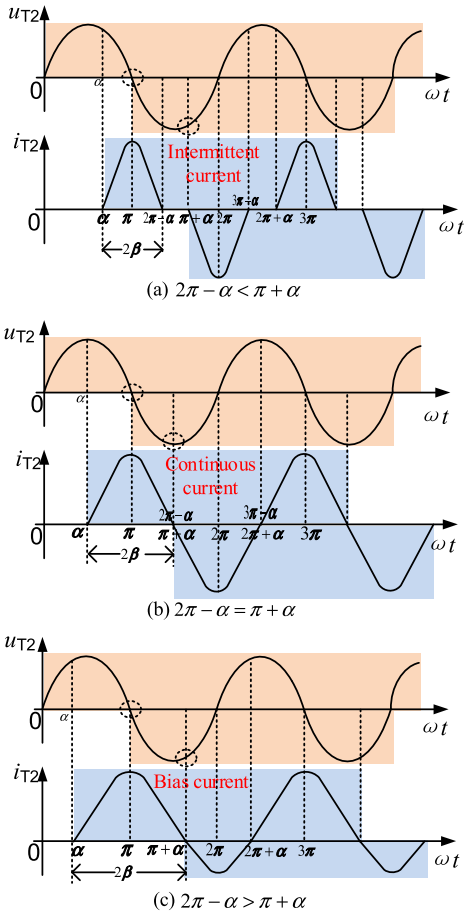

FIGURE 6. Voltage and current waveforms of the current-limiting module. (a) $(2\pi-\alpha)<(\pi+\alpha)$; (b) $(2\pi-\alpha)=(\pi+\alpha)$; (c) $(2\pi-\alpha)>(\pi+\alpha)$.

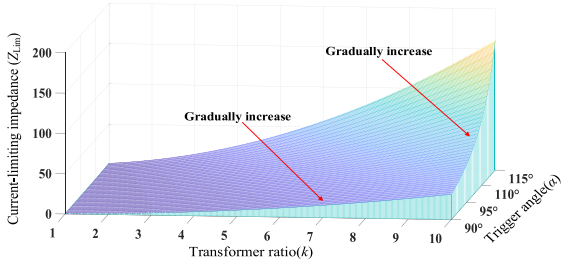

FIGURE 7. Relationship among the current-limiting impedance Z_{Lim}, transformer ratio k, and trigger angle α.

Therefore, in Fig. 8, Point a is the intersection with Curve-1 and Curve-4; Point b is the intersection with Curve-1 and Curve-5; Point c is the intersection with Curve-2 and Curve-5; and Point d is the intersection with Curve-2 and Curve-4.

The abovementioned analysis shows that Zone X_1 is the safety operation zone of the VSI, and the control system must block the driving signals of IGBTs to protect the VSI quickly before $2i_{rate}$. Moreover, Zone X_2 is the safety zone of the current-limiting module when the DFDVR is working in the FCL mode. α is controlled to satisfy the DFDVR–recloser coordination.

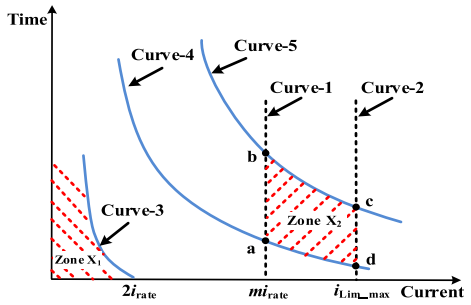

FIGURE 8. TCC curve for DFDVR–recloser coordination.

IV. DESIGN OF DFDVR PARAMETERS

Considering that the DFDVRs can operate in the DVR and FCL modes, the selection of DFDVR parameters is different from that of DVR and FCL parameters. In Fig. 9, the selection of energy storage, VSI, *LC*, and series transformer parameters must be considered when the DFDVR operates in the DVR mode. Moreover, considering that the fault current will flow through the series transformer, *LC* filter, and antiparallel thyristors when the DFDVR works in the FCL mode, the parameter selection of the *LC* filter and the series transformer must be analyzed in detail. Furthermore, the thermal limit of the components must be considered to meet operation requirements during the fault condition.

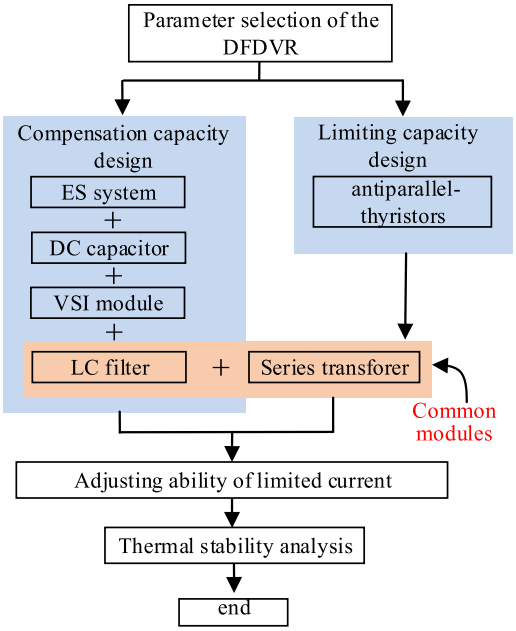

FIGURE 9. Method for selecting the parameters of the DFDVR system.

A. DESIGN OF THE CONVERTER OPERATION

The DFDVR can operate in one of the two operation modes in accordance with the grid state.

1) The control methods of cascade inverter-based DVRs when the DFDVR is in the voltage compensation mode have been extensively researched [26], [27]. Thus, during the DVR

mode, the DFDVR must inject an active power expressed as

$$P_{\mathrm{DVR}} = -C_{\mathrm{dc}} u_{\mathrm{dc}} du_{\mathrm{dc}}/dt = \sqrt{3} u_{\mathrm{Load}} i_{\mathrm{L}} \cos\varphi_{\mathrm{Load}} \Delta u, \quad (17)$$

where $P_L = \sqrt{3}\, u_{\mathrm{Load}} i_{\mathrm{L}} \cos\varphi_{\mathrm{Load}}$ is the rated load power during normal operation.

2) When the DFDVR is in the fault current-limiting mode, the secondary current is $k\lambda$ times greater than the load current.

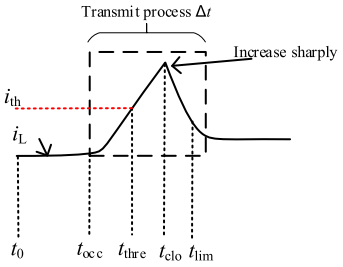

FIGURE 10. Fault current-limiting scheme sequence of the DFDVR.

In Fig. 10, during normal conditions, the line current i_{L} is in its normal range. At t_{occ}, a short-circuit fault causes the line current to increase rapidly. At t_{thre}, a fault current is detected when the line current's amplitude exceeds a preset threshold i_{th}. Thus, all IGBTs are turned off to deactivate the inverter. Considering a time delay (2–3 sampling periods), the IGBTs are completely turned off at t_{clo}. Thus, the fast detection algorithm of the fault current is crucial for the DFDVR [17], [19].

Then, the control system of the DFDVR transmits a trigger signal to antiparallel thyristors. The turn-on times of 10 μs have been obtained for thyristors, which are sufficiently fast to limit the fault current [28]. Finally, the DFDVR enters the FCL mode at t_{lim}.

Based on the abovementioned analysis, the period to complete switching to FCL reads is $\Delta t = t_{\mathrm{lim}} - t_{\mathrm{occ}}$. Therefore, the switching must be as brief as possible to limit the fault current.

B. LC ELECTRICAL PARAMETERS

1) IN DVR MODE

The resonance frequency of the LC filter is set as f_{c}, which is derived in Equation (18).

$$2\pi f_{\mathrm{c}} L_{\mathrm{f}} = 1/(2\pi f_{\mathrm{c}} C_{\mathrm{f}}) \quad (18)$$

The following equation can be obtained on the basis of Equation (18):

$$f_{\mathrm{c}} = \sqrt{L_{\mathrm{f}}/C_{\mathrm{f}}}/2\pi L_{\mathrm{f}}. \quad (19)$$

The damping factor is assumed to be $\rho = \sqrt{L_{\mathrm{f}}/C_{\mathrm{f}}} = (0.5 \sim 0.8)R_{\mathrm{L}}$ [17], [18], and R_{L} is the equivalent impedance of the VSI. Thus, L_{f} and C_{f} can be calculated as

$$\begin{cases} L_{\mathrm{f}} = \rho/2\pi f_{\mathrm{c}} \\ C_{\mathrm{f}} = 1/2\pi f \rho. \end{cases} \quad (20)$$

2) IN FCL MODE

During the FCL mode, the distortion of line currents due to the LC in the circuit does not exist because the resonant frequency of the filter is higher than the fundamental frequency. Given that limited current will flow through the filter, the thermal stress of L_{f} and the maximal withstand voltage of C_{f} must be considered. The thermal limit of the filter inductor is expressed as

$$Q_{\mathrm{Lf}} = \int_{t_{\mathrm{occ}}}^{t_{\mathrm{dis}}} (k i_{\mathrm{fault}})^2 t, \quad (21)$$

where t_{dis} is the instance of fault disappearance. The maximal withstand voltage U_{Cf} is expressed as

$$U_{\mathrm{Cf}} = \max(u_{\mathrm{Smax}}/k, u_{\mathrm{dc}}), \quad (22)$$

where u_{dc} and u_{Smax} are the maximum voltage of the DC-link and the series transformer, respectively. Thus, Equations (18)–(22) must be considered in the design of the DFDVR filter. Moreover, a dry-type air-core reactor, which has constant magnetic conductivity and good heat radiation, must be adopted to avoid magnetic saturation during filter inductance [29].

C. SERIES TRANSFORMER DESIGN

The series transformer is adopted to reduce voltage stress on the power converter and provide electric isolation between the DFDVR and the utility grid. The parameter selection method of the ratio k in the series transformer reported in [17] aims to achieve a balance between voltages and currents in the secondary side. A novel design method of the series transformer to protect the transformer against saturation was proposed in [30]. Moreover, the static and dynamic steadiness limit of the transformer [17] must be considered during normal and fault operations.

V. COORDINATION SEQUENCE DIAGRAMS

The coordination sequence diagram of the DFDVR and the recloser under instantaneous and permanent faults will be studied in detail in this section to understand the operation of the DFDVR. Converter operation has two switching processes, namely, the forward switching scheme and the backward switching scheme. The details of the two converter switching processes have been described in detail in [17] and are not discussed in this paper for brevity.

A. UNDER INSTANTANEOUS SHORT-CIRCUIT FAULTS

The coordinated operation of the DFDVR and the recloser during instantaneous fault is depicted in Fig. 11. At t_1, the line is subjected to an instantaneous three short-circuit faults. The faulty current is detected at t_2 when the current magnitude exceeds the threshold value i_{th} [18]; then, the DFDVR system blocks the driving singles of the IGBTs in the VSI. The fault current decreases slightly given the series transformer's excitation impedance. The thyristor branch (S) is triggered at t_3, and the DFDVR finally switches to the FCL mode finally at t_4. The action of the recloser lags behind that of

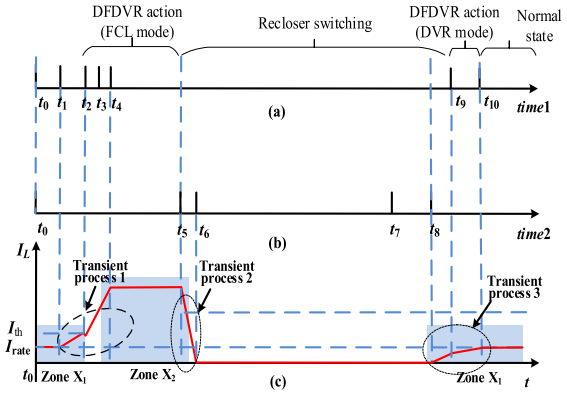

FIGURE 11. Coordinated operation of the DFDVR and recloser under instantaneous fault: (a) Switching sequence of the DFDVR, (b) Switching sequence of the recloser, (c) Profile of the fault current.

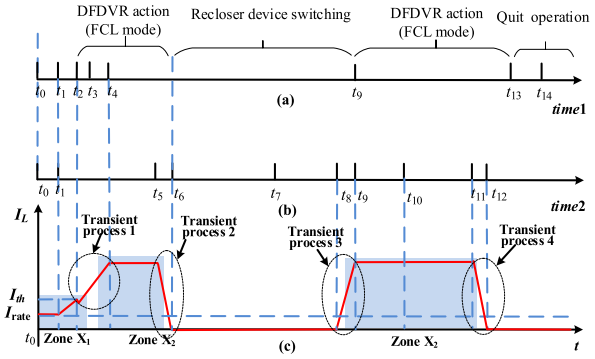

FIGURE 12. Coordinated operation of the DFDVR and recloser under permanent faults: (a) Switching sequence of the DFDVR, (b) Switching sequence of the recloser, (c) Profile of the fault current.

the DFDVR considering the high-switching frequency of the power semiconductors. Thus, the mechanical switch is turned off at t_5. Considering the transient switching of the switch (BK2), the fault is isolated completely at t_6. The reclosing signal of the switch (BK2) is triggered at t_7, and the mechanical switch closes completely at t_8. The instantaneous short-circuit fault is easily cleared. The thyristor branch (S) is turned off at time t_9, and the driving singles of the IGBTs are generated. Then, the DFDVR enters the DVR mode to compensate for the voltage fluctuations of the recovery due to short-circuit fault impact. Finally, the system returns to the normal state at time t_{10}. The FCL and DVR modes from t_2 to t_{10} are all related to the reclose operation. Therefore, three transient processes occur during coordinated operation, as demonstrated in Fig. 11(c).

B. UNDER PERMANENT SHORT-CIRCUIT FAULTS

The coordinated operation of the DFDVR and the recloser during a permanent fault is exhibited in Fig. 12. If a permanent three short-circuit fault occurs at t_1, then the switching sequence from t_1 to t_7 is the same as that displayed in Fig. 11. However, the permanent fault is not removed after the reclosing of the mechanical switch (BK2). Thus, the fault current remains after the switch is turned on again at t_8. The fault current is limited to the appropriate value again at t_9 because of the DFDVR. The relay (the overcurrent protection) operates again at t_{10}. The signal of the switch (BK2) is triggered at t_{11} and is turned off completely at t_{12}. Subsequently, the thyristor branch (S) is turned off at time t_{13}. The DFDVR must be controlled to quit operation at time t_{14}. Only the FCL mode is related to the reclose operation from t_2 to t_{14}. Therefore, four transient processes occur during the coordinated operation of the DFDVR and the recloser, as presented in Fig. 12(c).

VI. SIMULATION RESULTS

The scenarios under an instantaneous fault and a permanent fault are simulated in PSCAD/EMTDC with the circuit model illustrated in Fig. 2 to confirm the effectiveness and correctness of the coordinated operation of the DFDVR and the recloser. The simulation parameters of the DFDVR and the power system are listed in Table 1.

TABLE 1. Electrical parameters for simulation tests.

Parameters	Values
Source voltage (kV)	10
System impedance (Ω)	1.21
DC-link capacitor (μF)	15000
Filter inductor (mH)	1.5
Filter capacitor (μF)	27
Transformer ratio	4:1
Leakage reactance (p.u)	0.1
Magnetizing current (%)	0.4

A. SIMULATION RESULTS UNDER INSTANTANEOUS FAULT

The performance of the coordinated operation of the DFDVR and the recloser during a three-phase instantaneous fault is illustrated in Fig. 13. In Fig. 13(c), almost all of the voltage drops across the current-limiting module from t_5 to t_6 when a three-phase downstream fault occurs at t_1. Simultaneously, the load-side voltage is nearly zero during the fault, as depicted in Fig. 13(d). The fault currents are quickly limited to the desired value because of the DFDVR, as demonstrated in Fig. 13(b), and a current spike occurs during Transient process 1, as shown in Enlarged view I.

Considering the action time of the power system protection, the mechanical switches (BK2) are off at t_5, and oscillations occur during switching. Then, the fault short-circuit point enters the arc extinction period, as shown in Enlarged view II. The fault is cleared completely at t_6. At t_7, the control system triggers the recloser signal of the mechanical switch (BK2), and BK2 reworks. With the disappearance of the fault, the antiparallel thyristors quit operation, and IGBTs of the VSI are triggered again. The DFDVR enters the DVR mode to compensate for voltage fluctuations after the fault. Thus, the DC-link voltage must be maintained at a constant value to restore the DVR mode as soon as possible. Transient shock occurs during recovery given the switching delay, as presented in Fig. 13(c). Moreover, Fig. 13(e) illustrates that the DC-link voltage is unchanged during switching.

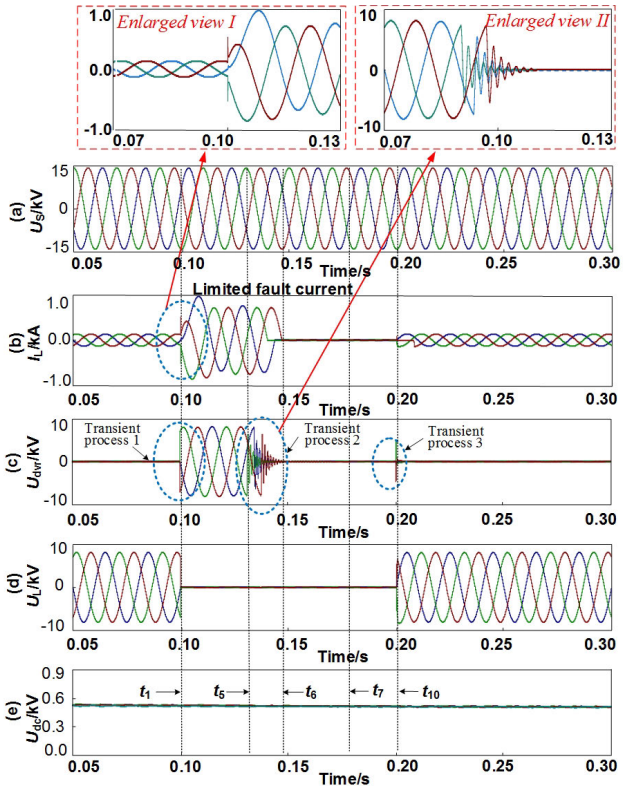

FIGURE 13. Simulation results under three-phase instantaneous fault: (a) system voltage U_S, (b) load current I_L, (c) primary voltage U_{dvr}, (d) load voltage U_L, and (e) DC-link voltage U_{dc}.

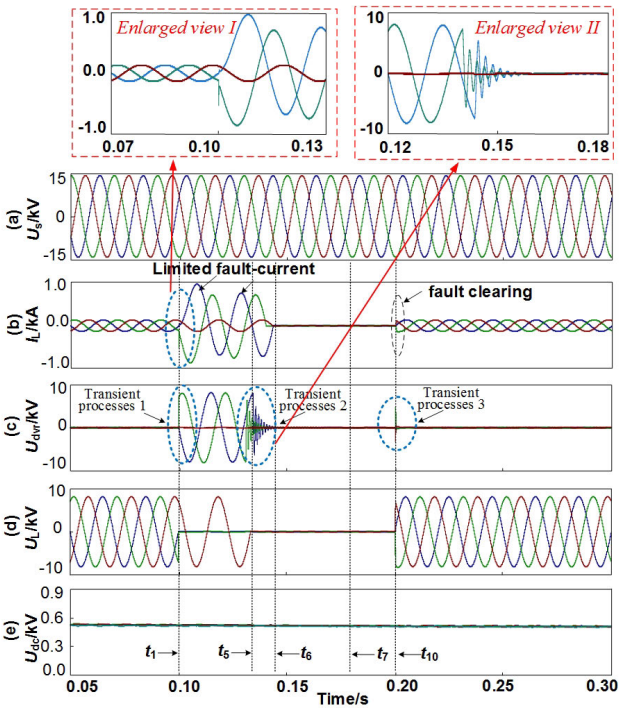

FIGURE 14. Simulation results under two-phase instantaneous fault: (a) system voltage U_S, (b) load current I_L, (c) primary voltage U_{dvr}, (d) load voltage U_L, and (e) DC-link voltage U_{dc}.

The performance of the coordinated operation of the DFDVR and the recloser during two-phase instantaneous fault is depicted in Fig. 14. Given that the DFDVR can control each phase independently, the currents of the faulty phases are limited to within a reasonable range, and the current of the healthy phase is unaffected. Considering that three-phase reclosure is constantly set in the distribution system, the three-phase switches (BK2) trip simultaneously (t_5), as demonstrated in Fig. 14(b). The DFDVR re-enters the DVR mode after the fault, and the power system returns to normal operation at t_{10}.

The simulation results exhibited in Figs. 13 and 14 verify that the DFDVR can limit the fault current quickly when the fault is detected. In practical applications, the DFDVR does not quit the FCL mode until reclosing successfully. Moreover, three transient processes (Transient processes 1, 2, and 3) occur during coordination and are acceptable for simulation results, as displayed in Figs. 13 and 14.

B. SIMULATION RESULTS DURING PERMANENT FAULT

The performance of the coordinated operation of the DFDVR and the recloser during a three-phase permanent fault is presented in Fig. 15. In the case of three-phase short-circuit faults, the load-side voltage is nearly zero (Fig. 15[d]), and nearly all of the voltage has dropped across the current-limiting module as illustrated in Fig. 15(c). The DFDVR enters the FCL mode quickly, and the load current will be quickly limited to the desired range as depicted in Fig. 15(b). The mechanical switches (BK2) are turned off at t_6, and two transient processes occur during switching, as shown in Enlarged views I and II. Therefore, the simulation results before t_6 are similar to those presented in Fig. 12.

The control system triggers the reclosing signal at t_7 and switches (BK2) rework at t_9. Given that the fault does not disappear, the DFDVR enters the FCL mode again, as demonstrated in Fig. 15(b). Considering that the limited current is higher than the protected value, the relay operates at t_{10}, as exhibited in Enlarged view III. Then, the switches are triggered to be turned off again at t_{11}. After the transient processes, the mechanical switches (BK2) are turned off completely at t_{12}, and the load current becomes zero, as shown in Enlarged view IV. The DFDVR must be controlled to quit operation at t_{14}. The DC-link voltage remains unchanged during switching as displayed in Fig. 15(e).

The performance of the DFDVR during the two-phase permanent fault at t_1 is presented in Fig. 16. The switching sequence is similar to that shown in Fig. 15. The only difference between Figs. 15 and 16 is that nonfault-phase currents are unchanged during the faults. Given that the three-phase recloser is always set in the power distribution network, three switches trip after the relay action, as illustrated in Fig.16 (c). After the switches are turned off again, the DFDVR quits operation. In Figs. 15 and 16, the DFDVR can effectively limit the fault current several times during the permanent fault. Moreover, the occurrence of four transient processes

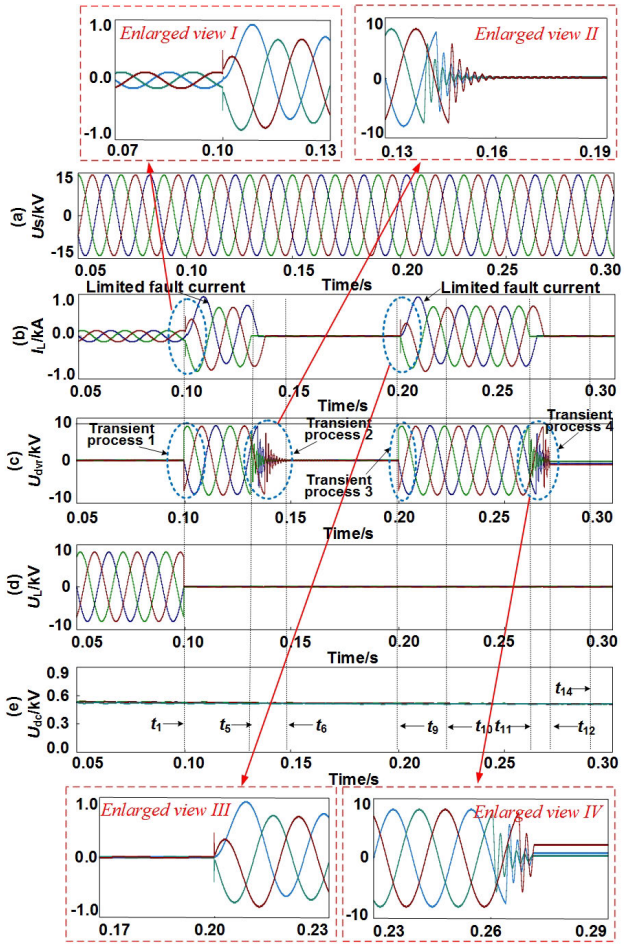

FIGURE 15. Simulation results under three-phase permanent fault: (a) system voltage U_S, (b) load current I_L, (c) primary voltage U_{dvr}, (d) load voltage U_L, and (e) DC-link voltage U_{dc}.

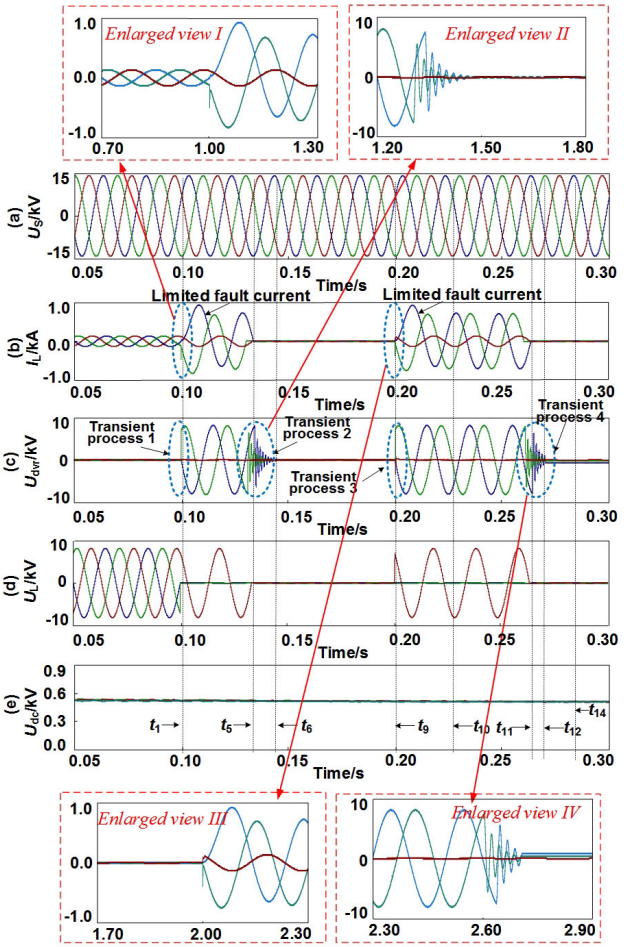

FIGURE 16. Simulation results under two-phase permanent fault: (a) system voltage U_S, (b) load current I_L, (c) primary voltage U_{dvr}, (d) load voltage U_L, and (e) DC-link voltage U_{dc}.

(Transient processes 1–4) during coordination is acceptable for simulation results.

C. SIMULATION RESULTS FOR SWITCHING BEHAVIOR

In Fig. 17, the performance of antiparallel thyristors triggers angle control during a two-phase permanent fault. In the case of two-phase short-circuit faults at 0.1 s, the load voltage of the fault phase is nearly zero, as shown in Fig. 17(c), and almost all of the voltage drops across the current-limiting module, as shown in Fig. 17(b). The DFDVR enters the FCL mode quickly during the fault phase, and the fault current will be quickly limited to the desired range as depicted in Fig. 17(b). However, the current of the nonfault phase is unchanged.

In Fig. 17 (a), the current limitation has two stages. In Stage 1, the firing angle of thyristors α is $\pi/2$, and the fault currents are continuous. The current-limiting impedance $Z_{\lim}(\pi/2)$ is easily calculated using Equation (12). Then, in Stage 2, the firing angle of thyristors α is $5\pi/9$. In Equation (12), the current-limiting impedance is $Z_{\lim}(5\pi/9) = 1.282\ Z_{\lim}(\pi/2)$, and the fault current is limited to a small

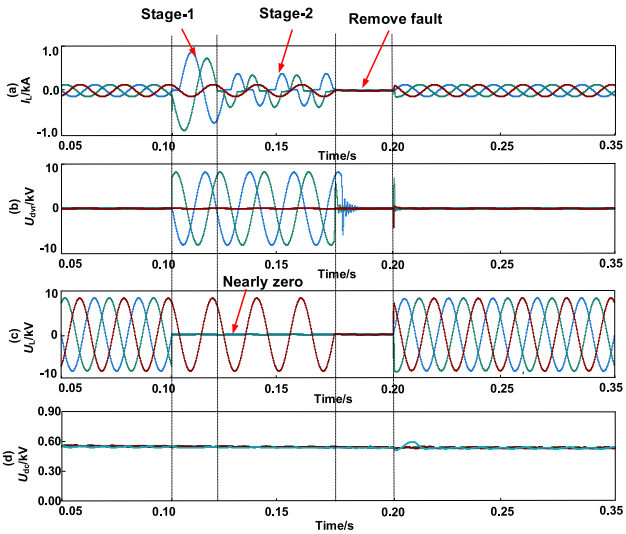

FIGURE 17. Simulation results for adjusting fault current: (a) load current I_L, (b) primary voltage U_{dvr}, (c) load voltage U_L, and (d) DC-link voltage U_{dc}.

value. Therefore, the mechanical switches are turned off easily, and the stress that they bear is smaller than that depicted in Fig. 14(b).

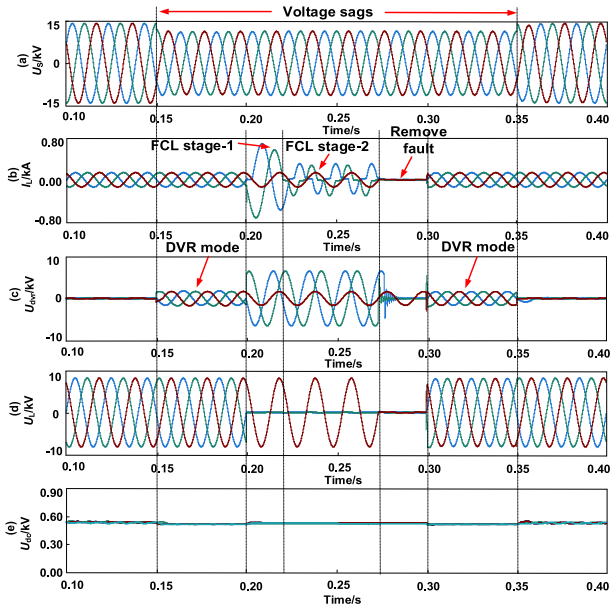

FIGURE 18. Simulation results for switching behavior: (a) system voltage U_S, (b) load current I_L, (c) primary voltage U_{dvr}, (d) load voltage U_L, and (e) DC-link voltage U_{dc}.

The performance of the switching behavior of the DFDVR between different modes is demonstrated in Fig. 18. In Fig. 18(a), a voltage sag at the source side occurs from 0.15 s to 0.35 s with a depth of 20%, and a two-phase downstream fault occurs from 0.2 s to 0.3 s. In Figs. 18(c) and 18(d), the DFDVR can provide the compensation voltage, and the load voltage is regulated to a constant amplitude from 0.15 s to 0.2 s and 0.3 s to 0.35 s.

At 0.2 s, the load voltages of the fault phases are nearly zero given the short-circuit faults. Almost all of the voltages will drop across the current-limiting modules as demonstrated in Fig. 18(c). The load current of the fault phase will be quickly limited to the desired value given the current-limiting function of the DFDVR. In Fig. 18(b), the current-limiting impedance can be adjusted during the faults. The mechanical switches (BK2) are turned off at 0.27 s. The DFDVR can enter the DVR mode again after 0.3 s to compensate for voltage sags. Fig. 18(e) shows that the DC-link voltage is unchanged during the whole process. Therefore, the DFDVR can switch flexibly among the DVR, FCL, and normal modes.

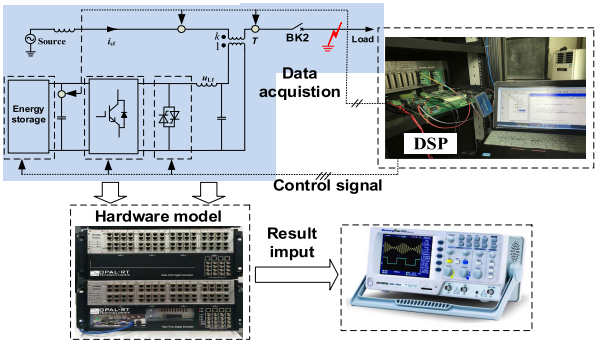

FIGURE 19. RT-Lab-based CHIL testing platform.

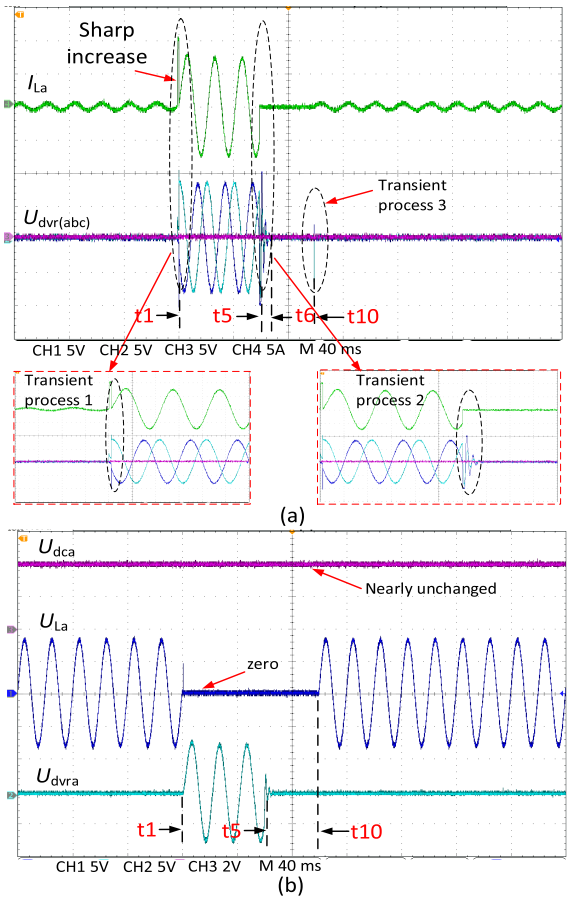

FIGURE 20. Experimental testing during two-phase instantaneous fault. (a) top to bottom: A-phase line current I_{La} and three-phase voltage at primary side $U_{dvr(abc)}$; (b) top to bottom: DC-link voltage U_{dca}, load voltage U_{La}, and primary voltage at phase-A U_{dvra}.

VII. EXPERIMENT RESULTS

Experimental implementation is introduced to verify the validity of the coordination sequence. The experimental parameters are the same as the simulation parameters listed in Table 1. The hardware in the loop (CHIL) setup is built on the basis of RT-LAB, as presented in Fig. 19. The DFDVR is modeled in the master controller, and the real-time digital simulator (RTDS) simulation of the model is conducted in the slave controller with a time step of 10 μs. With the distribution system model running in RTDS, the parameters are measured with 6.4 kHz sampling frequency and outputted to the I/O port of the external selected DSP controller TMS320F2812 through the interface card. PWM signals are produced and received using the RTDS simulation model via the input interface card. The scales of the AC voltage signal, AC current signal, and DC voltage signal are 1000:1, 100:1, and 400:1, correspondingly.

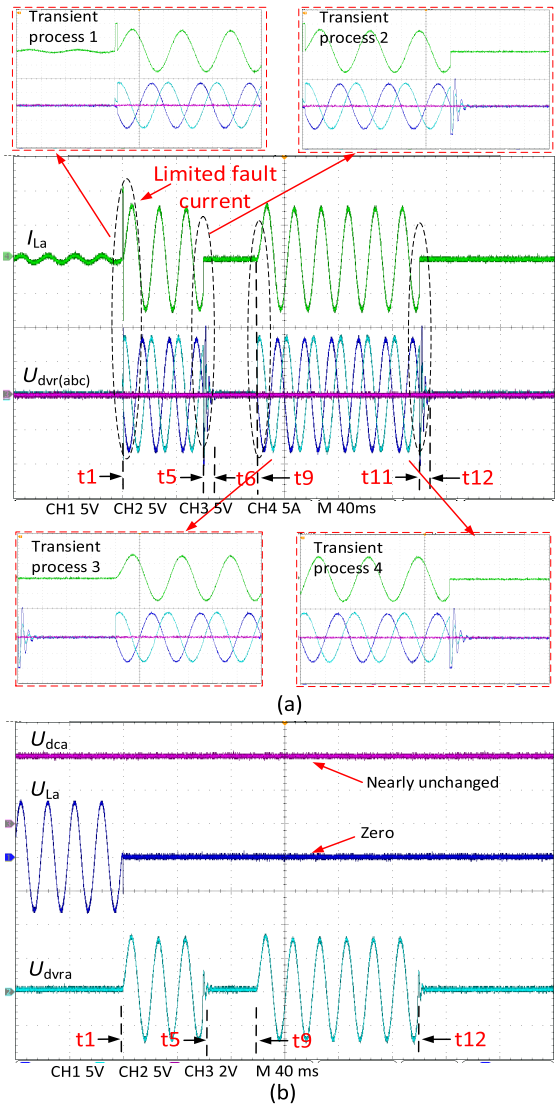

FIGURE 21. Experimental testing during a two-phase permanent fault, (a) top to bottom: A-phase line current I_{La} and three-phase voltage at primary side $U_{dvr(abc)}$; (b) top to bottom: DC-link voltage U_{dca}, load voltage U_{La}, and primary voltage at phase-A U_{dvra}.

A. EXPERIMENTAL RESULTS DURING INSTANTANEOUS FAULT

The performance of the DFDVR during two-phase instantaneous fault (A-phase and B-phase) is illustrated in Fig. 20. In Fig. 20(a), the system is initially in the steady state. When the system is subjected to two-phase downstream fault at t_1, nearly all of the voltage drops across the current-limiting module. The DFDVR switches from the DVR mode to the FCL mode, and the load current is quickly limited to the desired range. Given that the DFDVR controls each phase independently, the current of the healthy phase is unchanged, and the primary side voltage is nearly zero.

As analyzed previously, the mechanical switches (BK2) are turned off at t_5. Then, the fault short-circuit point enters the arc extinction period. The fault is cleared at t_6.

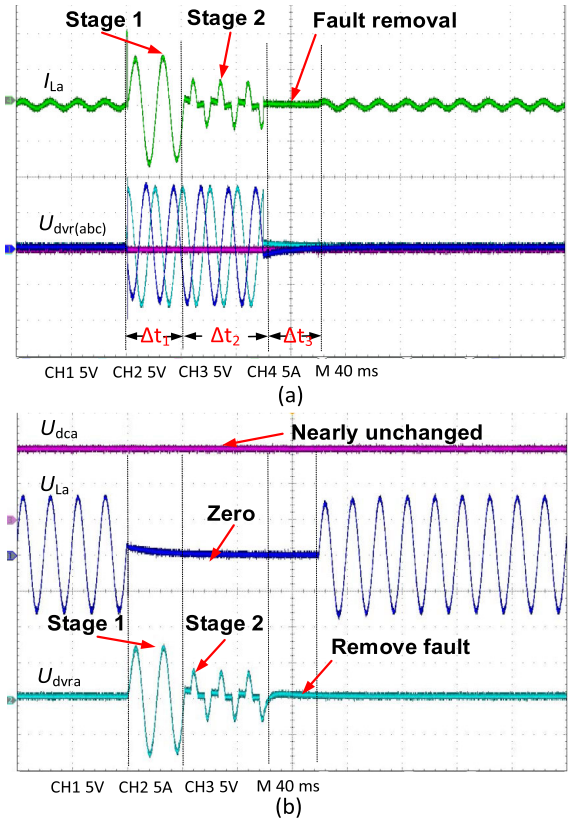

FIGURE 22. Experimental testing of fault current adjustment: (a) top to bottom: load current I_{La} and primary voltage $U_{dvr(abc)}$; (b) top to bottom: DC-link voltage U_{dca}, load voltage U_{La}, and load current I_{La}.

Oscillations occur during switching from t_5 to t_6. Moreover, the control system triggers the recloser signal, and the switches (BK2) rework. With the disappearance of the fault, the antiparallel thyristors quit operation, and the VSI is enabled at t_{10}. The DFDVR enters the DVR mode to compensate for voltage fluctuations after the fault. Transient shock occurs during the recovery procedure given the switching delay, as displayed in Fig. 20(a). Therefore, three transient processes occur during the coordination operation, as presented in Fig. 20(a). Moreover, Fig. 20(b) illustrates that the DC-link voltage is unchanged during switching. The primary side voltage (A-phase) is equal to the source voltage from t_1 to t_5, and the load voltage (A-phase) is nearly zero from t_1 to t_{10}.

B. EXPERIMENTAL RESULTS DURING PERMANENT FAULT

Fig. 21 depicts the performance of the DFDVR system during the two-phase permanent fault. In Fig. 21(a), initially, the system is in the steady-state regime. The system is subjected to two-phase permanent fault in the downstream grid at t_1. The switching sequence from t_1 to t_6 is the same as that in the instantaneous short-circuit fault. The DFDVR enters the FCL mode again at t_9 because the fault does not disappear. The switches are triggered to be turned off again at t_{11}. After

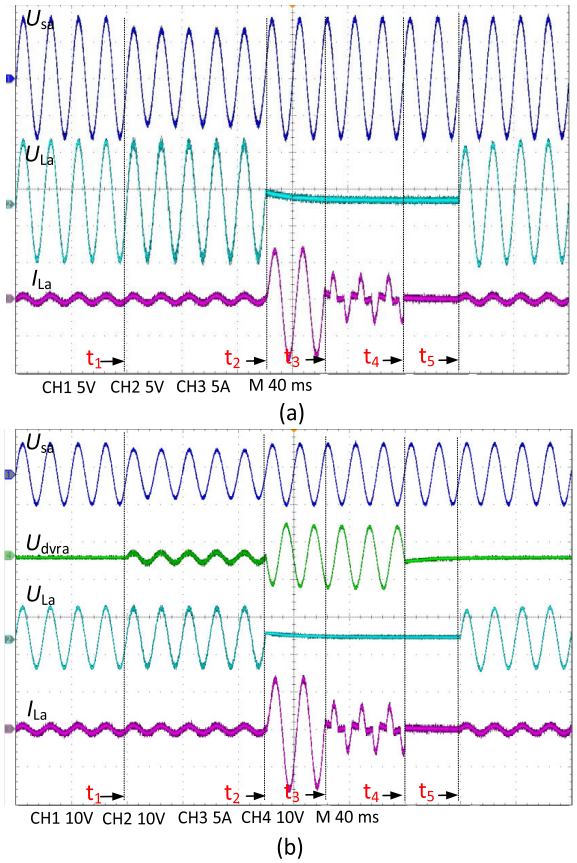

FIGURE 23. Experimental testing of switching behavior: (a) top to bottom: system voltage U_S, load voltage U_L, and load current I_L, (b) top to bottom: system voltage U_S, primary voltage U_{dvr}, load voltage U_L, and load current I_L.

the transient processes, the mechanical switches (BK2) are turned off again at t_{12}, and the load current becomes zero.

Therefore, four transient processes occur during coordinated operation, as demonstrated in Fig. 21(a). Then, the DFDVR must be controlled to quit operation. Fig. 21(b) exhibits that the load voltage is equal to zero after t_1, and the primary side voltage (A-phase) is equal to the source voltage from t_1 to t_5 and from t_9 to t_{12}. The DC-link voltage is unchanged during switching.

C. EXPERIMENTAL RESULTS FOR SWITCHING BEHAVIOR

In Fig. 22, the performance of the antiparallel thyristors triggers angle control during instantaneous fault. In case of two-phase short-circuit faults, nearly all of the voltages drop across the current-limiting module as exhibited in Fig. 22(a), and the load voltages of the fault phase are nearly zero. The DFDVR of the fault phase rapidly enters the FCL mode, and the fault current will be quickly limited to the desired range, as displayed in Fig. 22(a).

In Fig. 22 (a), during current limiting, the fault current is limited to a different value. The fault current is continuous during Δt_1 when α is $\pi/2$ and is limited to a small value during Δt_2 when α is $5\pi/9$. Therefore, the mechanical switches are turned off easily during Δt_3, and the stress they bear is smaller than that shown in Fig. 20(a).

The performance of the switching behavior of the DFDVR between different modes is shown in Fig. 23. In Fig. 23(a), a voltage sag occurs at the source side during t_1 to t_2 with a depth of 20%, and the instantaneous fault occurs at t_3. In Fig. 23(a), the DFDVR can provide the compensation voltage, and the load voltage is regulated to a constant amplitude from t_1 to t_2.

At t_2, the load voltages of the fault phases are nearly zero. Almost all of the voltages will drop across the current-limiting modules as demonstrated in Fig. 23(b). The load current of the fault phase will be quickly limited considering the current-limiting function of the DFDVR. Then, the angle control triggered by antiparallel thyristors is adjusted at t_3, and the fault current is limited to a small value. The mechanical switches are turned off at t_4. After t_5, the DFDVR can return to the normal mode. Therefore, the DFDVR can switch flexibly among the DVR, FCL, and normal modes.

VIII. CONCLUSION

This work presents a DFDVR that can perform voltage compensation and fault current limitation in accordance with the operation conditions of a power distribution system. The new system adds thyristors between the VSI and the *LC* rather than using a bypass thyristor at the secondary series transformer. Two operation sequence diagrams under different faults (instantaneous and permanent short-circuit faults) are considered to understand the operation of the DFDVR well and coordinate the multifunctional equipment and recloser. The DFDVR enters the FCL mode once during instantaneous fault and twice during permanent fault. Three and four transient processes occur during coordinated operation during instantaneous and permanent short-circuit faults, respectively. The simulation and experimental results verify the feasibility of the coordination strategy during different faults.

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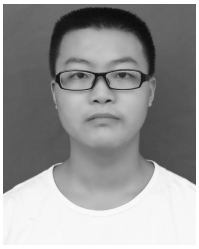

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