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Optimized FPGA Implementation of PWAM-Based Control of Three–Phase Nine–Level Quasi Impedance Source Inverter

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ABSTRACT Inherent buck–boost capability, reduced component count, controlled power injection and multilevel operation are some of the advantages which makes cascaded qZSI popular for integrating the generated solar energy with the utility grid. Phase–Shifted Carrier PWM (PSCPWM) and Pulse Width Amplitude Modulation (PWAM) are the most popular techniques for achieving multilevel qZSI operation. Generally, closed loop control implementation of three – phase qZSI system consists of large number of slave controllers (placed locally for voltage control) and one centralized master controller (for grid integration or load current control). Since the aim is to control single system with this highly distributed control structure, issues of clock pulse and interrupt signal synchronization, hardware and software redundancy are common in these implementations. This limits the utilization factor and step size of these control boards. To address these issues, either more optimized solutions must be suggested, or distribution of control structure must be reduced. In this paper, closed loop control of nine – level three – phase qZSI system is implemented using single FPGA control board thereby eliminating above said problems. Since, PWAM control algorithm is more complex than PSCPWM, FPGA based implementation for PWAM control is discussed. Critical implementation processes consisting of DAC – ADC interfacing, FPGA code per unitization, PI Controller realization and different clock pulse utilization are presented. For highlighting and comparing the resource consumption, PWAM and PSCPWM modulation are compared in terms of device utilization. Transient analysis and control algorithm are presented and validated during both starting and load transient conditions by means of simulation results. Finally, hardware results of these modulation methods are discussed and analyzed.

INDEX TERMS Cascaded multilevel inverter, phase shifted carrier PWM, pulse-width-amplitude modulation, quasi impedance source inverter, field programmable gate arrays.

I. INTRODUCTION

The most common configuration for feeding renewable power to the utility grid consists of two-stage conversion i.e., DC-DC converter connected to an inverter [1], [2]. DC-DC converter (generally boost converter) receives the variable energy generated from solar panels and converts it to a form with fixed dc voltage using MPPT algorithms [3]–[5]. This configuration utilizes five switches – boost switch and four H – Bridge switches. However, with advent of impedance source-based inverters, it is now possible to achieve grid integration with four switches thereby eliminating the extra dc – dc converter. It can perform both buck – boost operation and dc – ac inversion. Impedance based inverters are categorized into Z Source Inverter (ZSI) and quasi Z Source Inverter (qZSI). qZSIs have advantage of continuous input current which helps in minimizing the component size [6]–[10].

Cascaded multilevel qZSI is also discussed in literature. It offers all benefits of multilevel operation including achievement of higher voltage and power ratings, lower dV/dt and lower THD [11]. However, it requires large number of isolated power supplies. This requirement can be easily

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met when solar PV panels are connected at input of qZSI modules [12]–[16].For achieving multilevel operation, many modulation methods are used for conventional multilevel inverters [17]. For multilevel qZSI operation, PSCPWM and Space Vector PWM are the most commonly used modulation methods. PSCPWM is the most appropriate solution because of its simple implementation and improved performance [18]–[20]. However, in PSCPWM, the switching frequency of the H – Bridge switches is increased due to addition of shoot-through pulses. To counter this, soft-switching techniques and novel shoot – through methods are discussed [21]–[23]. However, this results in extra components in the hardware setup.

Pulse Width – Amplitude Modulation (PWAM) for three-phase electric motor drives applications is reported in the literature [24], [25]. Unlike PSCPWM, the amplitude of the carrier signal in PWAM method is varying and follows an envelope. This modification offers advantages of better voltage source utilization and lower switching losses when compared to other modulation methods. PWAM technique is also applied to qZSI topology to extract these benefits of multilevel operation [26], [27]. Implementation of PWAM to qZSI module is difficult as it requires incorporation of shoot-through pulses. Modification in PWAM technique is necessary to enhance its suitability for cascaded qZSI method [28], [29].

Implementation of control algorithm in power electronics is carried out using various platforms namely microcontrollers, FPGA and DSPACE etc. In recent times, FPGA technology has surfaced as one of the most popular platforms for implementation of real-time control algorithms for experimental setups. They can work up to 100MHz clock frequency and can accommodate more than 10 million equivalent gates in addition to other resources provided like DSPs [30], [31]. Higher on-board resources and large number of input – output (I/O) pins makes it easier to handle large algorithms. These advantages combined with significantly developed user-friendly programming software and verification tools have made it more popular for industrial implementations [32]–[34]. In electrical engineering, FPGA implementation of advance control algorithms [35]–[40], electric drives [41], [42], System Modeling and microgrids implementations [43]–[46] are also presented in the literature.

However, implementation of FPGA control based algorithm is restricted due to following limitations: (a) Issues of synchronism and resources redundancy due to use of multiple FPGA boards employed to control complex and distributed systems [47], [48], (b) Interfacing of peripheral devices like ADCs and DACs to FPGA [30], [31], (c) lack of available literature to deal with concept of per unitization, resources consumption and sensor calibration and (d) issues of selection of clock frequency and its associated timing constraints which results in a compromise between performance accuracy and memory consumption [30], [42], [46].

In this paper, optimized FPGA implementation of PWAM based control algorithm is discussed. To optimize both process and resources, control algorithm of three – phase nine – level system is achieved using single FPGA control board. Layout of the FPGA implemented control algorithm is presented with detailed elaboration of each block. Interfacing issues of external ADCs and DAC is also discussed. Optimization of available resources subjected to device utilization constraints and I/O ports is achieved which minimizes the footprint. Experimental setup is controlled with the generated control code.

This paper is organized as follows: Three-phase nine-level cascaded qZSI system connected to RL load is described in Section 2. Section 3 presents control algorithms based on two modulation techniques. Control of output dc bus voltage of quasi network is achieved by the implementation of two cascaded PI controllers. FPGA implementation of control algorithms subjected to constraints and resource utilization is discussed in Section 4. Hardware implementation of three-phase nine-level voltage are presented in Section 5. Section 6 concludes the paper.

II. SYSTEM DESCRIPTION

The system consists of three-phase multilevel qZSI connected to three-phase RL load as shown in Fig. 1(a). Each phase consists of four qZSI modules connected in cascade. Each qZSI module consists of input dc voltage source, quasi network and H-Bridge as shown in Fig. 1(b). The input dc voltage source is connected to the quasi network. The quasi network consists of two inductors, two capacitors and one diode. The output of quasi network is connected as input to the H-Bridge.

Number of levels in the phase output voltage are $2N + 1$ where N is the number of modules connected in cascade. As four modules are connected in cascade, the maximum number of voltage levels in output phase voltage is nine. These voltage levels are: $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ and $-4V_{dc}$ where V_{dc} is the output voltage of the quasi network.

For achieving the multilevel qZSI operation, different modulation methods are available in the literature [15]. Phase shifted carrier PWM (PSCPWM) is the most popular PWM technique as it offers even power distribution and lower THD. PWAM switching technique is also recommended due to its better voltage utilization and lower switching losses.

III. CONTROL ALGORITHM

The control algorithm must meet the following requirements:

(a) V_{dc} of each quasi network must be controlled

(b) Nine-level phase output voltage must be achieved and

(c) Obtained three-phase currents must be balanced.

Conclusively, to achieve this, three – phase nine – level qZSI system must be controlled both at module level and system level.

A. QUASI NETWORK VOLTAGE CONTROL

Single module of qZSI is shown in Fig. 1(b). To achieve closed loop control of quasi network output voltage (V_{dc}), two PI controllers connected in cascaded are used as shown

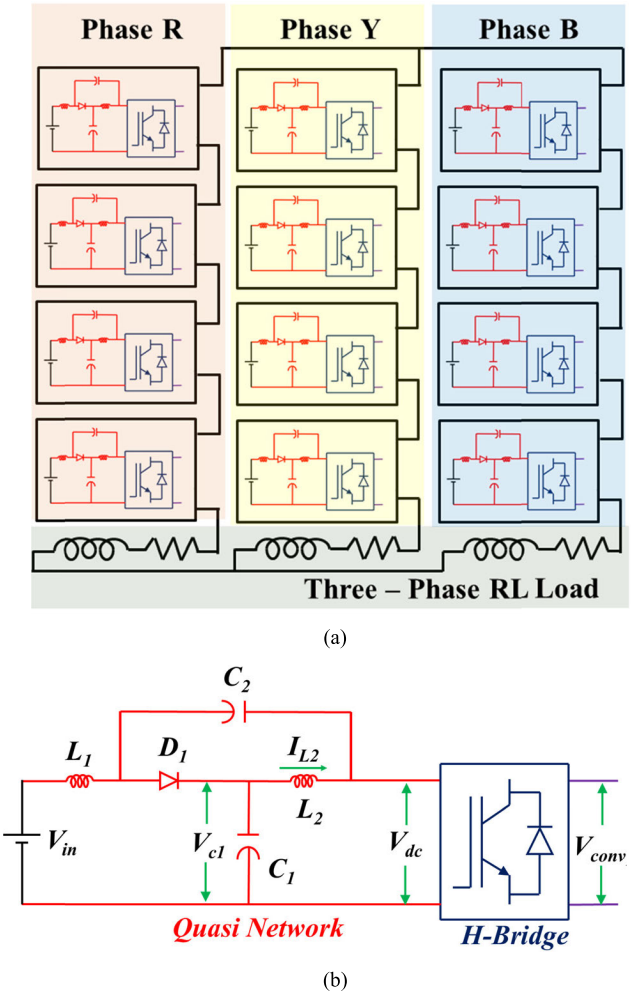


FIGURE 1. System Description – (a) three phase Nine-Level qZSI connected to three-phase RL load (b) module of Quasi Z Source Inverter consisting of quasi network and H-Bridge inverter.

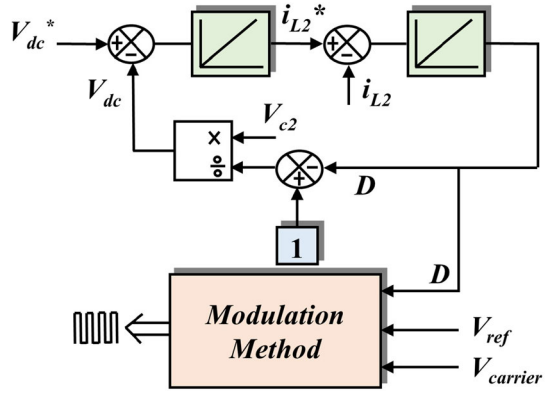


FIGURE 2. Control structure consisting of cascaded PI controller and switching pulse generation.

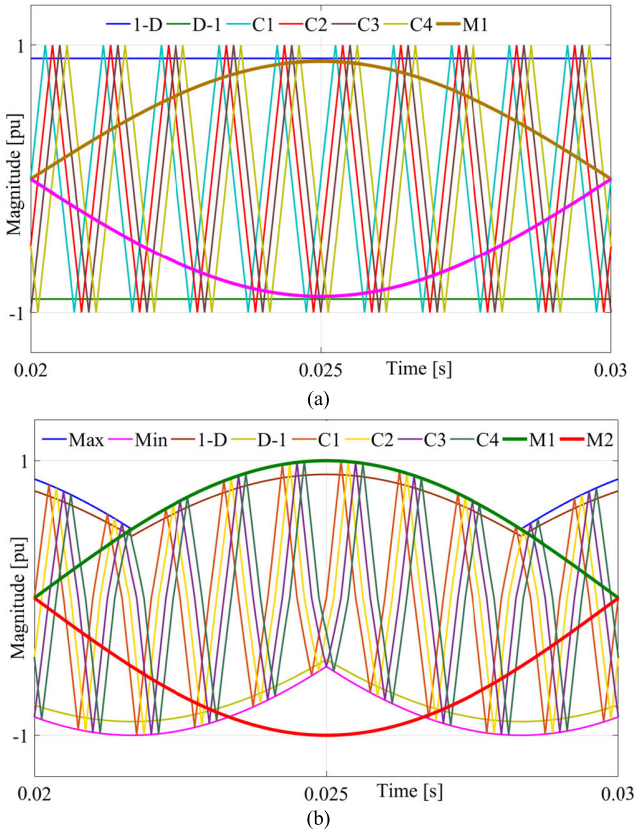


FIGURE 3. Carrier phase - shifted modulation techniques (a) pulse width modulation (b) pulse width amplitude modulation, maxima (Max), minima (Min), carrier signals (C1 – C4), modulating signals (M1 & M2).

in Fig. 2. The first loop compares the reference V_{dc} with the actual V_{dc} and generates inductor current reference through PI controller. This reference is compared with actual i_{L2} to generate the current error. The output of this control loop is the shoot-through duty cycle (D). D obtained here is used for generation of shoot through pulses, which are used for boosting the applied voltage [5].

B. MODULATION METHOD

In conventional methods, comparison of modulation signal with carrier signal is performed to generate switching pulses for H-Bridge switches. However, in qZSI, additional shoot-through pulses must be incorporated. There are two modulation methods discussed for generation of switching pulses:

1) PHASE SHIFTED CARRIER PULSE-WIDTH MODULATION (PSCPWM)

In this method of multilevel inverter control, carrier signals must be shifted by 180°/N (where N = Number of modules) with respect to each other. This modulation method is described in Fig. 3(a). It shows four carriers signals shifted by 45° with respect to each other. These carrier signals are compared with the modulation signal (sine wave) to give switching pulses. However, these pulses will not boost the quasi network output voltage. To achieve boosting, the carrier signals are compared with 1 – D and D – 1 to give shoot through pulses. To obtain the final switching pulses, logical OR operation is performed between these pulses and the pulses obtained with conventional sine-triangle comparison.

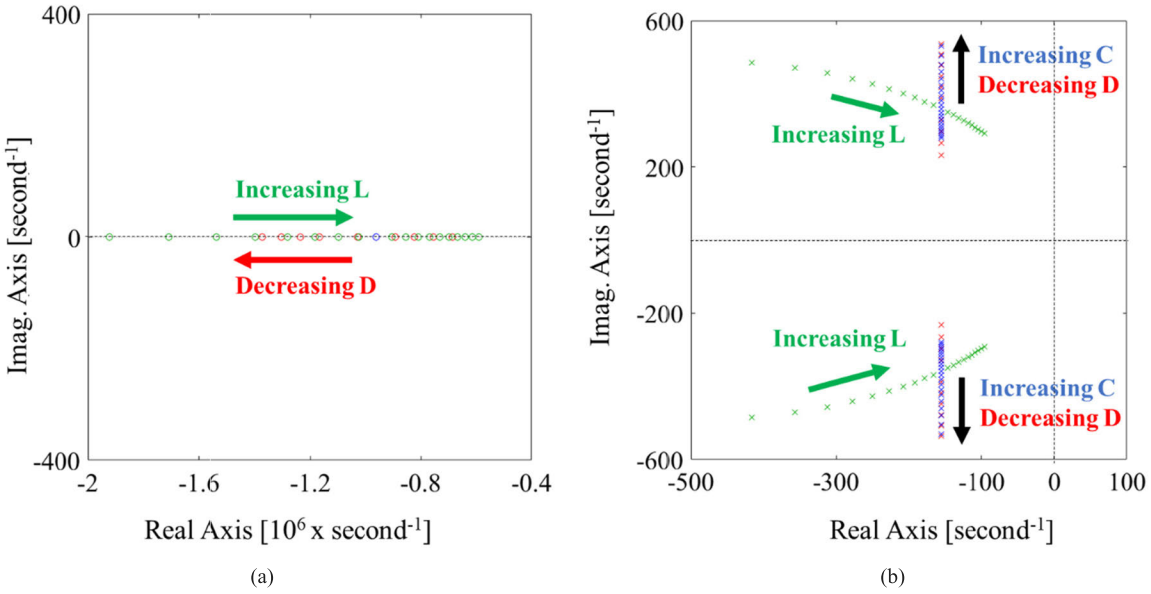


FIGURE 4. Variation of (a) poles and (b) zero of the transfer function $\left(\frac{V_{c1}(s)}{d(s)}\right)$ for variation of different circuit parameters.

C. PULSE WIDTH-AMPLITUDE MODULATION (PWAM)

In this method also, the carrier phase shift is maintained at 45°. Here, amplitude of the carrier signals is not clamped to unity. The amplitude of the carrier signal follows an envelope on both positive and negative sides. m_a, m_b and m_c are the modulation signals of the three phases of the multilevel inverter. Carrier signals amplitude follows the envelope of maximum of $\{m_a, m_b, m_c\}$ on the positive side and minimum of $\{m_a, m_b, m_c\}$ on the negative side. The resulting carrier signals with modulation signal are shown in Fig. 3(b).

Modification of this carrier also demands for change in the shoot-through pulses generation. This is implemented by multiplying 1 – D with absolute value of max $\{m_a, m_b, m_c\}$ and D – 1 with absolute value of min $\{m_a, m_b, m_c\}$. Here also, to obtain the final switching pulses, logical OR operation is performed between these pulses and the pulses obtained with modulation signal and carrier signals comparison.

IV. TRANSIENT STABILITY & SIMULATION RESULTS

A. TRANSIENT STABILITY

As discussed, control algorithm for qZSI consists of two cascaded PI controllers. To validate the stability of the system, transfer function of these two loops must be developed and stability of these loops for variation in parameters must be studied [49]–[51]. For this purpose, two transfer functions for qZSI are derived here.

Transfer function governing effect of shoot – through duty cycle on inductor current and capacitor voltage is given by (1) and (2),

Transfer function governing effect of shoot – through duty cycle on inductor current is given by:

$$\frac{iL_1(s)}{d(s)} = \frac{(V_{c1}+V_{c2}-RI_{load})\,Cs+(I_{load}-I_{L1}-I_{L2})\,(1-2D)}{LCs^2+C\,(r+R)\,s+(1-2D)^2} \tag{1}$$

Transfer function governing effect of shoot – through duty cycle on capacitor voltage is given by:

$$\frac{v_c(s)}{d(s)} = \frac{(V_{c1}+V_{c2}-RI_{load})(1-2D)+(I_{load}-I_{L1}-I_{L2})(sL+r+R)}{LCs^2+C(r+R)s+(1-2D)^2} \tag{2}$$

where V_{in} = applied input voltage [V], I_{L1} and I_{L2} are average inductors' L_1 and L_2 currents [A], V_{c1} and V_{c2} are dc voltages of C_1 and C_2 capacitors [V], I_{load} is peak load current [A], D is the shoot – through duty cycle [per unit], r is inductor stray resistance [Ohms], R is capacitor stray resistance [Ohms], L_1 and L_2 are equal to L stands for quasi inductor [mH], C_1 and C_2 are equal to C stands for quasi capacitor [mF].

Perturbation is introduced in the system by varying the value of quasi inductor (1.6 mH ± 1mH), quasi capacitor (2mF ± 1mF) and duty cycle (0 to 0.25), which are possible in actual system due to aging and control.

Zero plot for the transfer function $\frac{v_c(s)}{d(s)}$ is shown in Fig. 4(a). When the value of duty cycle is decreased from 0.25 to 0, the zeros of the transfer function moves farther from origin implying that the system stability increases for decrease in duty cycle. Similarly, when inductor value is

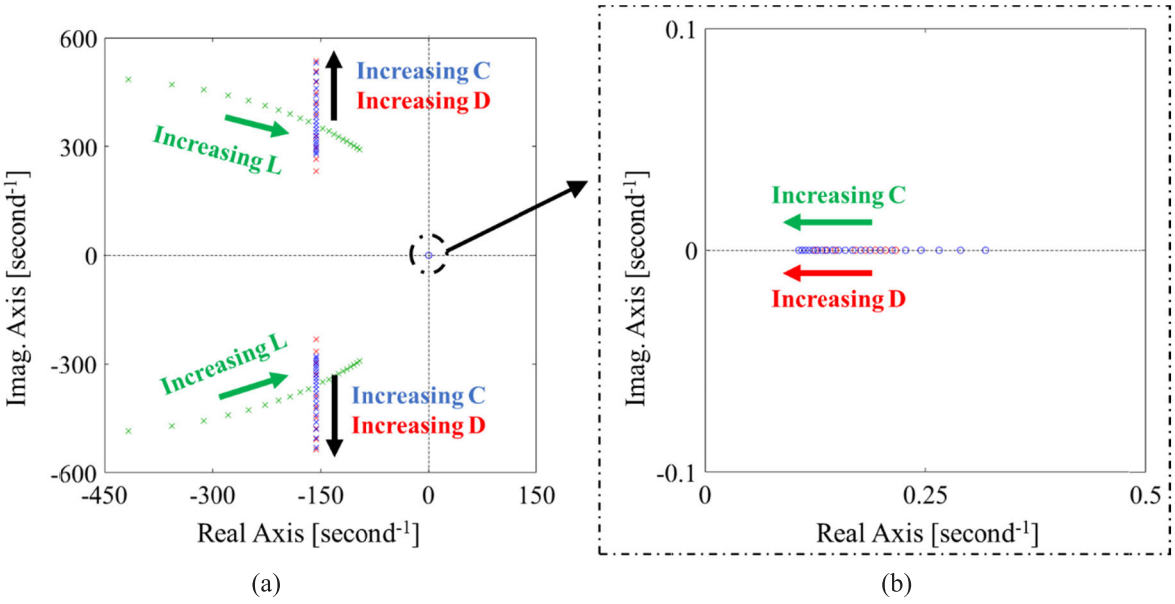


FIGURE 5. (a) Variation of poles and zero of the transfer function $\left(\frac{iL_1(s)}{d(s)}\right)$ for variation of duty cycle (D = 0 to 0.25), qZSI capacitor (C = 1mF to 3mF) and qZSI inductor (L = 0.6mH to 2.6mH) (b) zoomed version showing variation of systems zero for parameters variations.

increased from 0.6mH to 2.6 mH, the zero of the system move towards origin. However, even at 2.6 mH value of quasi inductor, zero of the system is still negative implying stable response. Since the denominator of the transfer function does not have any quasi capacitor term, location of system zeros is not affected by variation in value of quasi capacitor.

Pole plot of the system shows that the stability of the system increases when the value of quasi inductor is decreased as shown in Fig. 4(b). Complex conjugate poles obtained by increasing C or decreasing D moves far away (towards infinity) on the imaginary axis with their real part remaining constant. This movement only on the imaginary axis suggests effect on the damping coefficient and natural frequency of the system i.e., damping decreases and natural frequency increases conveying underdamped response with large transients when C value is increased and shoot – through duty is decreased.

For the second transfer function given by $\frac{iL_1(s)}{d(s)}$, dynamic stability of the system is plotted as shown in Fig. 5(a). Poles of the system lies on the left – hand side of the pole-zero plot implying stables poles. Stability of the system is increased by increasing the value of quasi inductor. However, increasing duty cycle and shoot – through duty cycle makes the system under damped and increases its natural frequency thereby making leading to poor transient performance.

Zeros of this transfer function (for these parameter variations of capacitor and shoot – through duty cycle) lies on the right-hand side of the pole-zero plot as shown in Fig. 5(b). This means that the transient response of the system may tend to become unstable if not controlled properly. To mitigate this, while designing control structure, pole – zero cancelation technique is applied for inner inductor current control loop. Due to this, the effect of right-hand side zero of the system is suppressed.

B. SIMULATION RESULTS

To validate the robustness and accuracy of the developed control algorithm (based on inputs from transient stability), simulation results during starting and load transients are presented here.

1) STARTING PERFORMANCE

Performance of different PWM methods during start – up of a V/f-controlled induction motor drive is reported in [27]. When conventional Phase – Shifted PWM control is used for induction motor control, no mechanical and electrical transients are observed. This is due to control of both shoot – through duty cycle and modulation index in qZSI. However, with PWAM control, qZSI always operate at unity modulation index (i.e., the peak of carrier signal is same as that of modulation signal), resulting in electrical and mechanical transients.

On the same basis, when the PWAM controlled multilevel qZSI connected to RL load is turned on, starting transients are observed as shown in Fig. 6. Fig. 6(a) shows tracking performance of qZSI during starting. Since the inductors and capacitors are not charged initially, the system draws large among of current as shown here. Initially, due to PI controller-based control, overshoot of 60% is observed. Fig. 6(b) and 6(c) shows phase voltage and line current for three phases during starting of the proposed inverter. Effect of starting transient in individual qZSI module is evidently reflected in multilevel inverter output voltage and current signals.

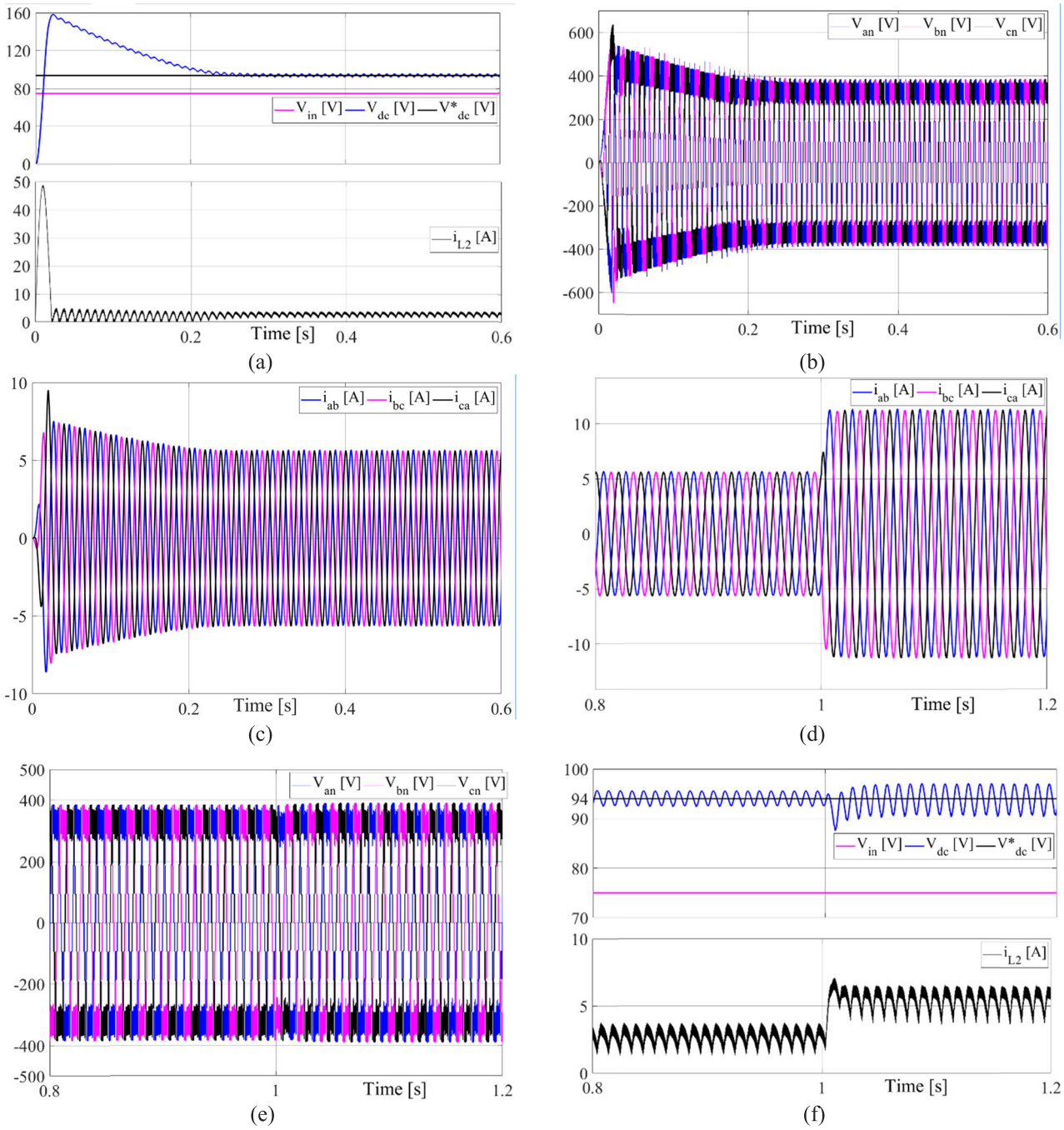


FIGURE 6. Starting response of qZSI module during start – up (a) dc bus tracking (b) phase voltages (c) line current, Load Transient performance of qZSI (d) line current transient (e) phase voltages and (f) dc bus tracking.

2) LOAD TRANSIENT PERFORMANCE

Response of the system for increase in load current of multi-level qZSI is also shown in Fig. 6. Fig. 6(d) shows load current transient when load current is increased from 5.5A peak to 11A (i.e., when load current is doubled). This increase in load current is also reflected in inductor current rise as observed in Fig. 6(f). This perturbation of load current increase is felt momentarily in dc voltage bus. Post increase in load current, ripple in dc bus voltage is increased as it is now supplying higher load current. Fig. 6(e) shows no transients in phase voltage thereby showing ideal performance of a voltage source.

V. FPGA IMPLEMENTATION OF CONTROL ALGORITHMS

A. LAYOUT OF PWAM CONTROL ALGORITHM

FPGA implementation of PWAM based control algorithm for voltage control of three – phase nine – level qZSI connected to RL load is shown in Fig. 7. Central controller block generates

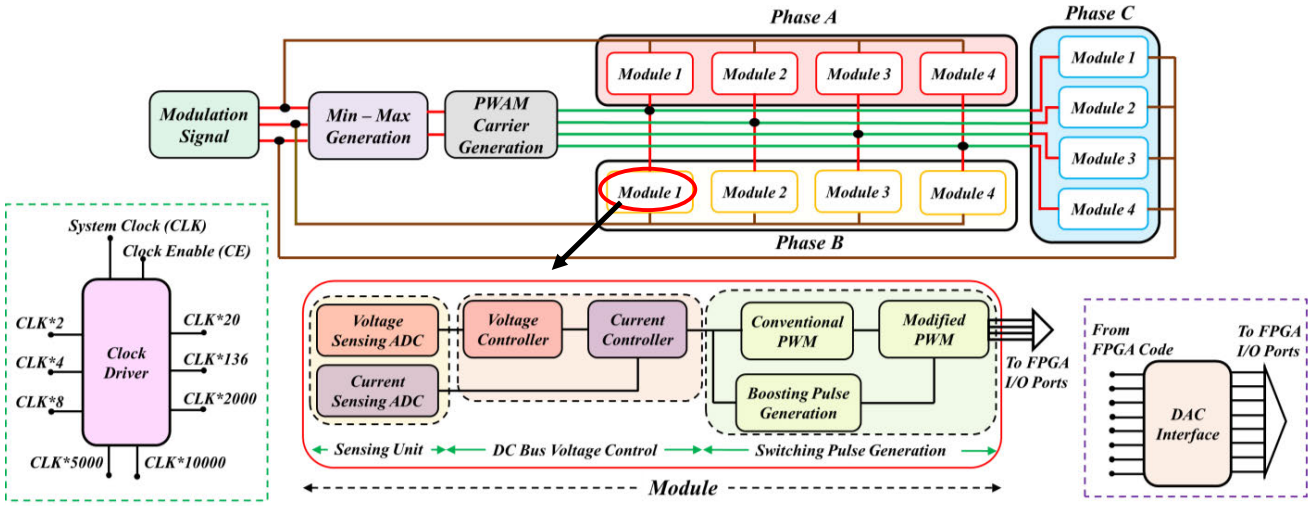


FIGURE 7. FPGA Implementation for voltage control of three – phase nine – level qZSI connected to RL load.

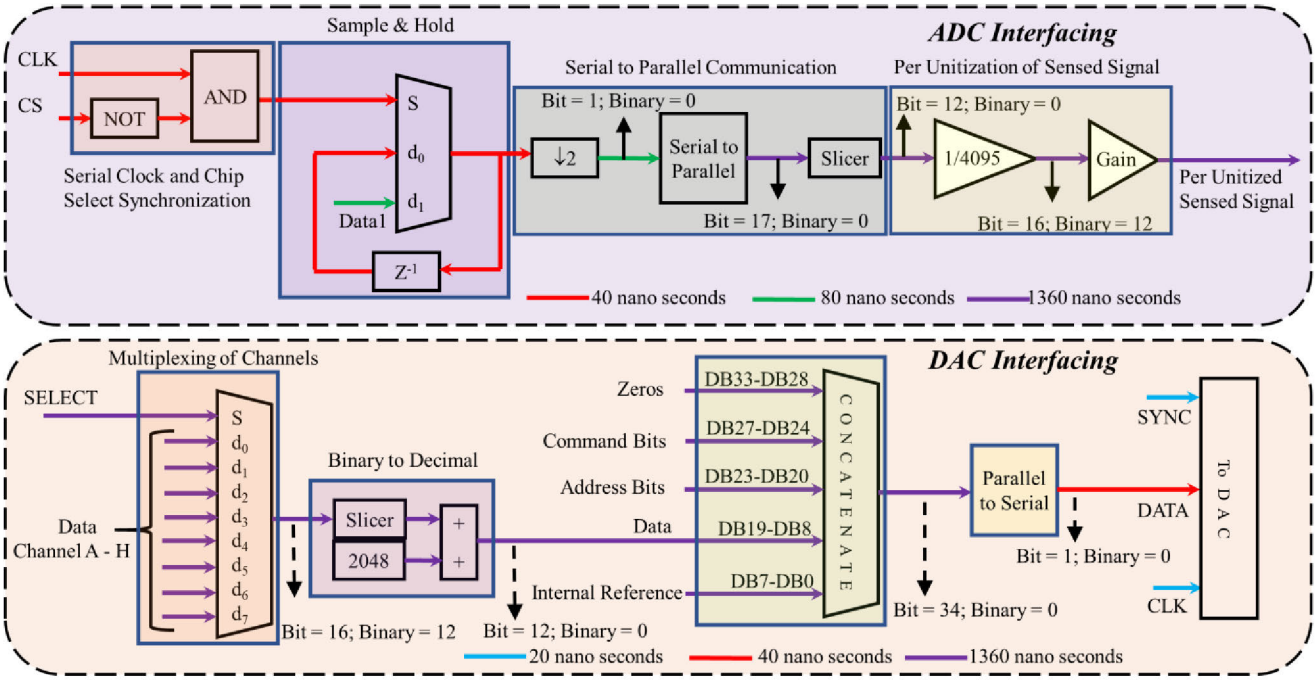


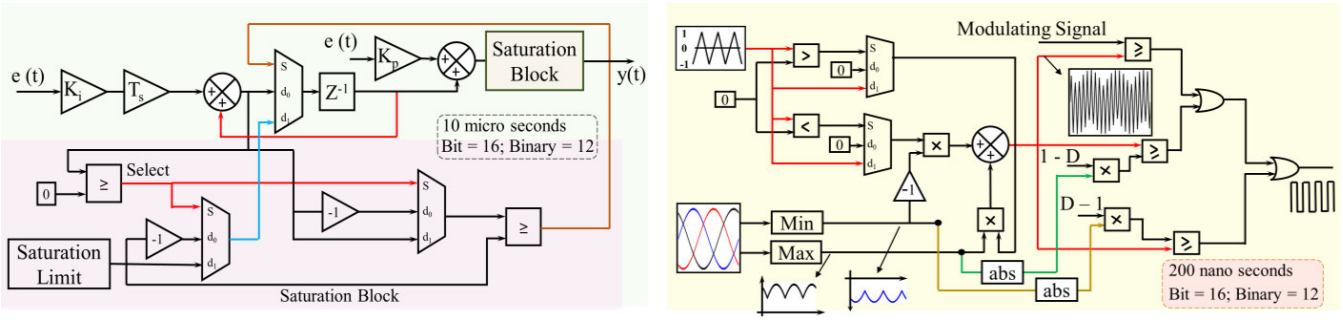
FIGURE 8. ADC and DAC interfacing for FPGA.

three – phase modulation signal and PWAM carrier signals for four modules of each phase. Clock driver block takes system clock (CLK) of 10 ns and Clock Enable (CE) as input and generates different sample times required in the entire FPGA code.

Each module as shown in Fig. 7, consists of dc bus voltage and inductor current sensing unit. ADC interfacing unit is used to sense the signal from ADC to FPGA. Detailed description of ADC interfacing along with bit format and sample times is shown in Fig. 8. Data is processed with ''Sample and Hold Circuit'' and then passed on to the serial to parallel communication buses. Slicing and per unitization of sensed signal is done to replicate per unitized actual signal.

Sensed signal is passed through cascaded Proportional + Integral (PI) controller block to generate shoot – through duty cycle reference. Detailed implementation of a PI controller with embedded saturation block is shown in Fig. 9(a). Saturation block helps to incorporate physical and operating restrictions in FPGA implementation. Entire controller block is processed at fixed time sample and bit format. To maintain stability of cascaded control loop, the two control loops are operated at different sample times (voltage control loop operates ten times faster than current control loop).

Modified carrier signal is obtained by estimating ''Maxima'' and ''Minima'' of the three modulation signals as shown in Fig. 9(b). This carrier signal is compared with modulating



(a) (b)

FIGURE 9. (a) Proportional + Integral Controller embedded with saturation block (b) switching pulses generation for PWAM logic consisting of "Min – Max Estimation", "Carrier Signal Generation" and "Modified PWM".

TABLE 1. List of components used for control implementation.

Component	Part Number
FPGA Board	VIRTEX 5 – xc5vlx50t
Voltage Sensor	LV 25P
Current Sensor	LA 55P
Gate Driver	GDA2A2S1
ADC	PMOD AD1
DAC	PMOD DA4

signal and shoot – through duty cycle references to obtain conventional PWM pulses and shoot – through pulses.

Logical OR operation is performed between these two pulses to achieve both inverter operation along with voltage boosting. Either fixed bit format of 16 – 12 or Boolean format is used in this block at fixed time sample of 200 ns. DAC is required to investigate, examine and tune the control algorithm. Fig. 8 shows the FPGA interfacing of 8 – channel DAC. Multiplexing of eight signals (channels) is achieved first and then 34 – bit word is written to the DAC by means of parallel to serial converter. This helps to pass one signal to the DAC each time specific address bit is mentioned in the 34 – bit word.

B. UTILIZATION OF INPUT – OUTPUT (I/O) PORTS OF FPGA BOARD

The list of components used for implementation of hardware control are given in Table I.

For dc bus voltage control of twelve modules, twenty – four signals must be sensed into the system (two signals per module). PMOD AD1 is a two channel, 12-bit analog-to-digital converter. Each ADC requires 4 I/O pins, VCC and GND as shown in Fig. 10. Conclusively, 72 pins of FPGA (12 ADCs) are required for signal sensing of the three – phase system.

From Fig. 10, it should be observed that CS (chip select), CLK (ADC clock), GND (ground) and VCC (3.3 V) are common to all the ADCs. To optimize the FPGA ports, an auxiliary board is designed which connects these four pins of all ADCs to FPGA. Thus, total number of FPGA pins required will be 24 (sensed signals) + 4 (common pins) = 28 thereby saving 44 I/O pins of FPGA.

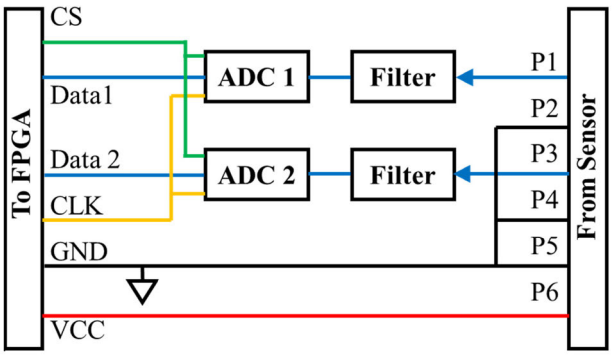


FIGURE 10. PMOD AD1 Circuit Diagram.

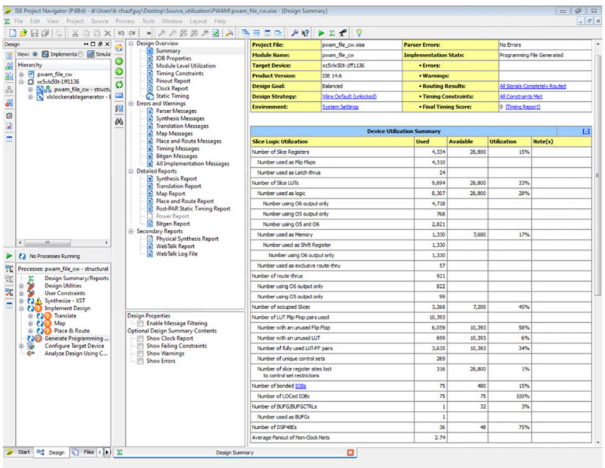


FIGURE 11. XILINX ISE Project Navigator screen.

C. FPGA RESOURCES UTILIZATION

A typical window showing design overview summary in Xilinx ISE Project is shown in Fig. 11. Important point for consideration is "Device Utilization Summary". Comparison of resources used for PWAM and PWM algorithm is given in Table – II.

Here, number of DSP48Es required in PWAM is 75% of 48 whereas no such DSP48Es are required for PWM. These blocks are used for implementation of "Multiplier" in FPGA. From Fig. 9(b), it should be observed that for generation of

TABLE 2. Device utilization summary of FPGA board.

Device Utilization Summary			
Slice Logic Utilization	Available	PWAM	PWM
Number of Slice Registers	28800	15%	15%
Number of Slice LUTs	28800	33%	31%
Number used as Logic	28800	28%	26%
Number used as Memory	7680	17%	17%
Number of occupied Slices	7200	45%	42%
Number of fully used LUT-Flip Flop pairs	9760	34%	37%
Number of bonded IOBs	480	15%	15%
Number of LOCed IOBs	76	100%	100%
Number of DSP48Es	48	75%	0%
Average Fanout of Non-Clock Nets		2.74	2.78

each carrier signal, two multipliers are used. For four such carrier signals, eight multipliers are utilized. Additionally, shoot – through reference offsets "1 – D" and "D – 1" must be multiplied with "Maxima" and "Minima" respectively in each module for switching pulse generation. Thus, twenty – four such multipliers are required. Conclusively, additional 32 multipliers are used for PWAM control algorithm resulting in higher consumption of DSP48Es. Extrapolating in this way, with single FPGA control board, 16 such modules can be controlled using PWAM based control algorithm. For control of further modules, pipelining of multipliers can be employed to achieve desired task with high latency.

However, compromise between clock frequency and latency occurring must be made for implementation of control for $>$ 16 modules. Higher resource realization is also reflected as higher power consumption on FPGA board during real time operation of the two modulation methods as shown in Table – III.

VI. HARDWARE RESULTS

Hardware prototype developed is shown in Fig. 12. Component specification used in hardware are given in Table IV. In this section, control response for closed loop quasi network voltage control is discussed followed by three-phase hardware results.

TABLE 3. Parameter specification for qZSI module.

Power Supply	PWAM			PWM		
	Voltage [V]	Current [A]	Power [mW]	Voltage [V]	Current [A]	Power [mW]
3.3V	3.324	0.318	1057	3.324	0.316	1050
1.8V	1.808	0.014	25	1.808	0.01	18
1.0 V	1.012	0.442	447	1.012	0.416	420
2.5 V	2.484	0.076	188	2.484	0.074	183
	Total Power [mW]		1718	Total Power [mW]		1673

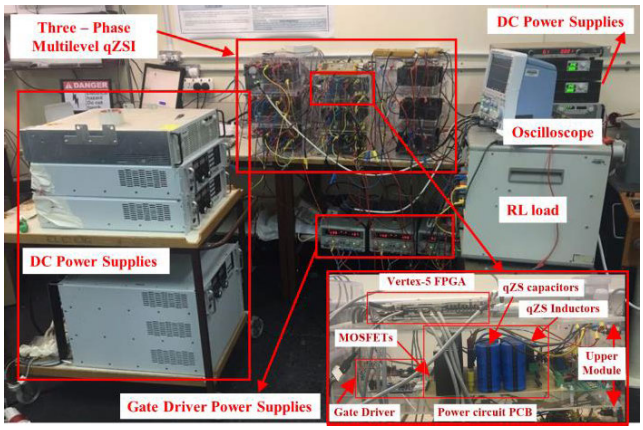


FIGURE 12. Hardware setup for nine – level three – phase qZSI system connected to RL load.

TABLE 4. Parameter specification for qZSI module.

Parameter	Specification
Switching Frequnecy [kHz]	1
Input Voltage [V]	75
Quasi Inductor [mH]	1.6
Quasi Capacitor [mF]	2
D_{max} [pu]	0.1
Modulation Index [pu]	0.88
Load Impedance	50 Ω, 150 mH

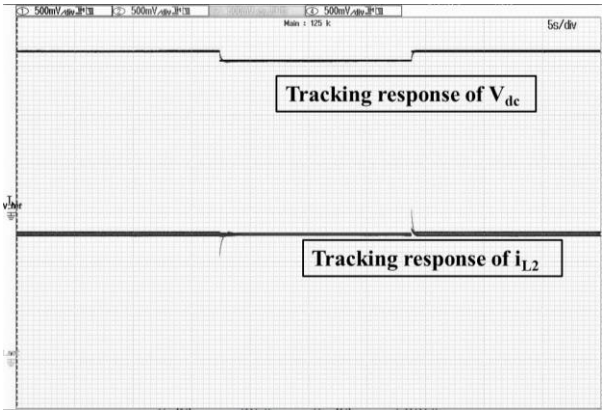


FIGURE 13. DAC output of the controller response.

A. PERFORMANCE OF CASCADED PI CONTROLLER BASED DC BUS VOLTAGE CONTROLLER

To verify the control algorithm, quasi network output voltage reference is varied. System's response is as shown in Fig. 13. This is the output of DAC which shows tracking of dc bus voltage and inductor current for different references. Control algorithm tracks the reference absolutely with minimal error as the two signals are overlapping. It should also be observed that change in dc bus reference are also reflected in inductor current references due to cascaded PI control algorithm.

B. COMPARISON OF QZSI PERFORMANCE WITH THE TWO MODULATION TECHNIQUES

Fig. 14 shows the experimental results of three – phase qZSI system with two different modulation techniques.

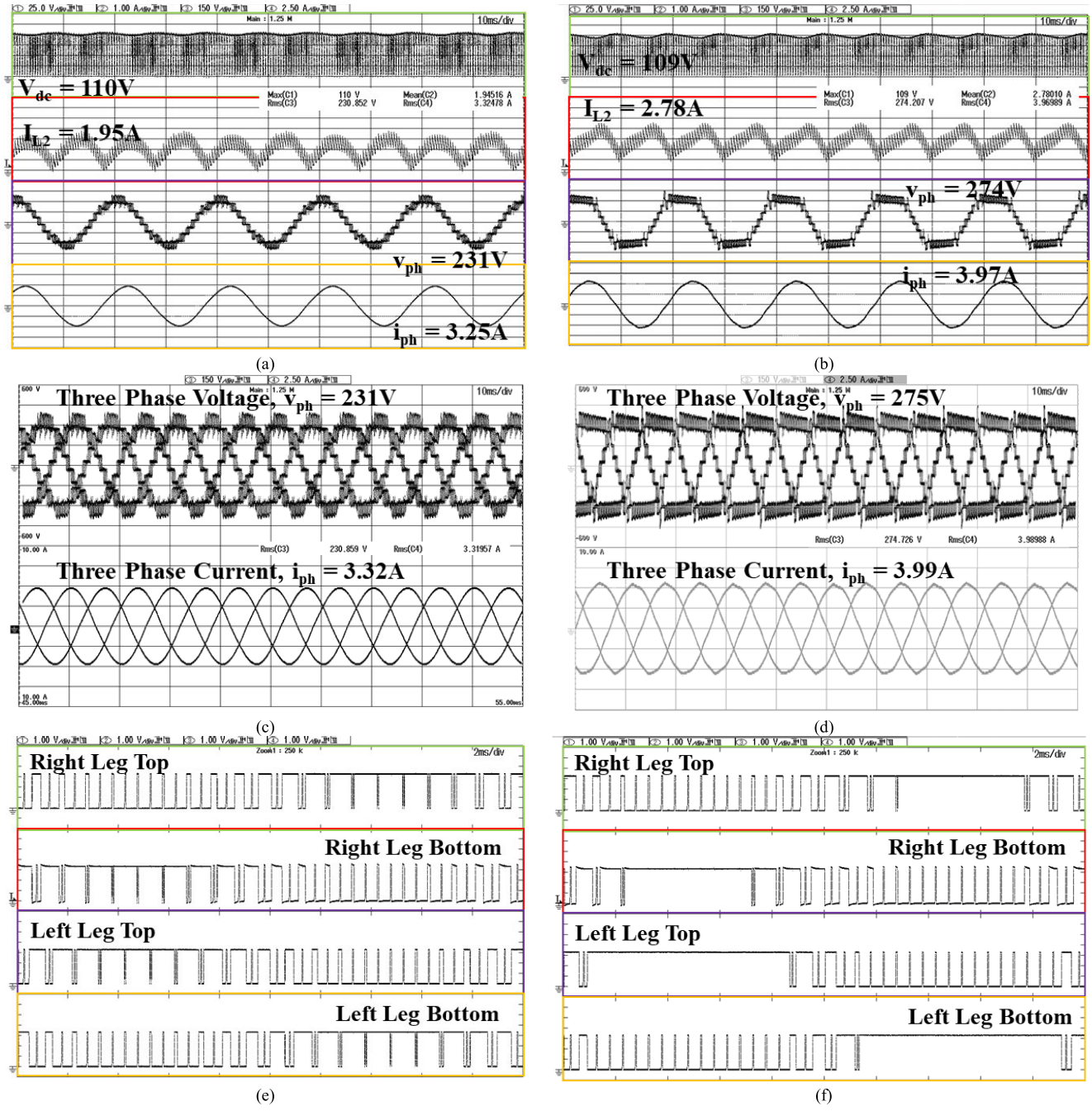


FIGURE 14. Hardware Results for two modulation methods – PSCWM Control Algorithm (a) qZSI performance (c) three – phase circuit output phase voltage and phase current (e) H – Bridge Switching Signals, PWAM Control Algorithm (b) qZSI performance (d) three – phase circuit output phase voltage and phase current (f) H – Bridge Switching Signals.

Fig. 14(a) shows qZSI performance with PWM control algorithm whereas Fig. 14(b) shows the performance with PWAM control. DC bus voltage and inductor current are shown along with phase voltage and phase current. Output voltage of quasi network consists of pulses due to shoot-through state. The inductor current consists of two ripples – a) double the switching frequency and b) double the fundamental frequency as observed in both waveforms.

Fig. 14(c) shows three phase voltages and currents obtained with PWM control algorithm. Phase output voltage consists of nine-level voltage waveform and the corresponding current is sinusoidal in nature. RMS value of output voltage is 230V with the corresponding load current of 3.32A

Fig. 14(d) shows qZSI performance with PWAM control algorithm. Here also, the phase output voltage consists of nine-levels. The output voltage waveform is peaky in nature. However, rms value of output voltage of 274 is higher compared to the value obtained of 230V obtained with PWM for the same dc bus voltage of 110V resulting in higher source voltage utilization. It should also be observed that inductor

TABLE 5. Comparison of the two modulation methods.

Parameters	PWM	PWAM
Switching losses Right Leg Switches [28]		
Active – State	100%	50%
Shoot – through	100%	< 67%
Switching Losses Left Leg Switches [28]		
Active – State	100%	13.4%
Shoot – through	100%	<84%
No. of switching (in all H – Bridge switches)	Same	Different
Heat Sink requirement	Same	Different
Efficiency comparison for 4.5kW load [28]		
Efficiency (at D = 0)	94.5%	95%
Efficiency (at D = 0.2)	92.7	94%
Steady State performance		
Voltage Utilization	100%	115.6%
THD Phase Voltage	16.71%	23.47%
THD Phase Current	0.89%	0.64%

current drawn from the power supply is also higher (as shown in Fig. 14(b)) in case of PWAM.

Fig. 14(e) shows the gating signals for the four switches of a single module for PWM switching technique. Here, number of switching of all the four switches of the module remains the same due to symmetric nature of carrier and modulation signals. However, in PWAM control, modifying the envelope of carrier amplitude results in generation of continuous switching pulse at the peak of the modulation signal as shown in Fig. 14(f).

Due to this continuous gating pulse, no active or shoot-through state switching are implemented in this region resulting in lesser number of switching and reduced switching losses. However, number of switching in different switches of the H – Bridge calls for different heat sinks for PWAM algorithm. Also, the continuous gate pulse near the peak hints at peaky voltage and current waveform as observed in Fig. 14(d) thereby resulting in higher THD content with PWAM algorithm as compared to PWM. For summarizing, comparison of the two modulation methods is given in Table – V below:

VII. CONCLUSION

In this paper, closed loop control implementation of three – phase nine – level qZSI connected to RL load using single FPGA control board is reported. Detailed FPGA logic for PWAM based control algorithm is presented considering the design and constraint guidelines. Capability of FPGA based control to operate at different sample times resulting in flexibility, resource optimization, faster implementation, significantly lower impact of delay – based logics, and system stability are highlighted.

Interfacing of externally connected ADCs and DAC is presented which gives an insight of different bit format and sample times requirements of these components. Device utilization summary is presented for both control algorithm which helps in understanding higher FPGA resource consumption of PWAM based control algorithm. It also helps in extrapolating the maximum number of closed loop controlled qZSI modules (16 modules) implementation possible with single FPGA board. Experimental results suggest better source voltage utilization and reduced switching losses with PWAM control implementation of three – phase nine – level qZSI system with single FPGA control board.

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