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Simplified Four-Level Inverter-Based Dynamic Voltage Restorer With Single DC Power Source

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ABSTRACT This paper proposes a simplified four-level (S4L) inverter based dynamic voltage restorer (DVR). In the proposed configuration, the dual buck stage can output full, two thirds, and one third of dc link voltage. Including the zero voltage provided by the two-level inverter, the output of the proposed inverter can be four levels. With the same switching frequency, the S4L inverter based DVR achieves better performance than the existing two-level and three-level inverters based DVRs. Moreover, compared with the existing four-level inverter based DVRs, it requires less active switches/diodes and only requires a single DC power source. The experimental results are provided for the validation of the proposed system.

INDEX TERMS Dynamic voltage restorer (DVR), simplified four-level (S4L) inverter, voltage sag, total harmonic distortion (THD).

I. INTRODUCTION

In modern power systems, more and more critical loads are integrated. The critical loads can be chip manufacturing factory, programmable logic controllers, computer numerical control equipment, etc. These types of loads are sensitive to the power quality (PQ) of the supply voltage [1], [2]. Voltage fluctuations may lead to shut down and even irreversible damage of the critical loads [1], [2]. Thus, it is essential to maintain a rated voltage for the safe operation of the system [3].

Among all the voltage conditioners, the dynamic voltage restorer (DVR) is one of the most comprehensive solutions for voltage PQ problems [4], [5]. Fig. 1 shows the basic topology of the single-phase DVR. A typical DVR consists of a two-level inverter, a series capacitor, an inductor, and a dc source. The DVR is able to maintain the load voltage at the rated sinusoidal waveform by injecting a voltage of a specific phase angle and magnitude into the distribution line [4], [5]. From the literatures, it is noted that a DVR can provide other benefits in addition to its basic function.

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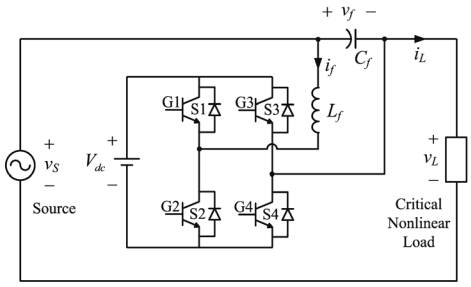

FIGURE 1. Topology of the two-level single-phase DVR.

For example, in the pre-sag operation [6]–[8], the DVR can restore the exact amplitude and phase of the load voltage when the sag and phase jump happens in the source voltage. The magnitude of the injected voltage of the pre-sag method is higher than that of the in-phase method. The DVR can inject the minimum amplitude of the compensation voltage by using the in-phase method [9]–[13]. In the self-supported mode [14]–[17], the DVR does not require external energy storage by utilizing the capacitor connected at the dc link of the VSI. However, the energy stored in the capacitor is limited. In the energy optimized strategy [18], [19], the energy handled by the DVR can be optimized. Using reduced active

TABLE 1. Comparison of performance and required components of the two-level, three-level and four-level inverters in DVRs.

	Topology	THD	Number of active switches	Number of diodes	Number of DC sources
Two-level	H-bridge [6]	High	4	4	1
Three-level	NPC [26]	medium	8	12	1
	CHB [28]	medium	8	8	2
Four-level	CHB [29]	Low	12	12	3
	Proposed S4L	Low	8	8	1

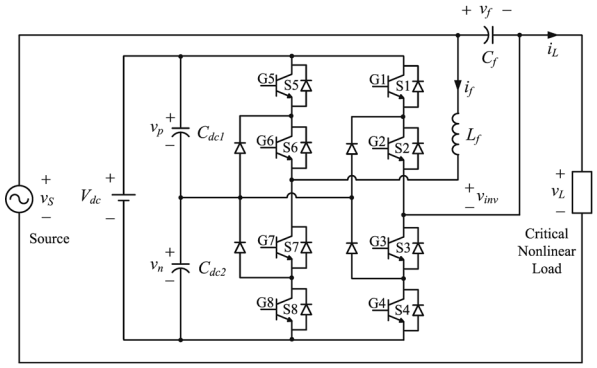

FIGURE 2. Topology of the 3L-NPC inverter based single-phase DVR.

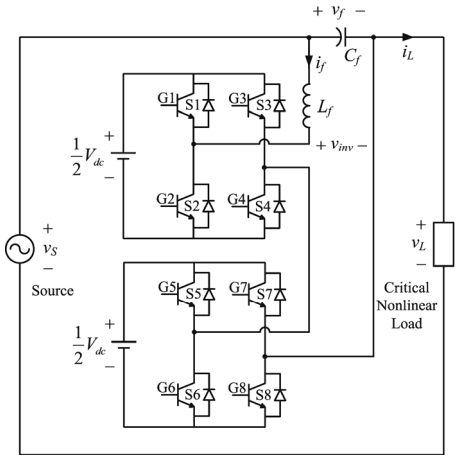

FIGURE 3. Topology of the three-level CHB inverter based single-phase DVR.

power injection, the energy optimized strategy maintains balanced load voltages under unbalanced large voltage sags. In [20], a two-degree freedom control strategy is proposed to reduce the number of measured variables. In this way, the conventional current loop can be avoided in the control scheme of the DVR. In [21], a dual-function DVR is utilized to operate under normal voltage compensation mode and short-circuit fault current-limiting mode. In [22], an open-end winding transformer is used in a DVR to connect two conventional two-level inverters in series for harmonic reduction in the system. In [23], the elliptical restoration based compensation scheme is adopted in the DVR to provide a smooth changeover of the displacement angle during the transient status of the system. In [24]–[26], direct converters are applied in the DVRs, so that the DC link is no longer required in the DVRs. The elimination of the DC link reduces the cost and volume of DVRs. From the literature, it is noted that the conventional two-level inverter based DVR requires high switching frequency of the power converter to obtain a low total harmonic distortion (THD) of the load voltage. Unfortunately, the high switching frequency increases the switching losses and the controller computational burden.

To avoid the aforementioned problems, the use of multilevel inverters is a suitable approach, since multilevel inverters can provide low THD while their switches operate at a relatively low switching frequency. The commonly used multilevel inverters in DVR applications are the three-level neutral point clamped (3L-NPC) inverter [27], and the H-bridge cascaded inverters [28], [29]. The topology of the 3L-NPC inverter based single-phase DVR is illustrated in Fig. 2 [27]. Compared with the conventional DVR, the 3L-NPC inverter based DVR requires eight active switches and additional four clamping diodes. Fig. 3 shows the topology of the three-level cascaded H-bridge (CHB) inverter based single-phase DVR [28]. In this topology, the outputs of two H-bridge inverters are connected in series. Only eight active switches are required in the cascaded topology. Similarly, in the four-level CHB inverter based single-phase DVR [29], the outputs of three H-bridge inverters are connected in series, thus, twelve active switches are required. It has to be mentioned that in [29] the authors have demonstrated that if the injected voltage is in quadrature with the current, the sag compensation can be carried out with the aid of reactive power only. Thus, the DC link can be supported by the capacitors only. However, the amount of sag should be within a certain limit. If the amount of sag is larger than the limit, the sag correction with reactive power only is not possible. It means that the capacitor supported DVR has limited operating range. In this paper, the DVR with full operating range is investigated. Thus, the DVR will inject both active and reactive power into the system. The DC link of the inverter in the DVR has to be supported by DC power sources. Correspondingly, the two-level inverter and 3L-NPC inverter based DVRs need only one DC power source. In multilevel CHB inverter based DVR, each H-bridge should be fed by an individual DC power source. The required number of DC power sources in the different topologies is summarized in Table 1. Table 1 also shows the required number of active switches and diodes, as well as the THD performance. From Table 1, it is noted that the two-level inverter based DVR suffers from the high THD of the load voltage. The aforementioned two commonly

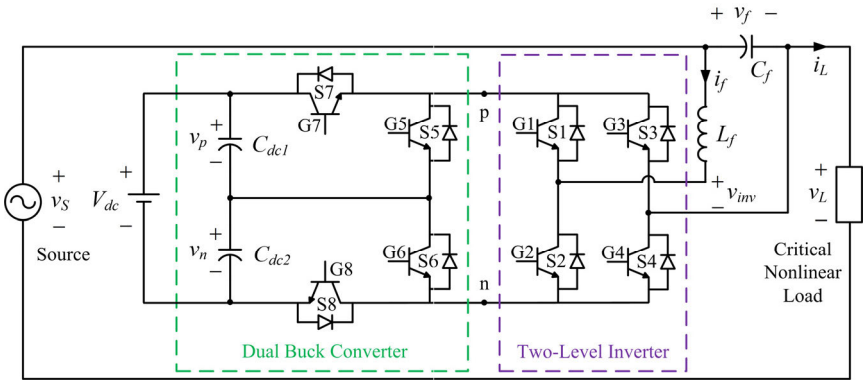

FIGURE 4. Topology of the S4L inverter based single-phase DVR.

used multilevel inverter based DVRs are not cost-effective solutions for voltage PQ problems compensation. The reason is that the 3L-NPC inverter needs additional diodes, while the multilevel CHB inverter needs multiple DC power sources.

In order to provide a cost-effective solution, a simplified four-level (S4L) inverter in the DVR application as shown in Fig. 4 is proposed. The proposed S4L inverter is based on a three-level simplified NPC inverter [30], [31], which comprises a dual buck converter and a conventional two-level inverter. This new S4L inverter does not require additional components compared with the three-level inverters. It is also noted the proposed S4L inverter based DVR only requires a single DC power source compared with the multilevel CHB inverter based DVR. Thus, the proposed S4L inverter based DVR is more cost-effective. Moreover, the proposed S4L inverter based DVR can provide four level voltages at the output of the inverter, which significantly helps to mitigate the harmonic problem in the system. Specifically, the upper arm capacitor shares two thirds of the DC link voltage. The lower arm capacitor shares one third of the DC link voltage. Thus, the dual buck converter can output full, two thirds, and one third of DC link voltages. Taking into account the zero voltage generated by the two-level inverter, the proposed inverter can output four voltage levels for the DVR and, therefore, it provides less harmonics in the load voltage compared with the conventional three-level inverter based DVRs.

In order to provide the four-level inverter based DVR with fast dynamic, a model predictive control (MPC) method is applied in this paper. The MPC is able to offer smooth transient performance and fast dynamics response [32]–[39].

The main contributions of this paper are summarized as follows:

1) The proposed S4L inverter based DVR does not require additional diodes and only requires a single DC power source compared with the commonly used multilevel inverter based DVRs. It is a more cost-effective solution for load voltage compensation.
2) Compared with the commonly used three-level inverter based DVR, the proposed S4L inverter based DVR can output four level voltages without adding additional components. Thus, the harmonics in the load voltage can be further mitigated.

TABLE 2. Switching combinations and terminal voltage of dual buck converter.

Switching Combinations				Terminal Voltage
S5	S6	S7	S8	v_{pn}
0	0	1	1	$+V_{dc}$
0	1	1	0	$v_p = +2V_{dc}/3$
1	0	0	1	$v_n = +V_{dc}/3$

The rest of this paper is arranged as follows. The detailed topology and discrete-time model of the four-level inverter based DVR are presented in Section II. Using the derived discrete-time model, the MPC based controller is designed in Section III. Section IV shows the experimental results of the laboratorial prototype. Section V concludes this paper.

II. TOPOLOGY OF FOUR-LEVEL INVERTER BASED DVR

A. SYSTEM CONFIGURATION

As presented in Fig. 4, the S4L inverter based single-phase DVR consists of a conventional two-level inverter (S1, S2, S3 and S4), a dual buck converter (S5, S6, S7 and S8), a DC power source (V_{dc}), a inductor (L_f), a series capacitor (C_f), and two DC-link capacitors (C_{dc1} andC_{dc2}). C_{dc1} and C_{dc2} will share 2/3 and 1/3 of V_{dc}, respectively. In Fig. 4, i_L and i_f are the load current, and inductor current, respectively.v_f, v_S and v_L are the series compensation voltage, source voltage and load voltage, respectively. v_p and v_n represent the upper and lower arm voltages.

As mentioned previously, the dual buck converter is responsible for generating three voltage levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$) from the available dc source V_{dc}. These voltage levels are obtained from the switching combinations of S5, S6, S7 and S8 tabulated in Table 2. Considering the zero voltage generated by the two-level inverter, the output voltage v_{inv} of the proposed inverter can take four levels ($+V_{dc}$, $+2V_{dc}/3$, $+V_{dc}/3$, 0). Symmetrically, the negative part of v_{inv} can also provide four levels ($-V_{dc}$, $-2V_{dc}/3$, $-V_{dc}/3$, 0).

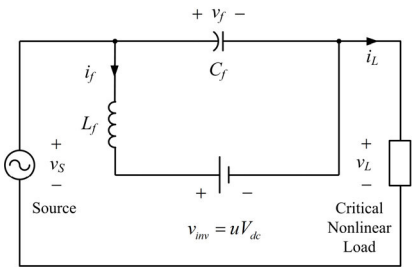

FIGURE 5. Equivalent circuit of the S4L inverter based single-phase DVR.

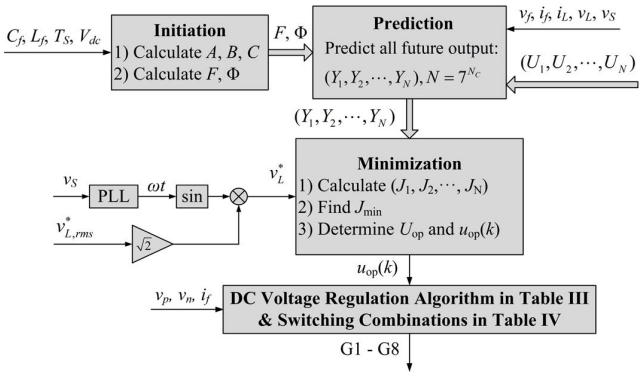

FIGURE 6. Control diagram for the S4L inverter based single-phase DVR.

B. DISCRETE-TIME MODEL

The equivalent circuit of the system is illustrated in Fig. 5. The output voltage of the full-bridge inverter is derived as

$$v_{inv} = uV_{dc} \tag{1}$$

where u is the switching variable, which can take the values $u \in \{1, 2/3, 1/3, 0, -1/3, -2/3, -1\}$.

In Fig. 5, the following equations describe the dynamics of the S4L inverter based single-phase DVR.

$$C_f \frac{dv_f}{dt} + i_f - i_L = 0 \tag{2}$$

$$v_{inv} + L_f \frac{di_f}{dt} - v_f = 0 \tag{3}$$

$$v_S - v_f - v_L = 0 \tag{4}$$

Discretization of (2), (3) and (4) is realized by utilizing the forward-Euler method as

$$v_f(k+1) = v_f(k) - \frac{T_S}{C_f} i_f(k) + \frac{T_S}{C_f} i_L(k) \tag{5}$$

$$i_f(k+1) = i_f(k) + \frac{T_S}{L_f} v_f(k) - \frac{T_S}{L_f} v_{inv}(k) \tag{6}$$

$$v_L(k+1) = v_S(k+1) - v_f(k+1) \tag{7}$$

where T_S is the sampling time. Due to a small value of T_S, the values of the sensed signals i_L and v_S are treated as constant in two subsequent sampling instants. Consequently:

$$i_L(k+1) = i_L(k) \tag{8}$$

$$v_S(k+1) = v_S(k) \tag{9}$$

Equation (7) can be rewritten as follows:

$$v_L(k+1) = v_S(k) - v_f(k) + \frac{T_S}{C_f} i_f(k) - \frac{T_S}{C_f} i_L(k) \tag{10}$$

The discrete-time state-space model of the four-level inverter based single-phase DVR is derived as

$$x(k+1) = Ax(k) + Bu(k) \tag{11}$$

$$y(k) = Cx(k) \tag{12}$$

where

$$A = \begin{bmatrix} 1 & -\frac{T_S}{C_f} & \frac{T_S}{C_f} & 0 & 0 \\ \frac{T_S}{L_f} & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ -1 & \frac{T_S}{C_f} & -\frac{T_S}{C_f} & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix};$$

$$B = \begin{bmatrix} 0 \\ -\frac{T_S V_{dc}}{L_f} \\ 0 \\ 0 \\ 0 \end{bmatrix}; \quad C = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \\ 0 \end{bmatrix}^T;$$

$x(k) = [v_f(k) i_f(k) i_L(k) v_L(k) v_S(k)]^T$ represents the state variable vector; and $u(k)$ represents the switching variables, i.e., the control input of MPC. $y(k) = v_L(k)$ is the system output. Then the system output can be regulated to track the reference signal. In this work, it is the load voltage reference.

III. MPC BASED CONTROLLER DESIGN

The MPC method is utilized to control the S4L inverter based single-phase DVR, due to the superior performance in the control of power electronic devices [30]–[37].

A. REFERENCE GENERATION FOR LOAD VOLTAGE

In Fig. 6, it can be observed that a phase-locked loop (PLL) is used to generate the synchronization angle ωt from v_S. The reference of v_L is calculated by using the reference load voltage root-mean-square (RMS) value, $v_{L,rms}^*$, in the following.

$$v_L^* = \sqrt{2} v_{L,rms}^* \sin(\omega t) \tag{13}$$

B. MINIMIZATION COST FUNCTION OF MPC

In order to obtain the minimum error between the reference and predicted load voltages, a cost function is defined, in which N_p and N_c are prediction horizon and control horizon, respectively. The MPC will apply N_c number of control

variables $(u(k), u(k+1), \ldots, u(k+N_c-1))$ to predict N_p number of future output variables $(y(k+1), y(k+2), \ldots, y(k+N_p))$. The cost function J is defined as

$$J = (Y - R)^T (Y - R) \tag{14}$$

where $Y = [v_L(k+1)\ v_L(k+2) \ldots v_L(k+N_p)]^T$; $R = \underbrace{[11 \cdots 1]}_{N_P}^{T} v_L^*(k)$; and $v_L^*(k)$ represents the reference of load voltage. Y is computed as in [37]

$$Y = Fx(k) + \Phi U \tag{15}$$

where $U = [u(k)u(k+1) \ldots u(k+N_c-1)]^T$;

$$F = \begin{bmatrix} CA \\ CA^2 \\ CA^3 \\ \vdots \\ CA^{N_P} \end{bmatrix};$$

$$\Phi = \begin{bmatrix} CB & 0 & 0 & \cdots & 0 \\ CAB & CB & 0 & \cdots & 0 \\ CA^2B & CAB & CB & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ CA^{N_P-1}B & CA^{N_P-2}B & CA^{N_P-3}B & \cdots & CA^{N_P-N_C}B \end{bmatrix}$$

Based on the seven possible control actions (1, 2/3, 1/3, 0, −1/3, −2/3, −1) of u given in (1), all possible control actions of U are $(U_1, U_2, \cdots, U_N)$, where $N = 7^{N_C}$. The future output $(Y_1, Y_2, \cdots, Y_N)$ is computed utilizing (15) and U. Then, $(Y_1, Y_2, \cdots, Y_N)$ and R are substituted into (14) to obtain the values of objective function $(J_1, J_2, \cdots, J_N)$. The minimal value $J_{\min}$ can be found. Then, $J_{\min}$ corresponds to the optimal control action U_{op} at the minimum error. The present control action is the first control action of U_{op}, i.e., $u_{\text{op}}(k)$. The aforementioned procedure has been summarized in Fig. 6.

C. DC VOLTAGE REGULATION

In order to ensure the voltage balancing between the two DC capacitors, the carrier based PWM method is a commonly utilized approach [40]–[42]. In this paper, the magnitude of v_p is twice of that of v_n. To maintain v_p and v_n at $2V_{dc}/3$ and $V_{dc}/3$, respectively, a DC voltage regulation algorithm is used in the controller. The error between v_p and v_n is defined as

$$\Delta = v_p - v_n \tag{16}$$

A threshold δ is defined so that, Δ should be within the range of $[V_{dc}/3 - \delta,\ V_{dc}/3 + \delta]$. If $\Delta > V_{dc}/3 + \delta$, it means v_p is higher than its upper boundary and v_n is lower than its lower boundary. The voltages can be balanced by actively charging v_n or discharging v_p. If $\Delta < V_{dc}/3 - \delta$, it means v_p is lower than its lower boundary and v_n is higher than its higher boundary. The voltages can be balanced by charging v_p or discharging v_n. If $\Delta \in [V_{dc}/3 - \delta,\ V_{dc}/3 + \delta]$, the switching combinations just follow the calculated $u_{\text{op}}(k)$. When $u_{\text{op}}(k) = 0$, the output voltage of the four-level inverter is zero. The DC voltage regulation algorithm is summarized in Table 3.

TABLE 3. DC voltage regulation algorithm.

Input $u_{op}(k)$, v_p, v_n and i_f
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) > 0$ and $i_f \geq 0$
Lower arm is charged; v_{inv} is positive.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) > 0$ and $i_f < 0$
Upper arm is discharged; v_{inv} is positive.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) < 0$ and $i_f \geq 0$
Upper arm is discharged; v_{inv} is negative.
If $\Delta > V_{dc}/3+\delta$, $u_{op}(k) < 0$ and $i_f < 0$
Lower arm is charged; v_{inv} is negative.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) > 0$ and $i_f \geq 0$
Upper arm is charged; v_{inv} is positive.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) > 0$ and $i_f < 0$
Lower arm is discharged; v_{inv} is positive.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) < 0$ and $i_f \geq 0$
Lower arm is discharged; v_{inv} is negative.
If $\Delta < V_{dc}/3-\delta$, $u_{op}(k) < 0$ and $i_f < 0$
Upper arm is charged; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 1$
Full DC link is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -1$
Full DC link is connected; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 2/3$
Upper arm is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -2/3$
Upper arm is connected; v_{inv} is negative.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = 1/3$
Lower arm is connected; v_{inv} is positive.
If $V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$ and $u_{op}(k) = -1/3$
Lower arm is connected; v_{inv} is negative.
If $u_{op}(k) = 0$
$v_{inv} = 0$.
Output gate signals G1-G8

Based on the DC voltage regulation algorithm, the corresponding switching combinations are listed in Table 4. (S1, S2), (S3, S4), (S5, S7) and (S6, S8) are complementary pairs.

D. SUMMARY OF MPC ALGORITHM

The MPC algorithm utilized in this paper is summarized as follows:

1) Step 1: Compute the load voltage reference.
2) Step 2: Calculate the augmented model A, B, C. Compute the F and Φ matrices.
3) Step 3: Predict all future output using the F and Φ matrices, measured voltage and current signals, and the control actions.
4) Step 4: Calculate the values of the objective function and determine the optimal control action based on the load voltage reference and the predicted future output.
5) Step 5: Based on the DC link voltages and the inductor current, determine the switching actions using the DC voltage regulation algorithm in Table 3 and the switching combinations in Table 4.

TABLE 4. Switching combinations of S4L inverter based single-phase DVR.

Error of DC Voltages	Present Control Action	Inductor Current	Dual Buck Converter Terminal Voltage	Full-bridge Inverter Output Voltage	Switching Combinations			
Δ	$u_{op}(k)$	i_f	v_{pn}	v_{inv}	S1	S3	S5	S6
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) > 0$	$i_f \geq 0$	$+v_n$	$+v_n$	1	0	1	0
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) > 0$	$i_f < 0$	$+v_p$	$+v_p$	1	0	0	1
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) < 0$	$i_f \geq 0$	$+v_p$	$-v_p$	0	1	0	1
$\Delta > V_{dc}/3+\delta$	$u_{op}(k) < 0$	$i_f < 0$	$+v_n$	$-v_n$	0	1	1	0
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) > 0$	$i_f \geq 0$	$+v_p$	$+v_p$	1	0	0	1
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) > 0$	$i_f < 0$	$+v_n$	$+v_n$	1	0	1	0
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) < 0$	$i_f \geq 0$	$+v_n$	$-v_n$	0	1	1	0
$\Delta < V_{dc}/3-\delta$	$u_{op}(k) < 0$	$i_f < 0$	$+v_p$	$-v_p$	0	1	0	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 1$		$+V_{dc}$	$+V_{dc}$	1	0	0	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -1$		$+V_{dc}$	$-V_{dc}$	0	1	0	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 2/3$		$+v_p$	$+v_p$	1	0	0	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -2/3$		$+v_p$	$-v_p$	0	1	0	1
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = 1/3$		$+v_n$	$+v_n$	1	0	1	0
$V_{dc}/3-\delta \leq \Delta \leq V_{dc}/3+\delta$	$u_{op}(k) = -1/3$		$+v_n$	$-v_n$	0	1	1	0
	$u_{op}(k) = 0$		$+V_{dc}$	0	1	1	0	0

TABLE 5. System parameters.

Source nominal frequency and voltage	$v_s = 110$ V; $f_s = 50$ Hz
DC-link voltage	$V_{dc} = 170$ V
Nonlinear load (Fig. 8)	$R_1 = 20\ \Omega$; $L_1 = 6.5$ mH; $R_2 = 20\ \Omega$; $C_1 = 3900\ \mu$F;
Inductor	$L_f = 2.5$ mH
Series capacitor	$C_f = 30\ \mu$F
DC-link capacitor	$C_{dc1} = 2200\ \mu$F; $C_{dc2} = 2200\ \mu$F;
Sampling time	$T_s = 150\ \mu$s
Predict horizon and control horizon	$N_p = 3$; $N_c = 1$
Threshold	$\delta = 10$ V

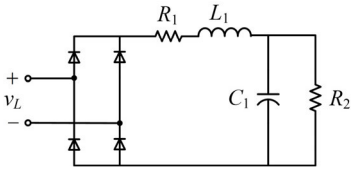

FIGURE 7. Configuration of nonlinear load.

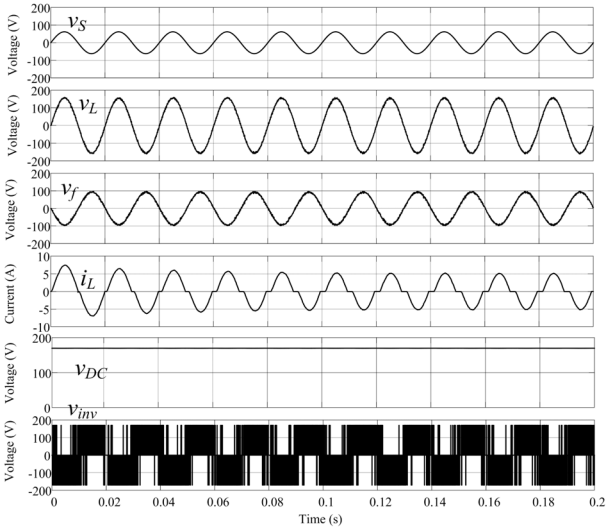

FIGURE 8. Simulation results of conventional two-level inverter based DVR under $T_s = 50\ \mu$s: source voltage v_S, load voltage v_L, compensation voltage v_f, load current i_L, DC link voltage v_{DC} and inverter output voltage v_{inv}.

IV. SIMULATION RESULTS

In order to verify the proposed S4L inverter based DVR, the simulation study is conducted based on the MATLAB/SIMULINK platform. The system parameters are summarized in Table 5. The rated voltage magnitude in this system is 110 V. The DVR is operating under the nonlinear load condition. A *RLC* load is connected via a diode bridge rectifier to form the nonlinear load as illustrated in Fig. 7. The source is operated under a 60% deep sag condition.

The simulation results of the two-level inverter, three-level inverter and S4L inverter based DVRs are illustrated in Figs. 8-10, respectively. THD values of the load voltage are analyzed in Fig. 11 and summarized in Table 6. It is noted the three types of DVRs can restore v_L to the rated magnitude. However, compared with the two-level inverter and three-level inverter DVRs, the S4L inverter based DVR provides voltages v_L with less distortion. The THD of v_L in the S4L inverter based DVR is 4.15%, which are lower than those in the other two DVRs. It is obvious that with reduced number of components, the proposed S4L inverter based DVR can further reduce the THDs in the system. In Fig. 10, the reference points of v_p and v_n are 113 V and 57 V, respectively. It is noted that v_p and v_n are maintained within the predefined threshold. In Fig. 10, it can be observed that v_{inv} has four voltage levels in the proposed DVR. The normalized values respected to V_{dc} are 1, 2/3, 1/3 and 0, respectively. The symmetrical negative parts are -1, $-2/3$, $-1/3$ and 0.

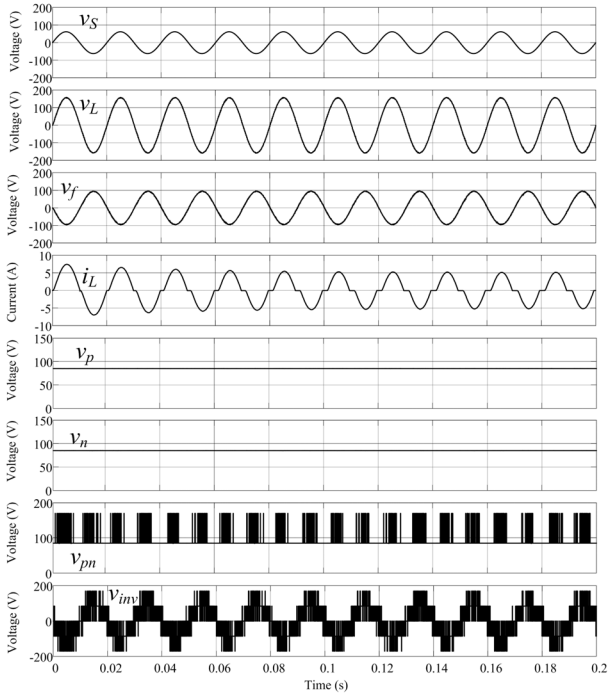

FIGURE 9. Simulation results of three-level inverter based DVR under $T_s = 50\ \mu s$: source voltage v_S, load voltage v_L, compensation voltage v_f, load current i_L, upper arm voltage v_p, terminal voltage v_{pn} and inverter output voltage v_{inv}.

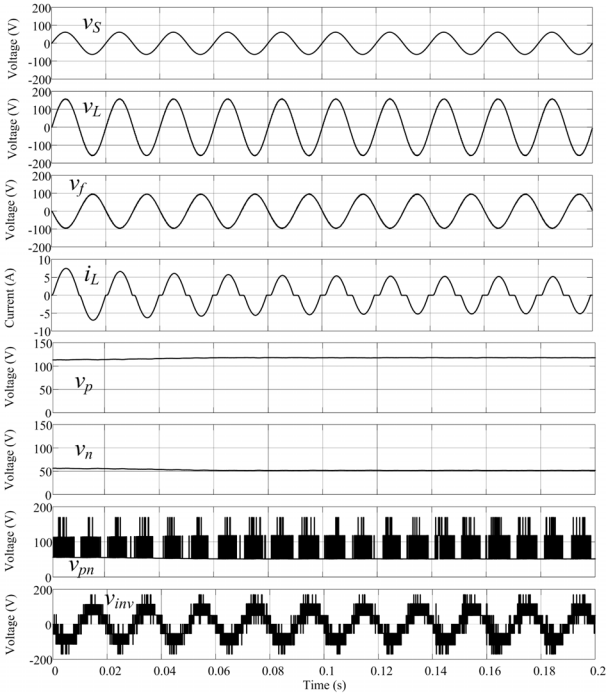

FIGURE 10. Simulation results of S4L inverter based DVR under $T_s = 50\ \mu s$: source voltage v_S, load voltage v_L, compensation voltage v_f, load current i_L, upper arm voltage v_p, terminal voltage v_{pn} and inverter output voltage v_{inv}.

TABLE 6. Voltage THD values from the simulation results.

DVR type	THD (%)
	v_L
Two-level inverter	2.69
Three-level inverter	1.43
S4L inverter	1.03

V. EXPERIMENTAL RESULTS

A laboratory prototype of the four-level inverter based DVR has been built to verify the system performance as shown in Fig. 12. The parameters of the system are the same with those in the simulation study as shown in Table 5. In the experimental study, the sampling time is reduced to 50 μs. The AC voltage supply is programmed to provide a 60% voltage sag with $v_{S,rms} = 44$ V. The DC link of the DVR is supported by a Chroma 62012P-600-8 programmable DC power supply. The experimental results are presented in Figs. 13-15. Experimental results from the conventional two-level and three-level inverter based DVRs are also presented for comparison.

Figs. 13-15 show the experimental results of the conventional two-level inverter, the three-level inverter and the proposed S4L inverter based DVRs under $T_s = 50\ \mu s$, respectively. The THD values of the load voltage in the experiment are analyzed in Fig. 16 and summarized in Table 7. In Figs. 13-15, it can be observed that the aforementioned three DVRs can restore the load voltage to the rated magnitude under the deep sag condition. In Fig. 13(c), it is noted

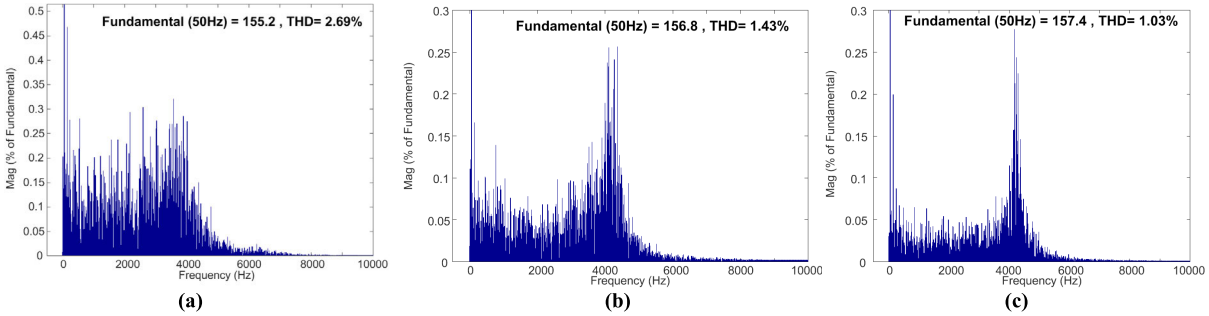

FIGURE 11. THD values in simulation results: (a) two-level inverter based DVR, (b) three-level inverter based DVR and (c) S4L inverter based DVR.

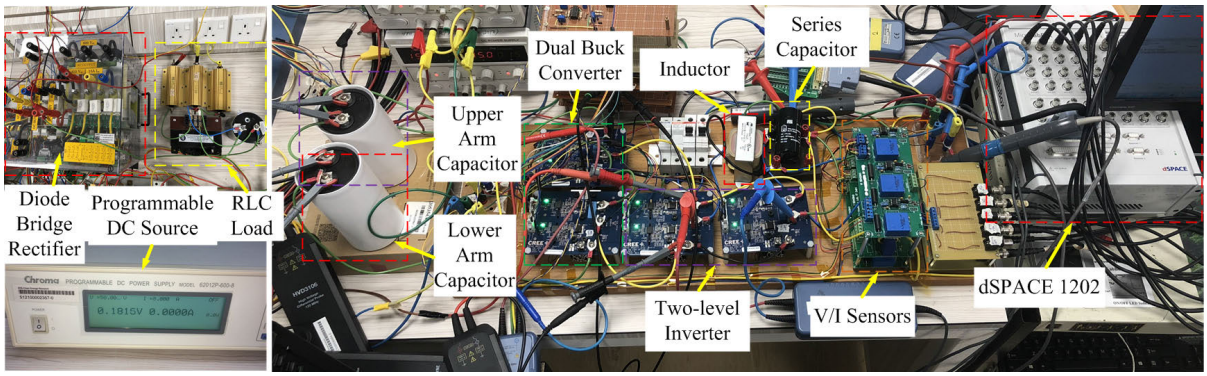

FIGURE 12. Laboratory prototype of the S4L inverter based DVR.

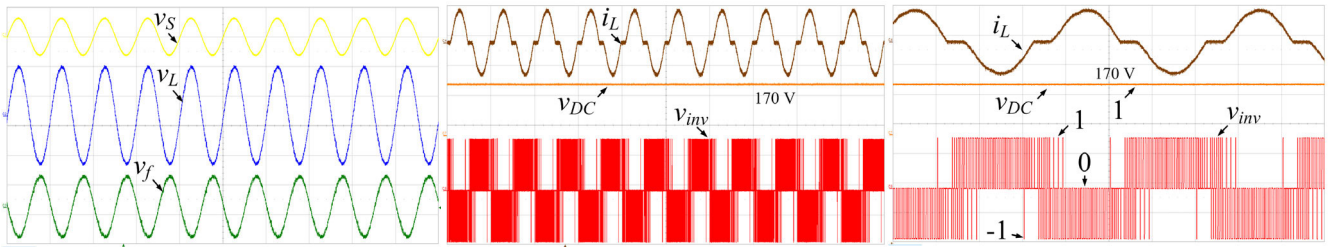

FIGURE 13. Experimental results of conventional two-level inverter based DVR under $T_s = 50\ \mu s$ (a) Time (20 ms/div), v_S (100 V/div), v_L (100 V/div), v_f (100 V/div); (b) time (20 ms/div), i_L (5 A/div), v_{DC} (100 V/div), v_{inv} (100 V/div); and (c) time (5 ms/div), i_L (5 A/div), v_{DC} (100 V/div), v_{inv} (100 V/div).

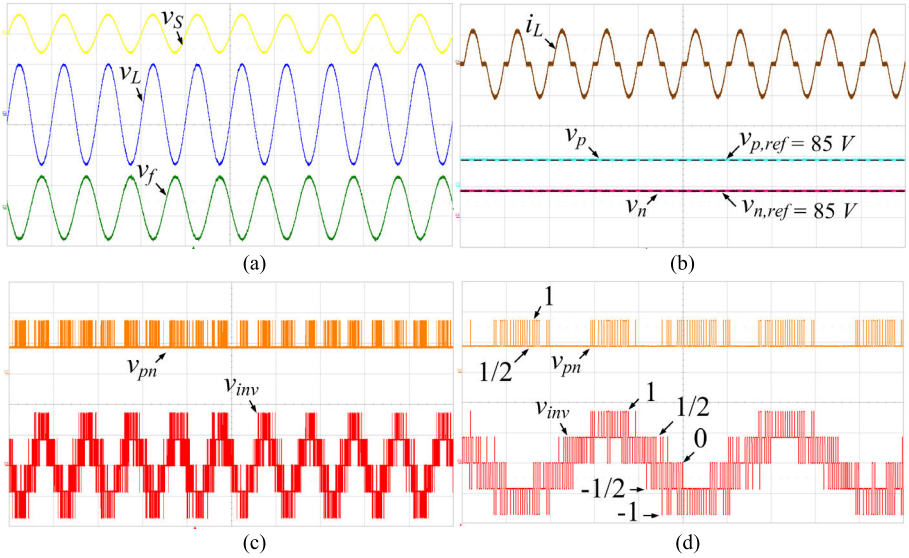

FIGURE 14. Experimental results of three-level inverter based DVR under $T_s = 50\ \mu s$ (a) Time (20 ms/div), v_S (100 V/div), v_L (100 V/div), v_f (100 V/div); (b) time (20 ms/div), i_L (5 A/div), v_p (100 V/div), v_n (100 V/div); (c) time (20 ms/div), v_{pn} (100 V/div), v_{inv} (100 V/div); and (d) time (5 ms/div), v_{pn} (100 V/div), v_{inv} (100 V/div).

the inverter output voltage is (1, 0, −1) for the two-level inverter. In Fig. 14(b), for the three-level inverter based DVR the reference points of v_p and v_n are 85 V, respectively. v_p and v_n are maintained at the reference values. In Fig. 14(d), the inverter output voltage is (1, 1/2, 0, −1/2, −1) for the three-level inverter. In Fig. 15(b), the reference points of v_p and v_n are 113 V and 57 V, respectively. v_p and v_n are maintained within the predefined threshold. In Fig. 15(d), the output voltage (1, 2/3, 1/3, 0, −1/3, −2/3, −1) can also be observed in the proposed S4L inverter. Compared with

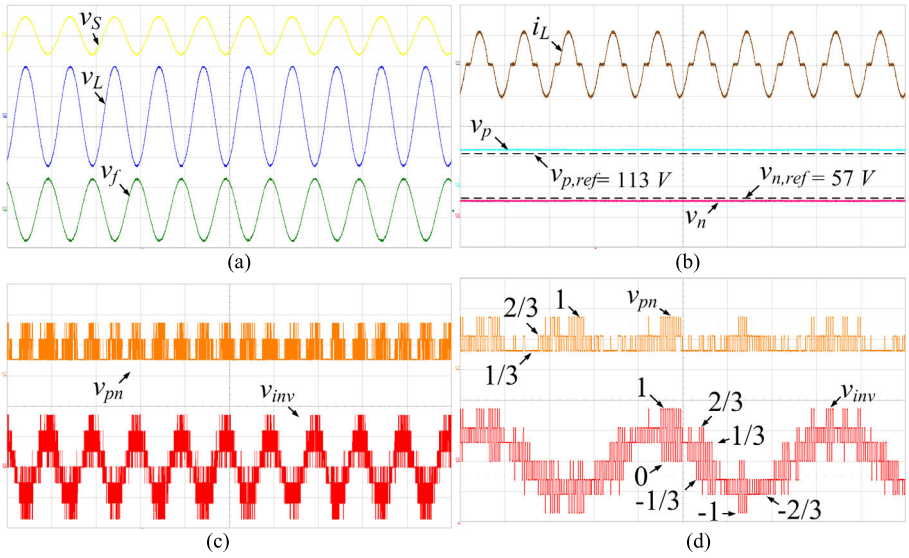

FIGURE 15. Experimental results of S4L inverter based DVR under $T_s = 50\ \mu s$ (a) Time (20 ms/div), v_S (100 V/div), v_L (100 V/div), v_f (100 V/div); (b) time (20 ms/div), i_L (5 A/div)0, v_p (100 V/div), v_n (100 V/div); (c) time (20 ms/div), v_{pn} (100 V/div), v_{inv} (100 V/div); and (d) time (5 ms/div), v_{pn} (100 V/div), v_{inv} (100 V/div).

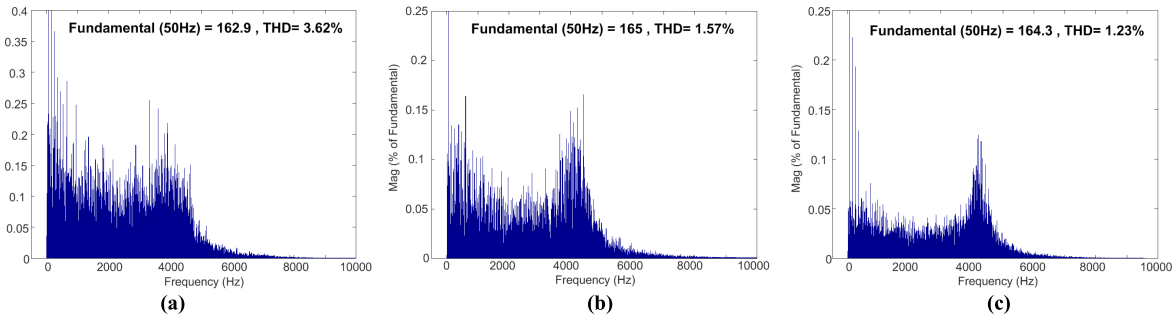

FIGURE 16. THD values in experimental results: (a) two-level inverter based DVR, (b) three-level inverter based DVR and (c) S4L inverter based DVR.

TABLE 7. Voltage THD values from the experimental results.

DVR type	THD (%)
	v_L
Two-level inverter	3.62
Three-level inverter	1.57
S4L inverter	1.23

the conventional DVRs, THD of v_L in the S4L inverter based DVR is the lowest, which is 1.23%.

It has to be mentioned that the proposed S4L inverter based DVR requires less components compared with the NPC and CHB three-level inverters based DVRs as compared in Table 1. From the simulation and experimental results, it is noted that the proposed S4L inverter based DVR can provide a better performance compared with the three-level inverter based DVR in terms of the THD value of the load voltage.

VI. DISCUSSION

The conventional two-level inverter, three-level inverter and proposed S4L inverter based DVRs are compared in this paper. From the simulation and experimental results, it is noted that the load voltage contains more harmonics in the two-level inverter based DVR system. The reason is that the two-level inverter can only provide zero and full DC voltages. In the three-level inverter based DVR system, the load voltage harmonics are reduced, as the three-level inverter outputs zero, full and half DC voltages. Compared with the two-level inverter, the three-level inverter can better mimic a sinusoidal voltage waveform. Thus, in the proposed S4L inverter based DVR system, the S4L inverter outputs zero, full, two thirds and one third of DC voltages. This is why the load voltage harmonics in the S4L inverter based DVR system are the lowest.

VII. CONCLUSION

This paper has proposed a S4L inverter based single-phase DVR that obtains better performance compared to those of the conventional two-level inverter and three-level inverter based DVRs. The discrete-time model of the DVR has been derived using the equivalent circuit of the system. By applying the

discrete-time model, a MPC based method has been used to control the DVR. Furthermore, a voltage regulation algorithm is utilized to keep the upper and lower arm DC voltages at the desired values. The S4L inverter based DVR can generate high quality voltages with reduced THD values. As the S4L inverter based DVR can reduce the number of components compared with the existing multilevel inverters based DVRs, it is a more cost-effective voltage compensation device.

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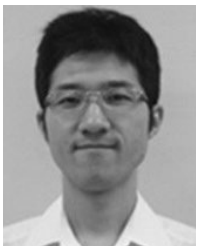

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