

Received August 31, 2019, accepted September 11, 2019, date of publication September 13, 2019, date of current version September 27, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2941375

Modified Modulation Strategy With Balanced Power and Switching Losses Distributed for Seven-Level Cascaded H-Bridge Inverters

MANYUAN YE^{ID}, JUNFEI ZHANG, LE CHEN, LIXUAN KANG, HAN WU, AND SONG LI

College of Electrical and Automation Engineering, East China Jiaotong University, Nanchang 330013, China

Corresponding author: Manyuan Ye (yemanyuan1@163.com)

This work was supported in part by the National Natural Science Foundation of China under Grant 51767007, in part by the Jiangxi Provincial Industrial Science and Technology Support Project under Grant 20192BBEL50011, in part by the Jiangxi Natural Science Foundation Project under Grant 20192BAB206036, and in part by the Natural Science Foundation of Jiangxi Provincial Department of Education under Grant GJJ180306.

ABSTRACT In this paper, the problems existing in common modulation methods are analyzed, and an optimized modulation strategy is proposed. Firstly, the single-pole frequency doubling modulation technique is adopted to reduce the maximum switching frequency to 1/2 of the original switching frequency, and the equivalent switching frequency of inverters remain constant. On this basis, the trigger signal of each unit is rotated in units of 1/4 cycle, so the output power of each cell is balanced after 3/4 cycles. The method is simple in control, and the Total Harmonic Distortion (THD) of line voltage is better than the carrier phase shift technique. The working stress of all the unit switching tubes is the same, the heat dissipation distribution is uniform, the switching loss is effectively reduced, and the service life and system reliability are improved. Finally, simulation and experimental results verify the correctness and feasibility of the optimized modulation strategy.

INDEX TERMS Optimized modulation strategy, balanced, working stress, switching loss.

I. INTRODUCTION

The Multi-level inverters have drawn increasing attention in high voltage high power applications due to their advantages of reducing the harmonic component and the voltage stress on the power devices, when compared with two-level converters [1]–[5]. The most common multilevel inverters can be mainly divided into neutral-point clamped(NPC) Multi-level inverters, flying capacitor(FC) Multi-level inverters, and cascaded H-bridges(CHB) Multi-level inverters. Among which the CHB Multi-level inverters has the advantages of simple structure, phase voltage redundancy, high reliability, being easy to modular design and manufacture, compared to other multilevel inverters, it does not required any clamping diodes and flying capacitors, so it has been used in various application, such as photovoltaic (PV) [6], electric vehicle [7], flexible alternating current transmission systems (FACTS) [8], static synchronous compensator (STATCOM) [9].

The associate editor coordinating the review of this manuscript and approving it for publication was Zhouyang Ren.

Modulation strategy is the key technique for CHB-MLI, which do direct influence on the performance of inverter such as output waveform quality, system reliability, service life and efficiency. Various modulation strategies have been proposed for the CHB-MLI, the most common one are selective harmonic elimination pulse width modulation (SHEPWM) [10], Space Vector pulse width modulation (SVM-PWM) [11] and Multi-carrier pulse width modulation (Multi-carrier PWM) [12]. SHEPWM have the advantage of less switching loss, but it is often necessary to calculate a set of complex non-linear equations, resulting in slow dynamic response. SVM-PWM is one of the promising high frequency modulation methods, it have good performance at low modulation ratio and suitable for digital signal processing (DSP) implementation, however, as the number of levels increases, the amount of calculation increases, and is generally only applicable to multi-level inverters below five levels. For Multi-carrier PWM, Phase-shifted pulse width modulation (PS-PWM) [13] and level-shifted PWM (LS-PWM) are the most popular schemes [14]. The THD of line voltage of the PD-LS-PWM is the best [15], however, it has the problem that the output

power of each H-bridge units is not balanced [16], it is necessary to optimize and improve In-Phase Displacement PWM (IPD-PWM) technique, and the switching frequency distribution of each switching device is not uniform [17].

The literature [17], [19] proposes a strategy of cyclically moving the sinusoidal modulation wave in different carrier regions, which achieves the output power balance between different cells and improves harmonic performance. However, the strategy is only for applications where the modulation index M is less than 0.5. The literature [16], [18] proposes a power balance control method of alternating changing the position for corresponding carrier of two cells on the time axis, which realizes the output power balance between cascade H-bridge cells within one cycle. However, alternating changing carrier will additionally add the switch times of the switching tubes, resulting in the increase in switching losses. The literature [20] proposes a modified staircase wave modulation strategy. This strategy does not need to recalculate the switching angle, only needs to adjust the switching angle of traditional staircase wave modulation. However, there is an H-bridge cell that does not work at low modulation index, and the output power of each cell can only be roughly balanced at high modulation index. Moreover, staircase wave modulation is just applicable to situation with low-frequency modulation and less cascaded cells. The literature [21] proposes a hybrid multi-carrier PWM strategy, which can achieve output power balance naturally between different cells. when this strategy is applied to CHB Seven-level inverters, the THD of line voltage u_{AB} is the same as IPD-PWM strategy at modulation index $M \in [0,0.35]$, but at modulation index $M \in [0.35,0.9]$, the THD of line voltage u_{AB} is higher or equal to CPS-PWM strategy.

In this paper, the PD modulation strategy is optimized by the single-pole frequency doubling technique, so that the maximum switching frequency of the switching tube is reduced to 1/2 of the original, thereby reducing the switching loss. On this basis, the trigger pulse signals of each unit are rotated in units of 1/4 cycle, and the power balance of each unit is realized after 3/4 cycles. The method not only realizes the time required for power balance, but also has the same working stress of all the switching tubes of each unit, and the heat distribution is uniform, which effectively improves the service life and reliability of the system.

II. TOPOLOGICAL ANALYSIS

The topology structure of H-bridge cascaded seven-level inverters is shown in Fig.1. It composed by a series connection of three H-bridge cells, each H-bridge unit is powered by a separate DC power supply. Assuming that the input voltages of the three H-bridge cells are $V_{dc1} = V_{dc2} = V_{dc3} = E$, the corresponding output voltages of each cell are v_{H1}, v_{H2}, v_{H3} . The generated output voltage of each cell composed of three voltage levels $+E, -E$ and 0 by a different combination of the four switches. The total output voltage v_{AN} of the inverter is as follows:

$$v_{AN} = v_{H1} + v_{H2} + v_{H3} \quad (1)$$

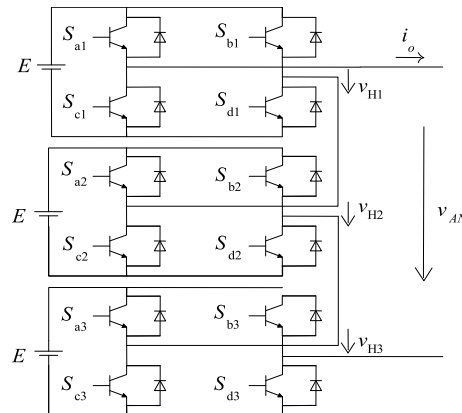


FIGURE 1. The topology of 3-cell CHB inverter r.

As shown in Fig.1, each single bridge gives three level as an output, if n cells are connected in series then the output voltage level is $2n+1$.

Defining the switch state function S_{ij} of each cell is

$$S_{ij} = \begin{cases} 1 & \text{Upper switch conduction} \\ 0 & \text{Lower switch conduction} \end{cases} \quad i = 1, 2, 3; j = 1, 2; \quad (2)$$

In the Equations (2), i denotes the i th cascade unit and j denotes the j th switching device in the i th unit.

Then the output levels of the different switching state functions of the connected units are

$$v_{Hi} = \begin{cases} E, & S_{i1}S_{i2} = 10 \\ 0, & S_{i1}S_{i2} = 00 \text{ or } 11 \\ -E, & S_{i1}S_{i2} = 01 \end{cases} \quad (3)$$

Table 1 shows the output voltage of the inverter under different output functions. It can be seen from the table that the phase voltage v_{AN} of the three-element CHB inverter can have a total of seven levels of $\pm 3E, \pm 2E, \pm E$ and 0. In order to avoid energy circulation, the output states of the opposite polarity of the output voltage of each unit are removed in Table 1. It can be seen from the table that when the output levels of the phase voltage v_{AN} are $\pm 2E, \pm E$ and 0, each unit has a redundant output state function.

III. PD-LS-PWM-ANALYSE

In the PD-LS-PWM, N -level CHB inverters need a total of $N-1$ triangular carriers. For seven-level CHB inverter, six triangular carriers (v_{c1} to v_{c6}) are required. The modulation principle of PD-LS-PWM is shown in Figure 2. Each carrier is vertically disposed with the same frequency and phase. Each pair of triangular carriers corresponding to each H-bridge unit is spatially symmetrically distributed on both sides of the X-axis. v_{ref} is a sinusoidal modulated wave, and its expression Formula

$$V_{ref} = 3M \sin \omega t \quad (4)$$

M is the modulation index.

TABLE 1. The output corresponding to different output state functions.

$S_1S_2S_3$	v_{H1}	V_{H2}	V_{H3}	v_{AN}
111	E	E	E	3E
110	E	E	0	
101	E	0	E	2E
011	0	E	E	
100	E	0	0	
010	0	E	0	E
001	0	0	E	
000	0	0	0	0
-100	-E	0	0	
0-10	0	-E	0	-E
00-1	0	0	-E	
-1-10	-E	-E	0	
-10-1	-E	0	-E	-2E
0-1-1	0	-E	-E	
-1-1-1	-E	-E	-E	-3E

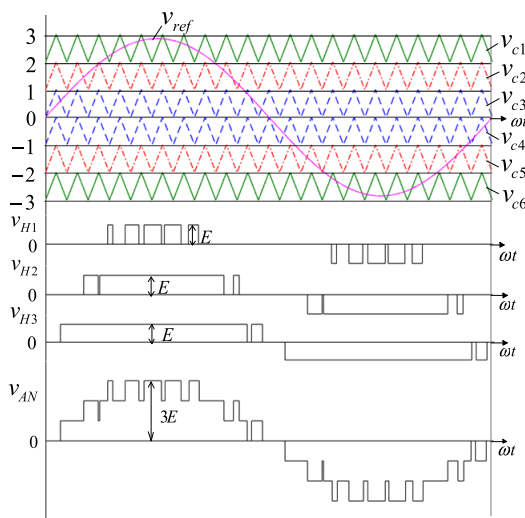


FIGURE 2. The principle of traditional PD modulation.

In the PD modulation method, the switching frequency can be divided into the maximum switching frequency and the average switching frequency. The maximum switching

frequency is equal to the carrier frequency, and the average switching frequency is calculated according to each period can be defined as

$$f_a = pf_m \tag{5}$$

where f_a is the average switching frequency, f_m is the modulation wave frequency, and p is the number of pulses generated by the switching tube in one cycle. The average switching frequency of the carrier Phase-shifted pulse width modulation (CPS-PWM) is the same as the maximum switching frequency, which is equal to the carrier frequency. For the PD modulation method, the average switching frequency is not the same as the maximum switching frequency. For example, in the PD modulation method shown in Fig. 2, the carrier frequency is 1050 Hz, the modulation wave frequency is 50 Hz, and the number of pulses generated by the cells 1, 2, and 3 in each cycle is 5, 3, and 2, respectively. The average switching frequency of each cycle of the cells 1, 2, and 3 is 250HZ, 150HZ, and 100HZ, respectively, and the maximum switching frequency is 1050HZ. Therefore, there is a significant difference in the average switching frequency of each unit in PD-LS-PWM. As the carrier frequency increases, the difference will become more significant.

The output power of each cell of the CHB inverter under PD modulation is proportional to the amplitude of the fundamental voltage of the output voltage [22]. When the modulation index is M , the amplitude of the fundamental voltage of the inverter phase output voltage is

$$v_{AN} = 3ME \tag{6}$$

According to the double Fourier analysis [23], the relationship between the output voltage of the cell 1, cell 2, and cell 3 and the amplitude of the fundamental wave is

$$v_{H1} = \begin{cases} 0, & M \in [0, 2/3] \\ 3ME[1 - \frac{2}{\pi} \arcsin \frac{2}{3M} - \frac{4}{\pi} \frac{\sqrt{9M^2 - 1}}{9M^2}], & M \in [2/3, 1] \end{cases} \tag{7}$$

$$v_{H2} = \begin{cases} 0, & M \in [0, 1/3] \\ 3ME[1 - \frac{2}{\pi} \arcsin \frac{1}{3M} - \frac{2}{\pi} \frac{\sqrt{9M^2 - 1}}{9M^2}], & M \in [1/3, 2/3] \\ ME[\frac{1}{\pi}(\frac{4\sqrt{9M^2 - 4}}{9M^2} - \frac{2\sqrt{9M^2 - 1}}{9M^2})] + \frac{2}{\pi}(\arcsin \frac{2}{3M} - \arcsin \frac{1}{3M}), & M \in [2/3, 1] \end{cases} \tag{8}$$

$$v_{H3} = \begin{cases} 0, & M \in [0, 1/3] \\ 3ME[1 - \frac{2}{\pi} \arcsin \frac{1}{3M} - \frac{2}{\pi} \frac{\sqrt{9M^2 - 1}}{9M^2}], & M \in [1/3, 1] \end{cases} \tag{9}$$

Figure 3 shows the Relationship curves between fundamental amplitude and modulation ratio M under PD-LS-PWM strategy. It can be seen from the figure that

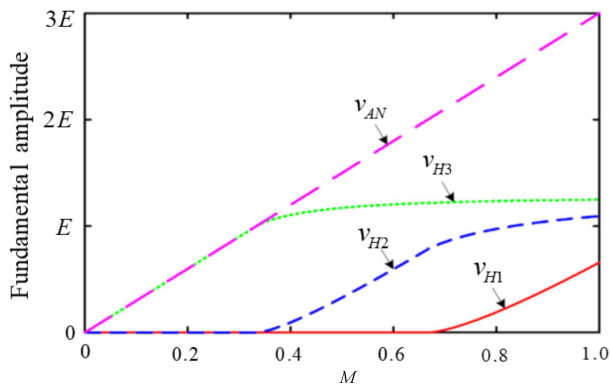


FIGURE 3. Function curve between fundamental amplitude and modulation depth of output voltage.

the amplitude of the fundamental voltage component of the output voltage of each cell is not equal under any modulation ratio. Therefore, under the traditional PD modulation strategy, there is a serious power imbalance between cascaded cells.

In view of the above analysis, although the output voltage waveform of the PD modulation method has good harmonic characteristics, the different switching frequencies of the switches in each unit will lead to uneven distribution of switching loss and heat in each unit, which will affect the service life and reliability of the system. At the same time, the unbalanced output power of each unit will also lead to the problems of inconsistent utilization of DC power and unbalanced charging and discharging of the inverters. Aiming at these problems, it is significant to optimize the traditional PD modulation strategy.

IV. OPTIMAL MODULATION STRATEGY

A. TWO COMMON POWER BALANCED METHODS

Aiming at the defects of PD-LS-PWM, the literature [24], [25] proposes a power balance method respectively. The literature [24] proposes a power balance method of By rotating each unit in 1/4 cycle. The modulation principle of literature [24] is shown in Figure 4 (a), A pair of carriers correspond to a H-bridge unit(such as v_{c1+} and v_{c1-} correspond to H1), a total of six carriers are required. This method takes 1/4 cycle as the basic unit, and strictly moves the carrier once every 1/4 cycle in the vertical direction region, and completes a carrier circulation cycle after moving 5 times, At this time, the carrier circulation cycle is equal to 3/2 cycles. This method makes use of the redundancy characteristics of output voltage of each cascaded unit. By rotating each unit in 1/4 cycle, the cyclic movement of the output voltage pulse is realized, the output voltage characteristic of each cascaded unit is changed, and the power imbalance caused by the spatial dimension is compensated by the time dimension, power balance control is realized in 3/2 cycles, as shown in Fig. 4(b). When the triangular carrier frequency is 2kHz, the equivalent switching frequency of inverter is also 2kHz,

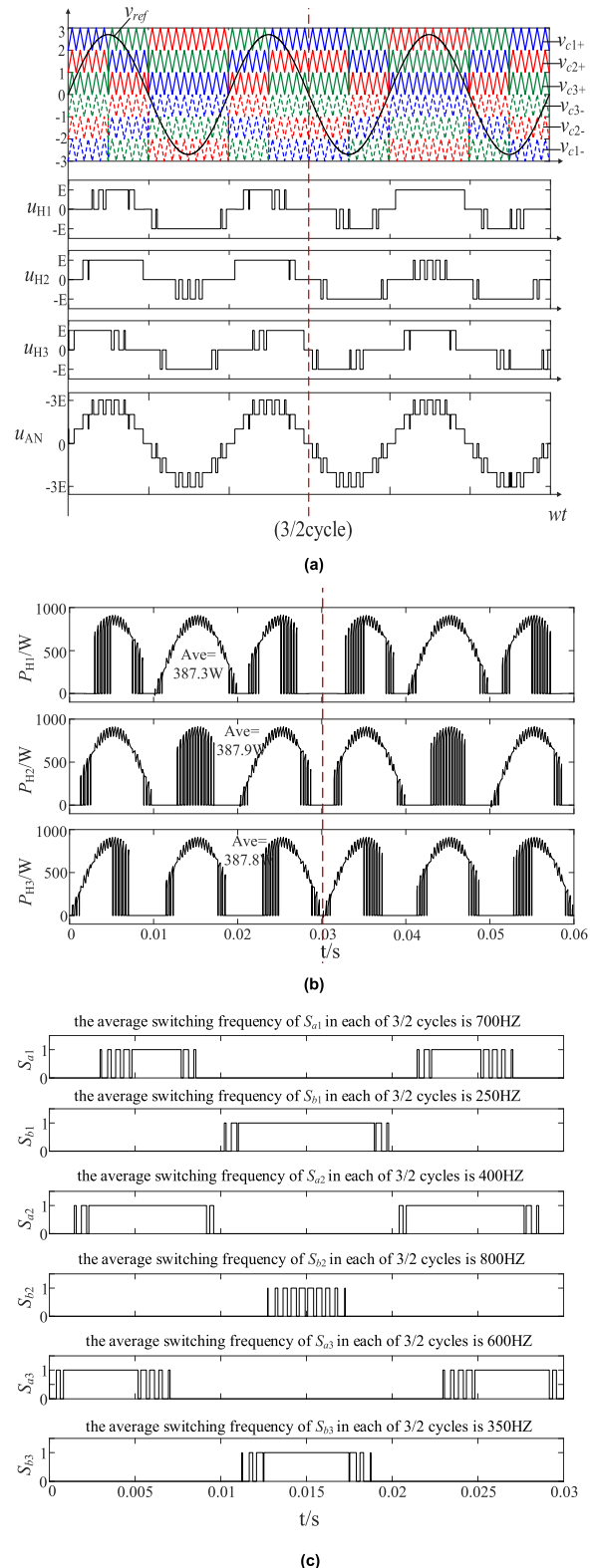


FIGURE 4. The strategy proposed in literature [24] (a) with the modulation principle diagram of literature [24] (b) with output Power of each Unit (c) with driving signal of the switching tube.

driving signal of all switching tubes in 3/2 cycle is shown in Fig.4(c) . According to the definition of average switching frequency in Equation (5), the average switching frequency of

all switching tubes in 3/2 cycles can be calculated. Obviously, it can be seen from Fig.4 (c) the average switching frequency of all switching tubes in each of 3/2 cycles is different, so switching loss is distributed unbalanced.

The literature [25] proposes a kind of carrier recycle power balance control method subject to output period as the basic unit, which has realized output power balance between different cells after 3 cycles. The modulation principle is shown in Figure 5(a), which moves the carrier once each 1 cycle in the vertical direction region, and completes a carrier circulation cycle after moving 5 times, the carrier circulation cycle is equal to 6 cycles. The power balance control is realized in 3 cycles, as shown in Fig. 5(b). When equivalent switching frequency of inverter is 2KHz, driving signal of all switching tubes in 3 cycle is shown in Fig 5(c). Obviously, the average switching frequency of all switching tubes in each of 3 cycles is different, so switching loss is distributed unbalanced. And it takes a long time for power balance when the number of cascaded units is large, so it has certain advantages in applications where the number of cascade units is small.

B. MODIFIED MODULATION METHOD

Aiming at the defects of PD-LS-PWM and other power balance control methods, an optimal modulation control method is proposed in this paper. Firstly, the modulated wave is adjusted. Assuming that the amplitude of triangular carrier of PD modulation method is 1, the modulated wave v_m can be expressed as

$$V_m = \begin{cases} V_{ref} - 2 & 2 < V_{ref} < 3, \\ V_{ref} - 1 & 1 < V_{ref} < 2, \\ V_{ref} & -1 < V_{ref} < 1, \\ V_{ref} + 1 & -2 < V_{ref} < -1, \\ V_{ref} + 2 & -3 < V_{ref} < -2, \end{cases} \quad (10)$$

The adjustment principle is shown in Figure 6. Since the optimized modulation method using unipolar frequency doubling modulation technology, the number of triangular carriers is changed from the original six to one while the modulation wave is adjusted. The new triangular carrier v_c amplitude is 2, and the maximum switching frequency is 1/2 of the original switching frequency.

Figure 7 shows the preliminary optimized modulation strategy. When the modulation wave $v_m > v_c$, S_{a1} turned on, when $-v_m > v_c$, S_{b1} turned on, otherwise turned off; When the initial modulated wave $v_{ref} > 2$, S_{a2} turned on, when $v_{ref} < 2$, S_{b2} turned on, otherwise turned off; when $v_{ref} > 1$, S_{a3} turned on, when $v_{ref} < 1$, S_{b3} turned on, otherwise turned off, The upper and lower switches of each bridge arm are complementary.

It can be seen from Fig.7 that the output voltage waveform of the inverter before and after the optimized modulation is basically the same as that of Fig.2, so the equivalent switching frequency of the inverter remains unchanged. The maximum operating frequency of the switch tube is reduced to 1/2 due to the carrier frequency is reduced to 1/2. Compared with the

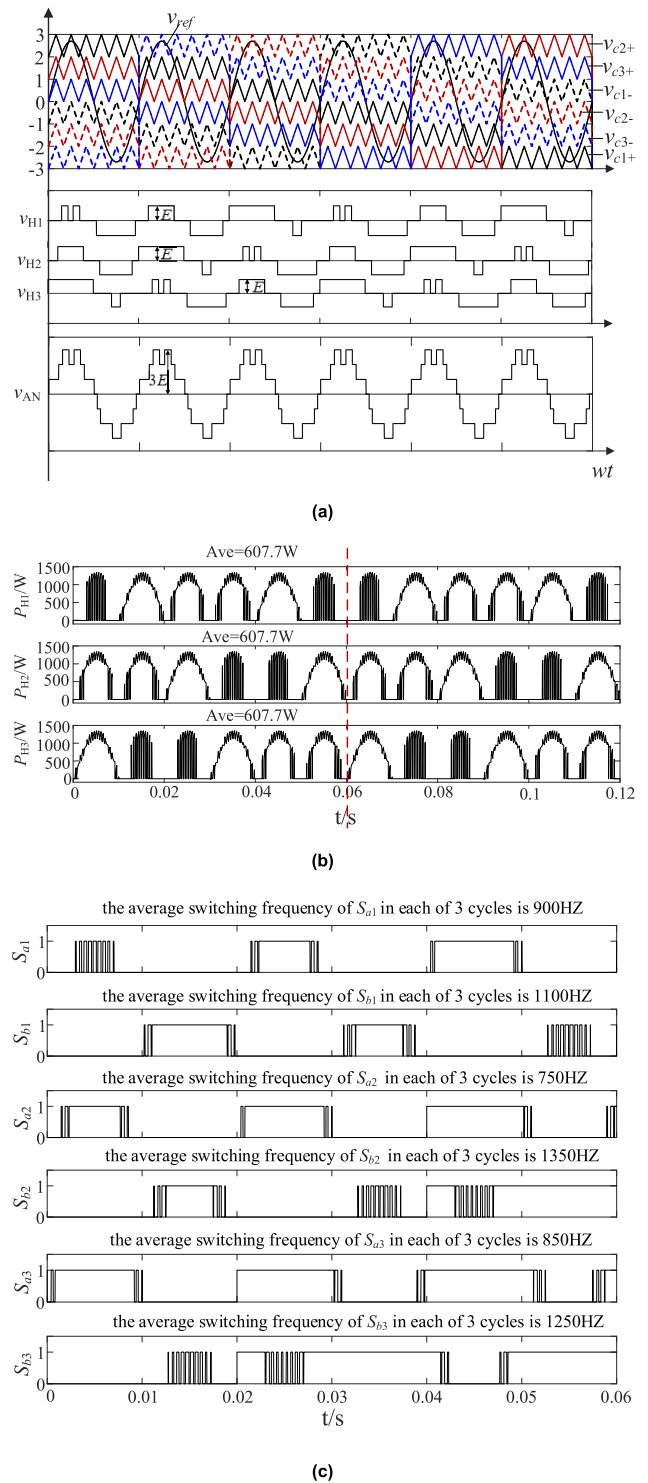


FIGURE 5. The strategy proposed in literature [25] (a) with The modulation principle diagram of literature [25] (b) with output Power of each Unit (c) with Driving signal of the switching tube.

PD-LS-PWM, the preliminary optimized modulation method only needs one triangular carrier and two modulated waves to realize the seven-level phase voltage output, which reduces the number of triangular carriers and simplifies the control

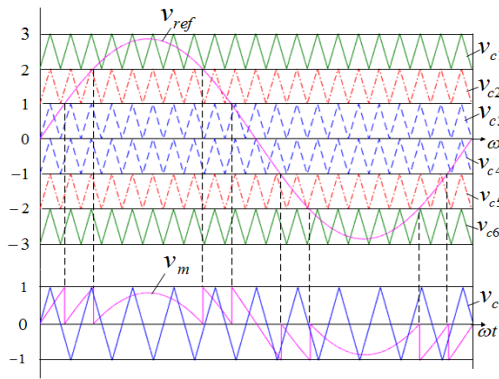


FIGURE 6. The Principle of modulation wave adjustment.

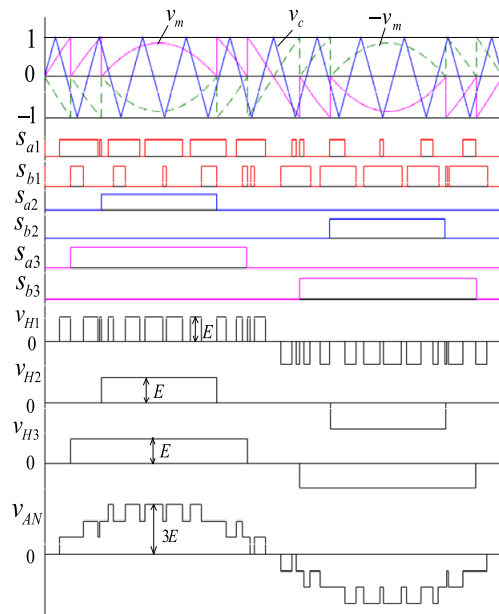


FIGURE 7. principle of the preliminary optimized modulation.

complexity. However, it still has the problems of uneven distribution of switching losses and output power of each cell. In order to balance the switching frequency and output power of each cell, a power equalization control method based on 1/4 cycle pulse signal rotation is proposed on the basis of one-time optimal modulation strategy. Its modulation principle is shown in Fig. 8.

In Fig.8, each output cycle is divided into four regions in units of 1/4 cycle, and each region is cyclically modulated by three different modulation modes, and the three modulation modes are respectively:

Mode a: When $v_m > v_c$, S_{a1} turned on, when $-v_m > v_c$, S_{b1} turned on, otherwise turned off; when $v_{ref} > 2$, S_{a2} turned on, and when $v_{ref} < 2$, S_{b2} turned on, otherwise turned off; when $v_{ref} > 1$, S_{a3} turned on, when $v_{ref} < 1$, S_{b3} is turned on, otherwise turned off.

Mode b: When $v_{ref} > 1$, S_{a1} is turned on, when $v_{ref} < 1$, S_{b1} is turned on, otherwise turned off; when $v_m > v_c$,

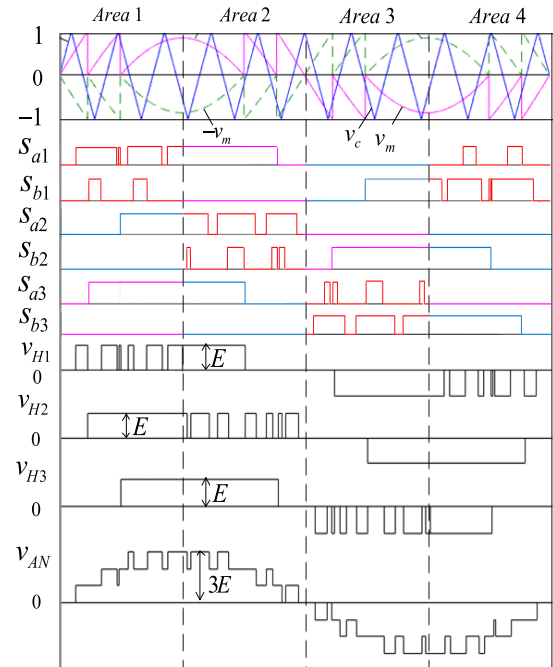


FIGURE 8. principle of the preliminary optimized modulation.

S_{a2} is turned on, when $-v_m > v_c$, S_{b2} is turned on, otherwise turned off; when the $v_{ref} > 2$, S_{a3} turned on, when $v_{ref} < 2$, S_{b3} turned on, otherwise turned off.

Mode c: When $v_{ref} > 2$, S_{a1} turned on, when $v_{ref} < 2$, S_{b1} turned on, when $v_{ref} > 1$, S_{a2} turned on, when $v_{ref} < 1$, S_{b2} turned on, otherwise turned off; when $v_m > v_c$, S_{a3} turned on, $-v_m > v_c$, S_{b3} turned on, otherwise turned off.

It can be seen from fig. 8 that the modulated wave v_m in the respective regions are symmetrical to each other, and therefore, the modulated wave v_m in different regions are symmetrical to each other, so the pulse signals and output voltage pulse widths generated in different regions will tend to be uniform. Assume that the pulse signals of the three H-bridge cells are SP1, SP2, SP3 respectively when modulation is performed by mode a, so that the pulse signals of three H-bridge cells in mode b are SP3, SP1, SP2, and the pulse signals of the H-bridge cells in mode c are SP2, SP3, SP1. When the inverter uses the pulse signals SP1, SP2, and SP3, the corresponding output voltages are EP1, EP2, and EP3, respectively, when the inverters are cyclically modulated by the inverter in the mode of a-b-c, after 3/4 cycles, each unit output voltage can be expressed as

$$\begin{cases} v_{H1} = EP1 + EP2 + EP3 \\ v_{H2} = EP3 + EP1 + EP2 \\ v_{H3} = EP2 + EP3 + EP1 \end{cases} \quad (11)$$

According to the formula (11), after 3/4 cycles, the output voltage of each unit is $v_{H1} = v_{H2} = v_{H3}$.

Therefore, the optimized pulse width modulation (OP-PWM) strategy can effectively balance the output power of different H-bridge units and the switching frequency of all

TABLE 2. Comparison of different strategies.

	Number of Carriers	Power Balance Cycle	Switching Losses Distributed	The Line Voltage v_{AB} THD (%)
The proposed OP - PWM	1	3/4 cycles	balanced	between IPD-PWM and CPS-PWM
The literature [16, 18]	6	3/2 cycles	unbalanced	the same as IPD-PWM
The literature [17, 19]	6	1 cycle	unbalanced	the same as IPD-PWM at Low Modulation index
The literature [20]	/	1 cycle	/	/
The literature [21]	6	1 cycle	balanced	more than or equal to CPS-PWM when the modulation index $M \in [0.35, 0.9]$
The literature [24]	6	3/2 cycles	unbalanced	the same as IPD-PWM
The literature [25]	6	3 cycles	unbalanced	the same as IPD-PWM

/ means no comparison

switching tubes. At the same time, the maximum switching frequency of the switching tube is reduced to 1/2, which improves the service life and reliability of the system.

Table 2 shows the comparison of different strategies, it can be seen that the main difference between the literature [16]–[25] proposed strategies and the proposed OP-PWM strategy is that the proposed OP-PWM strategy achieved the balanced distribution of output power and switching losses, and number of carriers and power balance cycle are the smallest. Although the strategy with balanced power and switching losses distribution is also presented in Literature [21], the harmonic performance of line voltage v_{AB} is poor.

V. SIMULATION ANALYSIS

In order to prove the feasibility of the optimized modulation strategy proposed in this paper, the simulation and verification are carried out on the Matlab/Simulink platform. Simulation parameters are as follows: DC side input voltage is 80V, modulation wave frequency is 50HZ, modulation ratio $M=0.85$, load $R=25$, $L=4mH$.

Fig.9a shows the pulse driving signals of the respective unit switching tubes. As can be seen from the figure, the pulse signals of the different cells switching tubes are evenly distributed. From the definition of the average switching frequency of equation (5), it can be calculated that the average switching frequency of all the switching tubes in each of 3/4 cycles is 300HZ, so the working stress of all the switching tubes is the same, indicating that the optimized modulation strategy can effectively balance all Switching loss of the switching devices.

Fig.9b shows the output voltage of inverter under optimized modulation strategy, it can be seen that the output voltage of each cells contains many different basic voltage waveforms, which are cycled every three cycles. The fundamental amplitudes of v_{H1} , v_{H2} , and v_{H3} are both 68.05V, which satisfies the conditions of output power balance of

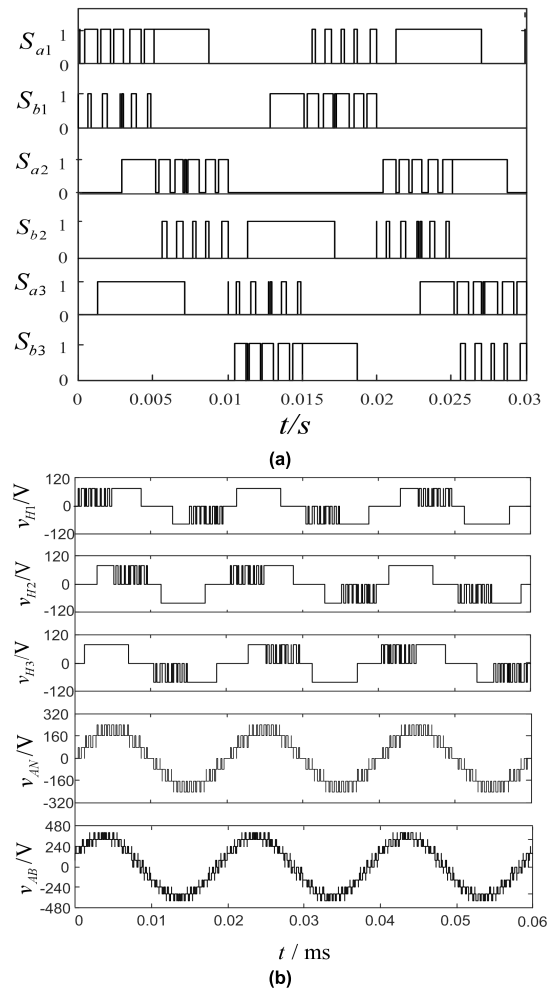


FIGURE 9. simulation result (a) with driving signal of the switching tube under OP-PWM (b) with output voltage of the inverters under OP-PWM.

each unit. The output phase voltage v_{AN} is a seven-level PWM waveform, and the line voltage v_{AB} is an eleven-level PWM waveform.

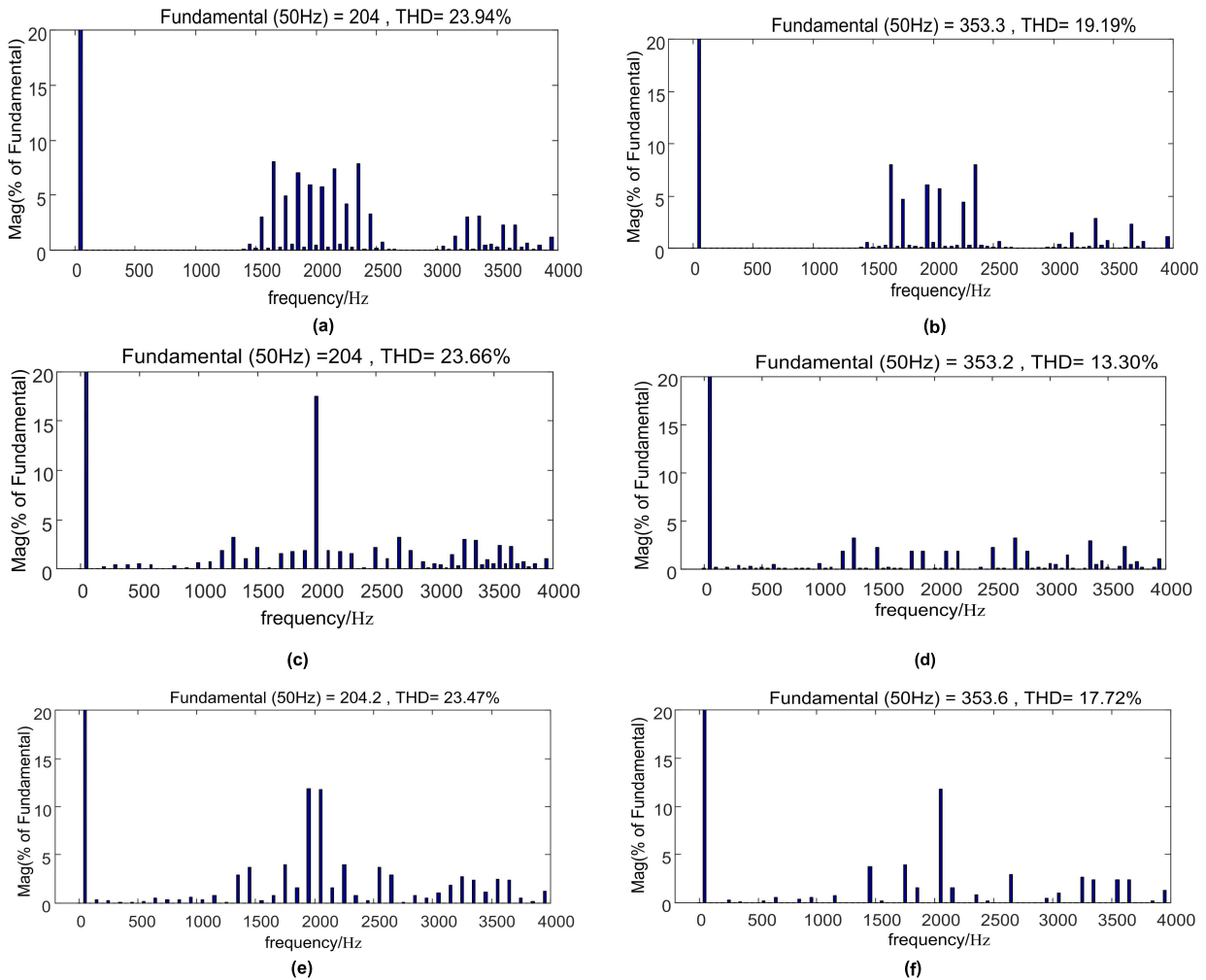


FIGURE 10. Harmonic analysis of output voltage (a) with harmonic analysis of phase voltage under PS-PWM (b) with harmonic analysis of line voltage under PS-PWM (c) with harmonic analysis of phase voltage under PD-LS-PWM (d) with harmonic analysis of line voltage under PD-LS-PWM (e) with harmonic analysis of phase voltage under OP-PWM (f) with harmonic analysis of line voltage under OP-PWM.

Figure 10 shows the harmonic analysis of the output phase voltage v_{AN} and the line voltage v_{AB} under PS-PWM, PD-LS-PWM and OPPWM. The triangular carrier frequency is 1/3kHz, 2kHz, 1kHz respectively, and the equivalent switching frequency are equal to 2kHz. It can be seen from the figure that the main harmonic content of the phase voltages of the three strategies is concentrated around 2 kHz. The phase voltage fundamental amplitude of the PS-PWM modulation method is 204V, the THD is 23.94%, the line voltage fundamental amplitude is 353.3V, and the THD is 19.19%. The phase voltage fundamental amplitude of the PD-LS-PWM modulation strategy is 204V. THD is 23.66%, line voltage fundamental amplitude is 353.2V, THD is 13.30%; PD optimized modulation strategy phase voltage fundamental amplitude is 204.2V, THD is 23.47%, line voltage fundamental amplitude is 353.6V, THD is 17.72%. The optimized modulation strategy output phase voltage THD is lower than PS-PWM and PD-LS-PWM, and the line voltage THD is lower than PS-PWM but increases compared to PD-LS-PWM.

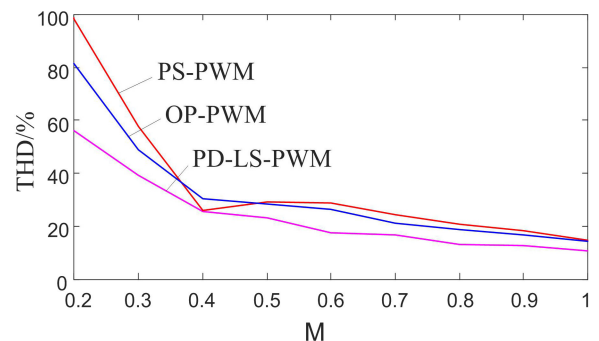


FIGURE 11. Line voltage THD for different modulation strategies.

Figure 11 shows the THD distribution curve of the output line voltage under different modulation strategies. It can be seen from Figure 11 that the OP-PWM strategy has a better phase voltage output waveform in the full modulation index range, and the output voltage quality of the line voltage is basically between PD-LS-PWM and PS-PWM.

only at $M=0.4$, the line voltage quality of the PS-PWM method is better.

Figure 12 shows the output power distribution for each cell under an optimized modulation strategy. P_{H1} , P_{H2} and P_{H3} are the output powers of unit 1, unit 2 and unit 3, respectively. It can be seen from the figure10 that when the modulation ratio is $M = 0.85$, the average output power of the inverter every $3/4$ cycles is $P_{H1} = 279.37W$, $P_{H2} = 279.37W$, $P_{H3} = 279.37W$, which effectively achieve output power balance of different cells.

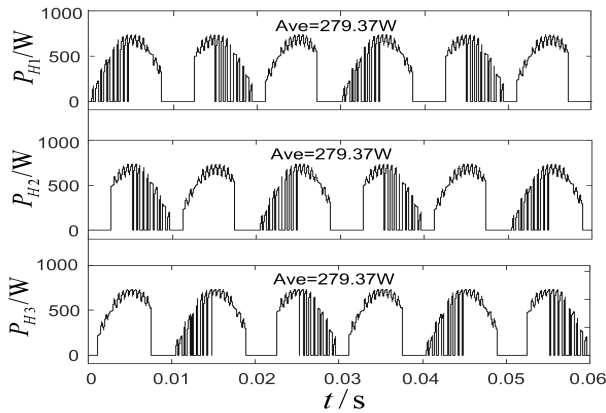


FIGURE 12. Output power of each unit.

Table 3 shows the output power distribution of the OP-PWM at different modulation ratios. It can be seen from the table 3 that the output power of different units is substantially the same in the full modulation ratio range, indicating that the proposed OP-PWM can achieve power balance of each cell over the entire modulation index M , and solve the

TABLE 3. Output power distribution of each cell.

M	0.2	0.5	0.7	0.9
P_{H1}	18.12W	98.24W	188.5W	313.2W
P_{H2}	18.11W	98.23W	188.5W	313.2W
P_{H3}	18.11W	98.23W	188.5W	313.2W

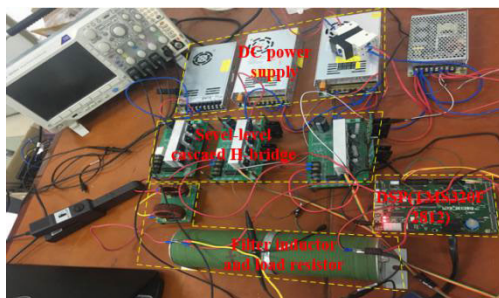


FIGURE 13. Experimental prototype.

extreme problem of output allocation for each unit at low modulation index under IPD-PWM technique.

VI. EXPERIMENTAL VERIFICATION

In order to further verify the effectiveness of the proposed control method, a three-unit CHB inverter experimental platform was constructed as shown in Fig.13. The experimental platform is controlled by DSP (TMS320F2812) with

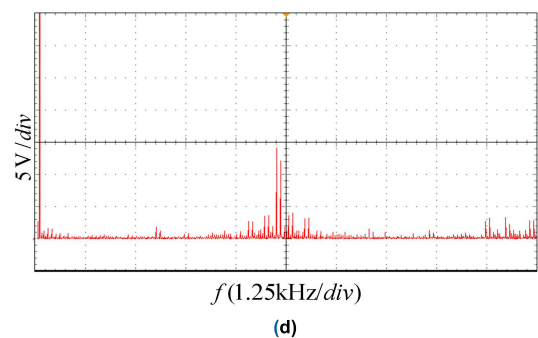
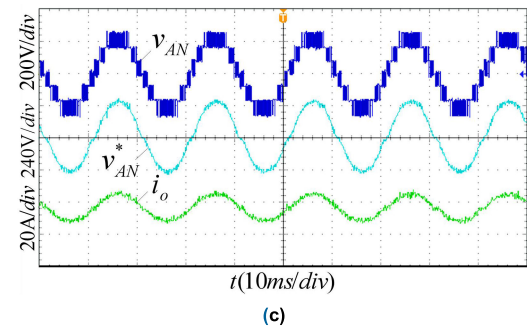
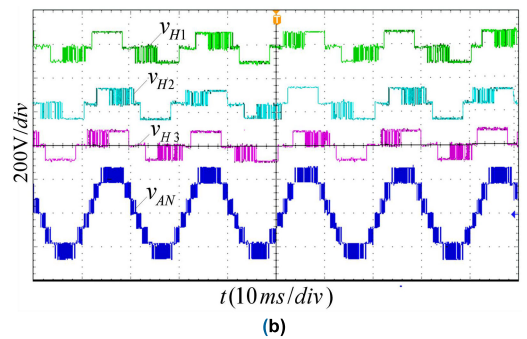
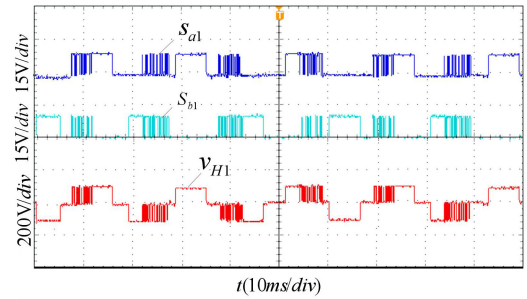


FIGURE 14. Output power of each unit (a) with pulse signal and output voltage waveform of cell 1 (b) with output voltage (c) with output phase voltage, phase current (d) with harmonic analysis of phase voltage.

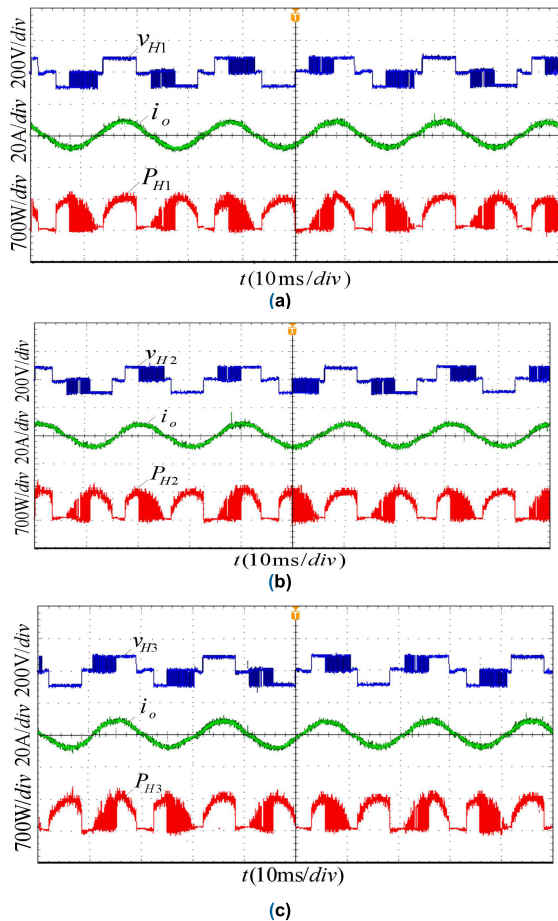


FIGURE 15. Output power of each cascaded Unit under OP-PWM (a) with output Voltage, phase current and output power of unit 1 (b) with output Voltage, phase current and output power of unit 2 (b) with output Voltage, phase current and output power of unit 3.

TX-KP101 as the drive. IGBT IXGH12N60BD1 is selected as the switching tube. The main parameters of the system are set as follows: DC input voltage is 80V, modulation ratio $M = 0.85$, carrier frequency is 3kHz, the output voltage frequency is 50Hz, the load is $R=25\Omega$, $L = 4\text{mH}$.

Figure 14a shows the pulse drive signal and output voltage waveform of the left and right bridge arms of unit 1 under the PD optimized modulation strategy. As can be seen from the figure, the frequency of the left and right bridge pulse drive signals is basically the same; Figure 14b shows the waveform of the output voltage. The output voltage of each battery contains various basic voltage waveforms, and its characteristics are consistent with the simulation results. The voltage is a seven-stage PWM waveform; Figure 14c shows the output phase voltage v_{AN} , the filtered phase voltage v_o^* and the phase current i_o . It can be seen from the figure that the output voltage and current are filtered to be a standard sine wave; Figure 14d OP-PWM The harmonic analysis diagram of the inverter output phase voltage under the strategy, it can be seen from the figure that the phase voltage harmonic content is mainly distributed around 6 kHz, and its distribution characteristics are consistent with the simulation results, and

the equivalent switching frequency is 6 kHz. It shows that the OP-PWM strategy has a frequency multiplication effect.

Fig.15(a), (b) and (c) show the waveform of the output voltage, current and output power for the cascaded unit 1, 2 and 3 respectively. The output power is obtained by multiplying the output voltage of each unit by the phase current. The output power of each unit are equal approximately to 279W, which indicates that the modulation strategy can achieve the power balance of each unit. The experimental results are basically consistent with the simulation results, indicating the correctness and feasibility of the OP-PWM strategy.

VII. CONCLUSION

In view of the shortcomings of the traditional PD modulation strategy, this paper proposes an OP-PWM strategy. Comparing with the PD-LS-PWM modulation strategy, the OP-PWM strategy has the following advantages.

(1) A similar single-pole frequency modulation technique is used to optimize the traditional PD modulation strategy, so that the maximum switching frequency of the switching tube is reduced to 1/2, the equivalent switching frequency remains constant, the switching loss are reduced, and the harmonic performance of line voltage is better than the PS-PWM.

(2) The trigger pulse signal of each unit is rotated in units of 1/4 cycle. After 3/4 cycles, the power balance of each unit is realized, which solves these problems that the unbalanced charging and discharging problem of the DC power supply for each unit and the inconsistent utilization problem. The switching loss of each unit is the same, and the working stress of all switching tubes is the same, which improves the service life and reliability of the system.

REFERENCES

- [1] L. Zhang, K. Sun, Y. Xing, and J. Zhao, "A family of five-level dual-buck full-bridge inverters for grid-tied applications," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7029–7042, Oct. 2016.
- [2] J. Rodríguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [3] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [4] X. Liang and J. He, "Load model for medium voltage cascaded H-bridge multi-level inverter drive systems," *IEEE Power Energy Technol. Syst. J.*, vol. 3, no. 1, pp. 13–23, Mar. 2016.
- [5] R. Khamooshi and A. Namadmalan, "Converter utilisation ratio assessment for total harmonic distortion optimisation in cascaded H-bridge multi-level inverters," *IET Power Electron.*, vol. 9, no. 10, pp. 2103–2110, Aug. 2016.
- [6] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Operation of cascaded H-bridge multilevel converters for large-scale photovoltaic power plants under bridge failures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7228–7236, Nov. 2015.
- [7] K. W. Sun, T. J. Summers, C. E. Coates, and C. J. Starkey, "Implementation of a multilevel cascaded H-bridge drive for an ironless axial flux permanent magnet motor for electric vehicle applications," in *Proc. 19th Eur. Conf. Power Electron. Appl. (EPE ECCE Eur.)*, Sep. 2017, pp. P.1–P.9.
- [8] I. Sanz, M. Moranchel, E. J. Bueno, and F. J. Rodríguez, "Nine-levels cascaded H-bridge converter prototype for FACTS applications," in *Proc. IEEE Int. Symp. Power Electron. Distrib. Gener. Syst. (PEDG)*, Jun. 2016, pp. 1–4.

- [9] W. Song and A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700–2708, Aug. 2010.
- [10] Y.-S. Lai and F.-S. Shyu, "Investigations into the performance of multilevel PWM methods at low modulation indices," in *Proc. Conf. IEEE Ind. Appl. Conf. 36th IAS Annu. Meeting*, Sep./Oct. 2001, pp. 603–610.
- [11] M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five level inverter," in *Proc. IEEE 32nd Annu. Power Electron. Spec. Conf.*, Jun. 2001, pp. 1351–1356.
- [12] K. Yamanaka, A. M. Hava, H. Kirino, Y. Tanaka, N. Koga, and T. Kume, "A novel neutral point potential stabilization technique using the information of output current polarities and voltage vector," in *Proc. IEEE Ind. Appl. Conf.*, Sep./Oct. 2002, pp. 851–858.
- [13] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.
- [14] S.-M. Kim, J.-S. Lee, and K.-B. Lee, "Fault-tolerant strategy using neutral-shift method for cascaded multilevel inverters based on level-shifted PWM," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015, pp. 1327–1332.
- [15] A. Razi, A. S. A. Wahab, and S. A. A. Shukor, "Improved wave shape-pattern performance using phase opposite disposition (POD) method for cascaded multilevel inverter," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf. (SPEC)*, Auckland, New Zealand, Dec. 2016, pp. 1–6.
- [16] K. K. Gupta, P. Bhatnagar, H. Vahedi, and K. Al-Haddad, "Carrier based PWM for even power distribution in cascaded H-bridge multilevel inverters within single power cycle," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016, pp. 6470–6475.
- [17] L. A. Tolbert, F. Z. Peng, T. Cunyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.
- [18] M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, "Level-shifted PWM for cascaded multilevel inverters with even power distribution," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Orlando, FL, USA, Jun. 2007, pp. 2373–2378.
- [19] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel PWM methods at low modulation indices," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 719–725, Jul. 2000.
- [20] M. Perez, S. Kouro, J. Rodriguez, and B. Wu, "Modified staircase modulation with low input current distortion for multicell converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 1989–1994.
- [21] I. Sarkar and B. G. Fernandes, "Modified hybrid multi-carrier PWM technique for cascaded H-bridge multilevel inverter," in *Proc. IEEE 40th Annu. Conf. Ind. Electron. Soc.*, Oct. 2014, pp. 4318–4324.
- [22] M. Ye, L. Kang, Y. Xiao, P. Song, and S. Li, "Modified hybrid modulation strategy with power balance control for H-bridge hybrid cascaded seven-level inverter," *IET Power Electron.*, vol. 11, no. 6, pp. 1046–1054, Mar. 2018.
- [23] G. Carrara, S. Gardella, M. Marchesoni, R. Salutati, and G. Sciotto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.
- [24] C. Zhong, X. Yaming, N. Xianlong, and S. Jianbo, "Power balance control and optimization methods with output voltage rotation for cascaded multilevel inverter," *Proc. Chin. Soc. Electr. Eng.*, vol. 38, no. 4, pp. 1132–1142, 2018.
- [25] D. Sreenivasarao, P. Agarwal, and B. Das, "Performance evaluation of carrier rotation strategy in level-shifted pulse-width modulation technique," *IET Power Electron.*, vol. 7, no. 3, pp. 667–680, Oct. 2013.



JUNFEI ZHANG received the B.Eng. degree in electrical engineering from the Jiangxi University of Science and Technology, Nanchang China, in 2016. He is currently pursuing the M.Sc. degree with East China Jiaotong University (ECJTU), Nanchang. His research interests include power electronics and cascaded multilevel converter.



LE CHEN received the B.Eng. degree in electrical engineering from the Shaanxi University of Science and Technology, Xi'an, China, in 2016. He is currently pursuing the M.Sc. degree with ECJTU, Nanchang, China. His research interests include power electronics and cascaded multilevel converter.



LIXUAN KANG received the B.Eng. degree in electrical engineering from Nanchang Hangkong University, Nanchang, China, in 2016. He is currently pursuing the M.Sc. degree with ECJTU, Nanchang. His research interests include power electronics and cascaded multilevel converter.



HAN WU received the B.Eng. degree in electrical engineering from Qufu Normal University, Rizhao China, in 2017. He is currently pursuing the M.Sc. degree with ECJTU, Nanchang, China. His research interests include power electronics and cascaded multilevel converter.



SONG LI received the M.Sc. degree in traffic control and information engineering from East China Jiaotong University (ECJTU), Nanchang, China, in 2005, where she is currently an Associate Professor with the School of Electrical and Automation Engineering. Her research interest includes power electronics.

• • •



MANYUAN YE received the B.S. and Ph.D. degrees in electrical engineering from East China Jiaotong University (ECJTU), Nanchang, China, in 2004 and 2019, respectively, where he is currently a Professor with the School of Electrical and Automation Engineering. His research interests include power electronics and electric drives, modular multilevel converter, pulse-width modulation, and selective harmonic elimination techniques.