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A *K*-Band High-Gain and Low-Noise Folded CMOS Mixer Using Current-Reuse and Cross-Coupled Techniques

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ABSTRACT A high-gain and low-noise folded down-conversion mixer for *K*-band applications is presented in this paper. Benefited from the folded double-balanced architecture, the transconductance (g_m) stage and the switch stage of the mixer can operate in-different bias conditions, providing a great freedom to optimize the two stages for noise reduction. By exploiting current-reuse and cross-coupled techniques, the conversion gain (CG) and noise figure (NF) of the mixer can be significantly improved. The proposed mixer has been designed and fabricated for verification in a 130-nm RF CMOS. Measured over the RF bandwidth from 23 to 25 GHz, the mixer achieves a maximum CG of 26.1 dB and a minimum NF of 7.7 dB under a local oscillator (LO) power of -3 dBm. The input 1-dB compression point (P_{1dB}) is −17.8 dBm at RF frequency of 24 GHz. From 23 to 25 GHz, the LO-to-RF, LO-to-IF, and RF-to-LO isolations are better than 58 dB, 51 dB, and 43 dB, respectively. With a 1.5-V supply voltage, the mixer consumes an overall dc power of 16.8 mW. These measurement results clearly demonstrate that the proposed mixer has potential to be used in highly-integrated *K*-band CMOS radios.

INDEX TERMS *K*-band, high-gain, low-noise, CMOS, down-conversion mixer, folded architecture, current-reuse, cross-coupled.

I. INTRODUCTION

Recently, the increasing demands for wireless applications with high data rates at *K* band have received great attention, e.g., 22–29-GHz short-range automotive radar, 24-GHz industrial–scientific–medical (ISM) band, and 18–23-GHz point-to-point communications. Attributed to constantly shrinking dimensions of devices, CMOS technology becomes a great competitor of III-V technologies, such as GaAs, InP, and pHEMT, to implement the millimeter-wave integrated circuits (mm-wave ICs) with low cost, high integration, and mass production. For instance, several transceivers for *K*-band radars have been demonstrated in CMOS in recent years [1]–[5].

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As critical building blocks, down-conversion mixers convert the RF signal to an intermediate (IF) band for the receivers. Since the passive down-conversion mixers exhibit conversion loss degrading the overall receiver performances and require high local oscillator (LO) voltages causing more power dissipation, active mixers with high conversion gain (CG), low noise figure (NF), large linearity, high port-to-port isolation (ISO), and low power consumption are imminently demanded for *K*-band CMOS radars. However, primarily owing to low-*Q* passive component, lossy silicon substrate, low breakdown voltage, and low maximum available gain of transistors in the mm-wave band, it's a challenge to design *K*-band CMOS mixers balancing the performances, e.g., especially high CG and low NF, mentioned above. So far, a large number of down-conversion mixers have been designed to improve the aforementioned performances in

CMOS for *K*-band applications. Chang, *et al.* and Lin, *et al.* respectively designed *K*-band down-conversion mixers with current-bleeding technique in 0.18-μm CMOS [7], [15]. The mixer in [7] has been improved to exhibit a CG of 8.4 dB, a NF of 11.6 dB, and an input $P_{1dB}(IP_{1dB})$ of -8.4 dBm. The mixer in [15] enhanced the IP_{1dB} to be -13.6 dBm with sustaining the high CG of 10.7 dB. Ahn, *et al.* demonstrated a *K*-band down-conversion mixer in 0.18-μm CMOS [12]. The mixer achieved a high CG of 9.12 dB and an IP_{1dB} of -11 dBm with a gain enhancement technique. Using the PMOS cross couple pair as an active load in 0.18-μm CMOS, Chang, *et al.* demonstrated a *K*-band down-conversion mixer with the measured peak CG of 11.9 dB at 23 GHz and a -3-dB bandwidth of 7 GHz [13]. Incorporating two on-chip Marchand baluns to convert single-ended signals into differential signals, a Gilbert down-conversion mixer was presented in 0.18-μm CMOS by Wang and Chen [14], the mixer exhibits a measured CG of 12.8 dB, an IP_{1dB} of -14.5 dBm, and LO-RF isolations better than 43 dB.

In this paper, a new *K*-band down-conversion mixer has been designed and fabricated using 130-nm RF CMOS process. With the folded double-balanced architecture, the DC paths of the g_m and switch stages are separated to provide independent bias conditions for two stages, hence the g_m stage can be biased to achieve high transconductance for noise reduction without affecting the bias condition of the switch stage. By exploiting current-reuse and cross-coupled techniques in the g_m stage and the load stage, respectively, the equivalent transconductance of the g_m stage and the equivalent load impedance of the load stage can be greatly improved to achieve the high CG and low NF for the mixer. The paper is organized as follows: Section II describes the proposed folded architecture of the double-balanced down-conversion mixer. The analysis and design of the mixer with current-reuse and cross-coupled techniques are addressed in Section III. Section IV discusses the measurement results that verify the design. Finally, the paper is concluded in Section V.

II. FOLDED MIXER ARCHITECTURE

Fig. 1 depicts the conceptual architecture of the proposed folded double-balanced Gilbert-cell mixer, which comprises two current-reuse g_m stages, a cross-coupled-pair-based load stage, a switch stage with resonating inductors, a current source pair, two transformer RF/LO baluns, and two IF buffers. RF/LO baluns provide the single-to-differential transformation and 50-Ω matching at the input RF_{in}/LO_{in} ports, respectively. The RF currents i_{RF+}/i_{RF-} generated by the g_m stage flow into the switch stage through AC-coupling capacitors, then i_{RF+}/i_{RF-} are switched to the IF currents i_{IF+}/i_{IF-} by the differential LO drive signals and converted to IF voltages through the load stage. Current source block, behaving as large resistance load to prevent RF currents from leaking to the ground, is used to provide bias currents for the switch and load stages. Furthermore, a differential IF buffer is designed to driving 50-Ω loads at the output IF_{out+}/IF_{out-} ports.

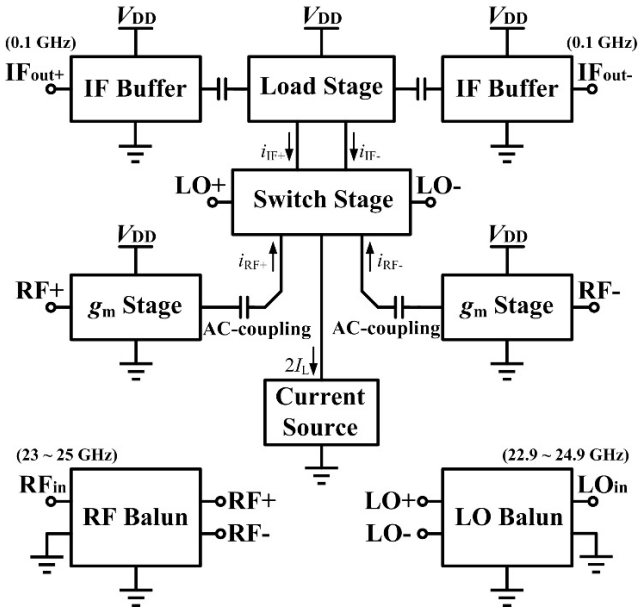


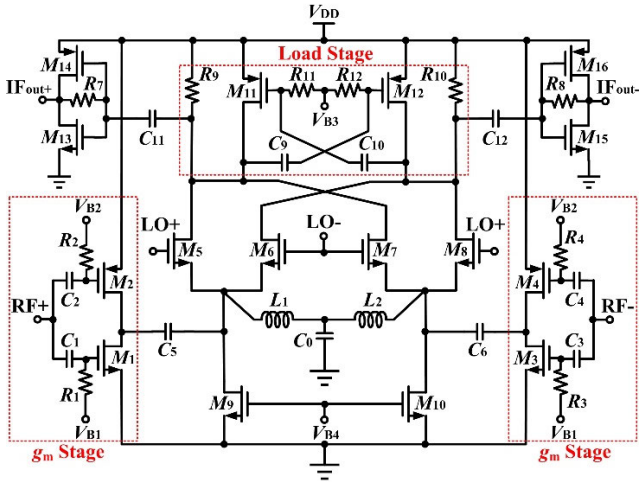
FIGURE 1. The conceptual diagram of the proposed folded double-balanced Gilbert-cell mixer for high gain and low noise operation.

The folded double-balanced architecture has several advantages as follows: 1) two ac-coupling capacitors between the g_m stage and switch stages allow the independent settings of the DC bias currents for the two stages. Since the bias current of the g_m stage should be configured to be high enough to achieve high transconductance gain and low input-referred noise whereas the bias current of the switch stage should be set to be low enough to suppress it's thermal and flicker noise [18], with the help of the folded architecture proposed in Fig. 1, the g_m stage and switch stages can be optimized independently to achieve high CG and low NF simultaneously. 2) Since the low bias current of the switch stage can be generated by the small transistors' sizes, the parasitic capacitances caused at the common nodes are reduced to further improve the CG and NF. 3) With the small DC current flowing through the load stage, the large values can be utilized for the load resistances to boost the CG, without altering the operating conditions of the switch stage.

III. MIXER CIRCUIT DESIGN

A. FOLDED DOUBLE-BALANCED MIXER

The schematic of the down-conversion mixer based on a folded double-balanced architecture is shown in Fig. 2. Two on-chip transformers T_1 and T_2 are designed to implement RF and LO baluns. The current-reuse g_m stages consist of the complementary pairs $M_1 - M_2$ and $M_3 - M_4$, which provide high transconductance gain and low input-referred noise for the differential input RF signals. Transistors M_5–M_8 building the switch stage are driven by the differential LO signals, their sizes are optimized to operate at the low overdrive voltage, hence reducing the required driving LO power [19]. Two inductors L_1 and L_2 and a bypass capacitor C_0 are inserted between the two switching common nodes



M_1, M_3	24μm / 130nm	M_9, M_{10}	20μm / 200nm	L_1, L_2	200pH
M_2, M_4	36μm / 130nm	M_{11}, M_{12}	60μm / 300nm	C_9, C_{10}	150fF
M_5~ M_8	32μm / 130nm	M_{13}, M_{15}	30μm / 300nm	R_7, R_8	10kΩ
		M_{14}, M_{16}	90μm / 300nm	R_9, R_{10}	1.2kΩ

FIGURE 2. Schematic of the proposed folded double-balanced mixer.

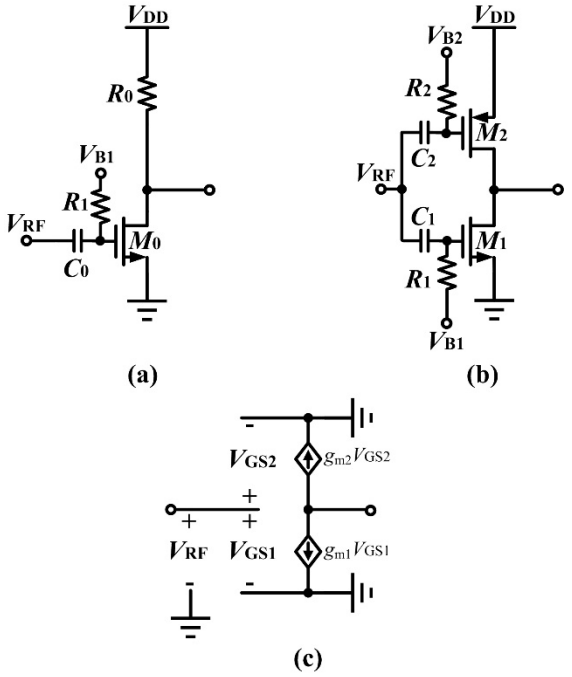


FIGURE 3. (a) Conventional g_m stage. (b) Proposed current-reuse g_m stage. (c) Simplified small-signal equivalent circuit of the current-reuse g_m stage.

for CG enhancement and NF reduction [20]. At the operating frequency, L_1 and L_2 can not only resonate with the parasitic capacitances at the switching common nodes to suppress the leakage of the differential RF currents, but also cancel the parasitic gate-to-drain capacitances of M_1–M_4 to reduce the LO-RF leakage for the isolation enhancement [21]. Inductors L_1 and L_2 are designed as a 1.5 turns spiral structure, which are realized by the top-metal with thickness of 2.5 μm. High quality factors of 15.8 are achieved at 24 GHz. The load stage is composed of two cross-coupled pairs M_{11}-R_9 and M_{12}-R_{10}, which feature the large equivalent load impedance, leading to high CG. Transistors M_9-M_{10} act as current sources. To obtain a strong driving characteristic, two amplifiers based on the self-biased inverters are utilized as the IF buffers, which include transistors M_{13}-M_{16} and feedback resistors R_7-R_8. The key active device dimensions and passive element values of the proposed mixer are optimized and listed in Fig. 2.

B. CURRENT-REUSE g_m STAGE

Since the g_m stage plays an important role in boosting the performance of the mixer, a current-reuse circuit is employed to obtain high CG and low NF in this work. For the active mixer, the transconductance of g_m stage is positively related to CG and negatively related to NF. Therefore, transconductance should be large enough to ensure the desired CG and NF. As shown in Fig. 3 (b), NMOS transistor M_1 and PMOS transistor M_2 are parallel connection and separately biased to amplify the input RF signal by two capacitors C_1 and C_2. Consequently, the g_m stage exhibits a higher overall transconductance than that of the conventional one in Fig. 3 (a). To illustrate the operation of the proposed g_m stage, the simplified small-signal equivalent circuit of the current-reuse g_m stage is plotted in Fig. 3 (c). It's obviously seen from Fig. 3 (c) that:

$$V_{RF} = V_{GS1} = V_{GS2} \tag{1}$$

V_{GS1} and V_{GS2} denote the gate-to-source voltage of transistors M_1 and M_2, respectively. The equivalent transconductance G_m can be derived as:

$$G_m = \frac{(g_{m1}V_{GS1} + g_{m2}V_{GS2})}{V_{RF}} = g_{m1} + g_{m2} \tag{2}$$

where g_{m1} and g_{m2} are the transconductance of transistors M_1 and M_2, respectively. As observed from (2), G_m can be increased by optimizing g_{m1} and g_{m2}. For M_1 and M_2 biased in the saturated region, g_{m1} and g_{m2} are enhanced normally by increasing the gate-source voltages V_{GS1} and V_{GS2} and device sizes. Considering that the large size of the transistor results in the large parasitic gate-source capacitance C_{GS}, which degrades the NF of the mixer significantly since the noise factor of the transistor is proportional to the square of C_{GS} [22], g_{m1} and g_{m2} are boosted mainly by elevating the gate-source voltages V_{GS1} and V_{GS2} in this work.

The curves of g_m vs. V_{GS} with the fixed W/L and V_{DS} are simulated in Fig. 4 (a) for M_1 and Fig. 4 (b) for M_2, respectively. Note that the V_{DS1} and $|V_{DS2}|$ are configured to balance the operations of M_1 and M_2 under the condition of $V_{DS1} + |V_{DS2}| = V_{DD}$ (1.5 V in this work). It is observed from Fig. 4 that the curves reach at the peak points of

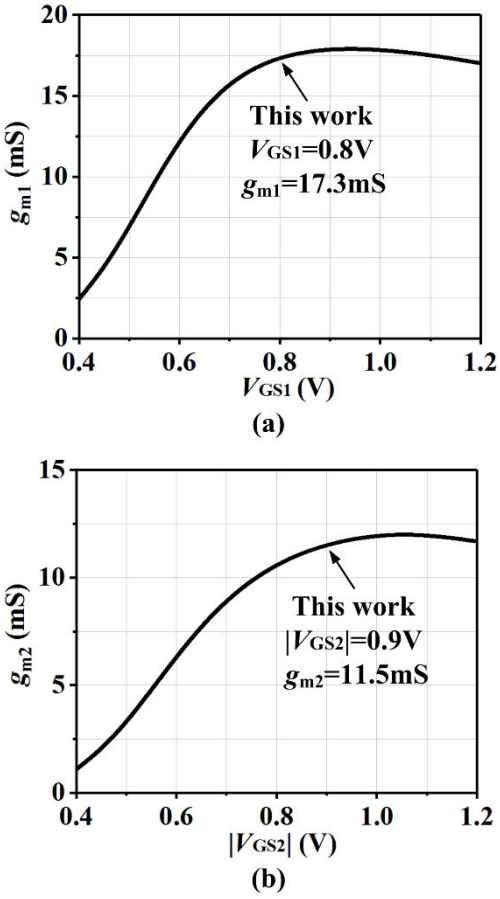


FIGURE 4. (a) Simulated g_{m1} vs. V_{GS1} for M_1 with W/L of 24-μm/130-nm and V_{DS1} of 0.7 V. (b) Simulated g_{m2} vs. $|V_{GS2}|$ for M_2 with W/L of 36-μm/130-nm and $|V_{DS2}|$ of 0.8 V.

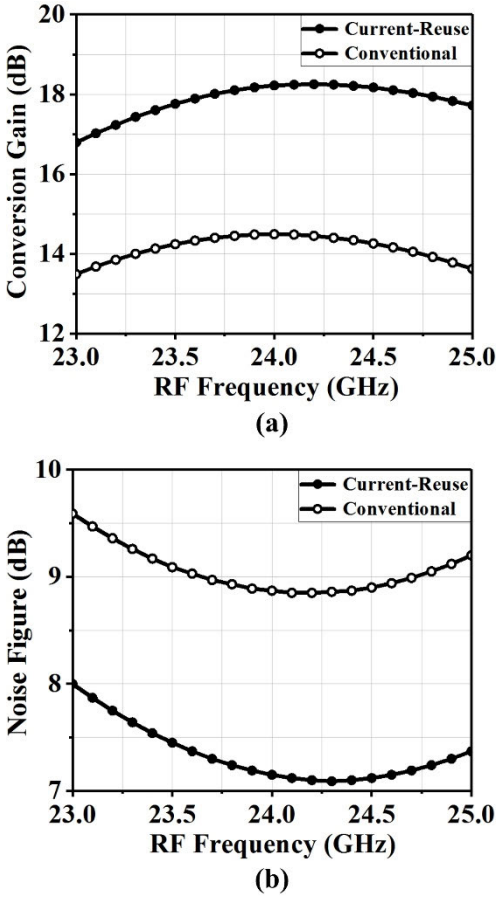


FIGURE 5. (a) Simulated CGs of the mixer with the different g_m stages vs. RF frequency. (b) Simulated NFs of the mixer with the different g_m stages vs. RF frequency.

g_{m1} and g_{m2} when V_{GS1} and $|V_{GS2}|$ increase from 0.4 to 1.2 V. For compromising the higher g_{m1}/g_{m2} and the lower bias current in the design, V_{GS1} and $|V_{GS2}|$ are configured to be 0.8 V and 0.9 V, respectively.

Under the same working conditions, the CGs and NFs of the mixers with the current-reuse and conventional g_m stages are simulated and compared in Fig. 5. The IF frequency is fixed at 0.1 GHz and the LO input frequency is 0.1 GHz lower than the RF input frequency. The input LO power is set to be -3 dBm for the simulations. For the operating RF range from 23 to 25 GHz in Fig. 5 (a), the mixer with the current-reuse g_m stage achieves the CG of 16.79 $\sim$ 18.25 dB, with the conventional g_m stage has the CG of 13.48 $\sim$ 14.51 dB. It is obvious that the CG of mixer with the current-reuse technique is boosted to be 3.3 $\sim$ 4.1 dB higher than that of one with the conventional g_m stage over the RF range. Moreover, the mixer with the current-reuse g_m stage also achieves the NF of 7.1 $\sim$ 8 dB, which is 1.6 $\sim$ 1.8 dB better than 8.85 $\sim$ 9.6 dB of the one with the conventional g_m stage over the RF range from 23 to 25 GHz in Fig. 5 (b).

C. CROSS-COUPLED-PAIR-BASED LOAD STAGE

Application of the large load impedance is an effective way to accomplish the high CG for the active mixer. In the proposed design, in Fig. 6 (b), a cross-coupled PMOS pair is constructed by M_L and R_L to obtain the large equivalent impedance for the load stage. Compared with the conventional load stage consuming the voltage headroom in Fig. 6 (a), the equivalent load impedance shown in Fig. 6 (b) can be enhanced to improve the CG in two aspects. One aspect that if M_L carries the injection current of $aI_L(0 < a < 1)$, the current through R_L is reduced to be $(1-a)I_L$, hence the value of R_L can be increased to be $1/(1\text{-}a)$ times higher than R_{L0} with the same voltage headroom. The other is that the cross-coupled PMOS pair can create the negative load resistance $1/-bg_{mL}$ to boost Z_{Load} for CG enhancement.

According to the small-signal equivalent circuit shown in Fig. 6 (c), Z_{Load} can be simply expressed as:

$$Z_{Load} = \frac{1}{-bg_{mL}} \parallel R_L = \frac{R_L}{1-bg_{mL}R_L} = \frac{R_{L0}}{1-a-bg_{mL}R_{L0}} \quad (3)$$

$$b = \frac{\omega_{IF}R_BC_C}{\sqrt{1+(\omega_{IF}R_BC_C)^2}}\cos\left(\arctan\frac{1}{\omega_{IF}R_BC_C}\right) \quad (4)$$

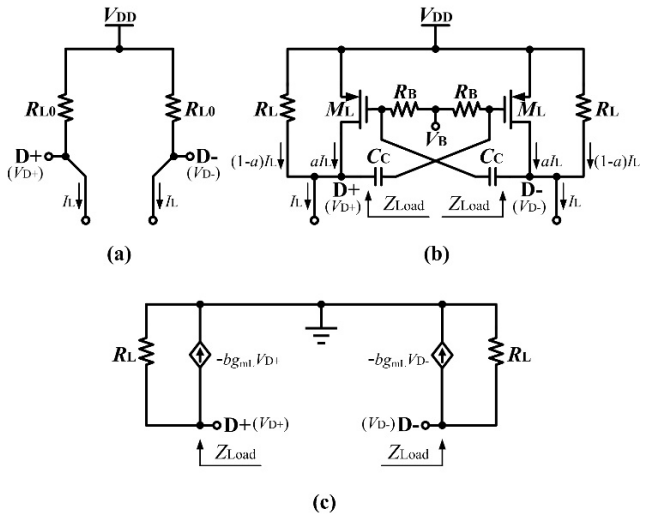


FIGURE 6. (a) Conventional load stage. (b) Proposed cross-coupled-pair-based load stage. (c) Simplified small-signal equivalent circuit of the cross-coupled-pair-based load stage.

where g_{mL} denote the transconductance of transistors M_L. Hence, the enhancement factor k of the equivalent load impedance is found to be:

$$k = \frac{Z_{Load}}{R_{L0}} = \frac{1}{1 - a - bg_{mL}R_{L0}} \tag{5}$$

Based on (3) and (5), Z_{Load} can be boosted by directly making a approach to 1 through increasing the injection current of transistors M_L. However, the noise performance of the load stage contributed by the injection current of M_L is degraded seriously with a increasing. To overcome the drawback, the drain of each PMOS pair is cross-coupled to the gate of the other through the capacitor C_C and the resistor R_B is utilized for biasing. As described in (4) and (5), Z_{Load} as well as CG can be further enhanced by properly selecting C_C and R_B with a definite a. In addition, noise contribution from M_L can be compensated by the improved CG due to the introduced negative load resistance. All in all, by adopting cross-coupled-pair technique in the load stage, the CG of the mixer can be enhanced significantly without deteriorating the noise performance.

Fig. 7 shows the simulated CG and NF vs. C_C of the mixer with the load stage. The RF input frequency is 24 GHz and the LO input frequency is 23.9 GHz. In this work, f_{IF}, R_L and R_B are equal to 0.1 GHz, 1.2 kΩ, and 5 kΩ, respectively. The input LO power is also -3 dBm set for the simulations. It is seen that the CG increases with C_C rising and arrives at the maximum value of 29.64 dB at the C_C of 235 fF in Fig. 7 (a), the reason for the phenomenon is that the Z_{Load} magnitude is restricted by the parasitic capacitance at nodes D+/D− and the input impedance of the following stage (e.g., IF buffers). On the contrary, the NF decreases with C_C increasing and reaches at the minimum value of 7.04 dB at the C_C of 235 fF in Fig. 7 (b). To ensure the stability of the mixer, the value of C_C is chosen to be 150 fF in the design, and then the

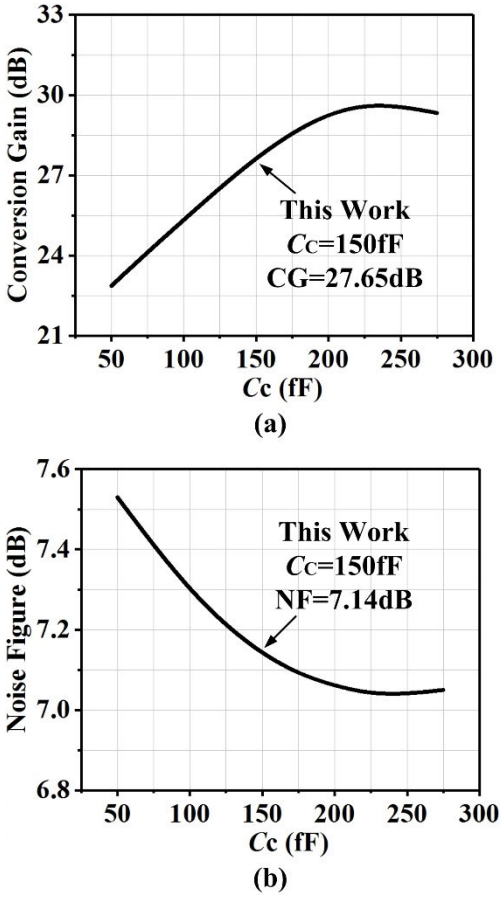


FIGURE 7. (a) Simulated CG vs. C_C of the mixer. (b) Simulated NF vs. C_C of the mixer.

mixer accomplishes the simulated CG of 27.65 dB and NF of 7.14 dB.

The CGs and NFs of the mixers with the cross-coupled-pair-based (CCPB) and conventional load stages are eventually simulated and compared in Fig. 8. The IF frequency is fixed at 0.1 GHz and the RF input frequency is 0.1 GHz higher than the LO input frequency. The input LO power is configured to be -3 dBm for the simulations. For the operating RF range from 23 to 25 GHz in Fig. 8 (a), the mixer with the CCPB load stage features the CG of 26.25 ∼ 27.66 dB, whereas the mixer with the conventional load stage has the CG of 16.79 ∼ 18.25 dB. It is observed clearly that the CG of mixer with the cross-coupled technique is improved to be 9.2 ∼ 9.5 dB higher than that of one with the conventional load stage over the RF range. Furthermore, the mixer with the CCPB load stage also achieves the NF of 7.12 ∼ 7.74 dB, which is close to 7.1 ∼ 8 dB of the one with the conventional load stage over the RF range from 23 to 25 GHz in Fig. 8 (b).

IV. MEASUREMENT RESULTS

The proposed K-band folded double-balanced down-conversion mixer with the current-reuse and cross-coupled techniques has been designed and implemented in a 130-nm RF CMOS technology with a 7-metal back end. The die

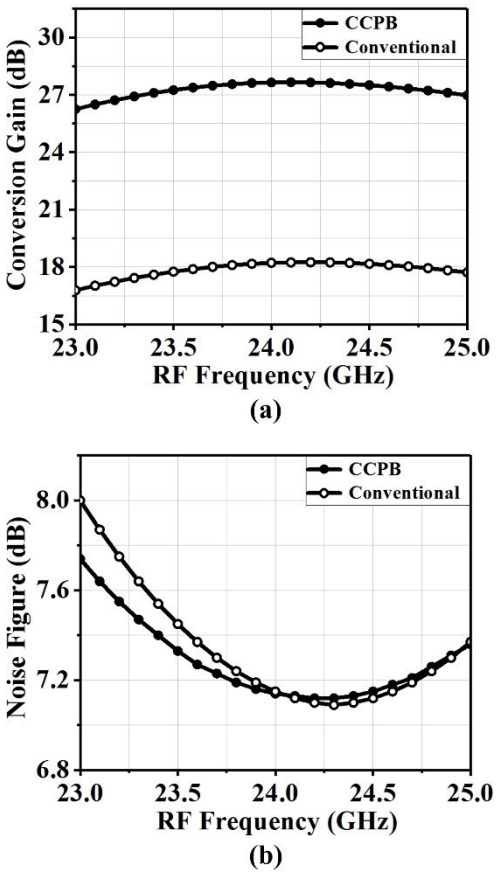


FIGURE 8. (a) Simulated CGs of the mixer with different load stages. (b) Simulated NFs of the mixer with different load stages.

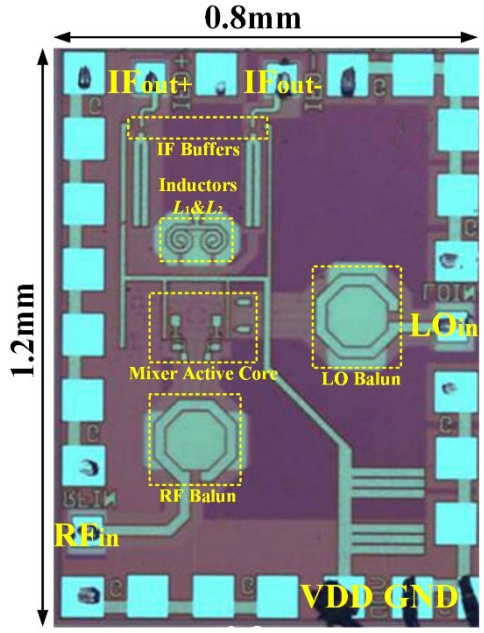


FIGURE 9. Die micrograph of the proposed mixer.

microphotograph of the chip is shown in Fig. 9. The whole chip area including two on-chip transformer baluns and all testing pads is 0.8 mm × 1.2 mm. In order to achieve the more accurate performance of the mixer, passive components containing inductors, transformers, capacitors, metal-connections, and vias, were simulated as a whole with a full-wave three-dimensional electromagnetic high-frequency structure simulator.

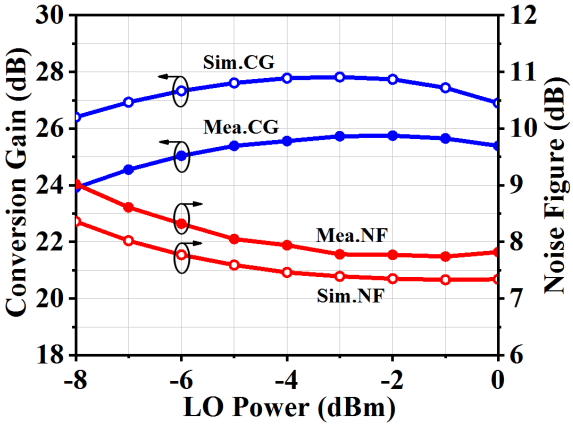


FIGURE 10. Simulated and measured CG vs. the LO power at RF frequency of 24 GHz.

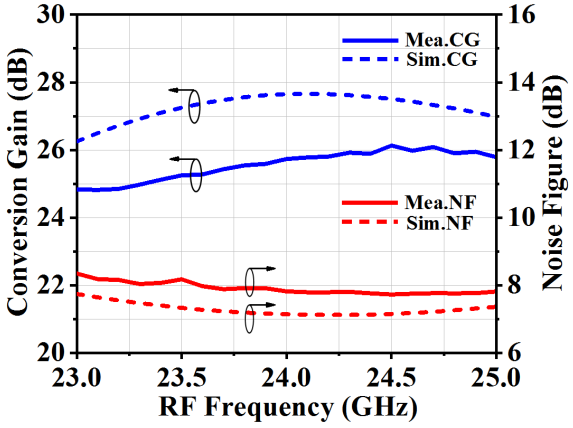


FIGURE 11. Simulated and measured CG and NF with RF frequency from 23 to 25 GHz.

On-wafer measurements of S-parameters were performed using Cascade 150-μm G-S-G probes, Keysight N6705B DC Power Analyzer, and Keysight PNA-X-N5245A 50 GHz Microwave Network Analyzer with TS200-SE probe station. Calibration was carried out using short-open-load-thru (SOLT) calibration technique.

With the RF frequency at 24 GHz and LO frequency at 23.9 GHz, the simulated and measured CG & NF vs. the input LO power are plotted in Fig. 10. For high CG and low NF in *K*-band applications, the low LO power of −3 dBm is selected for the measurements according to the simulation result. The simulated and measured CG & NF vs. RF frequency of the mixer are illustrated in Fig. 11. When the IF frequency is fixed to be 0.1 GHz, the LO frequency varies from 22.9 to 24.9 GHz with the RF frequency changing from 23 to 25 GHz. It can be seen that the mixer achieves the measured maximal CG of 26.1 dB and the minimal NF

TABLE 1. Performance summary and comparison to prior works.

References	Process	Topology	RF Freq. (GHz)	P_{LO} (dBm)	CG (dB)	NF (dB)	IP_{1dB} (dBm)	LO-to-RF ISO. (dB)	P_{DC} (mW)	Chip Area (mm^2)
[4]	180nm CMOS	LNA + Switch + Gilbert-Cell + Buffer	24	N.A.	6.9	14.6	-23.7	N.A.	90.6	13.84
[5]	130nm CMOS	LNA + Gilbert-Cell	23.8 ~ 24.5	N.A.	15.3	11.6	-13.2	N.A.	111.15*	1.53*
[10]	130nm CMOS	Gilbert-Cell + Buffer	9 ~ 50	5	12.5	16.4	N.A.	> 20	97	0.25
[11]	180nm CMOS	Dual-Gate Sub-Harmonic	23 ~ 25	0	10	23	-12.5	> 54	8.3	0.37
[12]	180nm CMOS	Current-Injection Gilbert-Cell	22 ~ 26	-2	10.26	10.5	-11	> 35	16.2	1.3
[13]	180nm CMOS	Gilbert-Cell with Active-Load + Buffer	20 ~ 26.5	1	11.9	N.A.	-20	> 33	17	0.36
[14]	180nm CMOS	Active-Balun + Gilbert-Cell + Buffer	22.6 ~ 25.8	0	12.8	15.8	-14.5	> 43	17.9	0.38
[15]	180nm CMOS	Current-Bleeding Gilbert-Cell + Buffer	21.7 ~ 24.2	3	10.7	N.A.	-13.6	> 55	23	0.51
[16]	130nm CMOS	Pre-Amp + Passive Sub-Harmonic + Buffer	24	9**	3.2	10	-12.7	> 62	31.6	0.58
[17]	180nm CMOS	Pre-Amp + Gilbert-Cell + Buffer	22.9 ~ 26.3	3	24	7.8	-20	> 55	35	0.4#
This Work	**130nm CMOS**	**Folded Gilbert-Cell + Buffer**	**23 ~ 25**	**-3**	**26.1**	**7.7**	**-17.8**	**> 58**	**16.8**	**0.96**

*RX System **Peak-to-Peak swing of 1.8 V #Mixer core

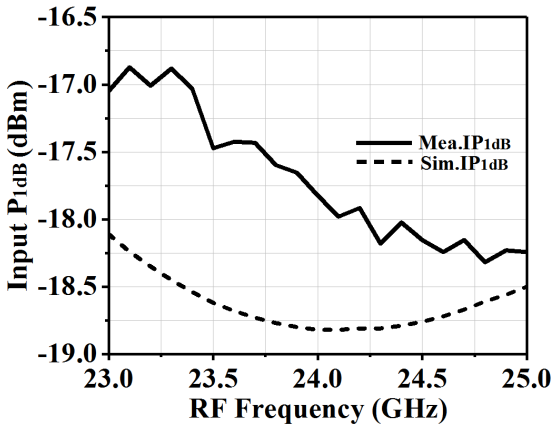


FIGURE 12. Simulated and measured IP_{1dB} with RF frequency from 23 to 25 GHz.

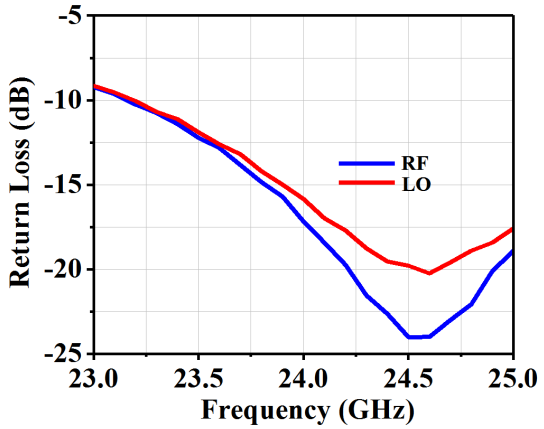


FIGURE 13. Measured return loss at the RF and LO ports from 23 to 25 GHz.

of 7.7 dB at 24.5 GHz. The linearity with the RF frequency from 23 to 25 GHz of the mixer is presented in Fig. 12. At the operating frequency of 24 GHz, the measured IP_{1dB} is −17.8 dBm, which is 1 dBm higher than the simulated value. There are discrepancies between the simulated and measured performances, which are mainly due to the inaccuracy of the transistor models.

The measured return losses at the RF and LO ports are plotted in Fig. 13. The measured return loss at the RF port is better than 10 dB from 23.2 to 25 GHz; the measured return loss at the LO port is higher than 10 dB from 23.25 to 25 GHz. The measured port-to-port isolations are shown in Fig. 14, it is obvious in Fig. 14 that isolations between LO-to-RF, LO-to-IF, and RF-to-LO are better than 58 dB, 51 dB, and 43 dB over the bandwidth of 23 ∼ 25 GHz, respectively. Operating at a 1.5-V supply voltage, the mixer draws a total dc current of 11.2 mA, which leads to a power consumption of 16.8 mW.

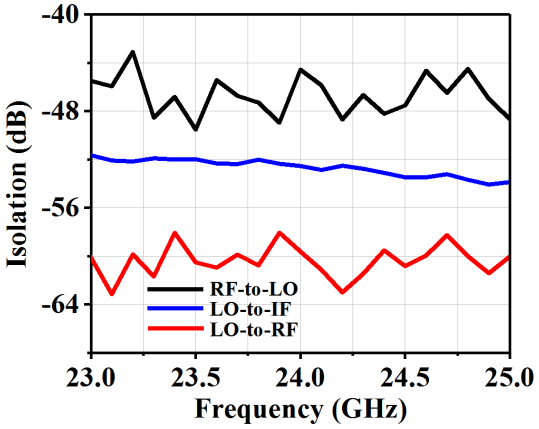


FIGURE 14. Measured port-to-port isolation between the RF and LO ports from 23 to 25 GHz.

The performance summary of the proposed mixer and comparison with the recently reported ones are given in Table 1. The CG and NF of the proposed mixer are significantly upgraded by using current-reuse and cross-coupled techniques in folded architecture. Compared with the recently reported mixers operating at *K* band, the proposed mixer achieves competitive performances, especially superior CG, NF, and ISOs.

V. CONCLUSION

The new *K*-band folded double-balanced down-conversion mixer has been proposed and analyzed. The mixer was fabricated in a 130-nm RF CMOS technology. The die area including all testing pads is 0.8 mm × 1.2 mm. The power consumption is 16.8 mW at a supply voltage of 1.5 V. With the current-reuse and cross-coupled techniques, the proposed mixer exhibits competitive performances to those of other mixers and therefore has potential to be used in highly-integrated *K*-band CMOS radios.

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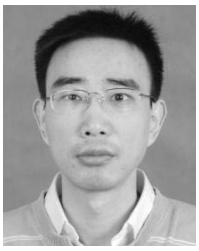

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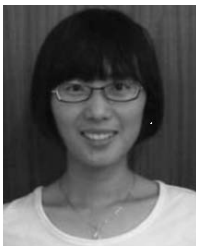

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