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A Sub-500 μW Interface Electronics for Bionic Ears

HASAN ULUŞAN[1], (Member, IEEE), ALI MUHTAROĞLU[2,3], (Senior Member, IEEE), AND HALUK KÜLAH[1,4], (Member, IEEE)

[1]Department of Electrical and Electronics Engineering, Middle East Technical University (METU), 06800 Ankara, Turkey
[2]Department of Electrical and Electronics Engineering, Middle East Technical University–Northern Cyprus Campus (NCC), 99738 Mersin, Turkey
[3]Center for Sustainability, Middle East Technical University–Northern Cyprus Campus (METU NCC), 99738 Mersin, Turkey
[4]METU-MEMS Research and Applications Center, Middle East Technical University, 06800 Ankara, Turkey

Corresponding author: Hasan Uluşan (hulusan@metu.edu.tr)

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ABSTRACT This paper presents an ultra-low power current-mode circuit for a bionic ear interface. Piezoelectric (PZT) sensors at the system input transduce sound vibrations into multi-channel electrical signals, which are then processed by the proposed circuit to stimulate the auditory nerves consistently with the input amplitude level. The sensor outputs are first amplified and range-compressed through ultra-low power logarithmic amplifiers (LAs) into AC current waveforms, which are then rectified through custom current-mode circuits. The envelopes of the rectified signals are extracted, and are selectively sampled as reference for the stimulation current generator, armed with a 7-bit user-programmed DAC to enable patient fitting (calibration). Adjusted biphasic stimulation current is delivered to the nerves according to continuous inter-leaved sampling (CIS) stimulation strategy through a switch matrix. Each current pulse is optimized to have an exponentially decaying shape, which leads to reduced supply voltage, and hence ~20% lower stimulator power dissipation. The circuit has been designed and fabricated in 180nm high-voltage CMOS technology with up to 60 dB measured input dynamic range, and up to 1 mA average stimulation current. The 8-channel interface has been validated to be fully functional with 472 μW power dissipation, which is the lowest value in the literature to date, when stimulated by a mimicked speech signal.

INDEX TERMS Fully implantable cochlear implant, bionic ear, neural stimulation, ultra-low power, current-mode.

I. INTRODUCTION

Hearing in mammals is induced by mechanical vibration at the ear drum, which is transferred to the inner ear via ossicles. Travelling waves in the cochlea of the inner ear bend different hair cells on the basilar membrane, depending on the frequency. The hair cells release electrochemical substances that stimulate the auditory neurons [1]–[3].

Traditional hearing aids treat moderate hearing disorders by amplifying the sound [4], [5]. Middle ear transducer implants convert incoming sound to micro-vibrations through a microphone in order to address disorders related to eardrum and ossicles [6], [7]. Damage of the hair cells on the other hand causes loss of fine tuning of the incoming sound, resulting in hearing loss from severe-to-profound level. This kind of impairment can be fixed by Cochlear Implants (CIs), which convert sound to electrical pulses for stimulation of the auditory neurons [8]–[10]. While modern CIs are the most successful neural prostheses that target high quality music perception [4], [11], [12], aesthetic concerns and frequent battery replacement have redirected recent studies to fully-implantable cochlear implants (FICIs) [13]–[15].

Many studies on FICIs include design of implantable microphones [16]–[18]. Single microphone output requires electrical filters to process different frequencies as the main disadvantage. In a previous study by our group, a PZT acoustic sensor acts as a mechanical filter to sense the incoming sound at certain frequency bands [19]. Interface electronics has to accompany implantable sensors for detecting sound in this approach. The previous studies are either focused on the front-end amplification [20] and filtering [21], [22] circuits or the neural stimulation [23], [24] part

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of the CIs. An ultra-low power programmable analog bionic ear processor is proposed by Sarpeshkar *et al.* for electret microphones [25], which provides 16-channel output to drive stimulation electrodes external to the implant. The design by Georgiou *et al.* includes a single-chip system with speech processor and stimulator for a totally implantable cochlear prosthesis with processor power dissipation of 126 μW [26]. Both of the cochlear implant circuits in [25] and [26] focus on the design of the front-end signal conditioning where they benefit from low power and low voltage operation of current mode circuits [27]. Nevertheless, these works exclude the high voltage neural stimulation unit for the delivery of the current pulses to the auditory neurons. More recently, an implantable low-power signal conditioning IC has been reported in [28] for a piezoelectric middle-ear sensor. Although energy-optimized (exponential-like) stimulation pulse shape at the back-end reduces system power dissipation to about 572 μW, single-sensor architecture with 8 filters to isolate distinct frequencies results in a relatively high power dissipation at the front-end circuit. Jang *et al.* proposes a micro-electromechanical system that senses the input sound through mechanical filters and delivers electrical stimulation to the auditory neurons [29]. The neural stimulation is implemented off-chip, and the system design does not consider important FICI criteria such as power dissipation, compression rate, stimulation current level, and patient fitting compatibility.

In this work, a bionic ear interface is proposed, which includes original power-efficient current-mode circuits to process the acoustic sensor signals at the front-end, and stimulates the auditory neurons through energy-optimized exponentially decaying current waveforms at the back-end with the lowest total system power dissipation to date. The input sound is sensed by the low-volume 8-channel PZT transducer operating with high sensitivity. The sensed signals are compressed into the dynamic range of the auditory neurons, which are then stimulated by the current pulses at the desired frequency and power level. The organization of this paper is as follows: The design specifications of the interface electronics is provided in Section II. Section III includes the details of the interface, which is followed by further discussion of neural stimulation scheme in Section IV. Section V presents the test results and discussions. Finally, conclusions are summarized in Section VI.

II. DESIGN SPECIFICATIONS

Fig. 1 shows the FICI system proposed at FLAMENCO Project[1] as a bionic ear with five distinct units: PZT transducers for multi-frequency sound detection, signal conditioning electronics to stimulate the auditory neurons according to transducer outputs, a cochlear electrode for neural stimulation, a rechargeable battery to supply the system, and an RF coil for patient fitting and battery charging.

[1]1FLAMENCO Project with ERC Consolidator Grant 2015 (GA:682756), https://cordis.europa.eu/project/rcn/204134_en.html.

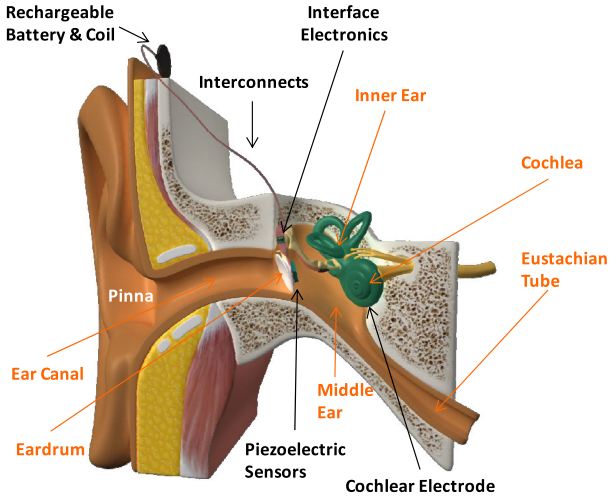

FIGURE 1. FICI system proposed at FLAMENCO Project.

The connections between PZT sensor, interface electronics, and battery can be sustained through flexible interconnects that minimize the damping on the vibration of the eardrum and the ossicles. Previous studies have shown that mass of the implantable sensor placed on the ossicles must be lower than 20 mg in order to limit the loading effect on the umbo vibration [14]. A flexible material (e.g. polyimide) will be utilized as the substrate with interconnect metallization paths, which will be optimized for minimum parasitic line resistance and maximum flexibility for the vibration of ossicles. The subject of this paper is the signal conditioning interface unit, for which design specifications are outlined in this section.

The conditioning electronics and the transducers must fit into the middle ear (2 cm^3), and the transducer footprint must be less than the size of the eardrum (55 mm^2 with 8-10 mm diameter) [30]. The low volume PZT sensor by our group [19] includes 8 cantilever beams with different resonant frequencies for sound detection, covering the common sound band from 200 Hz to 5 kHz. The center frequencies of the sensor channels are distributed linearly between 200-1300 Hz (300, 600, 900 and 1200 Hz), and are logarithmically spread above this range to cover the common sound band up to 5 kHz (1600, 2200, 3200 and 4800 Hz). High sensitivity of the PZT material provides higher signal amplitude and consequently higher signal to noise ratio can be achieved at the sensor output. The characteristics of the 8-channel PZT sensor are projected by considering miniaturization to fit the sensor to the middle ear, and provide multi-bandpass filtering with a similar peak voltage at the resonance frequency of each channel. The neural stimulation output at each channel can be programmed for per-patient calibration through digital control of stimulation current generator, as will be explained in Section III. The same control allows compensation for variances across PZT sensors. The number of cantilever beams determines the number of spectral channels, which highly influences the speech perception of the patients. Previous studies report that speech perception gets better with

increasing number of channels, but does not significantly improve beyond 7 channels [31]. Hence, 8 channels are utilized in the proposed design to provide sufficient spectral resolution with acceptable hardware complexity and power dissipation associated with the conditioning circuits.

PZT transducers collectively provide mechanical filtering since each one oscillates with the frequency component of the incoming signal that matches with its resonant frequency. The power requirement of the circuits that condition the PZT signals is the crucial part of the design. For a 200 mAh - 3.6 V implantable rechargeable battery [32], the total power consumption must be lower than 600 μW to dissipate 1% of the total energy with 12 hours continuous usage per day. Using this usage model, the battery is 10% depleted after 10 days, with battery voltage reduced to the marginal level for recharging. Typical power conversion (regulation) circuits have about 85% efficiency at best. Therefore, implantable signal conditioning system, such as the one presented in this work, must consume less than 500 μW to achieve lifetime beyond 30 years by recharging the battery for 1000 cycles [28], after which point rechargeable batteries start losing significant capacity.

Another critical design parameter for the signal conditioning circuit is the input dynamic range, which highly influences the speech perception of the patient. Daily sound level ranges between 40 dB SPL (e.g. in a quite library) and 100 dB SPL (e.g. helicopter noise) [14]. Previous studies have shown that an input dynamic range of 50 dB provides adequate speech perception in multichannel CIs [33], which is thus used as the lower bound for signal conditioning and transducer design.

III. INTERFACE CIRCUIT DESIGN

Fig. 2 shows the block diagram of the bionic ear interface that senses voltage signals from 8 piezoelectric (PZT) sensors with different center frequencies. The interface circuitry predominantly operates in current mode to minimize power dissipation due to current-to-voltage conversion and vice versa. Size constrained PZT sensors generate signals of limited amplitude. Therefore, a low-power wide-range Logarithmic Amplifier (LA) is designed as the first stage. Although the dynamic range of daily observed sounds is around 60 dB, the electrical dynamic range of the cochlea is about 20 dB [33], [34]. Thus, the LA is designed to logarithmically compress the input sound range to the electrical dynamic range of the cochlea. The AC current delivered by the LA feeds an original current rectifier and multiplier with a low-pass filter at the next stage. A sample/hold circuit samples the filter output to generate a reference for the stimulation current generator, which drives the current level required by the auditory neurons. The generated signal is converted into a biphasic pulse through a switch matrix, which directs the current pulse to the correct electrode (E_1-E_8) to stimulate the corresponding auditory neurons. The enable signals for the LAs and corresponding channel selection signals at sample/hold blocks are provided by the control unit. The selection signals are level shifted to be compatible with the high voltage switch control block for the biphasic current. Design and analysis of each sub-circuit are provided in the following sections.

A. POWER OPTIMIZED LOGARITHMIC AMPLIFIER

Each sensor output at the first stage is amplified using a custom designed logarithmic amplifier that also compresses the incoming sound to the electrical dynamic range of neurons. The dual function of the amplifier optimizes system power dissipation better compared to the previously reported cochlear implant interfaces, which implement a separate DC compression stage after the downstream envelope detector [34], [35]. The LA is a modified version of the one presented in [36] to accommodate a number of circuit power optimization features, in addition to system level power gating of the lower supply voltage (V_{DD} = 1.8 V) illustrated by switches in Fig. 2: The subthreshold design delivers a single ended AC current output and eliminates the load resistor compared to [36], which increases the dynamic range by trading off less critical per-stage gain. The number of stages in the circuit is otherwise minimized with the constraint to deliver the desired input compression range. Fig. 3 (a) depicts the five-stage LA utilized to amplify the sensor voltage range (0.1-100 mV) provided in [19] to the acceptable level of 20 dB range. As the input amplitude increases, each stage of the LA enters the limiting state (saturation) one by one from the last stage toward the first.

Fig. 3 (b) presents the details of the staging amplifiers (same for all stages) that form the LA, where each stage in the chain is driven through differential $V_{X+/-}$ outputs of the previous stage. M_4 current is mirrored to the output through M_5. DC component of the current (I_{Bias}) is extracted with the bias branch, allowing only the AC component (I_{ac} in Fig. 3 (b), $I_{out,i}$ in Fig. 3 (a)) to be summed with the output of the other stages as I_{OUT} in Fig. 3 (a). The relationship between output current and input voltage is provided by Eq. (1) in terms of the circuit parameters for the low input voltage level when all amplifier stages operate in the linear region:

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}\left(1 + A_v + (A_v)^2 + (A_v)^3 + (A_v)^4\right), \quad (1)$$

where A_v is the voltage gain of one differential pair stage and can be written as $A_v = g_{m,M1}/g_{m,M3}$. The output current of the logarithmic amplifier can be rewritten using Taylor series as:

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}\sum_{i=0}^{k-1}(A_v)^i, \quad k = 1, 2 \ldots 5, \quad (2)$$

$$I_{OUT} = v_{in}\frac{g_{m,M2}}{2}\left(\frac{(A_v)^k - 1}{A_v - 1}\right), \quad (3)$$

where k is the number of amplifiers operating in linear region. The logarithmic compression of the gain comes from the nonlinear characteristic of the saturated amplifiers. When all the amplifiers are in linear region, the output current in Eq. (3) has the highest slope with respect to the input.

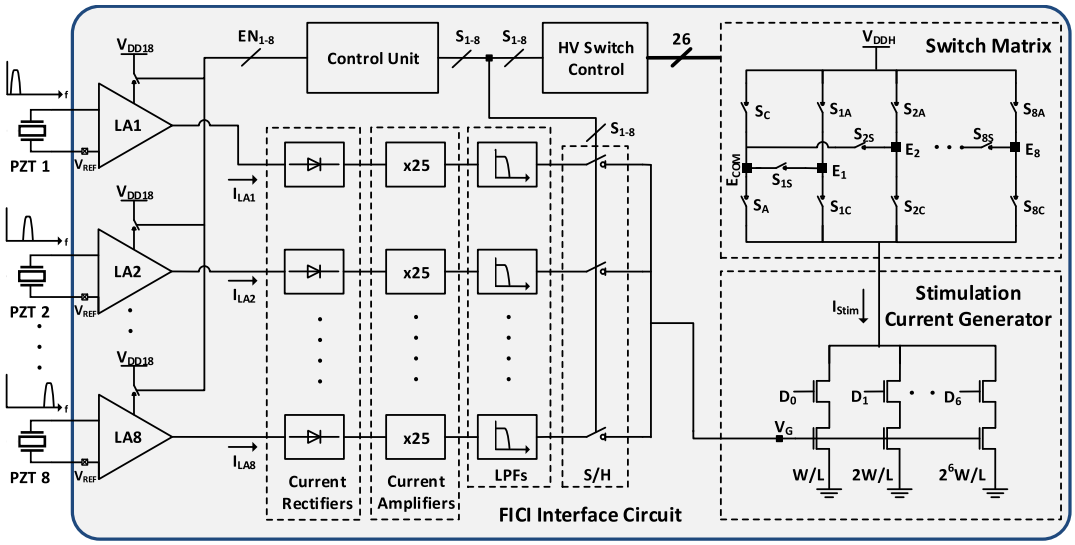

FIGURE 2. Fully-implantable cochlear implant (bionic ear) interface circuit block diagram.

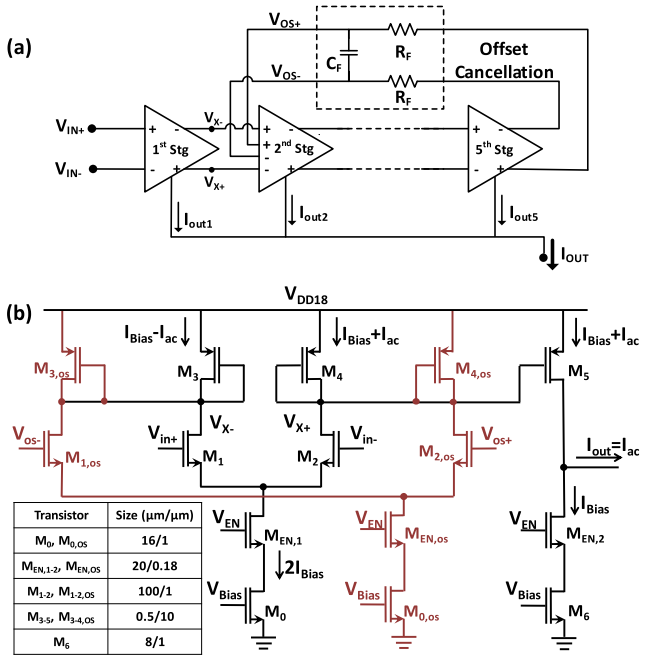

FIGURE 3. (a) Logarithmic amplifier circuit with offset cancellation feedback from the last stage to the 2nd stage, (b) amplifier stage design, with the 2nd stage additions for enhanced offset cancellation highlighted in red color.

However, increase in the input voltage leads to stage by stage saturation of the amplifier, and reduces the gain. The input output characteristic of the amplifier exhibits a logarithmic variation by proper tuning of the stage gain.

The amplifier stages are biased to operate in the subthreshold domain for lower power dissipation and higher gain due to increased transconductance. When a particular channel is not sampled, the LA is dynamically disabled through a power management control signal (V_{EN} in Fig. 3 (b)). The utilized diode loaded differential input and output stages enable fine definition of the common mode without feedback, which further reduces power dissipation compared to alternatives.

In viewpoint of noise performance, the input referred noise of the logarithmic amplifier is mainly determined by the first stage, while the noise generated by next stages are suppressed by the voltage gain (A_V) of the staging amplifiers, and can be ignored [36]. The input referred noise of the first stage is provided by Eq. (4).

$$\overline{v_{eq,stg1}^2} = 2\overline{v_{n,M_2}^2} + \frac{4g_{m4}^2}{g_{m2}^2}\left(2\overline{v_{n,M_4}^2} + \overline{v_{n,M_5}^2} + \frac{g_{m6}^2}{g_{m5}^2}\left(\overline{v_{n,M_6}^2} + \overline{v_{n,M_0}^2}\right)\right) \quad (4)$$

where $\overline{v_n^2}$ is the total noise of a transistor. As the logarithmic amplifier operates in subthreshold region, $\overline{v_n^2}$ is expressed as in (5).

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m} + \frac{K_f}{C_{ox}WLf} \quad (5)$$

where k is the Boltzman constant, T is operation temperature, g_m is transconductance of the MOSFET, and γ is the excess noise factor, which is around 1/2 for weak inversion region [37]. K_f is the flicker noise coefficient. C_{ox}, W, and L are technology and design parameters that represent the oxide capacitance, width and length of the MOSFET. f is the operation frequency. In order to minimize the noise at the input differential pair (M_{1-2}), which are the most dominant components, the following measures are implemented: Their transconductance is increased to reduce the thermal noise and their gate area is increased to minimize the flicker noise. Moreover, high transconductance of M_2 contributes to suppression of noise induced by M_{3-6}.

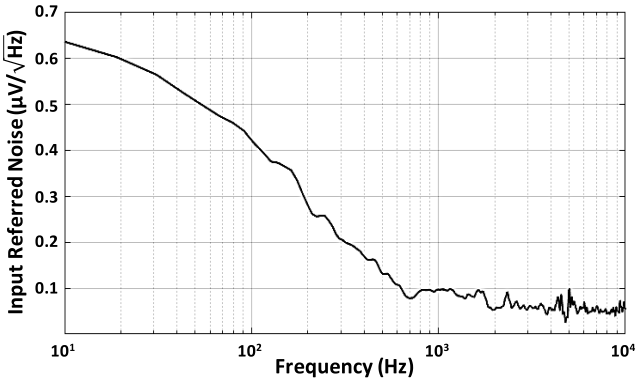

FIGURE 4. Measurement result of the input refer noise of LA.

Input DC offset is compensated through feedback from the last stage to the 2nd stage. Although applying feedback to the second stage is expected to impact the performance of the offset cancellation by a small fractional amount, the input referred noise of the amplifier is reduced by about 3x compared to the logarithmic amplifier design with feedback at the first stage (∼10 μV_{rms}). The total input referred noise of the designed logarithmic amplifier with feedback at the second stage is measured as 2.7 μV_{rms} (Fig. 4). Fig. 3 (b) highlights the offset cancellation enhancements (in red color) to the amplifier at the 2nd stage. The offset voltage has a direct effect on saturation of the amplifiers especially at the final stages of the amplifiers. As seen in Eq. (3) the output current is directly related to the differential input voltage. The uncontrolled DC offset at the input of the LA leads to saturate the staging amplifiers earlier, hence reduces the overall gain of the system. The feedback amplifier helps to keep the gain in the stable range by cancelling the differential offset. An RC filter has been applied as the feedback loop with cut-off frequency <0.1 Hz to avoid feedback interactions within the hearing band (20 Hz – 20 kHz). High value required from the RC product to achieve the target cut-off frequency is challenging for on-die integration of the filter. A pseudo-resistor MOS structure with high resistance has hence been utilized as shown in Fig. 5 (a). The pseudo-resistor is built from a parasitic source-body-drain pnp transistor, and is activated when the diode connected PMOS transistors are forward biased. Two series pseudo-resistor structures have been utilized to provide resistive operation at a wider offset range. Since this structure passes current only in one direction, another resistive pair with reverse direction has been connected in parallel to provide bidirectional operation. Fig. 5 (b) shows that the resistance of the structure is more than 450 GΩ for voltage difference lower than ±250 mV. The capacitance in the RC filter can thus be decreased below 10 pF, and is implemented using on-die MIM caps.

Fig. 6 (a) depicts the measured input/output characteristics of the LA operating at 5 kHz, with input representing the sensor output range from [19]. The amplifier compresses the 60 dB input dynamic range into 17 dB electrical range, while providing AC current output. The trendline in the figure

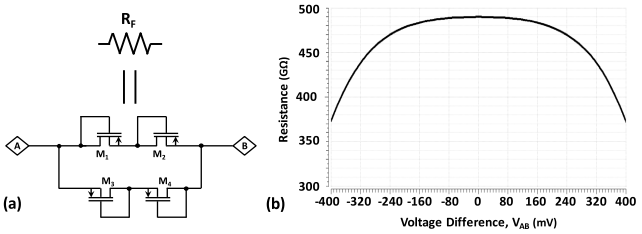

FIGURE 5. (a) Schematic of pseudo-resistor MOS structure, and (b) variation of resistance with voltage across the resistor.

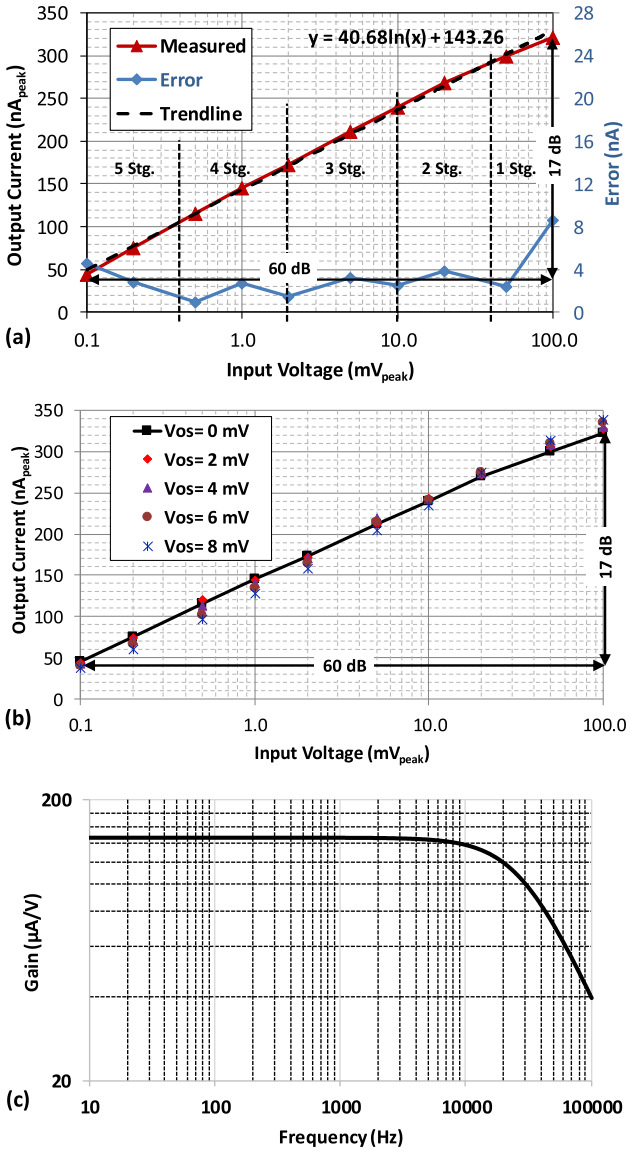

FIGURE 6. Measured (a) output current of the LA versus input voltage, (b) offset cancellation performance, and (c) gain response of the LA.

illustrates the logarithmic compression of the output current with respect to the input voltage. Fig. 6 (a) also includes the error at the output of the amplifier with respect to the ideal linear response. The error at the amplifier increases at the range boundaries to a maximum of around 8 nA. Moreover, the error at the output is always lower than 10%, which

shows that the LA design effectively utilizes the full sensing range. Fig. 6 (b) shows the amplifier response with varying input and offset voltage values. Results indicate the output voltage is slightly deviated with the applied offset voltage; however, the circuit is still functional. In absence of feedback, the staging amplifiers would have been saturated with a small offset voltage, and broken the overall LA operation, whereas the amplifier with the feedback circuit operates well with a slight deviation. Fig. 6 (c) shows the frequency response of the LA at 1 mV (60 dB) input. The LA has flat response up to 5 kHz which covers operation frequency range across the PZT sensors at the input. -3 dB bandwidth is >10 kHz, that provides enough margin for the flatness of the gain.

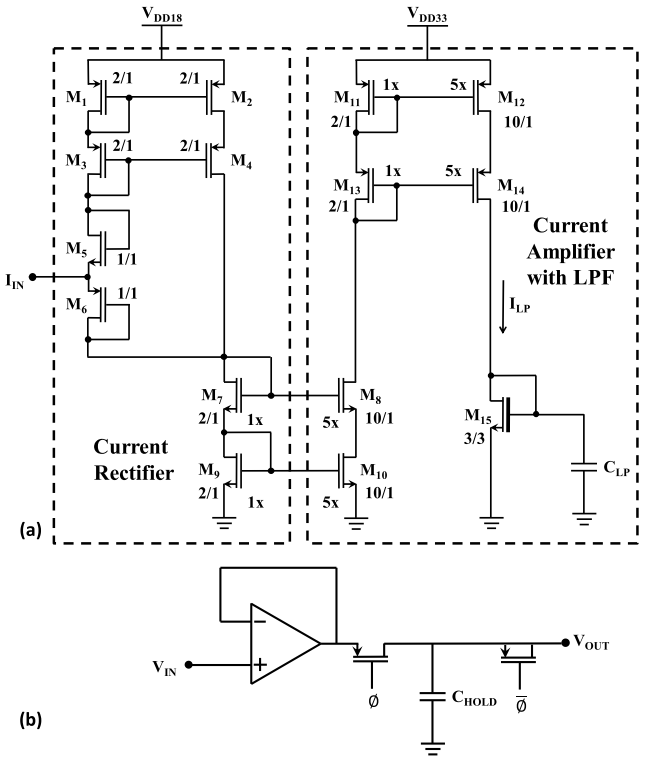

FIGURE 7. (a) Current rectifier and current amplifier with low-pass filter, (b) sample and hold circuit.

B. CURRENT RECTIFIER AND AMPLIFIER WITH LOW-PASS FILTER

The AC current signal from the logarithmic amplifier is rectified, amplified, and filtered by the next stage illustrated in Fig. 7 (a). Diode connected NMOS (M_5) and PMOS (M_6) transistors provide low resistance at the rectifier input. The operation principle is as follows: Input current (I_{IN}) flows through M_6 (M_5) with M_5 (M_6) turned OFF during the positive (negative) phase. Both positive and negative half cycles are summed at M_7 through the cascode current mirror. The rectified current is amplified through M_{7-10} and M_{11-14} cascodes with a total gain of 25, and is delivered to the low-pass filter (I_{LP}) made up of a diode connected high voltage NMOS transistor M_{15} and a 25 pF capacitor. Although the mechanical filters discriminate different frequencies in the speech band, the information carried by these frequencies are determined by the envelope variation of the signals. Therefore, a low pass filter with 400 Hz cut-off frequency is added to cover the frequency of temporal pitch observed in daily life [1], [8]. The settling time of the LPF is below 5 μs, which is a much lower than the characteristic period of the signal at the rectifier output (1/5 kHz $=$ 200 μs). The settling time can be further reduced by utilizing a 2nd order filter with additional power dissipation penalty. A 1st order filter provides a favorable power-delay product in this design. The amplified and rectified current (I_{LP}) is converted to voltage by the LPF MOSFET (M_{15}), whose gate is sampled to determine the least significant bit of the stimulation current generator. The voltage on the filter capacitor (C_{LP}) is buffered through a simple single-stage low-gain low-power differential amplifier to isolate LPF from the loading of the sampling circuit. The buffered voltage is sampled by the sample and hold circuit (Fig. 7 (b)) for 100 μs. A shorted switch located after the sampling capacitor is activated out of phase with the sampling switch to reduce charge injection effect. The system includes 8 Sample and Hold (S/H) circuits for which corresponding outputs are multiplexed to bias the current generator unit.

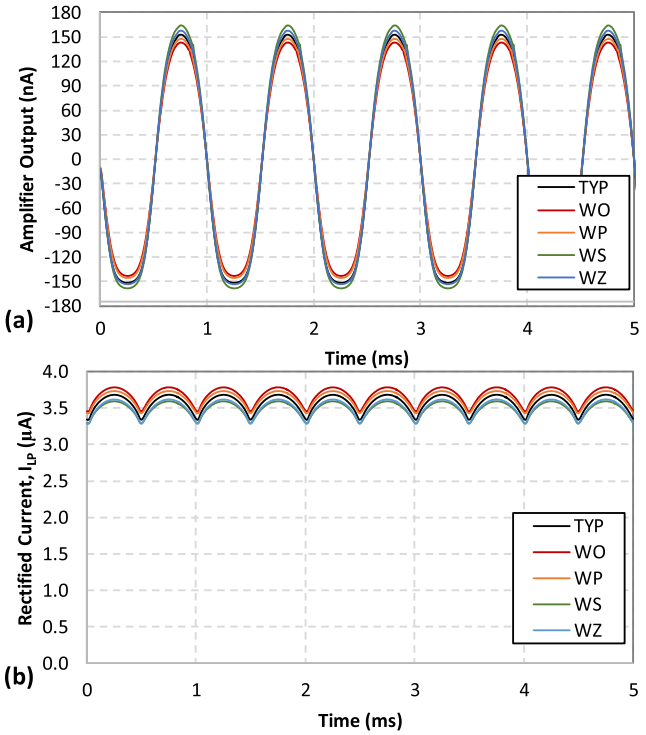

FIGURE 8. Process corner simulations of the (a) LA and the (b) rectifier circuits with 1 mV input amplitude and 1 kHz frequency.

In order to observe the effect of process and temperature variations on the design, the logarithmic amplifier and the current rectifier circuits have been simulated at the process corners. Fig. 8 presents the simulation results with 1 mV input peak voltage at 1 kHz, where TYP is typical, WP is worst case power, WS is worst case speed, WO is worst case ONE,

and WZ is worst case ZERO corner. The results show that process variations lead to slight deviations from the typical characteristics, but the variations are well within the calibration range of the stimulation current generator block, and can be accounted for during the per-part calibration procedure.

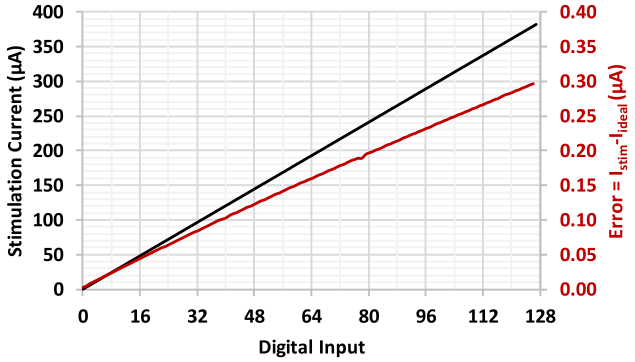

FIGURE 9. Measurement result of variation of the stimulation current level with respect to the 7-bit DAC setting.

C. STIMULATION CURRENT GENERATOR

The sampled voltage (V_G) from the previous stage controls the current source MOSFETs (Fig. 2). The current generator embodies a programmable 7-bit digital-to-analog converter (DAC) to set the stimulation current threshold for maximum comfort. Fig. 9 shows variation of the generated stimulation current level with respect to the 7-bit DAC control signals D_0-D_6, where the least significant bit (LSB) corresponds to 3 μA. Thanks to the analog layout techniques applied, the percent error of the generated current with respect to the LSB is negligible (<10%). Therefore, the utilized current generator circuit provides reliable calibration of the minimum threshold and maximum comfort level of the stimulation current at each channel according to patient's needs. Moreover, the 7-bit DAC circuit provides control of the stimulation current with high sensitivity, and the error at the front-end circuit response can be eliminated through calibration per patient, after implantation.

Digital pins D_0-D_6 are utilized to modify stimulation current pulse shape for optimal operation in terms of providing comfortable stimulation with lowest average power dissipation. The topology yields easy control with wide range. Moreover, integration of the DAC reduces power dissipation compared to the previous generator circuits [28], [38]. The circuit can generate more than 1 mA of stimulation.

D. SWITCH MATRIX

The generated stimulation current is converted into a biphasic pulse, and is transferred to the corresponding electrode (E_1-E_8) through a switch matrix. Fig. 10 depicts schematic diagram of the switch matrix for the first channel, and the generated biphasic stimulation current in time domain. After the cathodic pulse is generated through S_C and $S_{1,C}$ switches, the anodic pulse is applied with S_A and $S_{1,A}$ in order to supply

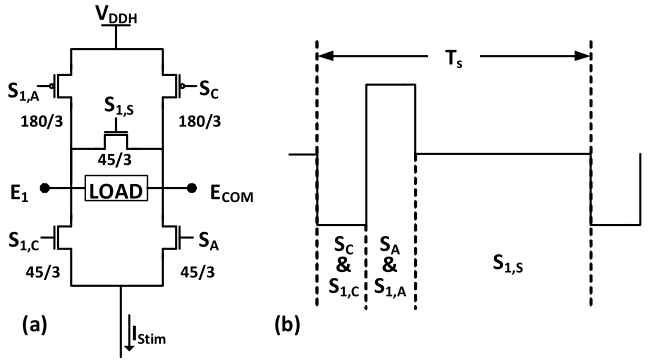

FIGURE 10. (a) Switch matrix utilized at Electrode 1, and (b) generated biphasic stimulation current.

the discharged current back to the neurons. S_C and $S_{1,A}$ in the switch matrix are PMOS switches whereas S_A, $S_{1,S}$, and $S_{1,C}$ are NMOS switches to enable better transmission at high and low voltage, respectively. Switch $S_{1,S}$ is utilized to remove the residual charge remaining on the capacitor at the load, and prevents charge imbalance at the electrodes. The switch matrix is supplied by high voltage (V_{DDH}) to deliver a sufficiently high potential at the stimulation electrodes. The electrodes are enabled according to the well-known Continuous Interleaved Sampling (CIS) sound processing strategy, which provides sequential interleaved stimulation at fixed frequency, and delivers better performance compared to other synchronous implementations [39], [40]. CIS switch control signal timing is explained in the next section.

E. CONTROL UNIT

The control unit generates power enable signals for the logarithmic amplifiers, selection signals to switch between channels for sampling, and switch matrix control signals for 8-channel CIS stimulation. The core is a resettable one-hot finite state machine (FSM), as depicted in Fig. 11 (a). The state machine generates interleaved enable signals (S[1:8]) that stimulate the electrodes sequentially according to CIS strategy. The stimulation is timed using a low frequency clock (CLK_{LO}) with 1 ms period. A 100 μs stimulation pulse at each channel enables 50 μs cathodic and anodic phase widths. After CLK_{LO} falling edge starts the operation, channel select signals are consecutively enabled through the one-hot FSM running on a higher frequency clock (CLK_{HI}) at 10 kHz. CLK_{HI} is generated by a ring oscillator and is also used to trigger a ring counter, as shown in Fig. 11 (b), in order to generate CLK_{LO}. This implementation ensures the two clocks have synchronous timing. The logarithmic amplifier enable and sampling signals (EN[1:8]) are acquired for 100 μs, and generated just before the enabling period of the corresponding channel. After the stimulation of the last channel, a done signal is generated to reset the machine, and the process repeats at the next falling edge of the low-frequency clock. The anodic and cathodic pulses at each stimulation electrode are obtained from the selection (S[1:8]) and clock

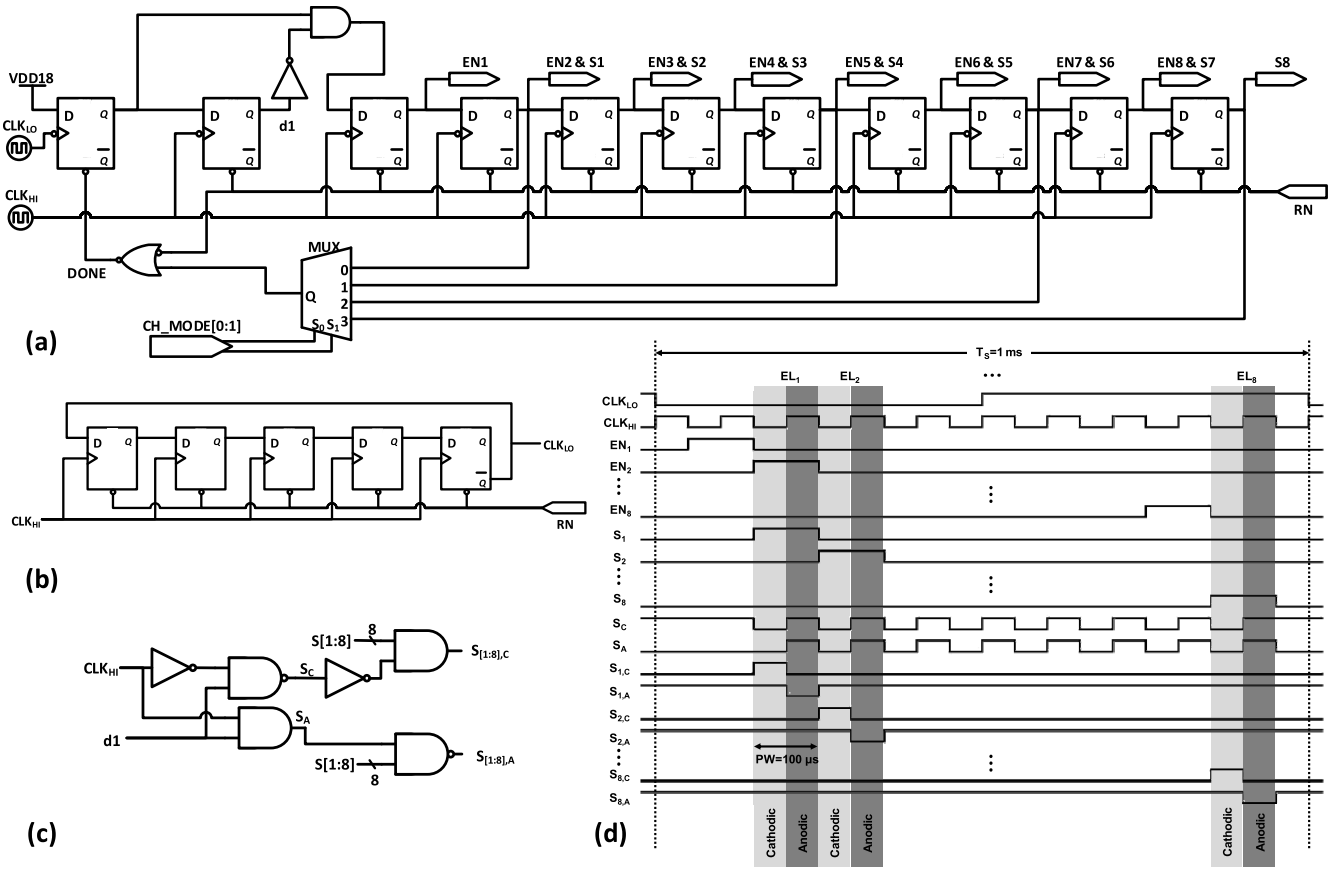

FIGURE 11. (a) Schematic diagram of the resettable one-hot state machine implementation for the control unit, (b) ring counter for generating CLK_{LO} from CLK_{HI}, (c) designed combinational circuit that generates switch matrix control signals, and (d) timing diagram of the control unit for 8-channel operation.

signals using the combinational logic circuit in Fig. 11 (c). Fig. 11 (d) illustrates the control unit timing diagram, which comprises of the control signals for the 8-channel CIS stimulation. Different channel modes can be programmed through "CH_MODE[0:1]" signals. The system can operate with 1, 4, 6 or 8 channels, which allows tradeoffs between sound perception quality and power dissipation. Since the digital control unit is on the 1.8 V supply for reduced power dissipation, control signals are level shifted at the unit interface before being delivered to the high voltage switches.

IV. EFFICIENT NEURAL STIMULATION

The neural stimulator is the most power hungry part of the design, and accounts for more than 90% of the total power dissipation due to the high voltage requirement at the stimulation electrodes. The well-known rectangular constant-current stimulation that is also utilized at commercial cochlear implants suffers from inefficiency of charge transfer and high voltage levels with few undesired consequences, including formation of undesirable chemical products. Although recent studies has improved the efficiency of charge transfer through modified stimulation current waveform shape [28], [41], the peak voltage remains high. Stepped decreasing current in [42] reduces the maximum electrode voltage for retinal prosthesis, but the waveform is not slope-optimized and utilizes limited number of steps at each phase.

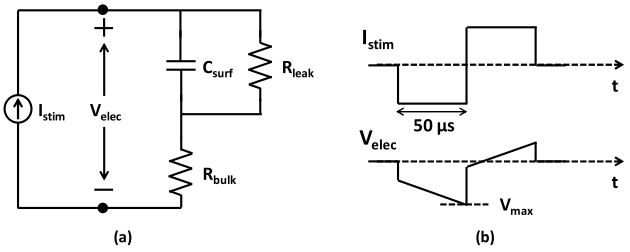

FIGURE 12. (a) Three-element model of the electrode tissue interface, and (b) the electrode current and voltage waveforms.

The conventional model of the electrode tissue interface is depicted in Fig. 12 (a) with three lumped system components. Bulk resistor (R_{bulk}) models the substance between two electrodes, whereas the electrode-tissue interface is modeled with a capacitor (C_{surf}). The leakage resistor (R_{leak}) is used to model the redox reactions occurring at the electrode surface that is connected in parallel with the C_{surf} [43]. R_{leak} is typically ignored, since it has a very large value. Bulk resistance and surface capacitance values have been reported in 1-10 kΩ and 1-10 nF range, respectively [23], [43], [44].

Fig. 12 (b) shows the rectangular stimulation current and the electrode voltage for the given R-C model. The electrode voltage increases during the stimulation and reaches its maximum value at the end of the pulse phase. The maximum electrode voltage can be reduced by applying a non-rectangular pulse shape, i.e. a decreasing current waveform, which maintains a low electrode voltage. Different waveforms such as linear decreasing, exponential decreasing, and Gaussian distributed current pulse shapes were tested with the electrical model to minimize the electrode voltage. The average current per phase must be identical for all to provide the same charge level. Since the stimulation current is supplied through a constant current generator circuit for simplicity, the waveform shape can only be changed in stepped manner, which is the most efficient and practical approach to apply different shapes. The discrete time expressions for different waveform shapes are given in Eq. (6)-(9).

$$I_{rect} = A_{rect}, \tag{6}$$

$$I_{gauss}(n) = A_{gauss} e^{-0.5\left(\frac{n(2\alpha_{gauss})}{N-1}\right)^2}, \tag{7}$$

$$I_{lin}(n) = A_{lin}(K - \alpha_{lin} n), \tag{8}$$

$$I_{ex}(n) = A_{ex} e^{-\alpha_{ex} n}, \tag{9}$$

where A is the amplitude coefficient of the applied currents, α_{gauss} is the coefficient that determines the standard deviation, N is the window length that is determined according to maximum step number, $K = 127$ is the design constant that is obtained from 7-bit current generator (2^6-1), α_{lin} and α_{ex} are the constants used to determine slope of the linear and exponential currents. The maximum step number of the current waveform is determined as N = 10 since any higher N does not provide significant resolution benefit at the electrode [42] while increasing the power dissipation due to higher switching losses. The net charge transferred to the electrodes is preserved at the same level to provide fair comparison across different waveform shapes, with total charge per phase given by:

$$\sum_{n=1}^{10} I(n)\Delta T_{ph} \tag{10}$$

where $I(n)$ is the current amplitude at the nth step and ΔT_{ph} is the current step size. For 50 μs stimulation phase width (T_{ph}) and 10 steps, waveform $\Delta T_{ph} = 5$ μs. The electrode voltage for a given electrical model is the sum of resistor and capacitor voltages, which can be expressed in discrete time domain as in Eq. 11:

$$V_{elec}(k) = R_{bulk} I_{stim}(k) + \frac{1}{C_{surf}} \sum_{i=0}^{k} I_{stim}(i)\Delta t \tag{11}$$

where Δt is the time step for summation, which is chosen as 1 ns ($\ll \tau_{RC}$ and T_{ph}) to provide accurate calculation. Fig. 13 illustrates stimulation currents with different pulse waveform shapes, and corresponding electrode voltages, where all pulses provide 500 μA average current at each

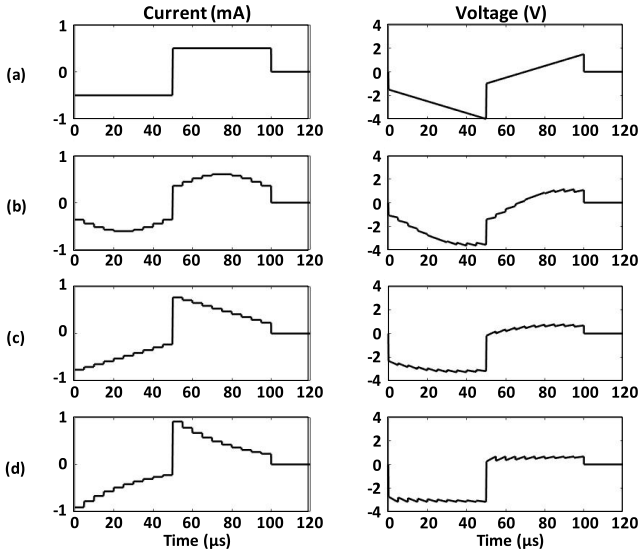

FIGURE 13. Stimulation current and corresponding electrode voltages for (a) rectangular, (b) Gaussian, (c) linear and (d) exponential pulse shapes.

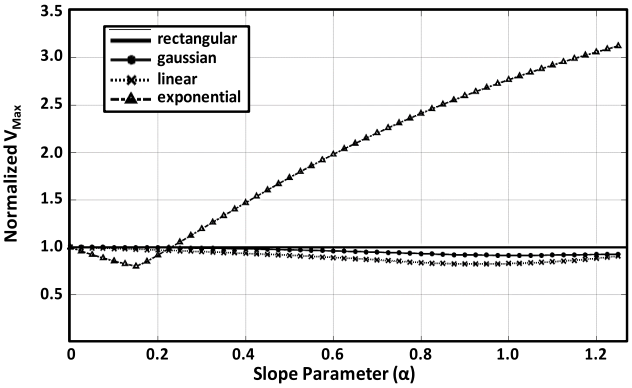

FIGURE 14. Variation of the normalized V_{Max} with the slope parameter (α).

stimulation phase. The electrode-tissue interface model has $R_{bulk} = 3$ kΩ and $C_{surf} = 10$ nF [28]. The waveform shapes are optimized by varying the slope parameter (α) to obtain the lowest maximum electrode voltage at each shape. Maximum electrode voltage (V_{Max}) is shown for each waveform type in Fig. 14, where all values are normalized with respect to the maximum of the rectangular waveform. The optimized waveforms provide 9%, 17% and 20% electrode voltage reduction for Gaussian, linear decreasing and exponential decreasing current pulses, respectively. Hence, the lowest electrode voltage is obtained for exponential decreasing waveform shape, which allows reduction in supply voltage by 20%. The power dissipation of the interface is thus reduced by at least 20% for the same average current, and potentially more depending on the extend of leakage diminution with voltage, which varies significantly with process technology.

V. RESULTS AND DISCUSSION

The micrograph of the 8-channel FICI interface circuit, designed and fabricated in 180nm high-voltage CMOS

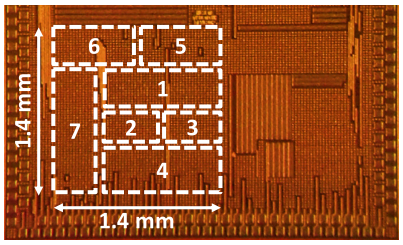

FIGURE 15. Die micrograph of the implemented FICI interface electronics.

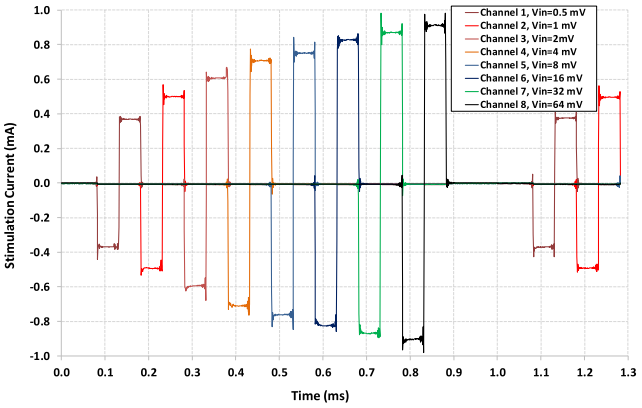

FIGURE 16. Generated 8-channel stimulation (CIS) currents where input peak voltage increases linearly from 0.5 mV (1st channel) to 64 mV (8th channel).

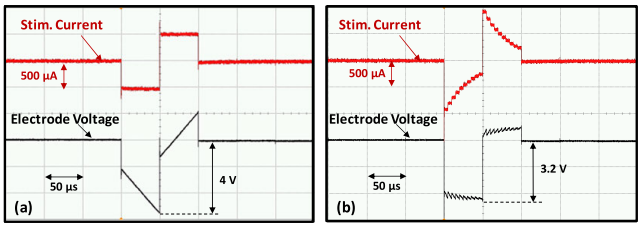

FIGURE 17. Stimulation current and electrode voltage for (a) rectangular and (b) optimized exponential current waveforms.

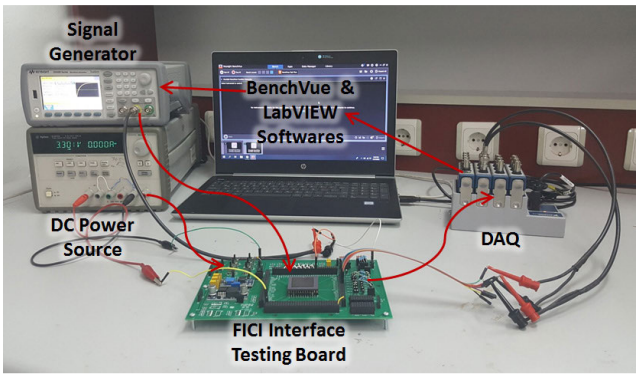

FIGURE 18. Test setup of the FICI Interface electronics with speech signal.

technology, is depicted in Fig. 15, with 1.4x1.4 mm^2 active die area. The interface circuit can be attached to the flexible interconnects through wire bonds or a small package such as QFN32, which has an area of 5x5 mm^2 and can be easily fit into the middle ear. The interface is validated by applying different input voltage levels as sensor output. Fig. 16 illustrates the measurement of the generated 8-channel stimulation currents based on CIS, where current level at each channel can be tuned by changing the digital control signals D_0-D_6. As illustrated, although the input voltage increases linearly from 1st to 8th channel, the stimulation current level changes logarithmically to fit the input to the electrical dynamic range of the ear.

Efficiency of the system is validated next by changing the neural stimulation waveform shape via D_0-D_6 control pins, which are driven from an external FPGA in an automated test environment. Once identified, the most efficient waveform configuration can be permanently stored on-chip using a 7x10 bit ROM to generate the required control bits with negligible power consumption(<1 μW) during regular user mode. Fig. 17 depicts the stimulation current and the electrode voltage for rectangular and optimized exponential decreasing waveforms with artificial neural load ($R_{bulk} = 3$ kΩ and $C_{surf} = 10$ nF [28]). As expected from simulations, optimized waveform shape leads to reduction in the maximum electrode voltage by 20%. Although the amplitude of the optimized stimulation current waveform is higher, the average value is not. The result firmly concedes 1.5 V reduction in high voltage supply, from 7 V to 5.5 V.

The implemented FICI interface electronics is then tested with a speech signal "A white silk jacket goes with any shoes", which is a common sentence utilized in speech-in-noise tests [45]. The environmental sound noise was measured at around 40 dB (sound level of a quite library) with a sound dB meter, before recording the speech. Fig. 18 depicts the test setup. The sound is detected through a microphone, and is converted into digital speech data through Matlab. The mechanical filters presented in [19] are imported into Matlab, and applied to the speech data to mimic the 8 channel PZT sensor output. The mimicked signals are then applied to the FICI interface electronics through Keysight 33522B signal generator, which is controlled by BenchVue software. The output response of the interface electronics is measured through NI9232 high voltage data acquisition board (DAQ) and LabVIEW software. Fig. 19 (a) and (b) show the histogram of the speech signal, and the measured electrodogram from the 8-channel FICI interface, respectively, confirming that different frequency components of the speech are correctly obtained at the corresponding FICI channels. The FICI outputs have high precision at low frequency (<3 kHz), which captures the voice range. The reconstructed speech signal from the stimulation electrodes of the FICI interface electronics (Fig. 20 (b)) is compared against the time-domain waveform of the speech signal recorded by the microphone (Fig. 20 (a)). Although mechanical filters lead to limited perception of high frequency components, the envelope of the reconstructed signal coincides with the envelope of the real speech signal, which validates operation of the interface in a real application (when the input is not a pure sine tone). The

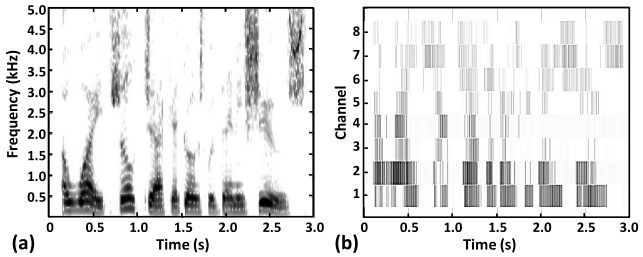

FIGURE 19. (a) Histogram of the speech signal recorded by the microphone, and (b) electrodogram from the stimulation electrodes of 8-channel FICI interface.

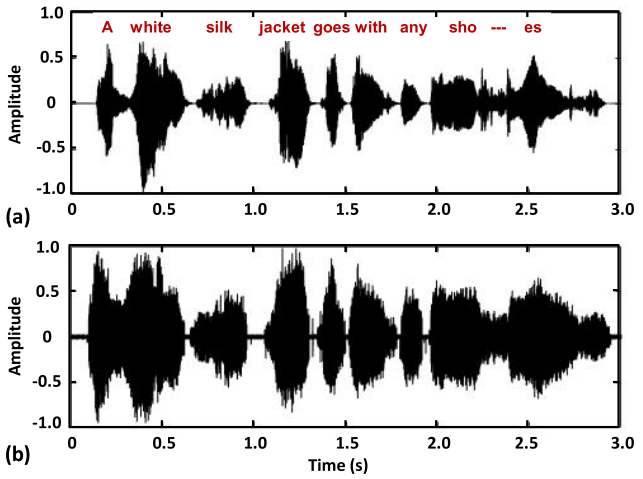

FIGURE 20. Time-domain waveform for (a) the speech signal recorded by the microphone, and (b) the reconstructed speech signal from stimulation electrodes of the FICI interface electronics.

power dissipation for the given speech signal is measured as 472 μW, while operating with the optimized current waveform. The 3-second test, which includes 3000 stimulation pulses, provides a representative average power dissipation for the interface circuit.

Table 1 details the power dissipation analysis of the 8-channel FICI interface electronics for rectangular and optimized exponential current pulse shapes. The optimized waveform enables reduction of the supply voltage of the current stimulator (switch matrix and HV switch control), which is the most power hungry part of the design. Hence, the total power dissipation of the system is reduced by about 20% through waveform shape optimization. Moreover, the front-end signal conditioning circuit (system excluding the stimulator) operates with 19.7 μW, which is one of the lowest values provided in the literature. Table 2 presents comparison of the FICI interface with the state-of-the-art circuits. The input dynamic range of the proposed circuit is similar to the previous reports, and provides adequate perception of the input sound. The input noise floor of the designed system is comparable with the previous state-of-the-art designs. 7-bit patient fitting resolution provides better control of minimum threshold and maximum comfort level of the stimulation current. The circuit predominantly operates in current mode,

TABLE 1. Power consumption of the 8-channel FICI interface circuit.

System Components	Voltage (V)	Power (μW)
Logarithmic Amplifier	1.8	2.1
Current Rectifier	1.8	2.0
Current Multiplier with LPF	3.3	2.3
Sample and Hold	3.3	3.2
Control Block	1.8	2
HV Switch Control	7-10* / 5.5-8**	10.2* / 8.1**
Switch Matrix (Stimulator)	7-10* / 5.5-8**	570* / 452**
Total Power		591.8* / 471.7**

*Rectangular and **Optimized Exponential current wavcforms

TABLE 2. Comparison of FICI interface circuit with state-of-the-art.

Parameters	Sarpeshkar [25]	Georgiou [26]	Yip [28]	This Work
Technology	1.5 μm	0.8 μm	180 nm	**180 nm**
Active Die Area (mm^2)	9.6 x 9.2	3.5 x 6.0	~1.76 x 1.9	**1.4 x 1.4**
Number of Electrodes	16	16	8	**8**
Dynamic Range (dB)	77	60	60	**60**
Input Noise Floor (μV_{rms})	5	-	2.5	2.7
Patient Fitting	7-bit	5-bit	6-bit	**7-bit**
Front-End Power (μW)	211	126	93	**19.7**
Stimulator Power (μW)	-	2000*	479	**452**

* Estimated by the authors and not implemented on the chip

with minimum overhead associated with current-voltage signal translations, and provides the lowest power dissipation both for the front-end signal conditioning and stimulator units.

VI. CONCLUSION

The presented ultra-low power bionic ear interface senses the implantable PZT outputs and stimulates the auditory neurons accordingly. The interface is designed, implemented, and fabricated in 180 nm HV process, and is validated through a speech signal to demonstrate proof-of-concept operation with both circuit design and waveform optimizations. The proposed system is the first FICI interface with 60 dB input dynamic range and patient fitting compatibility (stimulation current from 0 to 1 mA, minimum threshold and maximum comfort levels, respectively) that operates with total power dissipation of ~470 μW. The superior power dissipation profile of the system results from the concomitant optimizations in system architecture, circuit design, and stimulation waveform shape. Sub-500 μW operation of the interface electronics enables long-term system reliability with a lifetime of more than 30 years, using a typical implantable battery

with limited capacity. A major impediment in the prolonged use of cochlear implants is hence overcome, which results in reduction of healthcare cost and risks associated with surgical battery replacements.

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HASAN ULUŞAN received the B.Sc., M.Sc., and Ph.D. degrees in electrical and electronics engineering from Middle East Technical University (METU), Ankara, Turkey, in 2011, 2013, and 2018, respectively. He is currently a Postdoctoral Researcher with Bio Engineering Laboratory, Biosystems Science Engineering Department, ETH Zürich. His research interests include the integrated circuit design, especially for low-power applications, biosensor interfaces, power management circuits for energy harvesting systems, and mixed-signal circuits and systems for wearable and implantable medical applications.

ALI MUHTAROĞLU (SM'06) received the B.S. degree from the University of Rochester, in 1994, the M.S. degree from Cornell University, in 1996, and the Ph.D. degree from Oregon State University, in 2007, all in electrical engineering. He was with Intel Corporation R&D, USA, for 11 years. He joined the Department of Electrical and Electronics Engineering, Middle East Technical University–Northern Cyprus Campus (METU NCC), in 2007, as a Faculty Member, where he is currently chairing the Center for Sustainability. He has numerous publications and holds a number of patents. His experience and research interests include integrated circuit (IC) design, energy harvesting, and low-power system architectures. He has chaired, co-chaired, and served on the technical program committees for various IEEE conferences.

HALUK KÜLAH received the B.Sc. and M.Sc. degrees (Hons.) from Middle East Technical University (METU), Ankara, Turkey, in 1996 and 1998, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, in 2003, all in electrical engineering. During his Ph.D. degree, he worked on micromachined inertial sensors and their interface electronics. From 2003 to 2004, he was a Research Fellow with the Department of Electrical Engineering and Computer Science, University of Michigan. He joined the Electrical and Electronics Engineering Department, METU, as a Faculty Member, in August 2004. His research interests include MEMS, MEMS-based energy scavenging, microsystems for biomedical applications (BioMEMS), and mixed-signal interface electronics design for MEMS sensors. He received the 2009 Research Encouragement Award from the Prof. Mustafa PARLAR Education and Research Foundation, the 2013 Research Encouragement Award from TÜBİTAK, the 2013 IBM Faculty Award, and the 2015 Young Scientist Award from the Turkish Science Academy. He also received the Horizon 2020 ERC Consolidator Grant, in 2015, from the FLAMENCO project, which is on autonomous and fully implantable cochlear implants.