IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 30, 2019, accepted August 24, 2019, date of publication September 3, 2019, date of current version September 18, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2938980

An Asymmetric Switched Capacitor Multilevel Inverter With Component Reduction

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This work was supported in part by the Shaanxi Provincial Special Support Program for Science and Technology Innovation Leader, in part by the Shaanxi Industrial Key Project under Grant 2018GY-165, and in part by the Key Laboratory Research Program from Department of Education of Shaanxi Provincial Government under Grant 18JS081.

ABSTRACT This paper proposes a new switched capacitor (SC-Type) inverter for asymmetrical multilevel inverters (MLIs) with fewer components. In order to balance the voltages of the capacitors, the proposed topology uses a special method to charge/discharge the capacitors. In the proposed inverter, the number of switches, the number of dc voltage sources, the amount of blocked voltage in the switches, and the power losses are reduced. Fewer components result in lower size, complexity, and cost of MLI. Cascade connection of the proposed topology is used to achieve a higher number of output voltage levels. The MATLAB simulations and experimental results of a 25-level MLI verify the good performance of the proposed inverter.

INDEX TERMS Multilevel inverters (MLIs), switched capacitor inverter, asymmetric topology, components reduction.

I. INTRODUCTION

Multilevel inverters (MLIs) have been interested as necessary devices with a wide range of applications which growingly affect the power electronics. They have been considered for many benefits such as high-quality output voltage, better electromagnetic characteristics, low stress on switches, and so on [1]–[6]. They can be used in electric vehicles, photovoltaic systems, wind farms, static compensators, HVDC systems, and electric motor drives [7]–[11].

An MLI is formed by different arrangements of semiconductor switches and dc links to generate *n*-level output waveforms, which are divided into three main classifications [12]–[14]: neutral point clamped (NPC) [15], flying capacitor (FC), and cascaded H-bridge (CHB).

CHB converters are used to a greater extent than other types of converters due to their fewer switches. However, this topology needs several dc voltage sources. Several different methods have been proposed to determine the values of dc sources in CHB converters. One of them is the binary and another is the trinary method [16].

Some new cascaded multilevel inverter topologies have been proposed in [16]–[26]. Each of these topologies has some advantages and disadvantages with a different number of component counts and blocked voltage in switches. The topologies proposed in [19], [21] use an axillary H-bridge in their structures. Therefore, the switches of H-bridge withstand a high voltage level. These topologies are suitable for low-voltage applications. However, the CHB converters and the topologies proposed in [16], [17], and [22] use several H-bridges, allowing the reduction of the blocked voltage in the switches of H-bridge. In [20], a new topology is presented that uses a single developed H-bridge and two dc voltage sources on both sides of the inverter.

One of the most important studies on the MLIs points to the fewer number of dc voltage sources. Therefore, some researchers have tried to reduce the number of dc voltage sources by using capacitors instead of dc voltage sources in the cascaded topologies [27], [28]. However, it becomes complicated to make a balance in the voltage of the capacitors.

This paper proposes a switched capacitor (SC-Type) topology for asymmetrical multilevel inverters (MLIs). In the proposed SC-MLI, the number of components and the blocked voltage in switches are reduced. By reducing the component count, the size, complexity, and the cost of the MLI are reduced. Each proposed basic unit consists of two unequal dc sources, four capacitors, six unidirectional and four bidirectional switches and produces 25 levels in output voltage. In the presented topology, a special method to charge/discharge capacitors is used to keep the voltage

The associate editor coordinating the review of this article and approving it for publication was N. Prabaharan.

TABLE 1. Different switching patterns of the proposed SC-MLI.

V_O	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	Charged cap.
$2V_2+2V_1$	1	1	0	0	1	0	0	0	0	0	C_1-C_4
$2V_2+V_1$	0	1	0	0	1	0	1	0	0	0	C_3, C_4
$2V_2$	0	1	1	0	1	0	0	0	0	0	C_3, C_4
$2V_2$-V_1	0	1	0	0	0	0	1	0	1	0	C_3, C_4
$2V_2$-$2V_1$	0	1	1	0	0	0	0	0	1	0	C_1,C_4
V_2+2V_1	1	0	0	0	1	0	0	1	0	0	C_1, C_2
V_2+V_1	0	0	0	0	1	0	1	1	0	0	-
V_2	0	0	1	0	1	0	0	1	0	0	-
V_2-V_1	0	0	0	0	0	0	1	1	1	0	-
V_2-$2V_1$	0	0	1	0	0	0	0	1	1	0	C_1, C_2
$2V_1$	1	0	0	1	1	0	0	0	0	0	C_1, C_2
V_1	0	0	0	1	1	0	1	0	0	0	-
0	0	0	1	1	1	0	0	0	0	0	C_1-C_4
$-V_1$	0	1	0	0	0	1	1	0	0	0	-
$-2V_1$	0	1	1	0	0	1	0	0	0	0	C_1, C_2
$-(V_2-2V_1)$	1	0	0	0	0	0	0	1	0	1	C_1, C_2
$-(V_2-V_1)$	0	0	0	0	0	0	1	1	0	1	-
$-V_2$	1	0	0	0	0	1	0	1	0	0	-
$-(V_2+V_1)$	0	0	0	0	0	1	1	1	0	1	-
$-(V_2+2V_1)$	0	0	1	0	0	1	0	1	0	0	C_1, C_2
$-(2V_2-2V_1)$	1	0	0	1	0	0	0	0	0	1	C_1,C_4
$-(2V_2-V_1)$	0	0	0	1	0	0	1	0	0	1	C_3, C_4
$-2V_2$	1	0	0	1	0	1	0	0	0	0	C_3, C_4
$-(2V_2+V_1)$	0	0	0	1	0	1	1	0	0	0	C_3, C_4
$-(2V_2+2V_1)$	0	0	1	1	0	1	0	0	0	0	C_1-C_4

balance of the capacitors. In order to verify the performance of the proposed topology, the number of switches, the number of the dc voltage sources, the amount of blocked voltage in the switches, and the power losses in the proposed MLI are compared with several other topologies.

To confirm the performance of the proposed SC-MLI, a 25-level proposed inverter is simulated and experimented whose results verify one another.

II. THE PROPOSED TOPOLOGY

A. BASIC TOPOLOGY

This paper presents a new topology of the switched capacitor asymmetric multilevel inverter consisting of six unidirectional (S_1-S_6) and four bidirectional (T_1-T_4) switches, four capacitors (C_1-C_4), and two unequal dc voltage sources (V_1 *and* V_2). This asymmetric topology can produce 25 levels in the output voltage (12 positive levels, 12 negative levels, and a zero level). The circuit of the proposed basic unit is illustrated in *Fig. 1-a*. Different switching patterns of this topology are shown in *Fig. 1-c* and *Table 1*. In *Table 1*, 1 and 0 represent the on and off states of the switches, respectively. As shown in *Table 1*, this topology can produce 25 levels in the output voltage. In addition, the value of the dc voltage sources is assumed as follows:

$$V_1 = \frac{1}{5}V_2 = V_d \tag{1}$$

where V_d is a base magnitude of input voltage.

B. VOLTAGE BALANCING OF CAPACITORS

Before discussing the expansion of the proposed topology, it is necessary to investigate the voltage balancing between the capacitors in the basic unit. It means that the voltage of capacitor C_1 should be equal to the voltage of capacitor C_2 ($V_{C1} = V_{C2}$). Similarly, the voltage of capacitor C_3 should be equal to the voltage of capacitor C_4 ($V_{C3} = V_{C4}$). For this purpose, the energy released from the capacitor C_1 (C_3) must be equal to the energy released from the capacitor C_2 (C_4) in a cycle of output. Consider a basic unit that supplies an inductive load as shown in *Fig. 1-a*. In *Fig. 1-b*, the typical output voltage of a basic unit is shown in this condition. The voltage and current waveforms of the each positive levels are exactly the same as the related negative one [22]. For example, the voltage and current waveforms of level $+1V_d$ (in the interval $0\sim t_1$) are the same as those of level $-1V_d$ (in the interval $\pi\sim\pi + t_1$). As another example, the voltage and current waveforms of level $+5V_d$ (in the interval $t_4\sim t_5$) are the same as those of level $-5V_d$ (in the interval $\pi + t_4\sim\pi + t_5$). Therefore, the following equations can be written:

$$\int_0^{t_1} [v_o(t).i_o(t)]\,d\omega t = \int_{\pi}^{\pi+t_1} [v_o(t).i_o(t)]\,d\omega \tag{2}$$

$$\int_{t_2}^{t_3} [v_o(t).i_o(t)]\,d\omega t = \int_{\pi+t_2}^{\pi+t_3} [v_o(t).i_o(t)]\,d\omega t \tag{3}$$

where V_O, i_O are output voltage and current, respectively. With this method, the energy released from the capacitor $C_1(C_3)$ is equal to the energy released from the capacitor $C_2(C_4)$. Therefore, the voltage of the capacitor $C_1(C_3)$ remains in balance with the voltage of the capacitor $C_2(C_4)$. It is presented in *Fig. 1-b* that which capacitor(s) must be put to the current path in each output level to achieve the mentioned purpose. Another condition for capacitor voltage balancing is that both capacitors C_1 and C_2 (or C_3 and C_4) be charged equally. For this purpose both capacitors should connected to the dc voltage source at the same times. In last column of Table 1, it is mentioned that which capacitor(s) can be charged in each output levels.

C. TOPOLOGY EXTENSION

Cascaded connection of the proposed topology leads to achieving more levels at the output voltage. *Fig. 1-d* shows the extension of the proposed topology. As shown in *Fig. 1-d*, the sum of the output voltage of different units gives the total output voltage of the inverter as follows:

$$V_o = V_{o1} + V_{o2} + \ldots + V_{on} \tag{4}$$

where V_{O1}, $V_{O2}, \ldots V_{On}$ are output voltage of unit_1, $\text{unit}_2, \ldots \text{unit}_n$, respectively in cascaded inverter. *Table 2* shows the switching pattern of the proposed cascaded MLI. As shown in *Table 2*, for each level, just three switches from each unit are in the current path. This reduces conduction loss. In the proposed cascaded MLI, the value of the dc voltage sources for the *i-th* unit can be calculated as follows:

$$V_{1i} = \frac{V_{2i}}{5} = 25^{i-1}.V_d \tag{5}$$

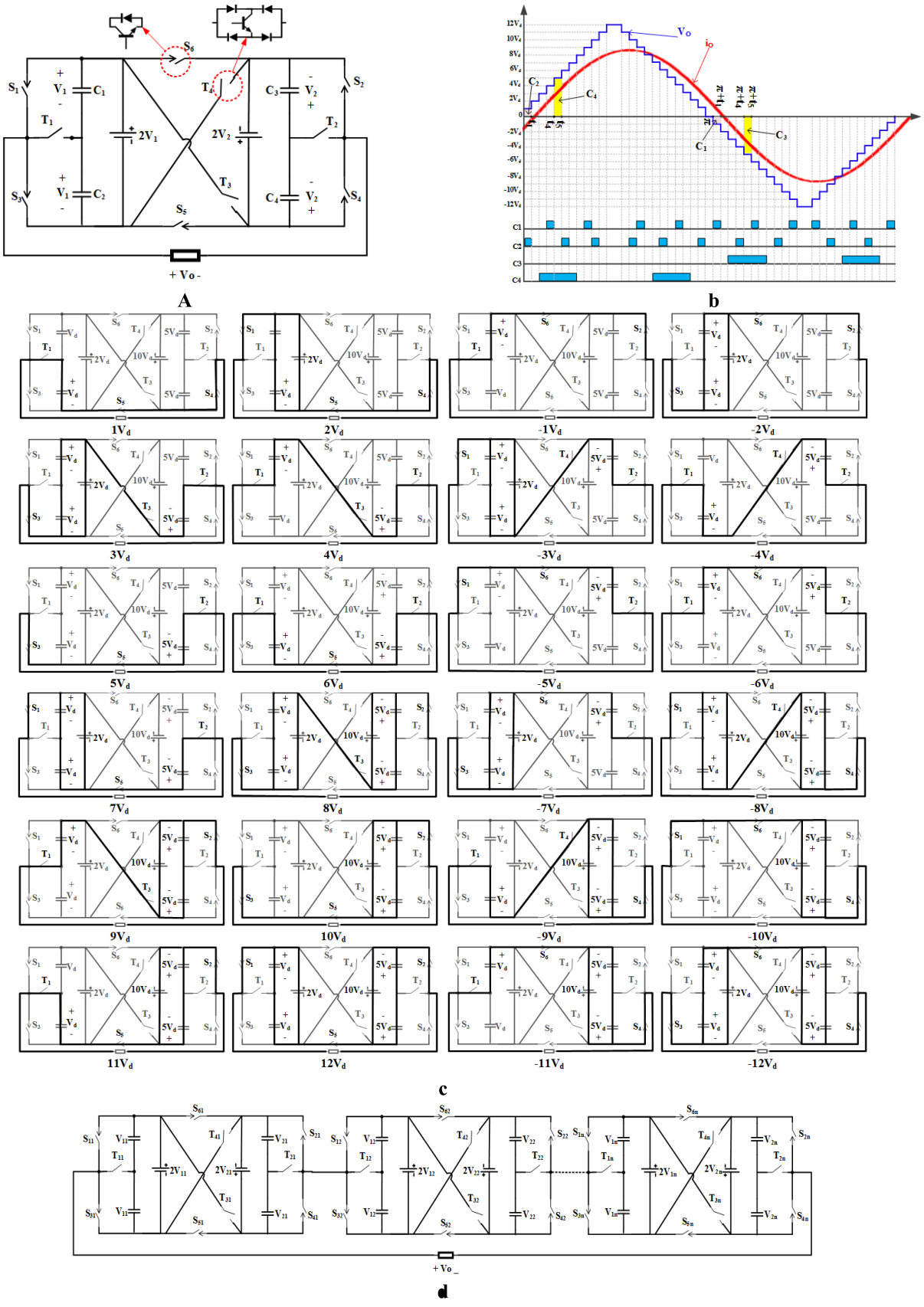


FIGURE 1. Proposed inverter; a) basic unit; b) Typical output of a 25-level topology; c) Different switching states of the proposed SC-MLI d) Proposed cascaded multi-level topology.

TABLE 2. The different switching pattern of the proposed cascaded MLI.

ON-State Switches				Output voltage of each unit [p.u]				
U_1	U_2	…	U_n	V_1	V_2	…	V_n	V_O
S_{11},S_{21},S_{51}	S_{12},S_{22},S_{52}	…	S_{1n},S_{2n},S_{5n}	12	12*25	…	$12*25^{n-1}$	$[(25^n-1)/2]$
S_{21},S_{51},T_{11}	S_{12},S_{22},S_{52}	…	S_{1n},S_{2n},S_{5n}	11	12*25	…	$12*25^{n-1}$	$[(25^n-1)/2]$-1
…	…	…	…	…	…	…	…	…
S_{11},S_{21},S_{51}	S_{22},S_{52},T_{12}	…	S_{1n},S_{2n},S_{5n}	12	11*25	…	$12*25^{n-1}$	$[(25^n-1)/2]$-25
S_{21},S_{51},T_{11}	S_{22},S_{52},T_{12}	…	S_{1n},S_{2n},S_{5n}	11	11*25	…	$12*25^{n-1}$	$[(25^n-1)/2]$-26
…	…	…	…	…	…	…	…	…
S_{11},S_{21},S_{51}	S_{12},S_{22},S_{52}	…	S_{2n},S_{5n},T_{1n}	12	12*25	…	$11*25^{n-1}$	$[(25^n-1)/2]$-25^{n-1}
S_{21},S_{51},T_{11}	S_{12},S_{22},S_{52}	…	S_{2n},S_{5n},T_{1n}	11	12*25	…	$11*25^{n-1}$	$[(25^n-1)/2]$-25^{n-1}-1
…	…	…	…	…	…	…	…	…
S_{41},S_{51},T_{11}	S_{32},S_{42},S_{52}	…	S_{3n},S_{4n},S_{5n}	1	0	…	0	1
S_{31},S_{41},S_{51}	S_{32},S_{42},S_{52}	…	S_{3n},S_{4n},S_{5n}	0	0	…	0	0
S_{21},S_{61},T_{11}	S_{32},S_{42},S_{52}	…	S_{3n},S_{4n},S_{5n}	-1	0	…	0	-1
…	…	…	…	…	…	…	…	…
S_{41},S_{61},T_{11}	S_{32},S_{42},S_{62}		S_{4n},S_{6n},T_{1n}	-11	-12*25		$-11*25^{n-1}$	-$[(25^n-)/2]$+25^{n-1}+1
S_{31},S_{41},S_{61}	S_{32},S_{42},S_{62}		S_{4n},S_{6n},T_{1n}	-12	-12*25		$-11*25^{n-1}$	-$[(25^n-)/2]$+25^{n-1}
…	…	…	…	…	…	…	…	…
S_{41},S_{61},T_{11}	S_{42},S_{62},T_{12}	…	S_{3n},S_{4n},S_{6n}	-11	-11*25	…	$-12*25^{n-1}$	-$[(25^n-)/2]$+26
S_{31},S_{41},S_{61}	S_{42},S_{62},T_{12}	…	S_{3n},S_{4n},S_{6n}	-12	-11*25	…	$-12*25^{n-1}$	-$[(25^n-)/2]$+25
…	…	…	…	…	…	…	…	…
S_{41},S_{61},T_{11}	S_{32},S_{42},S_{62}	…	S_{3n},S_{4n},S_{6n}	-11	-12*25	…	$-12*25^{n-1}$	-$[(25^n-)/2]$+1
S_{31},S_{41},S_{61}	S_{32},S_{42},S_{62}	…	S_{3n},S_{4n},S_{6n}	-12	-12*25	…	$-12*25^{n-1}$	-$[(25^n-1)/2]$

III. CALCULATION OF BLOCKED VOLTAGE IN THE SWITCHES

The other important parameter that affects the cost of an inverter is the blocked voltage of all switches (V_{sw}) because its reduction will contribute to the reduction of costs. The following equations can be written to calculate this parameter:

$$V_{sw} = V_{sw,u} + V_{sw,b} \tag{6}$$

where $V_{sw,u}$ and $V_{sw,b}$ are the blocked voltage in unidirectional and bidirectional switches, respectively. $V_{sw,u}$ is obtained as follows:

$$V_{sw,u} = \sum_{i=1}^{n} \sum_{k=1}^{6} V_{S_{ki}} \tag{7}$$

where n is the number of cascaded units. Also, V_{Ski} is the voltage blocked in the unidirectional switch of S_{ki} in the *i-th* unit. The blocked voltage of unidirectional switches in the *i-th* unit ($i = 1, 2 \ldots, n$) can be calculated as follows:

$$V_{S_{1i}} = V_{S_{3i}} = 2V_{1i} \tag{8}$$

$$V_{S_{2i}} = V_{S_{4i}} = 2V_{2i} = 10\ V_{1i} \tag{9}$$

$$V_{S_{5i}} = V_{S_{6i}} = 2V_{2i} = 10\ V_{1i} \tag{10}$$

where $V_{S1i}, V_{S2i,\ldots,} V_{S6i}$ are the blocked voltage in the unidirectional switches of S_{1i},S_{2i},…,S_{6i} at the *i-th* unit, respectively. So, the total blocked voltage in the unidirectional switches in the proposed cascaded MLI is:

$$V_{sw,u} = \sum_{i=1}^{n} 44\ V_{1i} \tag{11}$$

Similarly, $V_{sw,b}$ can be written as:

$$V_{sw,b} = \sum_{i=1}^{n} \sum_{k=1}^{4} V_{T_{ki}} \tag{12}$$

where V_{Tki} is the blocked voltage in the *k-th* bidirectional switch in the *i-th* unit (T_{ki}). Firstly, the blocked voltage in the bidirectional switches of the *i-th* unit is obtained to simplify the calculation. Then, the results can be extended for other units.

$$V_{T_{1i}} = V_{1i} \tag{13}$$

$$V_{T_{2i}} = V_{2i} = 5\ V_{1i} \tag{14}$$

$$V_{T_{3i}} = V_{T_{4i}} = 2\,V_{2i} = 10\ V_{1i} \tag{15}$$

where V_{T1i}, $V_{T2i,}V_{T3i}$ and V_{T4i} are the blocked voltage in the bidirectional switches of T_{1i}, T_{2i}, T_{3i} and T_{6i} at the *i-th* unit, respectively. Therefore, the total blocked voltage in the bidirectional switches in a cascaded converter can be written as follows:

$$V_{sw,b} = \sum_{i=1}^{n} 26\ V_{1i} \tag{16}$$

Substituting (12) and (16) in (6), the value of the total blocked voltage in all switches is obtained as follows:

$$V_{sw} = V_{sw,b} + V_{sw,u} = \sum_{i=1}^{n} 70\ V_{1i} \tag{17}$$

The maximum output voltage of the proposed MLI is given by:

$$V_{O,max} = \sum_{i=1}^{n} 2\ V_{1i} + 2\ V_{2i} = 12 \sum_{i=1}^{n} V_{1i} \tag{18}$$

TABLE 3. Equations of proposed MLI.

	number of units (n)	number of levels (N_{level})
units (n)	n	$log_{25}(N_{level})$
levels (N_{level})	25^n	N_{level}
switches (N_{sw})	$14n$	$14\ log_{25}(N_{level})$
sources (N_{source})	$2n$	$2\ log_{25}(N_{level})$
capacitors (N_{cap})	$4n$	$4\ log_{25}(N_{level})$
($V_{O,max}$)	$(25^n\text{-}1)/2$	$(N_{level}\text{-}1)/2$
blocked voltage (V_{sw})	$35(25^n\text{-}1)/12$	$35(N_{level}\text{-}1)/12$

By combining (17) and (18), we have:

$$V_{sw} = \frac{70}{12} V_{O,max} = 5.83\ V_{O,max} \tag{19}$$

Also, the relationship between $V_{O,max}$ and the number of output levels (N_{level}) is as follows:

$$V_{O,max} = \frac{N_{level} - 1}{2} \tag{20}$$

By combining (19) and (20), the value of V_{sw} is obtained as follows:

$$V_{sw} = \frac{35}{12}(N_{level} - 1) = 2.92(N_{level} - 1) \tag{21}$$

Table 3 shows the number of output levels (N_{level}), the number of switches (N_{sw}) the number of dc voltage sources (N_{source}), the number of capacitors (N_{cap}, the maximum output voltage ($V_{O,max}$), and the blocked voltage in switches (V_{sw}) based on the number of cascaded units (n) and the number of levels (N_{level}).

IV. COMPARISON OF THE PROPOSED INVERTER WITH OTHER TOPOLOGIES

To verify the proposed cascaded MLI, a comparison is made with some conventional topologies in terms of the number of components and blocked voltage in switches in this section. The proposed converter is compared with binary and trinary CHB [16] topologies and the topologies presented in [17]–[24].

Fig. 2-a depicts a comparison of the number of power switches against the number of levels for the proposed topology and other topologies. Like the topology proposed in [20], our inverter clearly requires the lowest number of switches than the topologies proposed in [16]–[19], [21]–[26].

Fig. 2-b compares the blocked voltage on switches for different topologies. This comparison shows that the blocked voltage in the switches of the proposed topology is lower than that of the proposed topologies in [17], [21], [22] and [26]. However, the inverter proposed in [19], [20], [23]–[25] and binary CHB have lower values. But, it is clear that these topologies require more switches than the presented topology.

Fig. 2-c compares the number of dc voltage sources in terms of the number of levels. According to the figure,

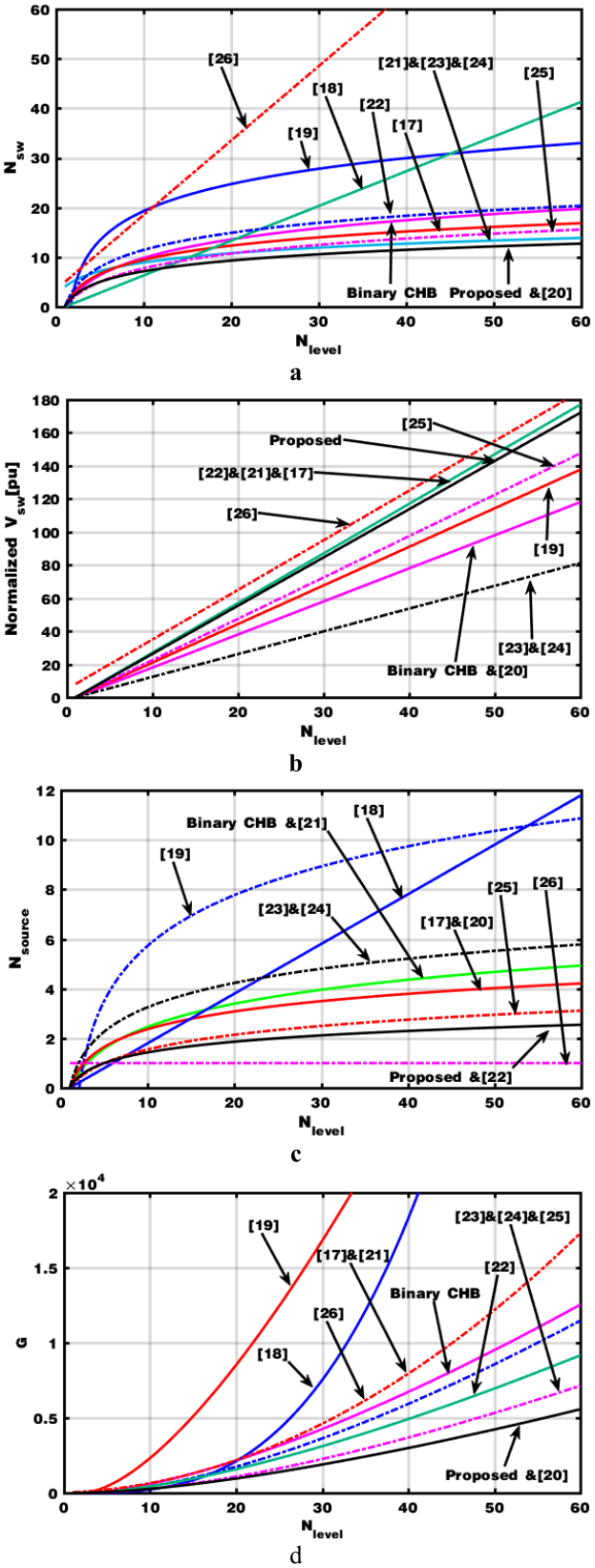


FIGURE 2. Comparison of different topologies; a) Comparison of N_{sw}; b) Comparison of V_{sw}; c) Comparison of N_{source}; d) Comparison of G coefficient.

TABLE 4. Comparison between the proposed topology and suggested structures in [16]–[26].

parameter	*Binary CHB*	*[17]*	*[18]*	*[19]*	*[20]*	*[21]*	*[22]*	*[23&24]*	*[25]*	*[26]*	*Proposed SCMLI*
N_{level}	31	49	31	25	49	31	25	17	17	25	25
N_{level}/N_{SW}	1.94	3.06	1.48	1.25	3.5	2.11	1.56	1.7	1.7	0.61	1.79
N_{level}/N_{Source}	7.75	12.25	5.16	4.17	12.25	7.75	12.5	4.25	8.5	25	12.5
$V_{block}/V_{O,\max}$	4	6	4.4	4.66	4	6	6	2.75	5	6.67	5.83
G/N_{level}	123.87	188.08	268.25	268.8	94.04	139.35	92.16	51.76	47.06	131.2	78.4
TDR/P_O	4	6	4.4	4.66	4	6	6	2.75	5	6.67	5.83

the proposed topology has the fewest number of dc sources like the topology in [22] except than topology of [26].

Another parameter in comparison is related to estimation of overall cost. The cost of the multilevel inverter has a direct relationship with the number of its components such as IGBTs and dc voltage sources and the voltage rating of IGBTs [29]. This is true for multilevel volume and size. Considering this fact, in order to compare the proposed topologies with other multilevel topologies from the viewpoint of cost and size, the G coefficient is defined as follows:

$$G = (N_{sw}) \times (N_{source}) \times (V_{sw}^{pu}) \tag{22}$$

According to equations at Table.3 and (21), the G coefficient can be written as follows:

$$\begin{aligned} G &= 14\log_{25}(N_{level})) \times (2\log_{25}(N_{level})) \times 2.92 \ \ (N_{level}-1) \\ &= 81.76\left[\log_{25}(N_{level})\right]^{2} \times \ (N_{level}-1) \end{aligned} \tag{23}$$

Fig. *2-d* shows the variation of G coefficient versus the number of voltage levels at the output. The smaller G means lower cost, weight, and size of the multilevel inverter. Fig. *2-d* shows that the proposed topology and topology presented in [20] have lower cost and size than the topologies presented in [16]–[26].

The last parameter in comparison is total device rating (TDR) of inverter. Each switching device in the proposed inverter is subject to a current stress equal to the load current (I_{ac}) and the voltage stress of each switch is equal to blocked voltage on it. Therefore TDR of the proposed topology calculated as follows:

$$\begin{aligned} TDR &= \sum_{i=1}^{N_{sw}} TDR_{s_i} \\ &= \sum_{i=1}^{N_{sw}} (voltage\ stress\ of\ s_i) \times (current\ stress\ of\ s_i) \\ &= I_{ac} \times \sum_{i=1}^{N_{sw}} V_{sw,s_i} = 5.83 \times I_{ac} \times V_{o,max} = 5.83 P_o \end{aligned} \tag{24}$$

where TDR_{Si} is devise rating of switch S_i and P_O is total output power. Table.4 provides a comprehensive comparison between the proposed topology and those presented in [16]–[26] from different view point. Obviously, with respect to the amounts of proportion of number of output voltage levels to number of needed components, the proposed topology requires minimum number of components as compared to their pertinent counterparts. For example, the suggested structures in [19], [22] and [26] require 20, 16 and 41 power switches to generate 25 levels of output voltage, respectively, while the proposed topology requires only 14 power switches for its 25- level structure. Meanwhile, for this considerable number of output voltage levels, the per unit value of total blocked voltage in the proposed 25-level structure is less than of that the structure of [17], [21], [22], [26]. According to above comparison, the proposed topology requires lower switches, lower dc voltage sources and has lower cost and size than others. However the blocked voltage is a large amount, yet.

V. CALCULATION OF LOSSES

There are two important types of losses in switches: 1) conduction losses; and 2) switching losses. *Fig. 3-a* shows typical power losses on switch voltage and current curve.

A. CONDUCTION LOSSES

Conduction loss (P_{cond}) is defined in ON-state of switches. A switch consists of a transistor and an anti-parallel diode. Therefore, the conduction losses of a transistor ($P_{cond,T}$) and a diode ($P_{cond,D}$) are defined as follows:

$$p_{cond,T} = \left[V_T + R_T.i^{\beta}(t)\right] i(t) \tag{25}$$

$$p_{cond,D} = \left[V_D + R_D.i(t)\right] i(t) \tag{26}$$

where V_T and V_D are the on-state drop voltage of the transistor and anti-parallel diode, respectively. Also, R_T and R_D are the on-state equivalent resistance of the transistor and anti-parallel diode, respectively. β is a constant related to the specifications of the transistor. Each transistor and its anti-parallel diode is conducting for (π-φ) radian and (φ) radian in the half cycle of output, respectively in which φ represents

the power factor angle. Therefore, the total conduction losses of the switches can be written as follows:

$$P_{cond} = \frac{1}{\pi}\int_{0}^{\varphi} p_{cond,D}\,d\omega t + \frac{1}{\pi}\int_{\varphi}^{\pi} p_{cond,T}\,d\omega t \tag{27}$$

Fig. 3-b show the normalized conduction loss of different topologies. According to this figure, the proposed inverter has the lowest conduction loss among all comparison topologies

B. SWITCHING LOSSES

It is assumed that the variations of the current and the voltage of a switch during turn-on and turn-off periods are linear. The dissipated energy in the turn-on period ($E_{on,k}$) and the energy loss in the turn-off period ($E_{off,k}$) of the *k-th* switch can be calculated as follow:

$$\begin{aligned} E_{on,k} &= \int_{0}^{t_{on}} v(t).i(t)\,dt \\ &= \int_{0}^{t_{on}} \left[\left(\frac{V_{SW,k}}{t_{on}}t\right).\left(-\frac{I}{t_{on}}(t-t_{on})\right)\right]dt \\ &= \frac{V_{SW,k}.I.t_{on}}{6} \end{aligned} \tag{28}$$

$$\begin{aligned} E_{off,k} &= \int_{0}^{t_{off}} v(t).i(t)\,dt \\ &= \int_{0}^{t_{off}} \left[\left(\frac{V_{SW,k}}{t_{off}}t\right).\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt \\ &= \frac{V_{SW},k.I.t_{off}}{6} \end{aligned} \tag{29}$$

where $E_{on,k}$ and $E_{off,k}$ are the turn-on and turn-off losses of the switch k, t_{on} and t_{off} are the turn-on and turn-off times of the switch, I is the current through the switch before (after) turning off (on), and V_{sw} is the OFF-state voltage on the switch k. Thus, the energy loss ($E_{sw,m}$) in the *m-th* unit and the total switching loss (P_{sw}) in the cascaded configuration is obtained as follows:

$$E_{sw,m} = \sum_{k=1}^{N_{sw}}\left(\sum_{i=1}^{N_{on,k}} E_{on,k,i} + \sum_{i=1}^{N_{off,k}} E_{off,k,i}\right) \tag{30}$$

$$P_{sw} = \sum_{m=1}^{n} f_m.E_{sw,m} \tag{31}$$

where N_{sw} is the number of switches in a basic unit, $N_{on,k}$ and $N_{off,k}$ are the number of turn-on and turn-off of the switch k during a period of output. Also, $E_{on,ki}$ and $E_{off,ki}$ are the energy loss of the switch k during the *i-th* turn-on and turn-off, respectively. f_m is the switching frequency of the *m-th* unit and n is the number of the cascaded units.

The total losses of the MLI will be:

$$P_{loss} = P_{sw} + P_{cond} \tag{32}$$

Fig. 3-c presents the normalized switching loss of different topologies. According to this figure, the switching loss of the proposed inverter is less than that of the Binary CHB and topologies presented in [19], [22]–[24] and more than that of topologies suggested in [17] and [20], [21].

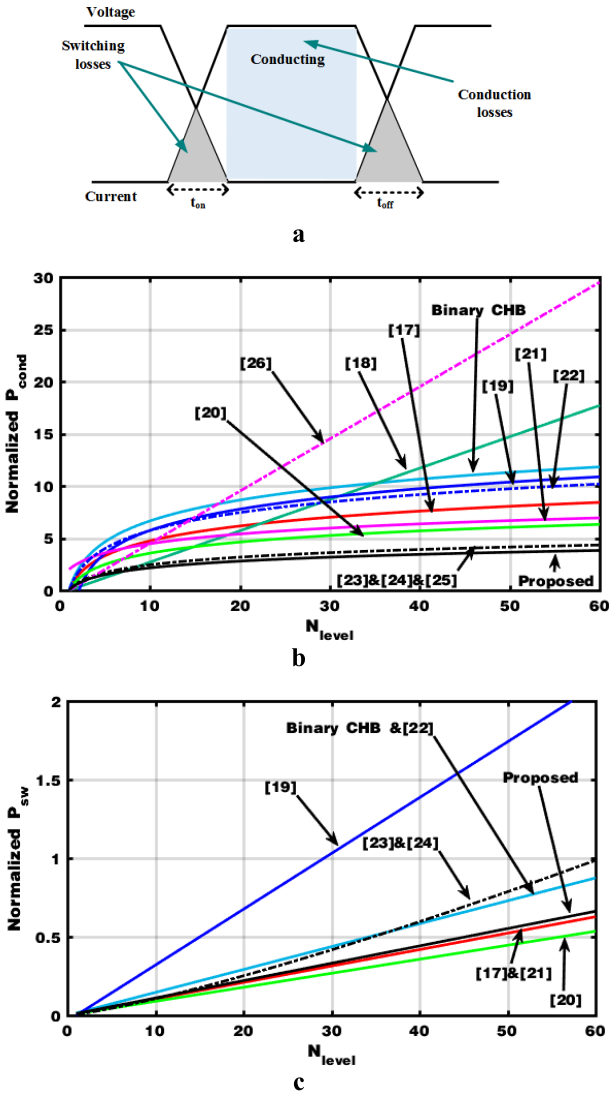


FIGURE 3. Power losses: a) typical power losses of switches; b) Comparison of normalized conduction loss; c) Comparison of normalized switching loss of different MLIs.

C. VARIATION OF SWITCHING LOSS OF THE PROPOSED INVERTER AGAINST THE OPERATING POINT

The output load current can be supposed as (33), where R and L are the resistance and inductance of the load, respectively. Also ω is the output frequency [30].

$$I_L = \frac{\sqrt{2}E}{\sqrt{R^2+L^2\omega^2}}\sin(\omega t - a\tan(\frac{L\omega}{R})) \tag{33}$$

Table 5 presents the inverter level changes in a half cycle of output voltage (from negative peak to positive peak of output). This table was derived from *Table 1* and *Fig.1* in section *II*. According to this table, the output voltage of the proposed structure changes *24* times in a half cycle of output. Column *3* of *Table 5* indicate switches which are turning ON/OFF in the end of related state. Column *4* of *Table 5* present the total blocked voltage of switches (V_{Bk}) The

TABLE 5. Inverter level changes in half cycle of output voltage (*from negative peak to positive peak of output*).

State (k)	Level change	State changing Switches	V_{Bk}	Time of State change (t_k)
1	From -12 to -11	S_3, T_1	$2V_d$	Sin wt=-11/12
2	From -11 to -10	S_1, T_1	$2V_d$	Sin wt=-10/12
3	From --10 to -9	S_1, S_6, T_1, T_4	$6V_d$	Sin wt=-9/12
4	From -9 to -8	S_1, T_1	$2V_d$	Sin wt=-8/12
5	From -8 to -7	S_1, S_3, S_4, S_6, T_2, T_4	$18V_d$	Sin wt=-7/12
6	From -7 to -6	S_3, T_1	$2V_d$	Sin wt=-6/12
7	From -6 to -5	S_1, T_1	$2V_d$	Sin wt=-5/12
8	From -5 to -4	S_1, S_6, T_1, T_4	$6V_d$	Sin wt=-4/12
9	From -4 to -3	S_1, T_1	$2V_d$	Sin wt=-3/12
10	From -3 to -2	S_1, S_2, S_3, S_6, T_2, T_4	$18V_d$	Sin wt=-2/12
11	From -2 to -1	S_3, T_1	$2V_d$	Sin wt=-1/12
12	From -1 to 0	S_2, S_3, S_4, S_5, S_6, T_1	$46V_d$	Sin wt=0
13	From 0 to 1	S_3, T_1	$2V_d$	Sin wt=1/12
14	From 1 to 2	S_1, T_1	$2V_d$	Sin wt=2/12
15	From 2 to 3	S_1, S_3, S_4, S_5, T_2, T_3	$18V_d$	Sin wt=3/12
16	From 3 to 4	S_3, T_1	$2V_d$	Sin wt=4/12
17	From 4 to 5	S_3, S_5, T_1, T_3	$6V_d$	Sin wt=5/12
18	From 5 to 6	S_3, T_1	$2V_d$	Sin wt=6/12
19	From 6 to 7	S_1, T_1	$2V_d$	Sin wt=7/12
20	From 7 to 8	S_1, S_2, S_3, S_5, T_2, T_3	$18V_d$	Sin wt=8/12
21	From 8 to 9	S_3, T_1	$2V_d$	Sin wt=9/12
22	From 9 to 10	S_3, S_5, T_1, T_3	$6V_d$	Sin wt=10/12
23	From 10 to 11	S_3, T_1	$2V_d$	Sin wt=11/12
24	From 11 to 12	S_1, T_1	$2V_d$	Sin wt=1

blocked voltage of the level is defined as sum of the blocked voltage of switches which are turned ON/OFF in related level state. In the column *5* of this table, the starting time of related level change (t_k) are calculated. For example, at *State1* output voltage start to change from level $-12V_d$ to level $-11V_d$ at time of $\omega t_1 = asin(-11/12)$. According to *Table1*, in the end of this state, switch S_3 turns OFF and switch T_1 turns ON. According to *Fig.1-c* the voltage blocked in switch S_3 after it turns OFF is equal to $1V_d$. Also, the voltage blocked in switch T_1 before it turns ON is equal to $1V_d$. Therefore total blocked voltage related this state is equal to $V_{B1} = 2V_d$.

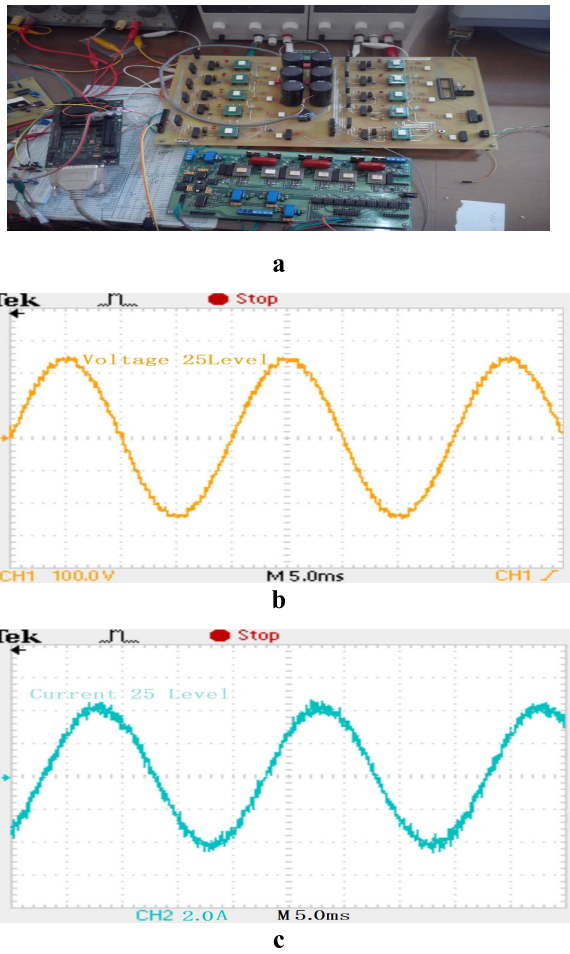
The switching loss of the inverter in a cycle can be determined as (34) in a cycle of the proposed inverter, where t_{on} is the turning ON/OFF time of the switches (supposed equal for all of them), respectively. Also, V_{Bk} and I_k are total blocked voltage and output current of the related state, respectively.

$$E_{SW} = \frac{2\,t_{on}}{6} \sum_{k=1}^{24} V_{Bk}.\ |I_k| \tag{34}$$

By applying the simulation and experimental results of section *VI* in equation (34), the switching loss of proposed inverter for a cycle of output can be calculated. Suppose the load is $\boldsymbol{R} = \mathbf{50\Omega}$ and $\boldsymbol{L} = \mathbf{100}\boldsymbol{mH}$ in series, $t_{on} = 20\mu s$, $V_d = 20V$. *Table 6* indicate the switching loss of the proposed inverter for simulation and experimental in a cycle of output. As it is clear, some differentiates exist between simulation and experimental results due to voltage drop of capacitors and other inverter components.

TABLE 6. Switching loss of the proposed inverter.

Parameter	$\sqrt{2}E$	I_{max}	E_{SW} (j)
simulation	*240*	*4.064*	*0.0506*
Experimental	*236*	*4.00*	*0.0496*



a

b

c

FIGURE 4. Experimental results; a) The experimental set up circuit scheme; b) output voltage, c) output current.

VI. EXPERIMENTAL AND SIMULATION RESULTS

To examine the performance of the proposed inverter and cascaded topology, the experimental and simulation results of a *25*-level basic unit, the experimental results of a *49*-level inverter and the simulation results of a *625*-level cascaded converter (two cascaded units) are presented. Also, the load is considered *R-L* with values of $R_O = 50\Omega$ and $L_O = 100\ mH$ for the simulation and experimental works.

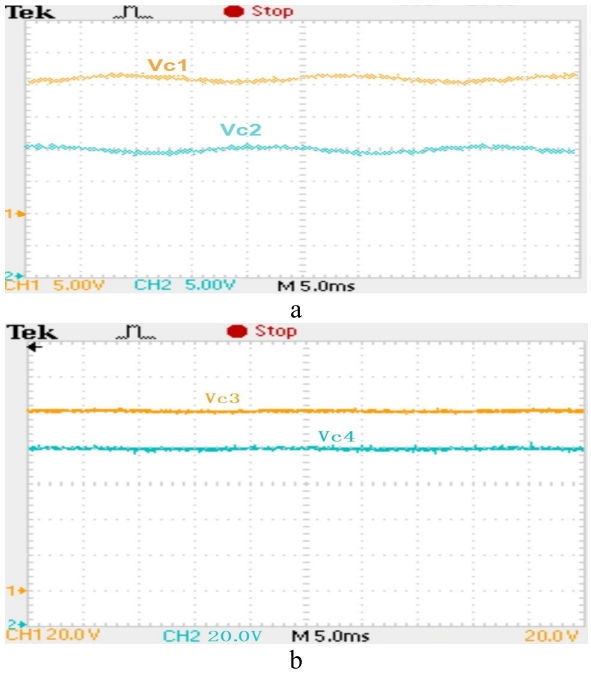


FIGURE 5. The voltage of capacitors in the 25-level inverter: a) V_{C1}, & V_{C2}, b) V_{C3} & V_{C4}.

A. EXPERIMENTAL AND SIMULATION RESULTS OF 25- LEVEL INVERTER

For experimental tests, the switch gating control is carried out by EZDSP2812 which produces the switching pulses. The switches are IGBTs from the BUP306D and BUP306. The nearest level method is used to control the inverter and its gating. The experimented inverter setup is shown in *Fig. 4-a*. The dc voltage values are considered $V_1 = 20V$ and $V_2 = 100V$. Based on *Table 3*, the maximum output voltage of an inverter is $V_O = 240V$, which has 25 levels.

Fig. 4 (b, c) shows the experimental output voltage and current of a *25*-level inverter, respectively. According to *Fig. 4 (b, c)*, the output current has some phase differences from the output voltage, and the current waveform is similar to the sinusoidal waveform, which is due to the inductive characteristic of the load. The maximum output voltage is *240* v which has *25* levels. The voltage of the capacitors is shown in *Fig. 5*. As it is clear from the figure, the voltage of the capacitor $C_2(C_4)$ and the voltage of the capacitor $C_1(C_3)$ are equal ($V_{C1} = V_{C2} = 20\ v \& V_{C3} = V_{C4} = 100\ v$) because the dissipated energy from the capacitors $C_1(C_3)$ and $C_2(C_4)$ are equal referred to the topology design.

Fig. 6 show the simulation results of 25- level inverter. *Fig. 6-a and b* show the voltage and current waveforms with their harmonic spectra. The *FFT* analysis shows that *THD* of the output voltage and current are equal to *3.25%* and *0.20%*, respectively.*Fig.6-c* indicate the voltage waveforms of the bidirectional switches in the 25-level inverter. It shows

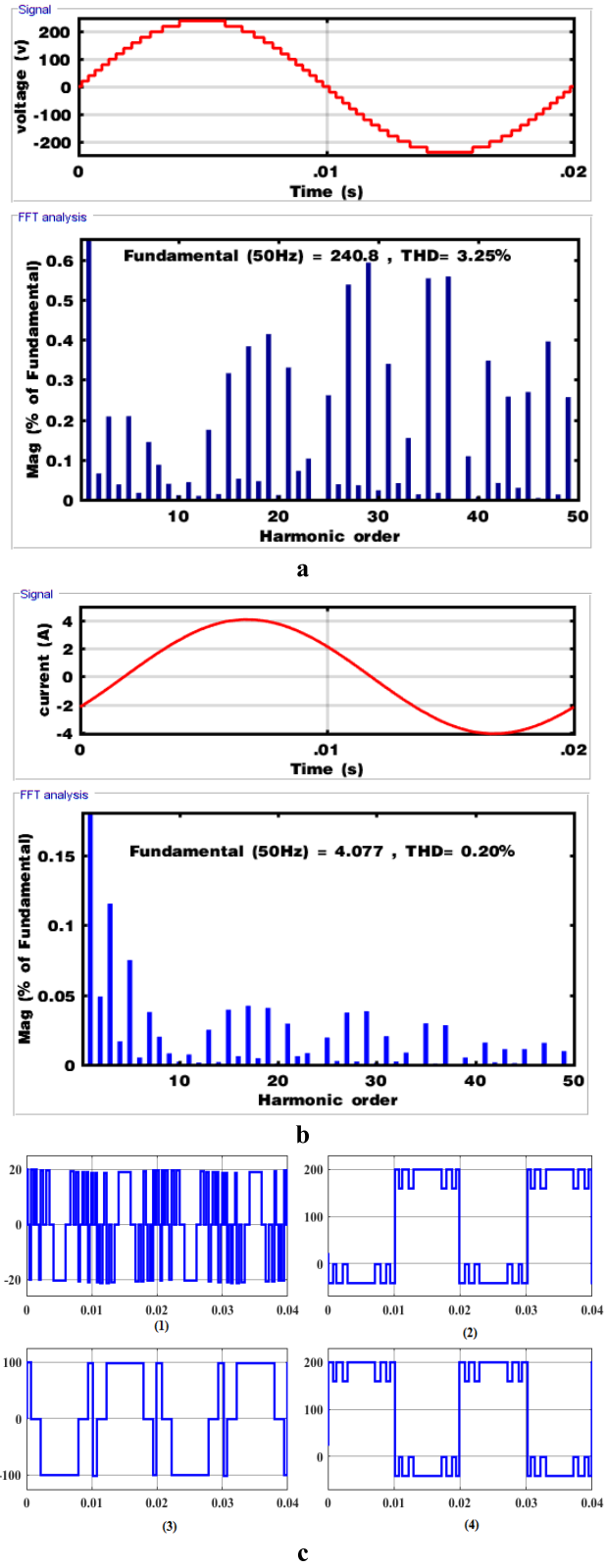


FIGURE 6. Simulation results a) Output voltage waveform with harmonic spectrum of 25-level inverter; b) Output current waveform with harmonic spectrum of 25-level inverter; c) Voltage waveforms of bidirectional switches in the 25-level inverter: 1) *T1*, 2) *T3*, 3) *T2* and 4) *T4*.

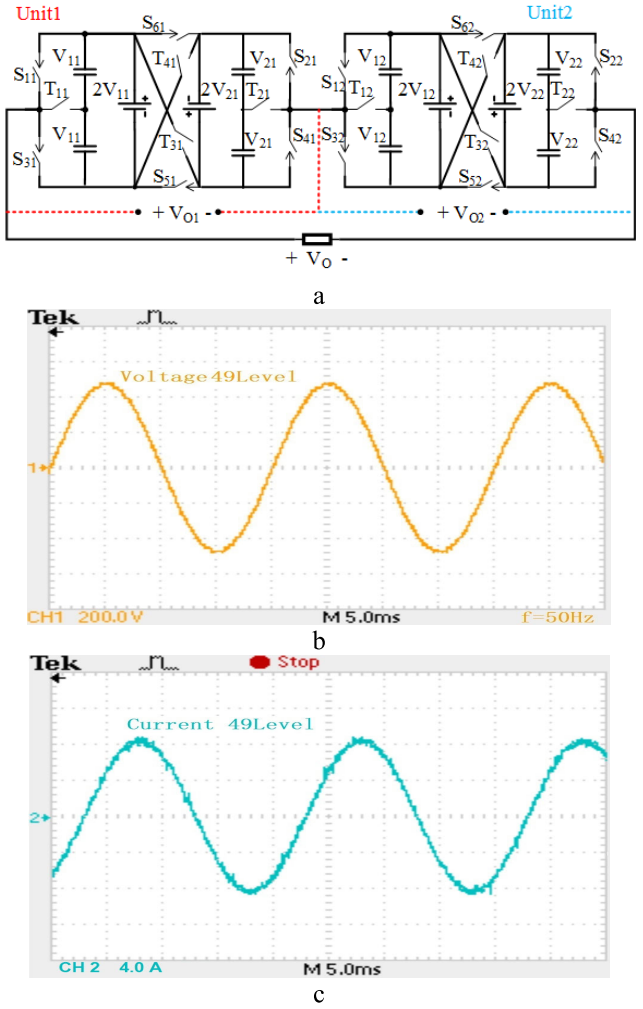


FIGURE 7. Experimental results; a) 49-level proposed inverter circuit scheme; b) output voltage, c) output current.

that the maximum blocked voltage on switches T_1, T_2, T_3, and T_4 are *20 V, 100V, 200V*, and *200V*, respectively.

B. EXPERIMENTAL RESULTS OF 49-LEVEL INVERTER

In this case study, the converter is supposed to be a *49*-level converter and to produce *480* V peak, *50* Hz output voltage. *Fig.7-a* shows the 49-level converter scheme. The converter includes four dc voltage sources that the value of each one is as follows:

$$V_{11}= 20V, V_{21}= 100V, V_{12}= 20V, V_{22}= 100V$$

The load data is as the same as the previous case. Experimental results of the proposed topology (*Fig. 7-a*) are shown in *Fig.7 (b, c)*. *Fig.7-b* shows the output voltage and *Fig.7-c* shows the output current. As the output voltage waveform indicates, the output voltage includes the desired levels and it is a *49*-level voltage as expected.

C. SIMULATION RESULTS OF 625-LEVEL INVERTER

To simulate the proposed inverter,*MATLAB* Simulink software has been used. The inverter scheme in this case is same as *Fig.7-a*, but the voltages are chosen as follows:

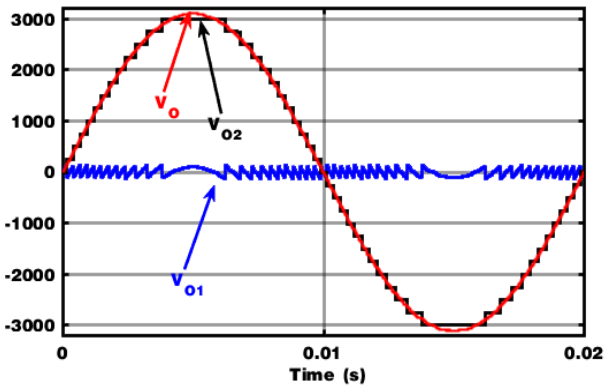


FIGURE 8. Simulation results; Output voltages of the unit1 (V_{o1}), the unit2 (V_{o2}) and total output voltage of cascaded inverter (V_o) in 625-level cascaded inverter.

$$V_{11}= 10V, V_{21}= 50V, V_{21}= 250V, V_{22}= 1250V$$

Fig. 8 presents the output voltage of the first unit (V_{O1}), the second unit (V_{O2}) and the total output voltage of the cascaded inverter (V_O). As shown in *Fig. 8*, the output voltage of the *625*-level topology (V_O) is the sum of the output voltage of unit1 (V_{O1}) and unit2 (V_{O2}). Also, the maximum output voltage is $V_{O,max}= 3120\ V$, which has *625* levels as already mentioned in *Table.3*.

VII. CONCLUSION

In this paper, a novel topology of asymmetrical configuration of MLI is proposed for a wide range of application (i.e. medium–to-high voltage) such as reactive power compensators, adjustable-speed drives, uninterruptible power supplies, PV systems and solar energy systems.

The presented topology exploits a special method for the charging/discharging of the capacitors, contributing to the voltage balance of the capacitors. The presented cascaded topology was compared with some other topologies to verify its performance. According to this comparison, the proposed cascaded MLI requires the fewest number of components, the lowest power losses, and a fewer value of blocked voltage in switches compared to some topologies. Experimental and simulation results were presented to validate the performance of the proposed multilevel inverter. In the 25-level, the *THD* of the voltage and current is *3.25%* and *0.20%*, respectively, that satisfies harmonics standard (*IEEE519*).

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