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True Random Number Generators Using Electrical Noise

LISHUANG GONG[1], JIANGUO ZHANG[1], HAIFANG LIU[1], LUXIAO SANG[1], AND YUNCAI WANG[1,2]

[1]Key Laboratory of Advanced Transducers and Intelligent Control System, Ministry of Education and Shanxi Province, College of Physics and Optoelectronics, Taiyuan University of Technology, Taiyuan 030024, China
[2]School of Information Engineering, Guangdong University of Technology, Guangzhou 510006, China

Corresponding author: Yuncai Wang (wangyc@gdut.edu.cn)

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ABSTRACT True random number generators (TRNGs) are a fundamental resource in information security and can guarantee the absolute security of information in principle. Entropy source is the most critical part of TRNGs, which provides the unpredictability and is the root of security for TRNGs. Electrical noise, which is inevitable and unpredictable in electronic systems, is always used as entropy source for TRNGs. This review discusses the different methods to harvest electrical noise in TRNGs, including the early amplify noise based on amplifier, phase jitter based on oscillator, the effect of electrical noise on the metastable behavior and amplify noise based on chaos circuits. Each method has its own strengths in aspect of speed, cost, complexity and portability. Finally, some post-processing technologies and TRNG evaluation methods are also discussed. With this review, we hope the current spots for TRNGs using electrical noise are summarized and some possible future directions are pointed out.

INDEX TERMS TRNGs, electrical noise, entropy source, post-processing, evaluation methods.

I. INTRODUCTION

Random number generator is always important for information encryption and decryption, numerical simulations, lottery games and stochastic experiments [1]. Historically, random number generator is divided into pseudo-random number generators (PRNGs) and true random number generators (TRNGs).

PRNGs use some initial seeds and deterministic algorithms to produce pseudo-random numbers and can result in high throughput. However, once the seeds are obtained by attacker, all security will be lost. Thus, it is dangerous that using PRNGs produce secret keys. For the sake of defending against such problems, TRNGs are designed by researches, which extract random numbers from physical random processes. These are contrary to the pseudo-random numbers produced by computer program and can guarantee the absolute security of information in principle.

The randomness of TRNGs comes from entropy source which is the root of security for TRNGs. Electrical noise is inevitable in electronic systems. Due to the unpredictability of white noise, it is an ideal entropy source for TRNGs. Several methods of harvesting electrical noise in TRNGs are available, such as amplify noise based on amplifier [2]–[4], phase jitter based on oscillator [5]–[8], the impact of electrical noise on the metastable behavior [9]–[12] and amplify noise based on chaos circuits [1], [13], [14]. Classical noise-based TRNGs use high-gain differential amplifier to amplify noise to a level and compared with a threshold in a comparator, then the amplified noise is converted to produce a digital signal [2]. However, this process will consume lots of power because noise is leveled up a few orders to meet the needs of digital logic level, and designing amplifier is a complex work [10]. Hence, some researches focused on these problems were carried out, including Si nano-devices [15], identical inverters [16], oxide breakdown [17], [18] and random telegraph noise [19].

Though these methods are valid to produce high quality true random bits, they show some great challenges when are manufactured in sub-14 nm processes. These circuits need stable supply voltage and they are sensitive to temperature and aging, which will induce device drifts. To solve these problems, generating random bits using digital circuits are studied because electrical noise also can lead to phase jitter

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in oscillator [20], [21]. These TRNGs extract entropy from edge-jitter of oscillator and sample jitter events using phase-detector, including ring oscillators [7], coupled oscillators [2], [22], [23] and Fibonacci/Galois ring oscillators [24], [25]. Another popular digital technique harvesting noise is using the metastable behavior [9], [12], [26], [27]. Because metastability of bi-stable circuits can be influenced by thermal noise then a random bit is produced [9], [12], [26].

Due to its non-periodicity and non-reproducibility, fast TRNGs are key in information security [28]–[30] and large-scale parallel computation [31]. Because of lacking infinite measurement precision in chaotic circuit, it is impossible to confirm initial conditions exactly and chaotic dynamic is sensitive to initial value. Additionally, the uncertainties can be amplified by chaotic systems [32]. What's more, chaotic systems have high wideband. These make chaotic circuits convenient candidates for fast TRNGs and TRNGs using chaotic circuit have been extensive researched [33]–[35].

Due to intrinsic bias and correlations derived from entropy source, raw bits are usually hard to achieve good statistical properties. In this case, post-processing is needed to reduce statistical flaws. And their exciting experiments are certified by randomness tests, such as NIST, Diehard, Test U01 and AIS 31. In this paper, we attempt to review the evolution of electrical noise-based TRNGs, the advantages and challenges are demonstrated and shown to the readers. TRNG model is given detailly in section II. And entropy source is introduced in section III. Subsequently, section IV reviews different methods of harvesting electrical noise in TRNGs. Section V gives a brief review on post-processing and Section VI introduces TRNG evaluation methods. In the end, conclusions are drawn in Section VII.

II. TRNG MODEL

Generally speaking, TRNGs consist of entropy source, a harvesting component and post-processing component, as shown in Figure 1. Entropy source, which is the most important component of TRNG, provides the unpredictability and is the root of security for TRNG. Harvesting component does not impede the physical of entropy source and collects entropy as much as possible. It reads data produced by entropy source and converts data to a series of bits. The output bits are called the raw data. Using harvesting component, entropy can be collected as much as possible and physical process of entropy source won't be disturbed. Though entropy source can provide true randomness, the raw bits are usually biased and not uniformly distributed for various reasons. Thus, post-processing is needed to reduce residual correlation in random sequence and make output uniformly distributed. It can cover up imperfections from entropy source or harvesting component.

III. ENTROPY SOURCE

Entropy source is the root of TRNGs. To ensure the effective of TRNGs, entropy source must be unpredictable in principle. Electrical noise, which is unpredictable and inevitable in

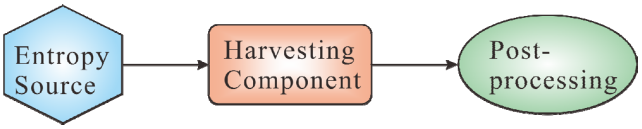

FIGURE 1. TRNG model.

electronic systems, is an ideal entropy source. Electrical noise mainly includes shot noise, thermal noise and flicker noise. The mean square variation of external current is known as shot noise and it exists in diodes, bipolar transistors and MOS transistors. It is written as i^2 and can be expressed as

$$\overline{i^2} = 2qI_D\Delta f \tag{1}$$

where q is electronic charge and equal to 1.6×10^{-19} C, I_D is the average value of a series of random independent pulses and Δf is the bandwidth in hertz.

Equation (1) demonstrates that shot noise is increased with bandwidth of measurement. The spectral density of noise-current is constant and shot noise is white noise. Equation (1) is perfectly valid into the gigahertz region. The amplitude distribution of shot noise is Gaussian and its standard variance is

$$\sigma = \sqrt{\overline{i^2}} = \sqrt{2qI_D\Delta f} \tag{2}$$

In electronic systems, random thermal motion of charge carriers will lead to thermal noise. Because electron thermal velocities in a conductor are much faster than typical electron drift velocities. Thermal noise is not affected by whether direct current present. Thermal noise is increased with absolute temperature T and it can be written as equation (3) or (4) [36]

$$\overline{v^2} = 4kTR\Delta f \tag{3}$$

where v^2 is voltage variation caused by thermal noise, k is Boltzmann constant and R is resistance.

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \tag{4}$$

Equation (3) and (4) demonstrate that the spectral density of thermal noise is also not depend on frequency and this is valid into 10^{13} Hz. Thus, thermal noise is another white noise. Because white noise is unpredictable and independent with frequency, it is an ideal entropy source for TRNGs.

Flicker noise is mainly resulted by traps connected with contamination and crystal defects. These traps random capture and release carriers and they cause a noise signal with energy concentrated at low frequencies. Flicker noise is connected with a flow of direct current and can be expressed as

$$\overline{i^2} = K_1\frac{I^a}{f^b}\Delta f \tag{5}$$

where K_1, a and b are constant ($0.5 \leq a \leq 2$, $b \approx 1$), I is direct current. If $b = 1$, the spectral density of flicker noise depends on $1/f$ frequency. Hence flicker noise is also known as $1/f$ noise. It is valid into the megahertz range.

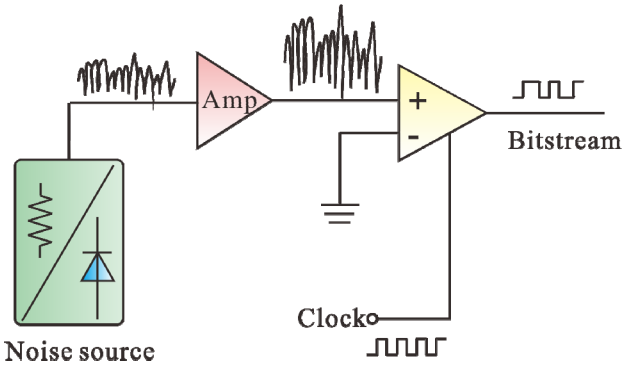

FIGURE 2. Amplify noise-based TRNGs.

According to equation (5), flicker noise may cause correlation in the output of random number generations. Thus, some researchers attempt to suppress flicker noise in TRNGs using electrical noise [37]. Also many researches take no account the effects of flicker noise [24]. And some researches manifest flicker noise has effect on random number generation [38], [39], while these researches are insufficient to make an interpretation confidently.

With respect to the methods of harvesting electrical noise, TRNGs can be divided into four main groups: amplify noise-based TRNGs, oscillator-based TRNGs, metastability-based TRNGs and chaotic TRNGs.

IV. TRNGS BASED ON DIFFERENT METHODS OF HARVESTING ELECTRICAL NOISE

A. TRNGS BASED ON AMPLIFY NOISE

Noise is inevitable in electronic systems. Because of its natural randomness, noise is one of the preferred entropy sources for TRNGs [40]. Early noise-based TRNGs utilize analog circuitries to directly amplify noise. After being amplified, noise is sampled and quantized in circuit devices [2], [41]. As shown in Figure 2, classical noise-based TRNGs employ an amplifier to deal with small voltage fluctuate caused by electrical noise from a resistor or semiconductor diode as initial randomness source. Then the amplified noise is compared with a threshold using comparator to produce digital signal. Subsequently, this digital signal is sampled and processed to generate random bit sequence.

For this kind of noise-based TRNGs, noise must be amplified to a level that the threshold has no bias compared by a comparator, which needs lots of power to bring the noise level up a few orders of magnitude to digital logic level, and designing amplifier is a complex work [10]. These also make it difficult to balance between circuit area and quality of random numbers. To solve these problems, S. Fujita proposed using Si nanodevices to produce high-amplitude device noise, which reduced the size of TRNGs and produced high quality random numbers [15]. Later, increasing noise magnitude with inserting a SiN layer rich in high-density electron traps was proposed [42]. The experimental results showed the area of this TRNG was reduced much and the throughput was increased than TRNG previously reported [2]. However, using this method required additional photo mask, which increased the expense. Then, other TRNGs were proposed. Because the electrical properties of metal-oxide semiconductor (MOS) after soft breakdown (SBD) shows large fluctuation [17], [18]. In 2004, a novel RNG using MOS capacitors after SBD as a random source was presented [17]. In 2010, Christophe De Roover and Michiel Steyaert amplified noise using identical inverters and produced a series of random bits consuming only 0.65nw [16]. Subsequently, TRNG using random telegraph noise (RTN) was proposed due to its unpredictability and some basic guidelines for designing RNT-based TRNG also were provided [19].

For noise-based TRNG, the threshold needs to be adjusted to a proper value so that the probabilities of "0" and "1" are equal. However, owing to environment variations and temperature perturbations, it is difficult to adjust to a precise and proper value in practice. Thus, the raw digitized bits are usually correlated or biased and post-processing is needed. What's worse, it needs extra device to reduce the influence of electromagnetic interference. In addition, this kind of TRNGs can be easily impacted by flicker noise, which will produce correlation sequences.

B. TRNGS BASED ON OSCILLATOR

Electrical noise also can lead to phase jitter in oscillator [20], [43], [44]. The research on phase noise and jitter in oscillator was introduced and developed until 1990s [45], [46]. In 2006, a simple and straightforward model for phase noise and jitter was published by Abidi [47]. Recently, due to its simple structure and produce random bits effectively, TRNGs using phase jitter have been extensively researched [5], [38], [48]. In theory, the simplest oscillator can contain only one inverter. However, in digital circuit, phase jitter using an inverter is very small. To increase jitter, odd inverters are chained then a simple oscillator is built. Its open loop structure is shown in Figure 3. It is perfect when the output of oscillator is a periodic square wave. But the transition spacing is variable actually on account of electrical noise. Arbitrary uncertainty in a previous transition influences all the subsequent transitions, and this influence persists indefinitely, this uncertainty will be increased with the number of inverters added.

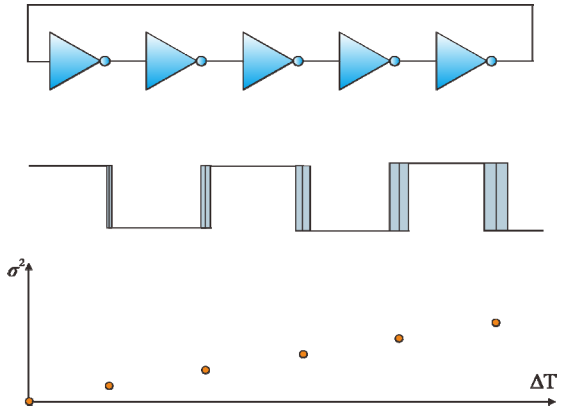

FIGURE 3. Jitter increasing with the number of inverters.

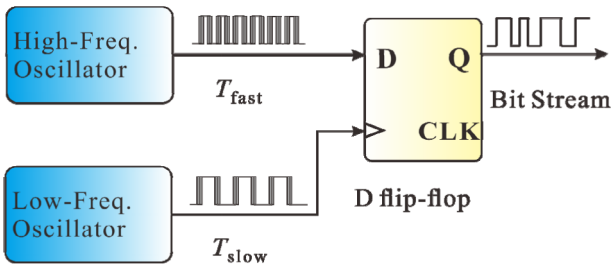

FIGURE 4. The schematic diagram of couple oscillator-based TRNG.

In this paper, for simplicity, the model of ring oscillator is simplified as a single inverter, a delay τ and a feedback loop and the ring oscillator follows Barkhausen criterion [49]. In 1996, it was modeled that a low-frequency ring oscillator sampled a high-frequency ring oscillator using a D flip-flop for generate unpredictable bits [50], as shown in Figure 4. Generally, this configuration is called coupled oscillators. TRNGs based on coupled oscillator can be designed purely digital and without amplifier. Subsequently, some researches realized it and provided some methods to enhance its performance [23], [37], [51]. However, precisely matching the period of coupled oscillators is quite hard and two signals of frequency oscillators may drift relative to one another. These don't make for very robust TRNG designs. Some researchers used additional circuitry to adjust waveforms to make the transitions matched. While it decreases the randomness of jitter and brings in some biases.

To alleviate these problems, Sunar *et. al.* put forward a classical TRNG combining and sampling some equal length ring oscillators [5], as illustrated in Figure 5 (a). The outputs of oscillators were XORed and sampled using D-type flip flop to generate random bits. Also, its security was proved by Sunar in [5]. Although, many resources were needed using this method, it was very popular due to its production of high entropy of random bits and easy implementation after post-processing. Ülkühan Güler and Günhan Dündar realized the first integrated circuit implementation using Sunar's method and generated high-quality random bits using the simple Von Neuman corrector instead of Sunar's post-processor [52], [53]. And to maximize randomness of CMOS ring oscillator-based TRNGs, Ülkühan Güler derived randomness equations and defined randomness parameter [38]. Later, an improved version of Sunar's method was put forward by Wold and Tan [6], as shown in Figure 5 (b). With a flip-flop added after each oscillator before the XOR tree, modified TRNG could pass randomness tests without post-processing and the number of oscillators was decreased. Subsequently, Knut Wold and Slobodan Petrović optimized the parameters of modified TRNG by spectral analysis and achieved 300 Mbit/s throughput [54]. However, Ring oscillator-based TRNGs using Word's method need constant oscillation of many ROs to accumulate enough jitter to produce high quality random bits, which still lead to large power consumption [55]. Also, Word's method may introduce pseudo randomness and this pseudo randomness

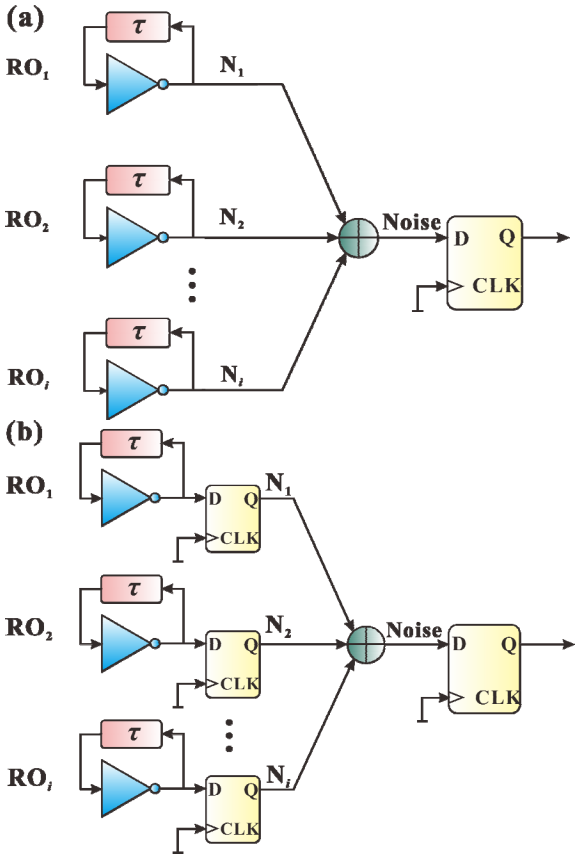

FIGURE 5. The basic schematic diagram of Sunar's method and its modification.

is impossible to be eliminated [56], thus the TRNG may be attacked.

Fibonacci ring oscillators (FIRO) and Galois ring oscillators (GARO) are two new forms of ring oscillators. These designs refer to linear feedback shift registers (LFSR) and use inverters instead of shift registers. Schematic diagrams of FIRO and GARO are shown in Figure 6. Their feedback connections need to be chosen appropriately to avoid dynamic collapse into the fixed points. When the number of inverters is reduced to only one, both FIRO and GARO become classical ring oscillator. Even or odd is allowed for the number of inverters in FIRO, but not equal to 2. And the output of FIRO can come from arbitrary inverter. While the number of inverters in GARO should be odd and the output of GARO is come from the last inverter. In 2006, FIRO and GARO for TRNG were proposed and analyzed in [24]. Subsequently, a novel sampling method nearly doubling the entropy was put forward by Dichtl and Golić [25]. In 2010, Ülkühan *et al.* designed the first ASIC implementation of TRNG combining FIRO with GARO and this design provided a throughput of 125Mbps [57]. Inspired by [24] and [25], Lijuan Li and Shuguo Li proposed a digital TRNG using cross feedback ring oscillator [58]. Compared with FIRO and GARO, it saved more than half of the time to accumulate very high entropy and generated one unpredictable bit.

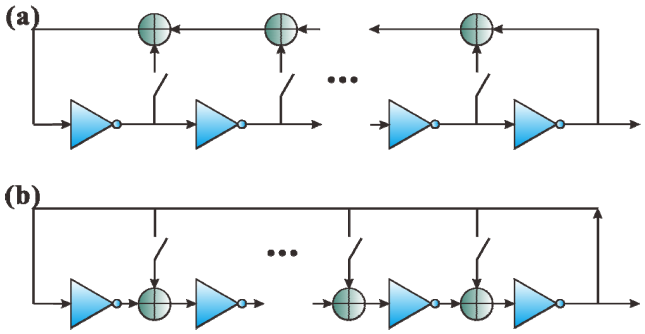

FIGURE 6. Fibonacci ring oscillators (a) and Galois ring oscillators (b).

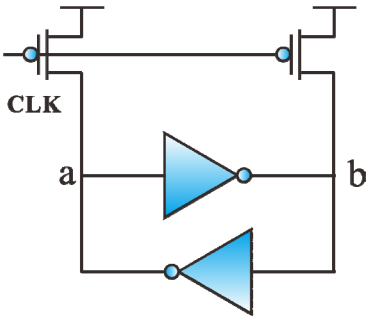

FIGURE 7. Cross-coupled inverter pair.

By restarting FIRO and GARO under the same initial conditions and calculating time evolution of standard deviation of output, their randomness was evaluated and analyzed [25], [59]. It was demonstrated that a higher and more robust entropy rate could be achieved using FIRO and GARO. Compared to other oscillators, the number of inverters using FIRO and GARO is reduced and FIRO and GARO are more sensitive to jitter [24], [25]. Thus, jitter is quickly propagated and transformed through feedback. Thus, FIRO and GARO are more suitable entropy source.

However, some drawbacks can hinder the usage oscillator-based TRNGs, such as aging, frequency locking, technology dependence and highly power consumption [60], [61]. What's worse, oscillator-based TRNGs suffer from frequency attacking easily [60], which can lead to entropy loss. Rahman *et al*. presented adding self-compensation mechanism or extra power supply noise for oscillator-based TRNG to avoid frequency attacks [62]. And Böhl *et al*. presented the on-line testable solution to ensure randomness [63].

Realizing in an all-digital design makes oscillator-based TRNGs easier to integrate into applications. Not only quality of the TRNGs are essential, but also its speed for practical applications. Additionally, the rapid development of quantum key distribution (QKD) systems will cause even more enormous challenges to the throughput of TRNGs in the next few years. Because ring oscillator-based TRNGs usually need a mass of logic gates to generate high speed random number, this method usually combines with other methods.

C. TRNGS BASED ON METASTABILITY

Metastable-based TRNG is another method can be realized using digital technique. It has been known that the final state between two equal desirable outputs can be determined by random processes. Hence, the final state of bi-stable circuit in metastable point is determined by circuit noise [9]. The classical metastable-based TRNG was developed by *Philips* in [64], which used metastable cross-coupled inverters to handle thermal noise, as shown in Figure 7. It is composed of a cross-coupled inverter pair. By pre-charging inverter diffusion nodes, the inverter pair can be driven into unstable state to identical logic values. Ultimately, either stable state (a=1, b=0) or (a=0, b=1) is decided by the differential noise at 'a' and 'b' during the metastable period.

Due to its easy integration and energy-efficient in circuits [55], metastability is a perfect solution for TRNGs. However, metastability events are very sensitive to manufacturing process and voltage and temperature (PVT) changes. Hence, it is hard to keep a bi-stable circuit in an unstable state [65], [66]. What's worse, these inaccuracies affecting the symmetry of the metastability will cause bias and decrease the entropy rate of the outputs bits of metastable circuit [67]. Hence, some researches focused on the symmetry of metastable circuit were carried out. In 2011, a metastability-based TRNG with adaptive control was proposed by Majzoobi *et al*. [66]. The experimental results showed using programmable delay lines could precisely equalize the signal arrival times to obtain metastability and produced throughput of 2 Mbit/s. Later, Hata and Ichikawa came up with a solution using almost identical RS latch to guarantee the quality of randomness and achieved throughput of 12.5Mbps [68]. Meanwhile, a self-calibrating 2-step tuning mechanism was used for metastability-based TRNG by Intel and it provided tolerance to 20% PVT variation [10]. Subsequently, Intel improved this TRNG using in-line decorrelators and a lightweight BIW extractor. It demonstrated that this TRNG could provide a throughput of 162.5 Mbps at 1.3 GHz operation, with 1.5 mW total power consumption and a 90 μW leakage component [11].

Metastability also exists in RS latches [69] and D-type flip-flops [64]. For their all-digital designs and simple structures, TRNGs using metastable circuits are increasingly popular [11], [55], [68], [70]. Meanwhile, many other solutions were proposed to keep a bi-stable circuit in a metastable state. In 2008, Tokunaga *et al*. presented the solution controlling the metastability proximity to produce random bit, which formed the bi-stable by adjusting the initial input inverters [12]. In 2010, Varchola and Drutarovsky put forward a new bi-stable structure which was known as transition effect ring oscillator for TRNG [71]. This TRNG extracted randomness from oscillatory metastability and the sensitivity of the global perturbations was lower than ring oscillator. However, the initial condition of TERO could not be adjusted. Later, Piotr Zbigniew Wieczorek proposed dual-metastability time-competitive TRNG [72], [73], which generated random number by comparing the unpredictable resolve time of two similar metastable D-latches (or flip-flops) to generate

random number and this method could be carried out with various logic programmable circuits. In 2016, Piotr Zbigniew Wieczorek proposed a novel TRNG, which adjusted the initial condition in pre-autonomous mode and extract randomness from parameters of two bi-stable transient response [61]. Due to the symmetry of the presented solution, its robustness and tolerating temperature and supply voltage variations was increased. Subsequently, Piotr Zbigniew Wieczorek combined chaotic circuit with metastability. Not only were the parameters of the circuit insensitive to PVT conditions using this method, but also this method had better performance of anti-attack of active injection side-channel attack [74]. Recently, Sha Tao and Elena Dubrova harvested entropy from latches comparators in their detectable metastable states and harnessed several ternary valued latches to address the bias caused by conditions [75]. And, Barangi *et al*. used metastable state in straintronics magnetic tunneling junction generated unpredictable random number at a high rate with low-energy overhead.

For one-time-pad, it needs abundant random bits. For this, speed is important because taking much time to produce random number is not permitted. To this end, TRNGs based on chaos are proposed and realized in recent years.

D. TRNGS BASED ON CHAOS

Due to its high bandwidth, unpredictability and insensitive to various disturbance and tolerances of components, chaos is a perfect entropy source for fast TRNGs [14], [76], [77]. In 2013, David P. Rosin *et al*. put forward a TRNG using autonomous logic gates, and this TRNG was claimed to reach the throughput of 12.8 Gbps. This does not rely on a clock and is promising candidates for TRNG because it is easily integrated [78]. Wen Li *et al*. proposed an all-electronic TRNG based on high amplitude chaotic oscillations [79]. This TRNG presented random bit throughput of 80 Gbps and its robustness and fully electronic implementation implies scalability and minimal post-processing compared with existing optical TRNG.

Physical randomness is derived from electrical noise and amplified by deterministic chaos [80]. The statistical properties can also be made more desirable by chaotic dynamics [81]. Figure 8 illustrates chaos-based TRNGs. The entropy source of the chaos-based TRNGs is a non-linear dynamical system operating in chaotic regime. Then entropy is harvested by a sampler and imperfection of entropy source is masked by post-processing.

In general, according to underlying dynamics, chaos-based TRNGs can be divided into continuous time and discrete time. The future state of the continuous time chaotic systems is decided by differential equations relating to the rate of change relating to the variables of current state. However, analog circuit blocks is needed for continuous time chaos-based TRNGs, such as operational amplifier (OPAMP) [82], [83], which makes continuous time chaos-based TRNGs have large area and high consumption. Compared with continuous time chaotic system, discrete time chaos-based TRNGs

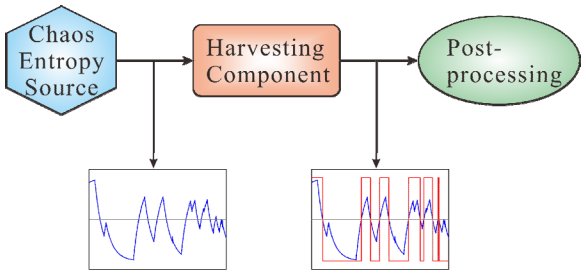

FIGURE 8. The schematic diagram of chaos-based TRNGs.

is able to be built by less components. Future state of the discrete time chaotic systems is decided by differential equations which merely relates to the current state [84]. Generally, the operation of the discrete time chaos-based TRNGs requires an external clock to drive chaotic dynamics. Thus, it depends on the clock frequency that the speed of generation and development for forming the chaotic dynamic. For discrete time chaos-based TRNGs, clock frequency can be adjusted dynamically at runtime. This makes it lower consumption and high throughput without any topological modifications. What's more, discrete time chaos-based TRNG can be implemented by digital circuit. Thus, it is simple to implement digital integrated circuit and its circuit only incorporates a few typical electronic devices. These make it desirable candidates for applying to lightweight and hardware efficient TRNGs [82].

However, digital chaotic implementations involve finite computational precision, which may lead to pseudo-random output [85]. Thus, it will be very helpful that identifying a continuous random variable which can be used in digital circuits. This variable can have complementary advantages of analog chaotic signal and digital circuit. Thus, a TRNG combined chaotic circuit and metastability was proposed [74]. Where chaotic behavior is resulted from switchable ring oscillators and metastability is resulted from a flip-flop. This method provided high quality random bits without additional post-processing. What's more, it is immune to active injection side-channel attacks.

E. COMPARISONS AND CHALLENGES

The methods of harvesting electrical noise are summarized briefly in Table 1. The table gives a few representative references, the order of the typical bit rates for every kind of TRNG, their advantages and challenges.

V. POST-PROCESSING

Due to intrinsic bias and correlations derived from entropy source, raw bits are usually hard to achieve good statistical properties. In this case, post-processing is needed to reduce statistical flaws. Generally speaking, using post-processing has two goals. One is adjusting the probability distribution of raw random bits conform to a uniform distribution. With this method, statistical defects in entropy source or harvest component are compensated. The other is increasing entropy

TABLE 1. Comparisons of entropy source using electrical noise and their challenges.

Classification		Technology	Reference	Rate(order)	Advantages	Challenges
Amplify noise		Analog	[2]	1Mbps	Simple structure	Low power consumption; High rate
Oscillator	Couple oscillator	Digital	[37]	10Mbps	Easy integration	Frequency attack; High rate
	Ring oscillator	Digital	[5]	1Mbps	Good portability	Injection locking
	FIRO/GARO	Digital	[24]	100Mbps	More sensitive to jitter	Directly prove randomness
Metastability		Digital	[74]	1Mbps	Easy integration	Symmetry
Chaos	Continuous time chaos	Analog	[83]	10Mbps	High rate	Low power consumption
	Discrete time chaos	Digital	[33]	100Mbps	High rate	Finite Computable precision

per bit using a compression function. Usually, using post-processing can increase that the probability of bits passing the test, while their throughput will be reduced [86].

A post-processing can be as simple as a XOR corrector and von Neumann corrector [73]. It can also be as complicated as a resilient function [5] and hash function [87]. XOR and Von Neumann are the most common post-processing for TRNGs because of their easy application [88]. Von Neumann algorithm is an ideal method to reduce bias, using it, uniformly distributed 0 and 1 numbers can be obtained. In addition, regarding only consequent number pairs makes Von Neumann is the simplest post-processing method. Its disadvantage is that the throughput of TRNG will be decreased, because the (0,0) and (1,1) number pairs are abandoned.

Post-processing is not needed in all TRNGs. Because post-processing may limit the bitrate of TRNGs substantially, the low rates of post-processing for TRNGs usually are not included in ultra-fast random number generation. As far as I know, the generation of fast random number bits is limited by their obtain methods with high-speed oscilloscopes. Thus, most studies of post-processing for ultrafast TRNGs are carried out offline [81]. The defects of post-processing are increased power consumption and decreased in the bit rate, respectively. And some challenges also are brought including scalability to higher rates, interfacing with computing and communication architectures [87].

VI. TRNG EVALUATIONS

To use TRNGs in cryptographic applications, we must certify the output bits are secure enough. Entropy provides a convenient way for measuring randomness. In the information theory, expressing entropy in bits is a natural formulation for information processing and communications. In different entropies, Shannon entropy is well known and interesting estimator for its a simplicity and validity. It evaluates the useful information of randomness from the perspective of probability. And it is defined as

$$H_{\mathrm{n}}(X) = -\sum_{x} P_X(x)\log_2 P_X(x) \tag{6}$$

where $H_{\mathrm{n}}(X)$ is Shannon entropy, X is random variable, $P_X(x)$ is the probability of outcome.

Shannon entropy provides a rough estimation of randomness. Higher Shannon entropy means closer to uniform distribution and we are able to harvest more random bits from entropy source. It is ideal to produce a nearly uniform distribution under the guidance of Shannon entropy.

The other popular entropy estimator is min-entropy that recommended by NIST [89]. Min-entropy evaluates the difficulty that the output of the TRNGs are predicted. The probability that a random bit is first inferred correctly is related to the distribution of min-entropy which the random bit is generated from. The min-entropy, which estimates randomness from the perspective of attacker, is strongly associated with negative logarithm of the maximum probability using the optimal guessing strategy. The min-entropy $H_\infty(X)$ can be defined as

$$H_\infty(X) = -\min_{1\le i\le k}(-\log_2 p_i) = -\log_2 \max_{1\le i\le k} p_i \tag{7}$$

where p_i is the probability of $X = x_i$ and X is the discrete random value from $\mathrm{A} = [x_1, x_2, \ldots, x_k]$. If H is the min-entropy, then the probability that any particular outcome X is observed will be no more than 2^{-H}. When random variable accord with a uniform probability distribution, min-entropy will attain its maximum value $\log_2 k$. As the number of uniform bits, min-entropy can be extracted from a given distribution.

Both Shannon entropy and min-entropy provide strong confidence in randomness. In practical, other entropy evaluations also can be used to give us a guideline when decide how to use a randomness extractor to make the most use of available randomness, such as Kolmogorov-Sinai entropy and T-entropy. However, entropy estimation spends lots of

time to achieve highly reliable results. Recently, the most common way to evaluate randomness is represented by statistical tests. NIST SP-800.22 statistical test suite [90] and Die-hard test suite [91] and Test U01 [92] and AIS31 [93] are most common statistical test suites to evaluate their RNGs by researchers. They report test results as fail or pass scores.

VII. CONCLUSION

TRNGs are playing an increasingly important role in information security and cryptography. TRNGs using electric circuits have shown wide prospect because of carried out on compact electronic chips and thus worth further investigating. Electrical noise is inevitable in electronic systems. Because white noise has a uniform power spectral density, that enables us to obtain uncorrelated random numbers. Therefore, it is a preferred choice in random number generation. Various methods of harvesting electrical noise serving as reliable entropy sources are reviewed, such as classical noise amplifier, oscillators, metastability and chaos. Each method has its own strengths in terms of speed, cost, complexity and portability. In our opinion, TRNGs based on oscillators and metastability are more easily integrated and have good portability. Chaos is the most suitable technique for fast random number generator and has good immunity to active injection side-channel attacks. We hope that they can be combined in the future to produce a high quality of fast random number generator which can be integrated easily. These combined circuits provide the additional advantage that they are insensitive to PVT conditions.

While some entropy sources are claimed to directly generate enough random bit sequences, most TRNGs produce imperfect random bits without post-processing. To avoid this problem, TRNGs should include a well-designed post-processing, which can reduce statistical flaws and provide prediction resistance. The random bits need to be tested to prove their reliability. Thus, TRNGs evaluation including entropy estimations and statistical tests are summarized at the end of the paper.

With this review, we hope the current spots for TRNGs using electrical noise are summarized and some possible future directions are pointed out.

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REFERENCES

[1] T. Addabbo, M. Alioto, A. Fort, S. Rocchi, and V. Vignoli, "A feedback strategy to improve the entropy of a chaos-based random bit generator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 326–337, Feb. 2006.

[2] C. S. Petrie and J. A. Connelly, "A noise-based IC random number generator for applications in cryptography," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 615–621, May 2000.

[3] M. Huang, A. B. Wang, P. Li, H. Xu, and Y. C. Wang, "Real-time 3 Gbit/s true random bit generator based on a super-luminescent diode," *Opt. Commun.*, vol. 325, pp. 165–169, Aug. 2014.

[4] N. C. Gov, M. K. Mihcak, and S. Ergun, "True random number generation via sampling from flat band-limited Gaussian processes," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 1044–1051, May 2011.

[5] B. Sunar, W. J. Martin, and D. R. Stinson, "A provably secure true random number generator with built-in tolerance to active attacks," *IEEE Trans. Comput.*, vol. 56, no. 1, pp. 109–119, Jan. 2007.

[6] K. Wold and C. H. Tan, "Analysis and enhancement of random number generator in FPGA based on oscillator rings," *Int. J. Reconfigurable Comput.*, vol. 2009, no. 1, pp. 385–390, 2009.

[7] K. Yang, D. Fick, M. B. Henry, and Y. Lee, "A 23 Mb/s 23 pJ/b fully synthesized true-random-number generator in 28 nm and 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2014, pp. 280–281.

[8] K. Yang, D. Blaauw, and D. Sylvester, "A robust –40 to 120 °C all-digital true random number generator in 40 nm CMOS," in *Proc. Symp. VLSI Circuits*, Kyoto, Japan, Jun. 2015, pp. C248–C249.

[9] D. J. Kinniment and E. G. Chester, "Design of an on-chip random number generator using metastability," in *Proc. 28th Eur. Solid-State Circuits Conf.*, Florence, Italy, 2002, pp. 595–598.

[10] S. K. Mathew, S. Srinivasan, M. A. Anders, H. Kaul, S. K. Hsu, F. Sheikh, A. Agarwal, S. Satpathy, and R. K. Krishnamurthy, " 2.4 Gbps, 7 mW all-digital PVT-variation tolerant true random number generator for 45 nm CMOS high-performance microprocessors," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2807–2821, Nov. 2012.

[11] S. K. Mathew, D. Johnston, S. Satpathy, V. Suresh, P. Newman, M. A. Anders, H. Kaul, A. Agarwal, S. K. Hsu, G. Chen, and R. K. Krishnamurthy, "μ RNG: A 300–950 mV, 323 Gbps/W all-digital full-entropy true random number generator in 14 nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1695–1704, Jul. 2016.

[12] C. Tokunaga, D. Blaauw, and T. Mudge, "True random number generator with a metastability-based quality control," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 78–85, Jan. 2008.

[13] S. Ergun, U. Guler, and K. Asada, "A high speed IC truly random number generator based on chaotic sampling of regular waveform," *IEICE Trans. Fundam. Electron. Commun. CComput. Sci.*, vol. E94-A, no. 1, pp. 180–190, Jan. 2011.

[14] T. Stojanovski and L. Kocarev, "Chaos-based random number generators—Part I: Analysis," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, no. 3, pp. 281–288, Mar. 2001.

[15] S. Fujita, K. Uchida, S. Yasuda, R. Ohba, H. Nozaki, and T. Tanamoto, "Si nanodevices for random number generating circuits for cryptographic security," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2004, pp. 294–295.

[16] C. D. Roover and M. Steyaert, "A 500 mV 650 pW random number generator in 130 nm CMOS for a UWB localization system," in *Proc. ESSCIRC*, Seville, Spain, 2010, pp. 278–281.

[17] S. Yasuda, H. Satake, T. Tanamoto, R. Ohba, K. Uchida, and S. Fujita, "Physical random number generator based on MOS structure after soft breakdown," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1375–1377, Aug. 2004.

[18] N. Liu, N. Pinckney, S. Hanson, D. Sylvester, and D. Blaauw, "A true random number generator using time-dependent dielectric breakdown," in *Symp. VLSI Circuits-Dig. Tech. Papers*, Honolulu, HI, USA, 2011, pp. 216–217.

[19] X. Chen, L. Wang, B. Li, Y. Wang, X. Li, Y. Liu, and H. Yang, "Modeling random telegraph noise as a randomness source and its application in true random number generation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 9, pp. 1435–1448, Sep. 2016.

[20] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 2002.

[21] A. Demir, "Computing timing jitter from phase noise spectra for oscillators and phase-locked loops with white and 1/*f* noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 1869–1884, Sep. 2006.

[22] Q. Tang, B. Kim, Y. Lao, K. K. Parhi, and C. H. Kim, "True random number generator circuits based on single- and multi-phase beat frequency detection," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2014, pp. 1–4.

[23] M. Bucci and R. Luzzi, "Fully digital random bit generators for cryptographic applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 3, pp. 861–875, Apr. 2008.

[24] J. D. J. Golic, "New methods for digital generation and postprocessing of random data," *IEEE Trans. Comput.*, vol. 55, no. 10, pp. 1217–1229, Oct. 2006.

[25] M. Dichtl and J. D. Golić, "High-speed true random number generation with logic gates only," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 2007, pp. 45–62.
[26] J. Holleman, S. Bridges, B. P. Otis, and C. Diorio, "A 3 μW CMOS true random number generator with adaptive floating-gate offset cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1324–1336, May 2008.
[27] S. Srinivasan, S. Mathew, V. Erraguntla, and R. Krishnamurthy, "A 4 Gbps 0.57 pJ/bit process-voltage-temperature variation tolerant all-digital true random number generator in 45 nm CMOS," in *Proc. 22nd Int. Conf. VlSI Design*, New Delhi, India, Jan. 2009, pp. 301–306.
[28] K. Yoshimura, J. Muramatsu, P. Davis, T. Harayama, H. Okumura, S. Morikatsu, H. Aida, and A. Uchida, "Secure key distribution using correlated randomness in lasers driven by common random light," *Phys. Rev. Lett.*, vol. 108, no. 7, pp. 070602-1–070602-5, Feb. 2012.
[29] H. Koizumi, S. Morikatsu, H. Aida, T. Nozawa, I. Kakesu, A. Uchida, K. Yoshimura, J. Muramatsu, and P. Davis, "Information-theoretic secure key distribution based on common random-signal induced synchronization in unidirectionally-coupled cascades of semiconductor lasers," *Opt. Express*, vol. 21, no. 15, pp. 17869–17893, Jul. 2013.
[30] T. Honjo, A. Uchida, K. Amano, K. Hirano, H. Someya, H. Okumura, K. Yoshimura, P. Davis, and Y. Tokura, "Differential-phase-shift quantum key distribution experiment using fast physical random bit generator with chaotic semiconductor lasers," *Opt. Express*, vol. 17, no. 11, pp. 9053–9061, May 2009.
[31] H. Miyazawa and M. Fushimi, "An implementation of a 5-term GFSR random number generator for parallel computations," in *Proc. Int. Symp. Oper. Res. Appl.*, Zhangjiajie, China, 2009, pp. 448–452.
[32] R. F. Fox and J. Keizer, "Amplification of intrinsic fluctuations by chaotic dynamics in physical systems," *Phys. Rev. A, Gen. Phys.*, vol. 43, no. 4, pp. 1709–1720, 1991.
[33] F. Pareschi, G. Setti, and R. Rovatti, "Implementation and testing of high-speed CMOS true random number generators based on chaotic systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3124–3137, Dec. 2010.
[34] I. Çiçek, A. E. Pusane, and G. Dundar, "A novel design method for discrete time chaos based true random number generators," *Integration*, vol. 47, no. 1, pp. 38–47, 2014.
[35] E. Farcot, S. Best, R. Edwards, I. Belgacem, X. Xu, and P. Gill, "Chaos in a ring circuit," *Chaos*, vol. 29, no. 4, p. 043103, Apr. 2019.
[36] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 32, no. 2984, pp. 50–51, Jul. 1928.
[37] M. Bucci, L. Germani, R. Luzzi, A. Trifiletti, and M. Varanonuovo, "A high-speed oscillator-based truly random number source for cryptographic applications on a smart card IC," *IEEE Trans. Comput.*, vol. 52, no. 4, pp. 403–409, Apr. 2003.
[38] Ü. Güler and G. Dündar, "Modeling CMOS ring oscillator performance as a randomness source," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 3, pp. 712–724, Mar. 2014.
[39] C. Liu, "Jitter in oscillators with 1/*f* noise sources and application to true RNG for cryptography," Ph.D. dissertation, Dept. Elect. Eng., Worcester Polytech. Inst., Worcester, MA, USA, 2006.
[40] M. Herrero-Collantes and J. C. Garcia-Escartin, "Quantum random number generators," *Rev. Mod. Phys.*, vol. 89, no. 1, pp. 015004-1–015004-48 Feb. 2016.
[41] V. Bagini and M. Bucci, "A design of reliable true random number generator for cryptographic applications," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 1999, pp. 204–218.
[42] M. Matsumoto, R. Ohba, K. Ikegami, T. Tanamoto, and S. Fujita, "1200 μm^2 physical random-number generators based on SiN MOSFET for secure smart-card application," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2008, pp. 414–624.
[43] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 179–194, Feb. 1998.
[44] A. Demir, "Phase noise and timing jitter in oscillators with colored-noise sources," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 12, pp. 1782–1791, Dec. 2002.
[45] A. A. Abidi and R. G. Meyer, "Noise in relaxation oscillators," *IEEE J. Solid-State Circuits*, vol. JSSC-18, no. 6, pp. 794–802, Dec. 1983.
[46] J. A. McNeill, "Jitter in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 870–879, Jun. 1997.
[47] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.
[48] U. Guler, A. E. Pusane, and G. Dunder, "Investigating flicker noise effect on randomness of CMOS ring oscillator based true random number generators," in *Proc. Int. Conf. Inf. Sci., Electron. Elect. Eng.*, Sapporo, Japan, 2014, pp. 845–849.
[49] J. Xu, S. Verma, and T. Lee, "Coupled inverter ring I/Q oscillator for low power frequency synthesis," in *Proc. Symp. VLSI Circuits*, Honolulu, HI, USA, 2006, pp. 172–173.
[50] C. S. Petrie and J. A. Connelly, "Modeling and simulation of oscillator-based random number generators," in *Proc. IEEE Int. Symp. Circuits Syst.*, Atlanta, GA, USA, May 1996, pp. 324–327.
[51] H. Bock, M. Bucci, and R. Luzzi, "An offset-compensated oscillator-based random bit source for security applications," in *Proc. 6th Int. Workshop Cryptograph. Hardw. Embedded Syst. (CHES)*, Cambridge, MA, USA, Jun. 2004, pp. 27–83.
[52] Ü. Güler and G. Dündar, "Modeling phase noise and jitter in subthreshold region and assessing the randomness performance of CMOS ring oscillators," in *Proc. Int. Conf. Synth., Modeling Anal. Simulation Methods Appl. Circuit Design*, Seville, Spain, 2012, pp. 257–260.
[53] Ü. Güler and G. Dündar, "Maximizing randomness in ring oscillators for security applications," in *Proc. 20th Eur. Conf. Circuit Theory Design*, Linkoping, Sweden, 2011, pp. 118–121.
[54] K. Wold and S. Petrovic, "Optimizing speed of a true random number generator in FPGA by spectral analysis," in *Proc. 4th Int. Conf. Comput. Sci. Converg. Inf. Technol.*, Seoul, South Korea, 2009, pp. 1105–1110.
[55] V. B. Suresh and W. P. Burleson, "Entropy and energy bounds for metastability based TRNG with lightweight post-processing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 7, pp. 1785–1793, Jul. 2015.
[56] N. Bochard, F. Bernard, and V. Fischer, "Observing the randomness in RO-based TRNG," in *Proc. Int. Conf. Reconfigurable Comput. (FPGAs)*, Quintana Roo, Mexico, 2009, pp. 237–242.
[57] Ü. Güler, S. Ergün, and G. Dündar, "A digital IC random number generator with logic gates only," in *Proc. 17th IEEE Int. Conf. Electron., Circuits Syst.*, Athens, Greece, Dec. 2010, pp. 239–242.
[58] L. Li and S. Li, "A digital TRNG based on cross feedback ring oscillators," *IEICE Trans. Fundam. Electron. Commun. Comput. Sci.*, vol. E97A, no. 1, pp. 284–291, Jan. 2014.
[59] M. Baudet, D. Lubicz, J. Micolod, and A. Tassiaux, "On the security of oscillator-based random number generators," *J. Cryptol.*, vol. 24, no. 2, pp. 398–425, 2011.
[60] A. T. Markettos and S. W. Moore, "The frequency injection attack on ring-oscillator-based true random number generators," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 2009, pp. 317–331.
[61] P. Z. Wieczorek, "Lightweight TRNG based on multiphase timing of bistables," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 7, pp. 1043–1054, Jul. 2016.
[62] M. T. Rahman, K. Xiao, D. Forte, X. Zhang, J. Shi, and M. Tehranipoor, "TI-TRNG: Technology independent true random number generator," in *Proc. 51st Annu. Design Autom. Conf.*, San Francisco, CA, USA, 2014, pp. 1–6.
[63] E. Bohl, M. Lewis, and S. Galkin, "A true random number generator with on-line testability," in *Proc. 19th IEEE Eur. Test Symp.*, Paderborn, Germany, May 2014, pp. 1–6.
[64] M. Epstein, L. Hars, R. Krasinski, M. Rosner, and H. Zheng, "Design and implementation of a true random number generator based on digital circuit artifacts," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 2003, pp. 152–165.
[65] P. Z. Wieczorek and K. Golofit, "Dual-metastability time-competitive true random number generator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 134–145, Jan. 2014.
[66] M. Majzoobi, F. Koushanfar, and S. Devadas, "FPGA-based true random number generation using circuit metastability with adaptive feedback control," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 2011, pp. 17–32.
[67] W. A. M. van Noije, W. T. Liu, and S. Navarro, "Metastability behavior of mismatched CMOS flip-flops using state diagram analysis," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Diego, CA, USA, May 1993, pp. 27.7.1–27.7.4.
[68] H. Hata and S. Ichikawa, "FPGA implementation of metastability-based true random number generator," *IEICE Trans. Inf. Syst.*, vol. E95D, no. 2, pp. 426–436, Feb. 2012.
[69] L. Kleeman and A. Cantoni, "Metastable behavior in digital systems," *IEEE Design Test Comput.*, vol. MDAT-4, no. 6, pp. 4–19, Dec. 1987.

[70] S. Mathew, D. Johnston, P. Newman, S. Satpathy, V. Suresh, M. Anders, H. Kaul, G. Chen, A. Agarwal, and S. Hsu, "μ RNG: A 300–950 mV 323 Gbps/W all-digital full-entropy true random number generator in 14 nm FinFET CMOS," in *Proc. ESSCIRC Conf. 41st Eur. Solid-State Circuits Conf.*, Graz, Austria, Sep. 2015, pp. 1–10.

[71] M. Varchola and M. Drutarovsky, "New high entropy element for FPGA based true random number generators," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.*, Berlin, Germany, 2010, pp. 351–365.

[72] P. Z. Wieczorek, "Dual-metastability FPGA-based true random number generator," *Electron. Lett.*, vol. 49, no. 12, pp. 744–745, Jun. 2013.

[73] P. Z. Wieczorek, "An FPGA implementation of the resolve time-based true random number generator with quality control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 12, pp. 3450–3459, Dec. 2014.

[74] P. Z. Wieczorek and K. Gołofit, "True random number generator based on flip-flop resolve time instability boosted by random chaotic source," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 4, pp. 1279–1292, Apr. 2018.

[75] S. Tao and E. Dubrova, "TVL-TRNG: Sub-microwatt true random number generator exploiting metastability in ternary valued latches," in *Proc. IEEE 47th Int. Symp. Multiple-Valued Logic*, Novi Sad, Serbia, 2002, pp. 130–135.

[76] A. Beirami and H. Nejati, "A framework for investigating the performance of chaotic-map truly random number generators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 7, pp. 446–450, Jul. 2013.

[77] M. Drutarovsky and P. Galajda, "A robust chaos-based true random number generator embedded in reconfigurable switched-capacitor hardware," in *Proc. 17th Int. Conf. Radioelektronika*, Brno, Czech Republic, 2007, pp. 1–6.

[78] R. Zhang, H. L. D. de S. Cavalcante, Z. Gao, D. J. Gauthier, J. E. S. Socolar, M. M. Adams, and D. P. Lathrop, "Boolean chaos," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 80, no. 4, p. 045202, Oct. 2009.

[79] W. Li, I. Reidler, Y. Aviad, Y. Huang, H. Song, Y. Zhang, M. Rosenbluh, and I. Kanter, "Fast physical random-number generation based on room-temperature chaotic oscillations in weakly coupled superlattices," *Phys. Rev. Lett.*, vol. 111, no. 4, p. 044102, Jul. 2013.

[80] T. Harayama, S. Sunada, K. Yoshimura, J. Muramatsu, K.-I. Arai, A. Uchida, and P. Davis, "Theory of fast nondeterministic physical random-bit generation with chaotic lasers," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 85, no. 4, p. 046215, Apr. 2012.

[81] I. Reidler, Y. Aviad, M. Rosenbluh, and I. Kanter, "Ultrahigh-speed random number generation based on a chaotic semiconductor laser," *Phys. Rev. Lett.*, vol. 103, no. 2, p. 024102, Jul. 2009.

[82] V. Tavas, A. S. Demirkol, S. Ozoguz, A. Zeki, and A. Toker, "Integrated cross-coupled chaos oscillator applied to random number generation," *IET Circuits, Devices Syst.*, vol. 3, no. 1, pp. 1–11, Feb. 2009.

[83] M. E. Yalcin, J. A. K. Suykens, and J. Vandewalle, "True random bit generation from a double-scroll attractor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1395–1404, Jul. 2004.

[84] J. Dvorakova, "Chaos in nonautonomous discrete dynamical systems," *Commun. Nonlinear Sci. Numer. Simul.*, vol. 17, no. 12, pp. 4649–4652, Dec. 2012.

[85] M. François, D. Defour, and C. Negre, "A fast chaos-based pseudo-random bit generator using binary64 floating-point arithmetic," *Informatica*, vol. 38, no. 2, pp. 115–124, 2014.

[86] Y. Wang, C. Hui, C. Liu, and C. Xu, "Theory and implementation of a very high throughput true random number generator in field programmable gate array," *Rev. Sci. Instrum.*, vol. 87, no. 4, p. 044704, Apr. 2016.

[87] T. Harayama, S. Sunada, K. Yoshimura, P. Davis, K. Tsuzuki, and A. Uchida, "Fast nondeterministic random-bit generation using on-chip chaos lasers," *Phys. Rev. A, Gen. Phys.*, vol. 83, no. 3, p. 031803, Mar. 2011.

[88] E. Avaroglu, T. Tuncer, A. B. Ozer, B. Ergen, and M. Turk, "A novel chaos-based post-processing for TRNG," *Nonlinear Dyn.*, vol. 81, nos. 1–2, pp. 189–199, Jul. 2015.

[89] M. P. Pawlowski, A. Jara, and M. Ogorzalek, "Harvesting entropy for random number generation for Internet of Things constrained devices using on-board sensors," *Sensors*, vol. 15, no. 10, pp. 26838–26865, Oct. 2015.

[90] L. E. Bassham, A. L. Rukhin, J. Soto, J. R. Nechvatal, M. E. Smid, S. D. Leigh, M. Levenson, M. Vangel, N. A. Heckert, and D. L. Banks, "A statistical test suite for random and pseudorandom number generators for cryptographic applications," Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Tech. Rep. 800-22, May 2001.

[91] G. Marsaglia. *The Marsaglia Random Number CD-ROM including the Diehard Battery of Test of Randomness*. Accessed: Jan. 1995. [Online]. Available: http://stat.fsu.edu/pub/diehard/

[92] P. L'Ecuyer and R. Simard, "TestU01: A C library for empirical testing of random number generators," *AMC Trans. Math. Softw.*, vol. 33, no. 4, Aug. 2007, Art. no. 22.

[93] W. Killmann and W. Schindler, "Evaluation criteria for true (physical) random number generators used in cryptographic applications," in *Proc. Int. Workshop Cryptogr. Hardw. Embedded Syst.* Bonn, Germany: Bundesamt für Sicherheit in der Informationstechnik, 2001.

LISHUANG GONG is currently a Reading Doctor with the Taiyuan University of Technology. Her current research interest includes physical random number generation.

JIANGUO ZHANG received the Ph.D. degree in circuit and system from the Taiyuan University of Technology, China, in 2013, where he is currently an Associate Professor with the Key Laboratory of Advanced Transducers and Intelligent Control System. His research interests include instrument science and measurement technology.

HAIFANG LIU is currently a Reading Doctor with the Taiyuan University of Technology. Her current research interest includes physical random number generation.

LUXIAO SANG is currently a Reading Doctor with the Taiyuan University of Technology. His current research interest includes generation and application of chaotic signal.

YUNCAI WANG received the Ph.D. degree in physics and optics from the Xi'an Institute of Optics and Precision Mechanics, Chinese Academy of Sciences, Shanxi, China, in 1997. Since 2003, he has been a Professor with the Key Laboratory of Advanced Transducers and Intelligent Control System, Taiyuan University of Technology. He is currently a Professor with the School of Information Engineering, Guangdong University of Technology. His current research interests include nonlinear dynamics of semiconductor lasers, fibers and their applications, and generation of physical random number.