A Carrier-Based PWM Strategy Providing Neutral-Point Voltage Oscillation Elimination for Multi-Phase Neutral Point Clamped 3-Level Inverter

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ABSTRACT General pulse width modulation (PWM) model for multi-phase neutral point (NP) clamped (NPC) 3-level inverter (3LI) is described. A novel PWM strategy for N-phase NPC 3LI with unconditional NP voltage balance is proposed as well as its carrier-based realization, in which PWM sequences are generated by comparing a single carrier wave with double modulation waves. The proposed PWM strategy is consistent with the principle of virtual space vector PWM (VSVPWM). However, the mechanism of NP voltage balance under the proposed PWM strategy is based on precisely calculating and executing level 1 action time of each phase, which may be influenced by some non-ideal factors. To avoid that, an active NP voltage control for the proposed PWM strategy is put forward. Then 3-phase and 5-phase NPC 3LIs are built as examples to verify the correctness of the proposed PWM strategy. Finally, the experimental results indicate that the proposed PWM strategy has better NP voltage control abilities.

INDEX TERMS 3-level inverter (3LI), N-phase, neutral point (NP) clamped (NPC), carrier-based, neutral point (NP) voltage.

I. INTRODUCTION

In recent years, researchers have been paying increasingly attentions to multi-level inverters [1], which have a lot of merits. Owing to relatively low total harmonic distortion (THD) and the voltage stress on power devices [2], [3], multi-level inverters are very popular in many fields, such as motor drives [4], [5]. The neutral point clamped 3-level inverter (NPC 3LI) is widely applied among all multi-level topologies, because the hardware circuit is simple and only one dc-voltage source is needed.

The potential unbalanced NP voltage inevitably appearing in some applications, is an inherent issue of NPC 3LI. The NP voltage contains DC offset and AC ripple [6]. Generally speaking, the DC offset should be eliminated and large AC ripple should be suppressed. Large NP voltage ripple can be

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caused by NPC 3LI. This problem can be released by increasing the DC-link capacitance to some extent. The authors of [7] suggested using two isolated dc-voltage sources to keep NP voltage constant. Another method is applying controllable active front-end to the NPC 3LI as DC side, for example back-to-back or 3-level boost circuit, which were studied in [8] and [9]. However, these methods require additional devices, which increase the system hardware costs and complexity. In addition, the reliability of the system is deteriorated due to the addition of the active devices.

Another solution to unbalance NP voltage relates to the improved PWM strategies applied to NPC 3LI [10], [11]. The traditional PWM strategies can be divided into two categories generally. One of these is the carrier-based PWM (CBPWM). An approach has been made to keep NP voltage constant under CBPWM strategy in [12], where the correct NP current direction in each phase is generated with an additional modulated wave injected into the corresponding

modulation wave. It can realize pre-compensation for an unbalanced NP voltage condition. Another is based on space vector PWM (SVPWM). In [13], the SVPWM based strategy takes not only the unbalanced NP voltage but also the influences on the length and position of basic voltage vector into account. Then NP voltage recovery can be achieved quickly by selecting appropriate basic voltage vector. In fact, these two categories are the same in essence [14]. By injecting particular zero-sequence voltage into the modulation wave under CBPWM, the same switching sequences can be thus acquired just like SVPWM. However, the NP voltage will appear low-frequency oscillation under these modulation strategies for NPC 3LI [15], especially when it operates at the conditions of low power factor and high modulation index. Then the output voltage contains low-order harmonics, which is the main drawback of these approaches.

A PWM strategy for NPC 3LI to reduce switching losses, called as discontinuous PWM (DPWM), has been researched in [16]. For the purpose of keeping NP voltage constant, the DPWM strategy is implemented by choosing the most suitable PWM sequence.

The virtual space vector PWM (VSVPWM) is an attractive PWM strategy for NPC 3LI, which can control NP voltage under the conditions of any power factor and modulation index. In recent years, the VSVPWM strategies have been studied intensively, particularly mixing with other modulation strategies, because of the excellent performance on NP voltage control. Hybrid PWM strategy combining VSVPWM with SVPWM is applied in [15], where fully controlling of NP voltage is achieved. In [17], the presented hybrid PWM strategy has excellent characteristic on NP voltage based on choosing proper proportional coefficient, at low switching frequency operating environment. The VSVPWM is extended from three-level to four-level converter in [18], even to arbitrary level in [19]. It is also expanded to some extreme conditions, such as over-modulation region [20]. An improved VSVPWM in [21] exhibits the good NP voltage control capability, which remains NP voltage balance by active NP voltage control.

However, almost all the literatures given above are for 3-phase NPC 3LI. Due to a lot of attractive features, such as fault tolerance, improved reliability, increased efficiency and lower power handling requirements of per-phase, *N*-phase NPC 3LI has been applied to ship propulsion, electric traction and aerospace industry, *et al.* [22], [23]. When the phase number is higher than three, it is very difficult to apply SVPWM to *N*-phase NPC 3LI. And there are few works about NP voltage balance control for *N*-phase NPC 3LI, but this issue is very crucial.

To perfectly control NP voltage like VSVPWM, a novel carrier-based PWM strategy is proposed in this paper, which can be easily extended to *N*-phase NPC 3LI. The main contributions of this paper are as follows. 1. A PWM strategy suitable for *N*-phase NPC 3LI is proposed, which can achieve NP voltage balance unconditionally under any modulation index and power factor. 2. Its carrier implementation is given,

which greatly simplifies the duty ratio calculation. 3. Moreover, an active NP voltage control method suitable for the proposed PWM strategy is presented.

II. *N*-PHASE NPC 3LI AND ITS PWM MODEL
A. *N*-PHASE NPC 3LI
Figure 1 shows the topology of *N*-phase NPC 3LI. C_1 is called the upper capacitance and C_2 is called the lower capacitance. The two will cut the DC-link voltage in half, when no unbalance occurs. Table 1 shows that the output levels are different according to the conducted devices.
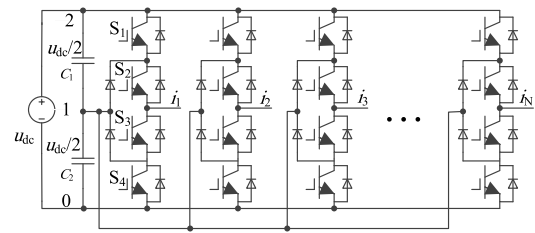

FIGURE 1. Topology of the *N*-phase NPC 3LI.

TABLE 1. The conducted devices corresponding to the output level.

Output level	Conducted device
2	S_1 and S_2
1	S_2 and S_3
0	S_3 and S_4

Assuming $u^{(1)}, u^{(2)} \ldots u^{(N)}$ stand for the *N* phase voltages and $i^{(1)}, i^{(2)} \ldots i^{(N)}$ stand for the *N* phase currents, where the positive current is defined as flowing from the inverter to the load. The phase voltages and currents can be normalized as:

$$u^{(k)} = \frac{mu_{dc}}{2} \cos[\omega t - \frac{2\pi(k-1)}{N}], \quad k = 1, \cdots, N \quad (1)$$

$$i^{(k)} = I_m \cos[\omega t - \frac{2\pi(k-1)}{N} - \varphi], \quad k = 1, \cdots, N \quad (2)$$

where I_m represents the peak value of phase current, φ represents the power factor angle of load, ωt is the phase angle of phase 1 and $\omega t \in [0, 2\pi]$, *m* is the modulation index and $m \in [0, 1.1547]$ [14]. The analysis is done by assuming that the value and direction of *N*-phase currents are considered as constant in a switching period.

These phases can be reclassified according to their instantaneous phase voltages, which are renamed as phase 1 to *N*:

$$u_1 > u_2 > \cdots > u_N \quad (3)$$

where u_1 and u_N are the maximum and minimum phase voltage, respectively.

B. PWM MODEL WITH NP VOLTAGE BALANCE
Based on the principle of volt-second equilibrium, the line-to-line voltages of adjacent two phases, for example u_i and u_{i+1}

and $i = \{1, 2, \ldots, N-1\}$, are satisfied with:

$$
\begin{cases}
d_{12} + 0.5d_{11} + 0d_{10} - d_{22} - 0.5d_{21} - 0d_{20} = \dfrac{u_1 - u_2}{u_{dc}} \\
\vdots \\
d_{i2} + 0.5d_{i1} + 0d_{i0} - d_{(i+1)2} - 0.5d_{(i+1)1} - 0d_{(i+1)0} \\
\quad = \dfrac{u_i - u_{i+1}}{u_{dc}} \\
\vdots \\
d_{(N-1)2} + 0.5d_{(N-1)1} + 0d_{(N-1)0} - d_{N2} - 0.5d_{N1} - 0d_{N0} \\
\quad = \dfrac{u_{N-1} - u_N}{u_{dc}}
\end{cases}
\tag{4}
$$

The duty ratio of all levels of each phase satisfies the following condition:

$$
\sum_{n=0,1,2} d_{kn} = 1, \quad k = 1, \cdots, N
\tag{5}
$$

where d_{kn} is the dwell time of level n of the corresponding phase k.

From the equations (2) and (3), the general PWM model for N-phase NPC 3LI is given. In a switching period, the NP voltage balance can be realized if the total NP current introduced by all phases equals to zero, which can be expressed as:

$$
\sum_{k=1}^{N} i_k d_{k1} = 0
\tag{6}
$$

where i_k is the current of the phase k.

According to the equations (4)-(6) given above, the general PWM model for N-phase NPC 3LI with its NP voltage equilibrium is acquired, where unknown duty ratios are 3N. However, there are only 2N equations. It means other additional restrictive conditions are needed to obtain specific solution for all duty ratios.

Considering that $\sum i_k = 0$ $(k = 1, \cdots, N)$ while the load of N-phase NPC 3LI is star-connected, the simplest solution for (6) is as follow:

$$
d_{11} = d_{21} = \cdots = d_{N1}
\tag{7}
$$

The switching sequence of the maximum phase consists of 1 and 2 levels; the switching sequence of the minimum phase consists of 0 and 1 levels; and the switching sequences of other phases consist of 0, 1 and 2 levels. Therefore, the following equations should be satisfied:

$$
d_{10} = d_{N2} = 0
\tag{8}
$$

After adding equations (7) and (8), the number of equations equals to the number of unknown duty ratios. From (4), (5), (7) and (8), all duty ratios can be expressed as:

$$
d_{k2} = \frac{u_k - u_N}{u_{dc}}, \quad d_{k1} = 1 - \frac{u_1 - u_N}{u_{dc}},
$$
$$
d_{k0} = \frac{u_1 - u_k}{u_{dc}}, \quad k = 1, \cdots, N
\tag{9}
$$

It should be noted that when $N = 3$, the calculated result of the duty ratios given by (9) is consistent with that in literature [21]. Equation (7) is consistent with the basic principle of VSVPWM, and it is extended to N-phase application.

From the above description, it can be seen that the phases corresponding to $u_2 \ldots u_{N-1}$ consist of three levels, which cause increased switching losses comparing to SVPWM. It is the main disadvantage of the proposed PWM strategy.

C. THE CARRIER-BASED REALIZATION

The carrier-based realization means PWM sequences are determined by comparing carrier wave with modulation wave. It is easy to be carried out comparing to other pulse generation methods. To obtain the dwell time of any level n of any phase k given by (9), the dual modulation waves under the proposed PWM strategy for phase k can be expressed as:

$$
u_k' = \frac{u_k - u_N}{2}, \quad u_k'' = \frac{u_{dc} - u_1 - u_k}{2}
\tag{10}
$$

The acquisition of the two PWM sequences depends on the single carrier wave and the dual modulation waves given by (10). And then the whole PWM sequences can be acquired. As a result, the PWM strategy can be realized like CBPWM. The detailed analysis of carrier-based realization can be referred to [21].

Under the proposed PWM strategy, while $m = 0.5$ and 1, the dual modulation waves of one phase for 3-phase, 5-phase and 7-phase NPC 3LI can be acquired, which are illustrated in Figure 2. It is worth noting that the modulation waves are no more sinusoidal, and their shapes change along with the increment of the phase number.

As described in [21], there are no low-order harmonics in output voltage, which is one of the merits of the proposed PWM strategy.

III. ACTIVE NP VOLTAGE CONTROL FOR THE PROPOSED PWM STRATEGY

In theory, under the proposed PWM strategy, the NP voltage does not appear AC ripple and DC offset. However, the practical issues are more complicated due to some non-ideal factors, which result in NP voltage unbalance. The non-ideal factors include: (1) Difference capacitance. Actually the upper and lower capacitances cannot be the same, which cause unbalanced NP voltage; (2) The actual duty ratios are different from the calculated duty ratios given by (9) because of the insertion of dead-time. Deeply discussion of the influences of these non-ideal factors can be referred to [21].

In [21], there are three active NP voltage control approaches based on CB_VSVPWM for 3-phase NPC 3LI, which are two common-mode voltage injection methods and one differential-mode voltage injection method. But these methods cannot be extended to the case of N-phase directly. Some modification is needed.

The NP current has an effect on the NP voltage. Therefore, changing the duty ratio of level 1 can control the NP voltage, which is the basic principle of active NP voltage
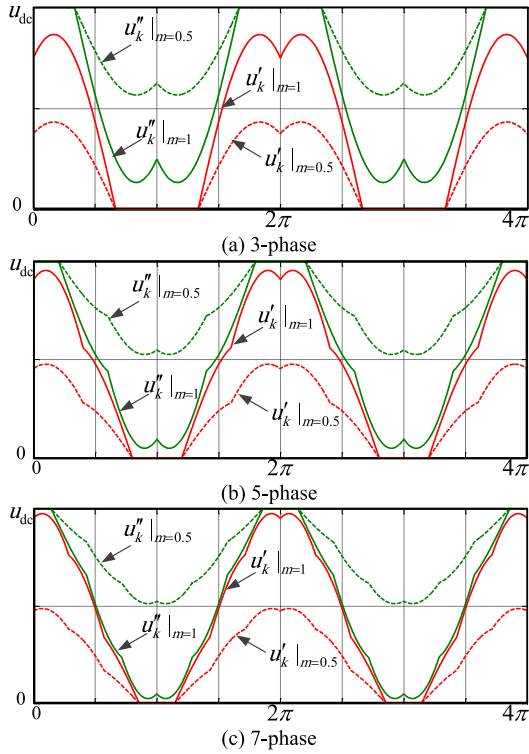
FIGURE 2. The dual modulation waves of one phase under the proposed PWM strategy for 3-, 5- and 7-phase NPC 3LI, while $m = 0.5$ and $m = 1$.

FIGURE 3. Duty ratio adjustment to achieve active NP voltage control.

control method. However, in the process of adjustment, the line-to-line voltage should be not affected, which should be paid attention. Otherwise, the phase current will be distorted.

If only the duty ratio of level 1 of the maximum phase or the minimum phase adjusts, the line-to-line voltage will change. To avoid that, the duty ratio of level 1 of others phase should be adjusted. It means the duty ratio of level 1 of all phases must be changed simultaneously. Active NP voltage control method can be realized by this approach, but it is complex to analyze the total compensation current.

Another approach is adjusting the duty ratios of level 1 of these phases corresponding to $u_2 \ldots u_{N-1}$ to realize active NP voltage control. For these phases, the switching sequences are composed of level 2, 1 and 0. Thus, it is easy to keep phase voltage unchanged after changing the duty ratios of this phase. This method is applied in this paper. For example, assuming the duty ratio of level 2 decreases by Δd_k, the duty ratio of level 1 increases by $2\Delta d_k$, and the duty ratio of level 0 decreases by Δd_k, respectively, then the adjusted phase voltage $u_{k,adj}$ can be rewritten as

$$u_{k,adj} = 2u_{dc}(d_{k2} - \Delta d_k) + u_{dc}(d_{k1} + 2\Delta d_k)$$
$$+ 0(d_{k0} - \Delta d_k) = u_k \quad (11)$$

From (11), the phase voltage is not changed in the process of adjusting the duty ratios, and the line-to-line voltage is thus unchanged. The illustration of this approach is shown
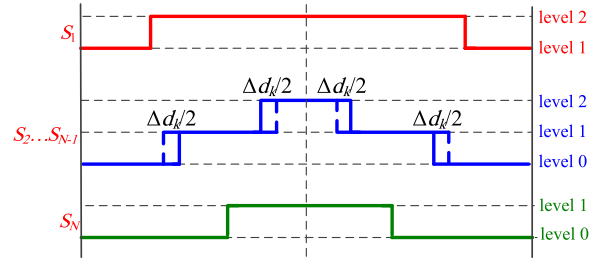
in Figure 3, where the dwell time of the maximum phase and minimum phase is not adjusted. After adjusting, the NP voltage compensation current $i_{k,cmp}$ introduced by the phase k can be expressed as

$$i_{k,cmp} = 2\Delta d_k i_k \quad (12)$$

If the duty ratios of the phases corresponding to $u_2 \ldots u_{N-1}$ are all adjusted, the total compensation current i_{cmp} can be calculated as

$$i_{cmp} = 2 \sum_{k=2,\cdots,N-1} \Delta d_k i_k \quad (13)$$

For convenience, assuming Δd_k is fixed, taking $\Delta d_k = \Delta d$ as an example. Then, (13) can be rewritten as

$$i_{cmp} = 2\Delta d \sum_{k=2,\cdots,N-1} i_k \quad (14)$$

In fact, if the duty ratios of the phases corresponding to $u_2 \ldots u_{N-1}$ are adjusted consistently, the polarity of some phase currents may be opposite, which will weaken the adjustment ability of active NP voltage control. In (14), it can be seen that the polarity of the compensation current can be varied by the polarity of Δd. For obtaining better adjustment ability of active NP voltage control, the polarity of Δd should be changed according to the polarity of i_k. Then, Δd_k can be determined as

$$\Delta d_k = \begin{cases} \Delta d, & \text{if } i_k > 0 \\ -\Delta d, & \text{if } i_k < 0 \end{cases} \quad (15)$$

Therefore, the total compensation current i_{cmp} used to adjust NP voltage can be obtained as:

$$i_{cmp} = 2\Delta d_k \sum_{k=2,\cdots,N-1} |i_k| \quad (16)$$

When $\Delta u_{NP} = u_{C1} - u_{C2} < 0$ is satisfied, the NP voltage should be decreased. Namely, the polarity of i_{cmp} should be positive. Therefore, i_{cmp} as a function of Δu_{NP} can be obtained as:

$$i_{cmp} = \frac{\Delta u_{NP}(C_1 + C_2)}{T_S} \quad (17)$$
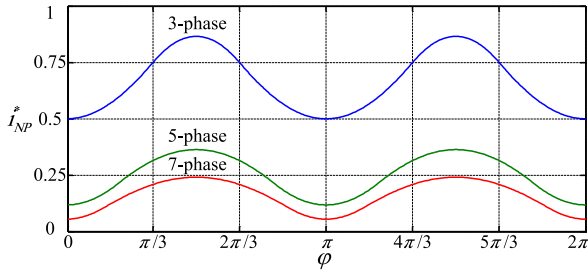
where T_S denotes the switching period.

FIGURE 4. The peak value of i_{NP}^* as a function of φ under SPWM.

From (17), i_{cmp} can be obtained based on Δu_{NP}. Then, the corresponding Δd_k can be obtained according to (16). When active NP voltage control for the proposed PWM strategy is considered, the dual modulation waves can be expressed as

$$\begin{cases} u'_{k,adj} = (d_{k2} - \Delta d_k)u_{dc} \\ u''_{k,adj} = (d_{k1} + d_{k2} + \Delta d_k)u_{dc} \end{cases} \quad k = 2, \cdots, N-1 \quad (18)$$

It is worth noting that when $N = 3$, the proposed active NP voltage control is consistent with the differential-mode voltage injection method proposed in literature [20].

IV. PERFORMANCE ANALYSIS

A. AC RIPPLE ON NP VOLTAGE UNDER SPWM

According to literature [24], the NP current i_{NP} under SPWM can be obtained as

$$i_{NP} = I_m m \sum_{k=1}^{N} \left\{ \left| \cos[\omega t - \frac{2\pi(k-1)}{N}] \right| \right.$$
$$\left. \times \cos[\omega t - \frac{2\pi(k-1)}{N} - \varphi] \right\}$$
$$= I_m m i_{NP}^*$$
$$i_{NP}^* = \sum_{k=1}^{N} \left\{ \left| \cos[\omega t - \frac{2\pi(k-1)}{N}] \right| \right.$$
$$\left. \times \cos[\omega t - \frac{2\pi(k-1)}{N} - \varphi] \right\} \quad (19)$$

(a) 3 phase

(b) 5 phase

(c) 7 phase

FIGURE 5. i_{NP}^* as functions of φ and ωt under SPWM.
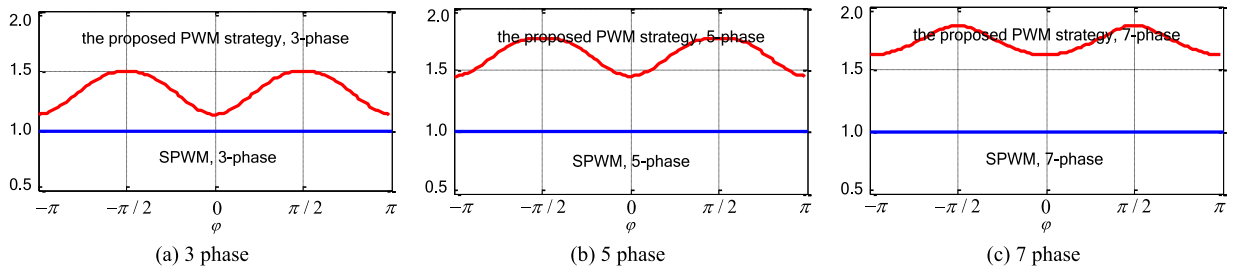

(a) 3 phase

(b) 5 phase

(c) 7 phase

FIGURE 6. Ratio of switching losses of the proposed PWM strategy to SPWM for 3-, 5- and 7-phase NPC 3LI with respect to φ.
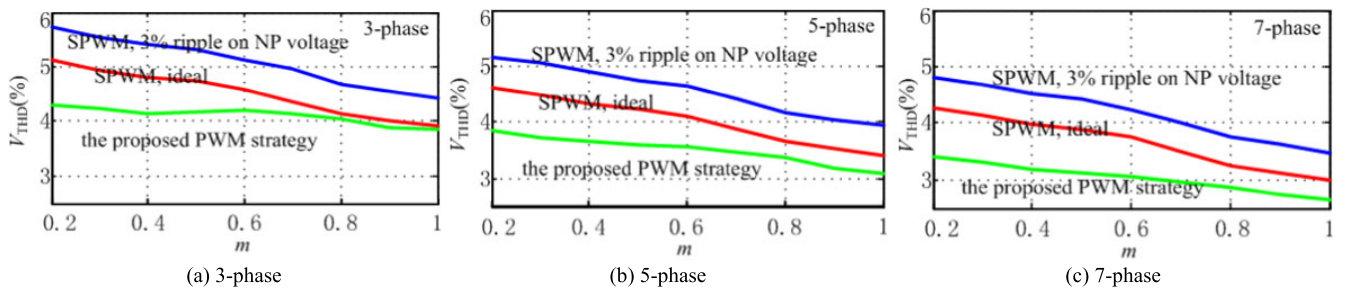

(a) 3-phase

(b) 5-phase

(c) 7-phase

FIGURE 7. V_{THD} for 3-, 5- and 7-phase NPC 3LI with respect to m under SPWM and the proposed PWM strategy.

FIGURE 8. Photograph of the prototype.

TABLE 2. The key inverter parameters for the experiment.

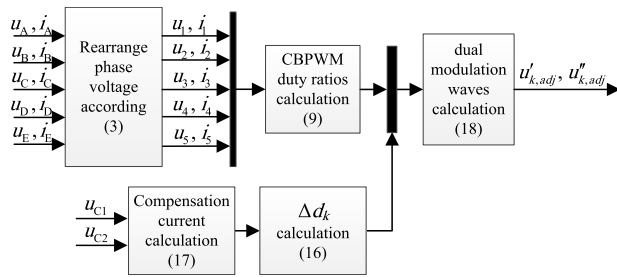| Parameters	Value
DC-link voltage	200V
The upper (lower) capacitance of dc-link	470μF
Resistive-inductive load for low pf (Z_L)	$6e^{j2\pi/5}\Omega$
Resistive-inductive load 1 for high pf (Z_{H1})	$1.5e^{j\pi/5}\Omega$
Resistive-inductive load 2 for high pf (Z_{H2})	$6e^{j\pi/5}\Omega$
Switching frequency	6kHz

FIGURE 9. The flow diagram of the proposed PWM strategy for 5-phase NPC 3LI.

where i_{NP}^* is the normalized NP current factor. Then, the NP voltage can be obtained as:

$$u_{NP} = \frac{1}{2C}\int i_{NP}dt = \frac{I_m m}{2C}\int i_{NP}^* dt \quad (20)$$

Taking $N = 3, 5$ and 7, as examples, the peak value of i_{NP}^* under SPWM strategy with respect to φ is shown in Figure 4. And i_{NP}^* as functions of φ and ωt is shown in Figure 5. From Figures 4 and 5, the peak value of i_{NP}^* is lowest under

$\varphi = 0, \pi$, and 2π, and it is highest under $\varphi = \pi/2$, and $3\pi/2$. Moreover, it can be noted that the peak value of i_{NP}^* decreases with the increment of phase numbers.

From Figure 5, it can be seen that there are obvious fluctuations with 3, 5 and 7 times of fundamental frequency on i_{NP}^* for 3-, 5- and 7-phase respectively, which will result in a low frequency fluctuation on NP voltage. In addition, by comparing Figure 5 (a), (b) and (c), it found that although the fluctuation frequency of i_{NP}^* is proportional to the phase number, the fluctuation amplitude is inversely proportional to the phase number.

However, with the proposed PWM strategy, i_{NP}^* is always zero in one switching cycle theoretically. Therefore, there is no NP voltage ripple in theory, which is one of advantage of the proposed PWM strategy. So, small DC-link capacitor can be used, such as film capacitor with a long life span.

B. SWITCHING LOSS

Compared to SPWM, the main disadvantage for N-phase NPC 3LI of the proposed PWM strategy may be the increased switching loss. In a fundamental period, average switching losses under SPWM and the proposed PWM strategy can be calculated based on the method presented in [25]. Letting the switching losses under SPWM as a baseline, Figure 6 shows the switching losses under the proposed PWM strategy with respect to φ.

From Figure 6, the switching losses under the proposed PWM strategy are always higher than that under SPWM. While $\varphi = 0$ and $\pm\pi$ for 3-, 5- and 7-phase, the switching losses under the proposed PWM strategy are about 1.15, 1.45 and 1.6 times of that under SPWM, respectively. While $\varphi = \pm\pi/2$ for 3-, 5- and 7-phase, the switching losses under the proposed PWM strategy are about 1.5, 1.75 and 1.85 times of that under SPWM, respectively.

C. THD

The total harmonic distortion V_{THD} is a tool for characterizing the harmonic performance of the output voltage, which can be calculated as follows:

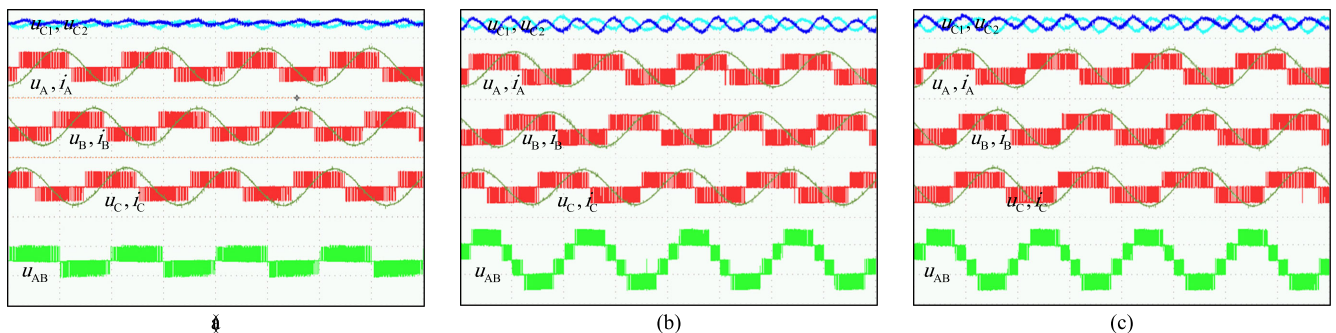$$V_{THD} = \frac{1}{V_1}\sqrt{\sum_{h=2}^{\infty}(V_h)^2} \quad (21)$$

FIGURE 10. Steady state experimental results for 3-phase NPC 3LI under SPWM. (a) m = 0.25, load=Z_{H1}; (b) m = 0.9, load=Z_L; (c) m = 0.9, load=Z_{H2}. (u_{C1} and u_{C2}: 10V/div; u_A, u_B, u_C and u_{AB}: 200V/div; i_A, i_B and i_C: 20A/div; t:10ms/div).

FIGURE 11. Steady state experimental results for 3-phase NPC 3LI under the proposed PWM strategy. (a) $m = 0.25$, load=Z_{H1}; (b) $m = 0.9$, load=Z_L; (c) $m = 0.9$, load=Z_{H2}. (u_{C1} and u_{C2}: 10V/div; u_A, u_B, u_C and u_{AB}: 200V/div; i_A, i_B and i_C: 20A/div; t:10ms/div).

FIGURE 12. Steady state experimental results for 5-phase NPC 3LI under SPWM. (a) $m = 0.25$, load=Z_{H1}; (b) $m = 0.9$, load=Z_L; (c) $m = 0.9$, load=Z_{H2}. (u_{C1} and u_{C2}: 10V/div; u_A, u_B, u_C, u_D, u_E and u_{AB}: 200V/div; i_A, i_B, i_C, i_D and i_E: 20A/div; t:10ms/div).
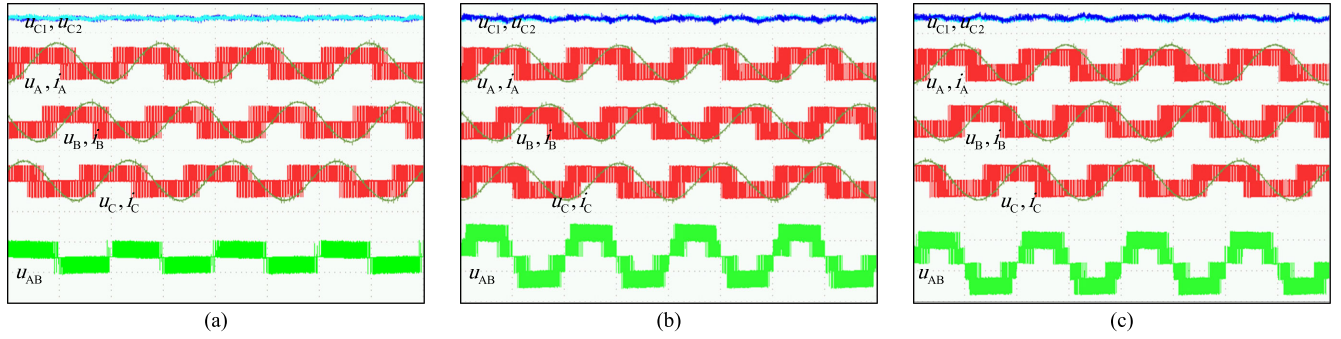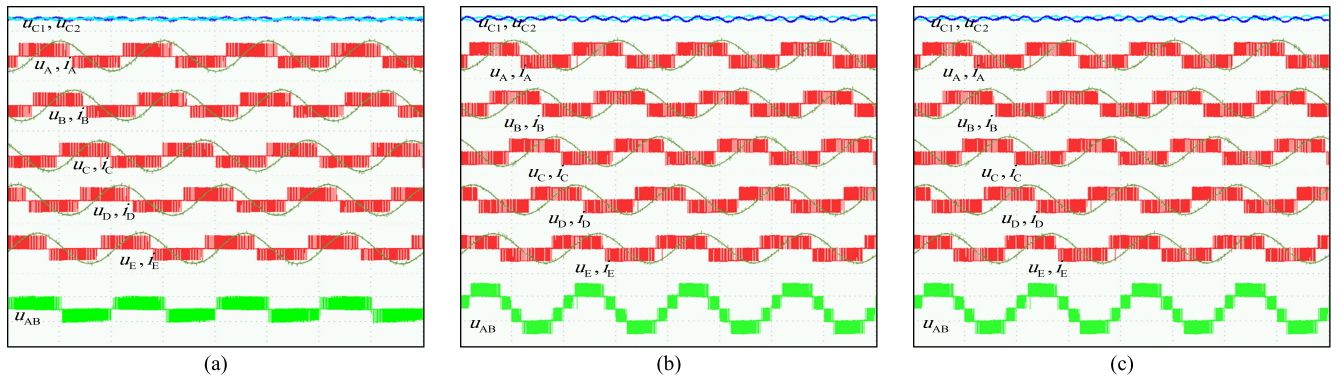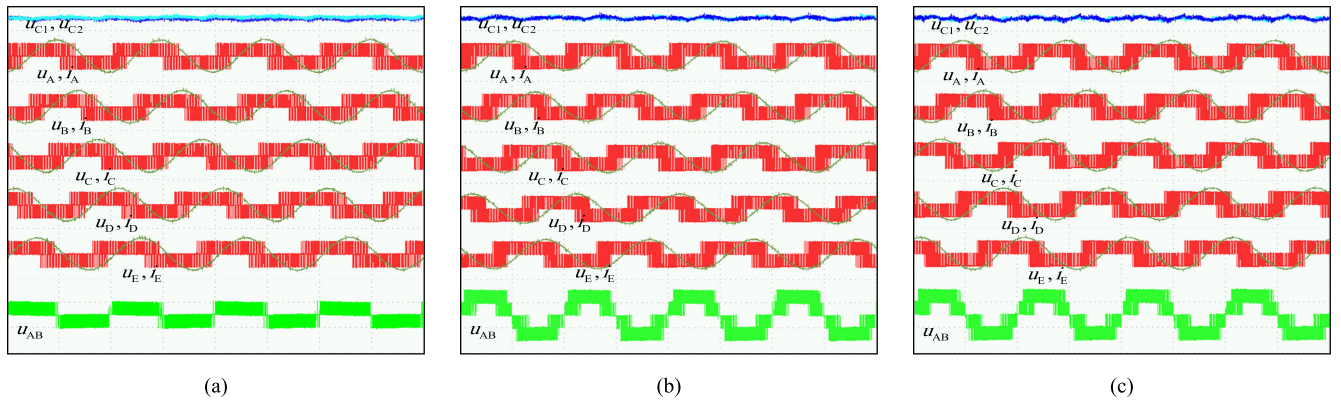

FIGURE 13. Steady state experimental results for 5-phase NPC 3LI under the proposed PWM strategy. (a) $m = 0.25$, load=Z_{H1}; (b) $m = 0.9$, load=Z_L; (c) $m = 0.9$, load=Z_{H2}. (u_{C1} and u_{C2}: 10V/div; u_A, u_B, u_C, u_D, u_E and u_{AB}: 200V/div; i_A, i_B, i_C, i_D and i_E: 20A/div; t:10ms/div).

where V_1 and V_h stand for the root mean square value of the fundamental frequency and the h-th harmonic component, respectively. Figure 7 shows the V_{THD} related to m under SPWM and the proposed PWM strategy. Under SPWM, the AC ripple on NP voltage is an inherent problem. Thus, without and with 3% ripple on NP voltage, V_{THD} under these two cases are considered respectively.

It can be seen from Figure 7 that the curve of V_{THD} under the proposed PWM strategy is always lower than that of SPWM, regardless of with or without NP voltage ripple. Under SPWM, V_{THD} with NP voltage ripple is about 0.5%

higher than that without NP voltage ripple. Moreover, with the increment of the phase numbers, V_{THD} are all reduced. Based on Figure 7, the output performance of line-to-line voltage under the proposed PWM strategy is better than that of SPWM.

V. EXPERIMENTAL RESULTS

The prototype of 3-phase and 5-phase NPC 3LI is built to verify the proposed PWM strategy, which is shown in Figure 8. As indicated in table 2, the main system parameters are presented. DSP MC56F834 is the main processor

TABLE 3. The percent of low order harmonics and THD for 3-phase and 5-phase NPC 3LI under SPWM and the proposed PWM strategy.

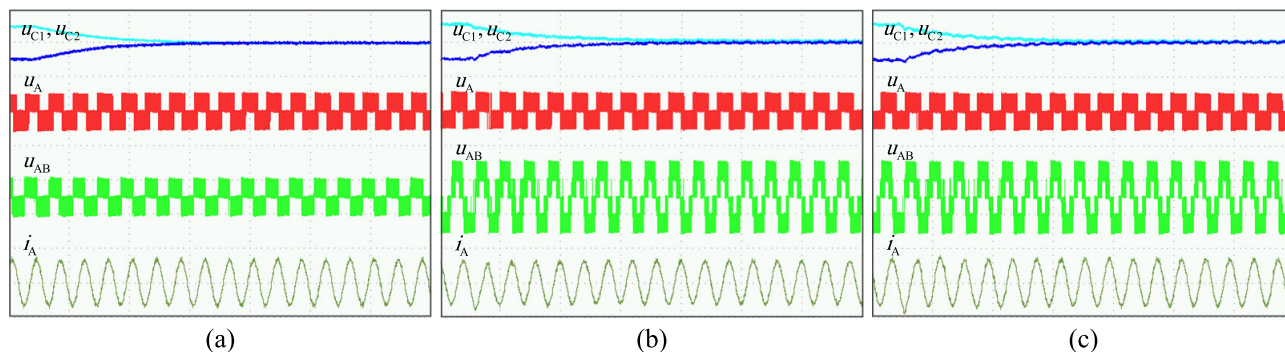|	Fig.10(a)	Fig.10(b)	Fig.10(c)	Fig.11(a)	Fig.11(b)	Fig.11(c)	Fig.12(a)	Fig.12(b)	Fig.12(c)	Fig.13(a)	Fig.13(b)	Fig.13(c)
dc	0.012	0.011	0.013	0.005	0.004	0.006	0.010	0.009	0.008	0.007	0.007	0.008
1	100	100	100	100	100	100	100	100	100	100	100	100
2	0.353	0.215	0.221	0.259	0.167	0.182	0.264	0.175	0.162	0.245	0.157	0.158
3	0.389	0.114	0.136	0.229	0.076	0.074	0.278	0.154	0.133	0.258	0.154	0.132
4	0.272	0.147	0.215	0.227	0.134	0.128	0.257	0.132	0.156	0.247	0.133	0.125
5	0.642	0.871	0.887	0.173	0.183	0.158	0.212	0.124	0.148	0.209	0.149	0.124
6	0.219	0.189	0.153	0.186	0.117	0.114	0.220	0.131	0.150	0.189	0.137	0.119
7	0.554	0.772	0.773	0.139	0.131	0.122	0.554	0.772	0.773	0.139	0.131	0.122
8	0.277	0.124	0.139	0.165	0.109	0.104	0.264	0.135	0.142	0.218	0.105	0.107
9	0.265	0.102	0.105	0.136	0.079	0.089	0.431	0.644	0.607	0.109	0.132	0.124
10	0.162	0.107	0.111	0.118	0.072	0.085	0.256	0.130	0.131	0.161	0.107	0.108
11	0.197	0.672	0.764	0.149	0.153	0.132	0.387	0.572	0.593	0.084	0.093	0.078
12	0.154	0.099	0.103	0.106	0.077	0.081	0.215	0.109	0.110	0.210	0.107	0.108
13	0.183	0.589	0.712	0.118	0.128	0.098	0.189	0.104	0.107	0.186	0.112	0.109
14	0.106	0.084	0.092	0.107	0.079	0.085	0.170	0.108	0.109	0.164	0.107	0.111
15	0.134	0.085	0.091	0.094	0.067	0.051	0.163	0.101	0.099	0.149	0.106	0.105
16	0.122	0.079	0.084	0.097	0.070	0.076	0.152	0.107	0.108	0.139	0.107	0.117
17	0.212	0.352	0.427	0.109	0.094	0.076	0.141	0.095	0.142	0.130	0.109	0.107
18	0.118	0.086	0.081	0.082	0.075	0.077	0.125	0.096	0.133	0.129	0.095	0.105
19	0.224	0.286	0.386	0.102	0.083	0.063	0.274	0.307	0.323	0.121	0.096	0.098
20	0.101	0.074	0.082	0.079	0.069	0.078	0.121	0.088	0.078	0.117	0.088	0.086
THD	5.720	4.822	4.849	4.526	4.127	4.013	4.813	4.574	4.208	3.754	3.319	3.278

FIGURE 14. The NP voltage recovery process under the proposed PWM strategy with active NP voltage control for 3-phase NPC 3LI. (a) $m = 0.25$, load=Z_{H1}; (b) $m = 0.9$, load=Z_L; (c) $m = 0.9$, load=Z_{H2}. (u_{C1} and u_{C2}: 20V/div; u_A and u_{AB}: 200V/div; i_A: 20A/div; t: 50ms/div).

of the system and the chip's manufacturer is Freescale. The flow diagram for 5-phase application is shown in Figure 9, and the similar flow diagram can be obtained for 3-phase system.

Under SPWM with active NP voltage control method, the steady state experimental results for 3-phase and 5-phase NPC 3LI with respect to m and φ are illustrated in Figures 10 and 12, respectively. As shown in Figures 10 and 12, there are obvious AC ripple on NP voltage respectively with triple and quintuple fundamental frequency. Moreover, the amplitude of AC ripple under 3-phase is greater than that under 5-phase, which is consistent with the simulation results in Figure 5. The steady state experimental results for 3-phase and 5-phase NPC 3LI under the proposed

PWM strategy with respect to m and φ, is illustrated in Figures 11 and 13, respectively. It can be seen that the NP voltage is well controlled. Due to that, film capacitor can be thus used as the DC-link capacitor for long service life.

Under SPWM and the proposed PWM strategy, the measured low order harmonics and THD (%) for 3-phase and 5-phase NPC 3LI are shown in Table 3 by power analyzer Yokogawa WT3000. Due to the NP voltage oscillation, the low frequency harmonics emerge under SPWM, which deteriorates the output characteristics. Since the NP voltage control ability under the proposed PWM strategy is better than that of SPWM, the low order harmonics are reduced significantly. The harmonic characteristics are similar to simulations presented in Figure 7.
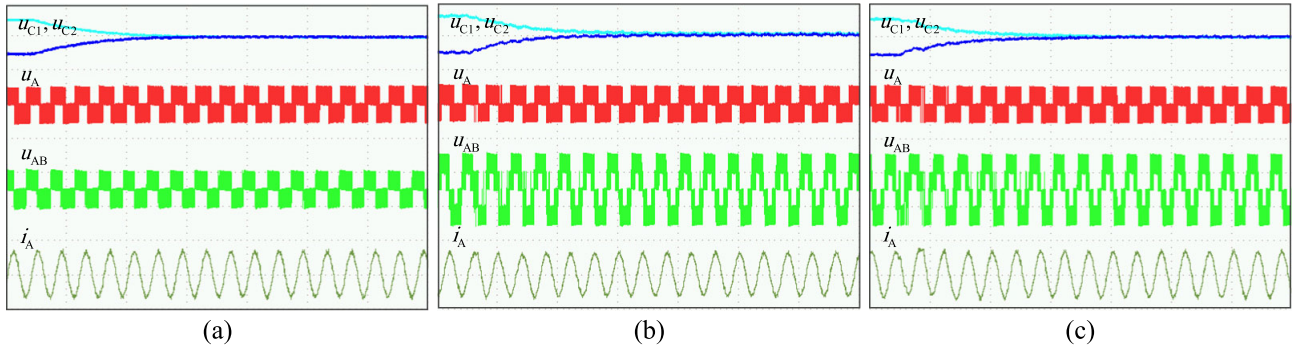
FIGURE 15. The NP voltage recovery process under the proposed PWM strategy with active NP voltage control for 5-phase NPC 3LI. (a) $m = 0.25$, load=Z_{H1}; (b) $m = 0.9$, load=Z_L; (c) $m = 0.9$, load=Z_{H2}. (u_{C1} and u_{C2}: 20V/div; u_A and u_{AB}: 200V/div; i_A: 20A/div; t: 50ms/div).
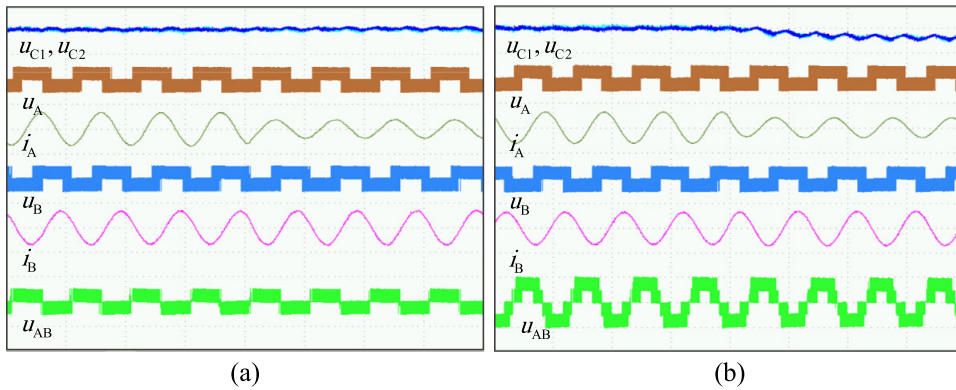

FIGURE 16. The proposed PWM strategy for 3-phase NPC 3LI when load of phase A is suddenly changed. (a) $m = 0.25$. (b) $m = 0.9$. (u_{C1} and u_{C2}: 20V/div; u_A, u_B and u_{AB}: 200V/div; i_A and i_B: 20A/div; t: 20ms/div).

TABLE 4. Comparison results between SPWM and the proposed PWM strategy.

	SPWM	the proposed PWM strategy
Switching numbers in one switching cycle	N	2N-2
Low frequency harmonics under unbalanced NP voltage	Bad	Good
Self-equilibrium ability of NP voltage	Yes	No
Active NP voltage control	Maybe no	Must

The NP voltage recovery abilities of active NP voltage control for 3-phase and 5-phase NPC 3LI under the proposed PWM strategy are shown in Figure 14 and 15. When active NP voltage control method is applied, the NP voltage can be adjusted quickly from the state of unbalance to balance.

The dynamic experimental results for 3-phase and 5-phase NPC 3LI under the proposed strategy with active NP voltage control method are illustrated in Figure 16, where the load of phase A is changed suddenly. Figure 16 shows a good control performance on NP voltage under the proposed PWM strategy, both in steady and dynamic process. To describe the characteristics between SPWM and the proposed PWM strategy, Table 4 shows the comparison results.

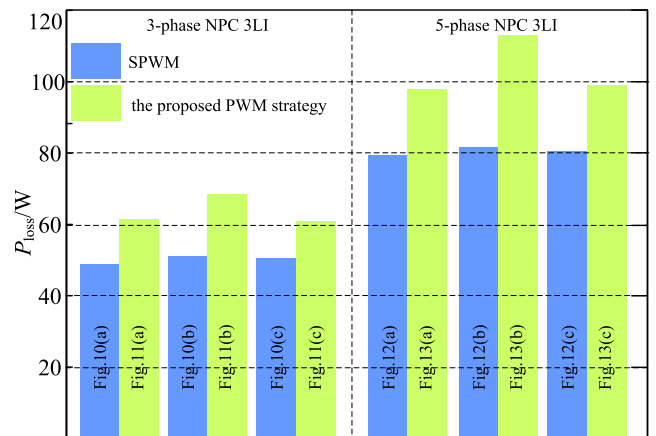The comparison of measured losses for 3-phase and 5-phase NPC 3LI under SPWM and the proposed PWM

FIGURE 17. The measured losses comparison for 3-phase and 5-phase NPC 3LI under SPWM and the proposed PWM strategy.

strategy is illustrated in Figure 17. In the experiments, the switching losses of only one phase including four IGBTs are measured by using Tektronix TPS2024 oscilloscope. The collector-to-emitter voltage and the corresponding collector current of each IGBT are simultaneously measured, and then the professional power analysis module of TPS2024 is used to calculate the switching losses. After simple calculation, the total switching losses of all IGBTs are finally obtained. Among these situations, the losses under the proposed PWM

strategy are significantly larger than that under SPWM, especially in the situation of Z_L. Moreover, under loads of high power factor, the switching losses of the proposed PWM strategy are a little larger than that SPWM.

VI. CONCLUSION

This paper presents a novel PWM strategy for N-phase NPC 3LI with unconditional NP voltage balance and its carrier-based realization. According to this method, by comparing a single carrier wave with the double modulation waves, the PWM sequences are then obtained. Under the proposed PWM strategy, the mechanism of NP voltage balance is analyzed based on calculating and executing the action time of level 1 of all phases precisely. In fact, to avoid the effect of non-ideal factors, the proposed PWM strategy with active NP voltage control method is also described in detail. The proposed PWM strategy has better NP voltage control abilities both in steady and dynamic process, which has been verified by experimental results. So, selecting film capacitor as the DC-link capacitor for long service life will become possible. However, the main disadvantage of the proposed PWM strategy is the increased switching loss, which limits its application in some degree. It should make a compromise mainly between NP voltage oscillation and switching loss according to practical applications.

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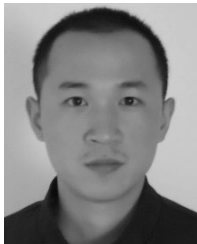
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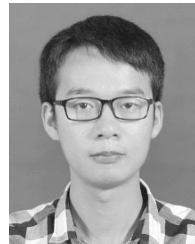
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