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Standard Cell-Based Ultra-Compact DACs in 40-nm CMOS

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ABSTRACT In this paper, very compact, standard cell-based Digital-to-Analog converters (DACs) based on the Dyadic Digital Pulse Modulation (DDPM) are presented. As fundamental contribution, an optimal sampling condition is analytically derived to enhance DDPM conversion with inherent suppression of spurious harmonics. Operation under such optimal condition is experimentally demonstrated to assure resolution up to 16 bits, with 9.4-239X area reduction compared to prior art. The digital nature of the circuits also allows extremely low design effort in the order of 10 man-hours, portability across CMOS generations, and operation at the lowest supply voltage reported to date. The limitations of DDPM converters, the benefits of the optimal sampling condition and digital calibration were explored through the optimized design and the experimental characterization of two DACs with moderate and high resolution. The first is a general-purpose DAC for baseband signals achieving 12-bit (11.6 ENOB) resolution at 110kS/s sample rate and consuming 50.8μW, the second is a DAC for DC calibration achieving 16-bit resolution with 3.1-LSB INL, 2.5-LSB DNL, 45μW power, at only 530μm^2 area.

INDEX TERMS Digital to analog converter (DAC), automated design, calibration, fully synthesizable, fully digital, ultra-low design effort, standard-cell-based analog circuits.

I. INTRODUCTION

Although digital circuits have benefitted tremendously from technology scaling, the design of analog and mixed signal blocks has become increasingly challenging. This is due to several factors, such as lower supply voltages, poor scaling of analog properties of transistors, very limited area shrinkage across technology generations, and significantly higher design effort. This limitation has led to recent efforts to introduce architectures of analog/mixed signal blocks that are mostly or completely based on digital standard cells, to meet the stringent area, cost and design effort requirements of nodes for the Internet of Things (IoT) [1]-[10]. This permits indeed to specify their operation through behavioral description in a hardware description language (HDL), and implement them through fully-automated design flows. This drastically reduces the design effort, and brings the advantages of digital circuits, such as design and technology portability, low-voltage operation, and effective area shrinkage at more advanced technology generations.

This paper focuses on digital-to-analog converters (DACs), which are key building blocks for sensor readout, on-chip tuning/calibration, reference generation, audio processing and threshold generation for event detection [11]–[15]. Conventional single-bit sigma-delta ($\Sigma\Delta$) DACs and pulse-width modulation (PWM) DACs are fully digital, but demand high-order $\Sigma\Delta$ modulators and digital interpolators at high clock rates [16], which make them not attractive in tightly area- and power-constrained systems. Also, PWM DACs require large, high-order reconstruction filters to suppress image frequencies [14], [15].

In view of the limits of single-bit $\Sigma\Delta$ and PWM fully-digital DACs, state-of-the-art low-frequency DACs are mostly based on hybrid architectures, including a high-order multi-bit $\Sigma\Delta$ noise shaper with low (e.g., 32-64X) oversampling ratio and an analog DAC (e.g., current-steering, resistive string) [11]–[13]. Compared to fully-digital DACs, the presence of the analog sub-DAC brings the limitations of analog designs. As a result, the minimum voltage $V_{DD,min}$ of

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DACs from prior art is in the 1.8-3.3V range, with very few exceptions at 1.2V [17], and 0.8V [18].

To address the above challenges, the Dyadic Digital Pulse Modulation (DDPM) was recently proposed in [19]. The DDPM modulation moves most of the energy of image spectral components to much higher frequencies than PWM, reducing the area of the reconstruction filter roughly by 2^N, being N the resolution [19]. Also, the DDPM modulation does not require area- and power-hungry interpolation as opposed to $\Sigma\Delta$ DACs, and has no stability issue thanks to its open-loop architecture.

In this paper, standard cell-based Nyquist-rate DDPM DACs are explored in terms of achievable resolution, and novel techniques to improve it. From the spectral analysis or the DDPM modulated signal, an optimal sampling condition is analytically derived to suppress spurious harmonics. Suitable digital calibration techniques and dynamic resolution-sampling rate tradeoff are also discussed and experimentally demonstrated. A testchip with two DDPM DAC designs in 40nm is experimentally characterized to evaluate the effectiveness of such techniques, and to demonstrate the versatility of the DDPM approach up to relatively high resolutions. The first design is a 12-bit, 110kS/s (DAC_12) general-purpose converter occupying an area of only $270\mu m^2$, and a power of $50.8\mu W$. The second design is a 16-bit DAC (DAC_16) for static signal generation, which targets the typical requirements of on-chip calibration and high-resolution on-chip DC voltage generation for analog and mixed-signal integrated systems. Such DACs are extensively required in several applications, including high-frequency A/D and D/A converter calibration [20], [21], RF transceiver calibration [22], on-chip filter tuning/reconfiguration [23], [24], beamforming [24], reconfigurable/digitally-assisted analog, reconfigurable reference voltage generation [25]–[28]. The DAC_16 design achieves 16-bit static resolution at ± 3.1LSB integral non-linearity (INL), ± 2.5LSB differential non-linearity (DNL) at $530\mu m^2$ area, and $45\mu W$ power. This work shows that DDPM DACs can actually be very competitive in terms of resolution, in spite of their very compact area (9.4-239X lower than prior art).

The paper is structured as follows. In Section II, the basic spectral properties and an optimal sampling condition for DDPM D/A conversion are derived. In Section III, the architecture of the proposed DACs is described, along with an off-line calibration strategy for resolution enhancement. In Section IV, measurement results are discussed. Section V concludes the paper.

II. D/A CONVERSION VIA DDPM MODULATION AND OPTIMAL SAMPLING CONDITION

In DDPM D/A conversion [19], the N-bit integer binary input D_{in} to be converted is expressed in terms of its binary representation $(b_{N-1}b_{N-2}\ldots 0)$ as:

$$D_{in} = \sum_{i=0}^{N-1} b_i 2^i \quad b_i \in \{0, 1\} \tag{1}$$

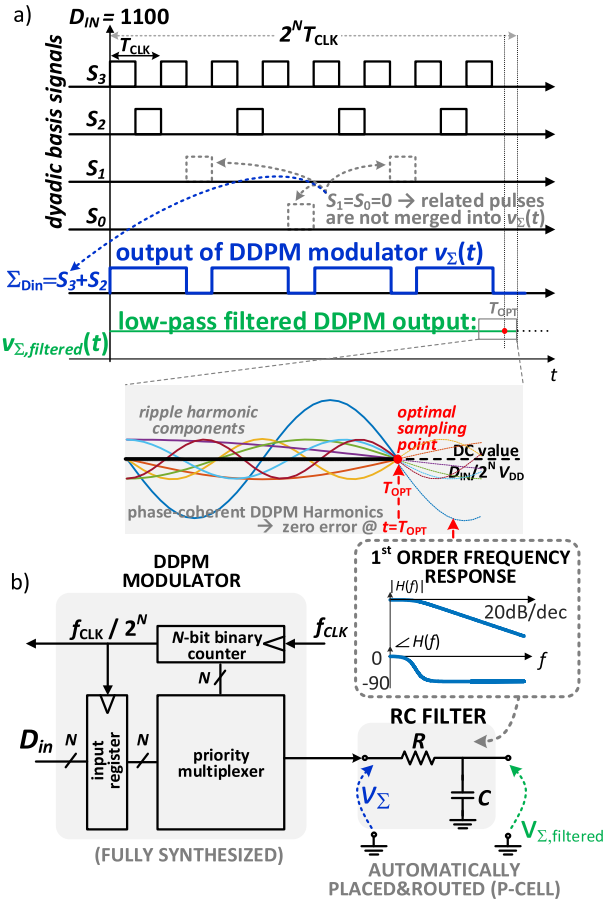

FIGURE 1. D/A conversion principle: a) example with detailed output ripple harmonic components showing coherent phase, resulting in zero error at optimal sampling time $T_{OPT} = 2^N T_{CLK}$; b) implementation of DDPM modulator.

and is associated to a digital DDPM output stream given by

$$\Sigma_{D_{in}}(t) = \sum_{i=0}^{N-1} b_i S_i(t). \tag{2}$$

The DDPM stream in (2) consists of the superposition of the dyadic basis signals $S_i(t)$ for $i = 0\ldots N-1$, as defined by [19]

$$S_i(t) = \sum_{h=-\infty}^{+\infty} \Pi\left[\frac{t}{T_{clk}} - h \cdot 2^{N-i} - 2^{N-i-1}\right]. \tag{3}$$

In (3), $\Pi(x)$ is the ideal digital pulse signal defined as

$$\Pi(x) = \begin{cases} 1, & \text{for } x \in [-1/2, 1/2] \\ 0, & \text{otherwise.} \end{cases} \tag{4}$$

As shown in Fig. 1, the generic basis signal $S_i(t)$ is a digital pattern of a pulse equal to 1 starting on the clock cycle 2^{N-i-1} and followed by $2^{N-i} - 1$ zeros, then periodically repeating with a period of 2^{N-i} cycles [19]. As an example with $N = 4$, the first pulse equal to 1 in $S_3(t)$ occurs in the first cycle. This is then followed by one zero, and the resulting pattern is then repeated every two cycles. In $S_2(t)$, the first pulse equal to 1 starts in the second cycle, it is followed by three zeros, and the pattern is then repeated every four cycles. Combining $S_i(t)$ for $i = 0\ldots N-1$ as in (2), the modulated DDPM output

is periodic with a fundamental frequency $f_0 = 1/2^N T_{clk}$, and is obtained by merging the pulses equal to 1 associated with the input digits b_i. Each input digit results in a pulse train with pulse density $2^{i-1}/2^N$ (i.e., fraction of the period $1/f_0$ in which the pulse train is at 1) equal to the corresponding weight, as shown in Fig. 1a. From an implementation viewpoint, the DDPM modulated digital signal $\Sigma_{D_{in}}(t)$ in (2) can be generated by a simple priority multiplexer [19], whose selection signals are provided by a free-running binary counter (see Fig. 1b).

The Fourier series expansion[1] of $\Sigma_{D_{in}}(t)$ in (2) is readily found to be

$$\Sigma_{D_{in}}(t) = \sum_{k=-\infty}^{+\infty} c_{k,D_{in}} e^{j2\pi k f_0 t} \tag{5}$$

where

$$c_{k,D_{in}} = V_{DD} \cdot \sum_{i=0}^{N-1} \left\{ 2^i b_i \left[\sum_{m=0}^{2^{N-i}} \mathrm{sinc}\left(\frac{k}{2^N}\right) \times \delta\left[k - 2^i m\right] e^{-j\pi m} \right] \right\},$$

being $\delta[\cdot]$ the Kroenecker function, and $\mathrm{sinc}(x)$ the normalized cardinal sine function $\sin(\pi x)/\pi x$. From (5), the DC component $c_{0,D_{in}}$ is proportional to the digital input $D_{in} = \sum_{i=0}^{N-1} 2^i b_i$, and can be extracted via a first-order RC low-pass filter as in Fig.1b. Having a voltage swing of V_{DD}, the RC filtered output $v_{\Sigma,filtered}$ corresponds to the outcome of the D/A conversion of the input D_{in}. The harmonics in (5) are spurious components to be filtered out.

From the above spectral analysis, in the following the DDPM modulation is shown to enable inherent and guaranteed suppression of most of the spurious harmonics under proper choice of the sampling period. In turn, this vastly relaxes the output filter specifications. Indeed, (5) reveals that the phase of all the harmonics in $\Sigma_{D_{in}}(t)$ is independent of D_{in}, and can be either 0 or 180° (as dictated by $e^{-j\pi m}$). The first-order RC filter in Fig. 1b introduces a further phase shift $\angle H(kf_0) \approx -\pi/2$, for the harmonics at frequency kf_0 in (5a) lying well above the filter cutoff frequency $f_c = 1/2\pi RC$ (e.g., one decade above). Such k-th harmonics above the filter cutoff frequency contribute to the filter output through an additive term that is equal to $\pm|H(kf_0)| \cdot |c_{k,D_{in}}| \cdot \sin(2\pi k f_0 t)$ from (5a). In turn, such contribution is equal to zero at $t = T_{OPT}$, being T_{OPT} defined as

$$T_{OPT} = \frac{n}{f_0} = i \cdot 2^N T_{clk}, \quad i \in \mathbb{Z}. \tag{6}$$

In other words, all harmonics lying at least one decade above the filter cutoff frequency give zero contribution to the filtered output at $t = T_{OPT}$, irrespective of the specific DC input code being converted, and of the magnitude of the filter frequency response. Thus, the DAC output sampled at $t = 2^N T_{CLK}$ (or any integer multiple i) is unaffected by harmonics above $10f_c$. Interestingly, such harmonics represent the vast majority of the overall energy of the spurious components above the DC component, as will be shown below.

[1]Compared to [19], the Fourier series expression has been obtained shifting the time origin by $T_{clk}/2$, for convenience

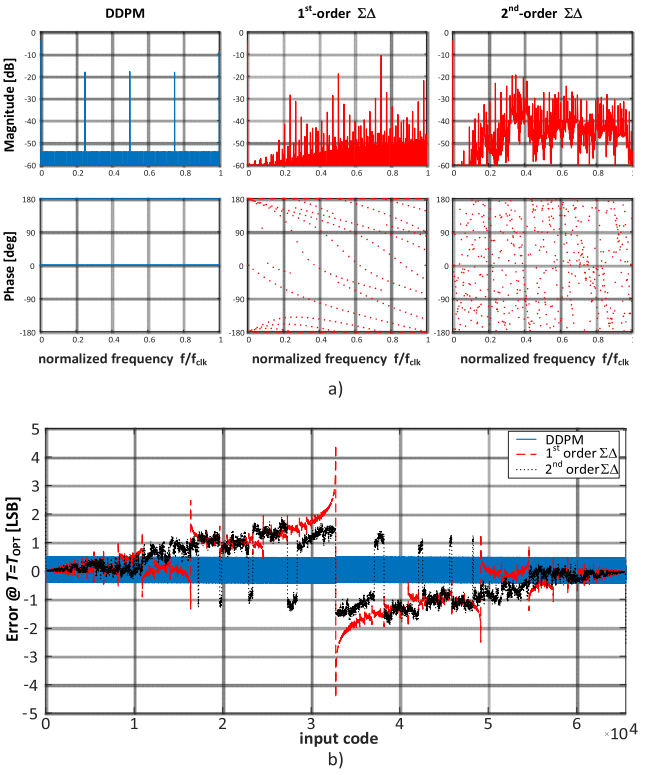

FIGURE 2. a) Amplitude (1st row) and phase (2nd row) spectra of the steady-state 2^{16} bit stream resulting from the DAC conversion of a constant input D_{IN} = 5363 by DDPM, 1st- and 2nd-order ΣΔ modulator. b) Output error when the DAC output voltage is sampled at t = T_{OPT} in (6) vs input code for DDPM and 1st- and 2nd order ΣΔ DAC.

From the above considerations, the choice of the sampling period $2^N T_{CLK}$ introduces inherent suppression of the dominant contribution of spurious harmonics in DDPM modulation, drastically relaxing the filter cut-off frequency requirement. In contrast, such spectral property of DDPM modulation does not apply to binary streams originated by ΣΔ modulators (e.g., by 1st- or 2nd-order). Indeed, the latter ones are well known to have a complex and input-dependent phase in the harmonic components, as exemplified in Fig. 2a. In this figure, the magnitude and the phase spectra of the output stream is plotted for a DDPM, a first-order and a second-order ΣΔ modulator, under the same DC input code $D_{in} = 5363$. Accordingly, in ΣΔ modulators it is not possible to derive an input-independent optimal sampling time at which the contribution of nearly all harmonics is zero, thus requiring more stringent filter specifications. Quantitatively, Fig. 2b shows that sampling the output of a first and second order ΣΔ modulator with the same filter and sampling time as the DDPM DAC leads to an error of several LSBs (e.g., up to five in the example of Fig. 2b). It is worth noting that the input-independent optimal sampling condition in (6) rigorously holds for DC signals, and is hence certainly well suited for resolution enhancement for calibration/tuning purposes.

III. STANDARD CELL-BASED DESIGN AND CALIBRATION OF DDPM DACs

The potential limitations of DDPM converters, the benefits of the optimal sampling condition in Section II, and the implications in terms of calibration were explored through the optimized design and the experimental characterization of two DACs with moderate (12 bit, named DAC_12) and high resolution (16 bit, named DAC_16). The designs are part of the 40nm testchip in Fig. 3. Both DACs were designed with a fully-automated digital design flow, with the first-order filter being implemented by simply instantiating the passive components in the form of p-cells, as commonly available from commercial design kits (i.e., they were implemented with simple scripting). The overall design was completed in less than a day, confirming that DDPM converters entail an extremely low design effort.

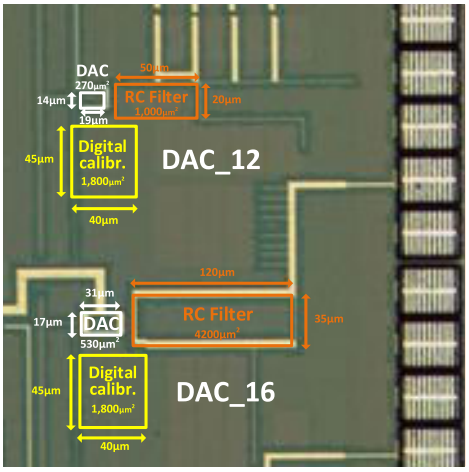

FIGURE 3. Micrograph of the two DACs in the 40nm testchip.

A. DDPM DACs AND DESIGN CONSIDERATIONS

In the DAC_12 design, the first-order reconstruction filter in Fig. 1b was designed by using a 5-pF metal-insulator-metal on-chip capacitor and a high-resistivity poly resistor with a resistance of 300kΩ. The DDPM modulator is very compact, as expected from its digital nature and intrinsic simplicity in Fig. 1b. The micrograph of the testchip in Fig. 3 shows that it occupies only $270\mu m^2$, i.e. approximately a square with only 15μm width. Being based on a fully standard cell-based approach, digital-like shrinking is also achieved when using CMOS technologies with finer minimum feature size. At the nominal 1-V power supply voltage, the DAC_12 circuit operates at a clock frequency up to $f_{\max} = 900$MHz. Since the best performance in terms of linearity and power-resolution tradeoff is achieved at $f_{\rm clk} = 450$MHz, the latter will be considered as nominal clock frequency in the following. Thanks to its digital nature, the DAC_12 circuit is able to properly operate down to 665mV (575mV) power supply voltage at $f_{\rm clk} = 450$MHz ($f_{\rm clk} = 112.5$MHz). Under $f_{\rm clk} = 450$MHz, the sample rate at the nominal 12-bit resolution is $f_{\max}/2^N = 110$kS/s.

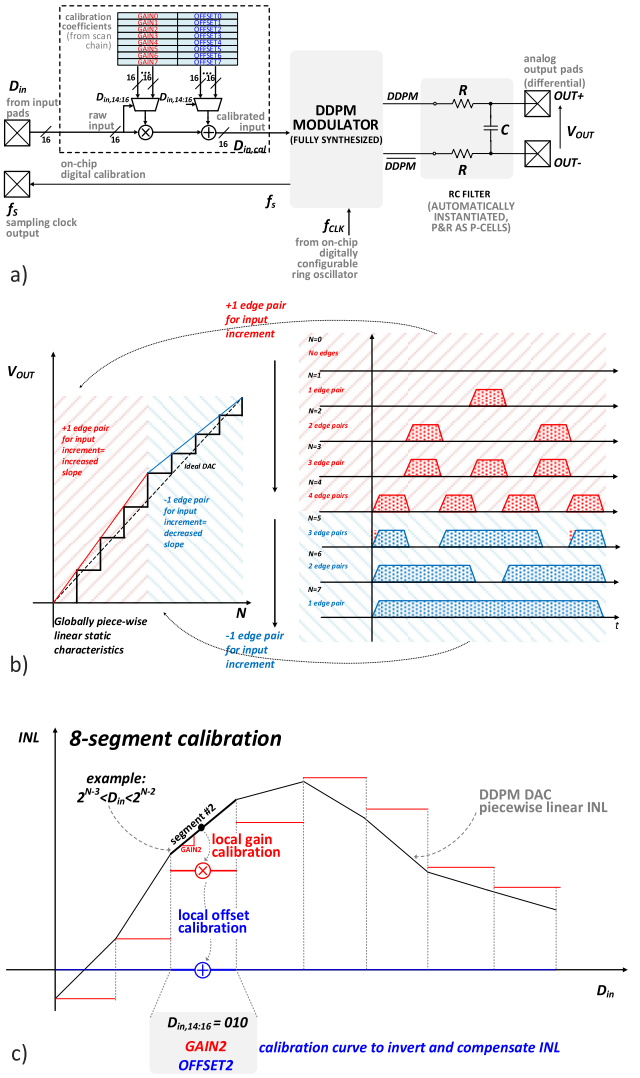

FIGURE 4. Proposed 16-bit DAC (DAC_16): a) architecture, b) nonlinearity error due to non-ideal pulse shape; c) 8-segment piecewise-linear calibration of INL error to compensate pulse shape and ISI non-idealities.

A similar architecture was also implemented to explore the potential of DDPM converters, and its resolution limit beyond moderate resolutions of 10-12 bits. Since the plain architecture used for DAC_12 is not able to achieve higher resolution, various techniques were introduced to approach the targeted range of 16 bits. As first consideration, differential operation was adopted to improve the robustness against substrate and supply noise, as well as to double the output voltage swing to further improve the signal-to-noise ratio. To this aim, the DDPM output digital stream and its complementary stream $\overline{DDPM}$ are generated. Such outputs are then fed to a differential first-order RC reconstruction filter, which comprises two matched 250-kΩ poly resistors, and a 5-metal 20-pF Metal-insulator-Metal (MiM) capacitor (both automatically instantiated, placed and routed), as in Fig. 4a. This permits to halve the capacitance and hence the related area, compared to two single-ended RC circuits. Regarding the targeted range of 16 bits. As first consideration,

differential operation was adopted to improve the robustness the 16-bit DDPM modulator, the nominal clock frequency f_{CLK} is 225 MHz at 1-V supply. The digital input D_{IN} is sampled by the modulator at the frequency $f_S = f_{CLK}/2^N =$ 3.4 kS/s, which is derived directly from the clock within the modulator.

As shown in Fig. 3, the overall silicon area of DAC_16 is only 4,730μm^2 and is dominated by the filter area (4,200μm^2), which could be further halved by using the entire 10-metal stack. To achieve higher resolution without significant area penalty, the filter cutoff frequency was set to keep the output voltage error at $t = T_{OPT}$ lower than $\pm 1/2$ LSB for all input codes. The cutoff frequency target was obtained via circuit simulations, leveraging the monotonic reduction in the output error when the filter cutoff frequency is reduced (i.e., more effective harmonics suppression). At the nominal 225MHz clock frequency, the required cutoff frequency was found to be 12kHz, which is 8X higher than the requirement in [19] to reduce the peak amplitude of all DDPM harmonics below the quantization error level. Such 8X increase in the cutoff frequency is enabled by the intrinsic suppression due to optimal sampling as in (6). In turn, such 8X cutoff frequency increase translates into an approximately 8X smaller area of the capacitor and resistor in the reconstruction filter, which are also the dominant contribution as discussed above. In other words, the optimal sampling condition in Section II enables significant area reduction, in addition to the more obvious suppression of spurious harmonics and hence better output accuracy.

B. DIGITAL CALIBRATION

As in any DAC architecture, DDPM-based converters are affected by pulse shape non-idealities, and inter-symbol interference (ISI). In particular, the INL error in DDPM DACs is mainly due to the asymmetric rise/fall transitions and inter-symbol interference, and has a piecewise-linear shape, as illustrated in Fig.3b.

Indeed, for $D_{in} \leq 2^{N-1}$ (i.e., $b_{N-1} = 0$), an increase of the input code by an LSB introduces a new pulse and hence an additional rising-falling edge pair, resulting to nearly the same incremental error at each input code increase, and hence a gain error. However, for $D_{in} > 2^{N-1}$ (i.e., $b_{N-1} = 1$), the increase of the input by an LSB actually reduces the number of rising-falling edge pairs by one, thus leading to a different gain error. This determines a double-slope non-linearity error, i.e. a piecewise-linear DAC characteristic. Moreover, based on the analysis [19], ISI and power supply noise at the harmonics of the sampling frequency also result in a piece-wise linear characteristics affected by different gain and offset errors over different input code segments.

This suggests the adoption of simple piecewise-linear calibration is sufficient for DDPM converters. In turn, piecewise-linear calibration is easy to implement in a fully digital multi-segment form, thus preserving the fully-digital standard-cell based approach that is distinctive of DDPM DACs. In multi-segment calibration, the dynamic range is divided into 2^M segments, and a different gain and offset correction are applied to the digital input in each segment, as shown in Fig. 4c. At higher (lower) resolution targets, a higher (lower) calibration accuracy is needed and the required number of segments is hence expected to increase (decrease).

For the DAC_16, transistor-level simulations showed that an 8-segment calibration scheme is sufficient to keep INL within $\pm 1/2$ LSB at 16 bit resolution, as illustrated in Fig. 4b. This calibration scheme can be simply implemented with two 8:1 MUXes, each being driven by the three most significant bits of the input $D_{\text{in},16:14}$, whose value selects the corresponding segment among the eight available as in Fig. 4a. The selected compensation basically inverts the INL curve in Fig. 4c, making the local error within the segment close to zero within the targeted accuracy. In particular, the MUXes select the desired gain $GAIN_i$ (offset OFF_i) to compensate the local gain (offset) error in the i-th segment, for $i = 0 \ldots 7$. Then, a multiplier and an adder simply generate the calibrated DDPM input $D_{\text{in,cal}}$ based on the actual input D_{in} as follows

$$D_{\text{in,cal}} = GAIN_i \cdot D_{\text{in}} + OFF_i \text{ if } 2^3 i \leq D_{\text{in}} < 2^3 (i+1) \tag{7}$$

as shown in Fig. 4a. In practical cases, (7) is often directly evaluated by the processor or DSP driving the DAC, thus not requiring any extra area.

The values $GAIN_i$ and OFF_i of the calibration coefficients can be obtained via foreground calibration, measuring the slopes of the DAC static transfer curve, similar to [19]. Interestingly, the calibration coefficients were found to be nearly unaffected by supply and temperature variations, and are weakly sensitive to process variations. Thus, in cost-sensitive applications, the additional testing time for traditional die-specific calibration can be eliminated at the cost of moderate resolution degradation, adopting a one-time offline calibration that is equal for all dice. Alternatively, full resolution is reached by applying a die-specific calibration at testing time.

The same calibration network in Fig. 4a was also adopted for the DAC_12 circuit, although its lower resolution requires only a simpler two-segment calibration, thus further simplifying the calibration process and implementation.

IV. EXPERIMENTAL RESULTS

The 40nm DAC_12 and DAC_16 testchip in Fig. 3 were characterized under nominal operating conditions, i.e. at 25°C temperature, 1-V supply, $f_{\text{CLK}} = 450$MHz for the DAC_12 and $f_{\text{CLK}} = 225$MHz for the DAC_16. The accuracy was tested over process, supply and temperature variations, as discussed below.

The DAC_12 converter was found to consume 50.8μW at nominal conditions and at 110kS/s sample rate, independently of the input code. The results of characterization under static conditions in Figs. 5a-c reveal a maximum (RMS) INL error of ± 3 LSBs (1.07 LSB), and a maximum (RMS)

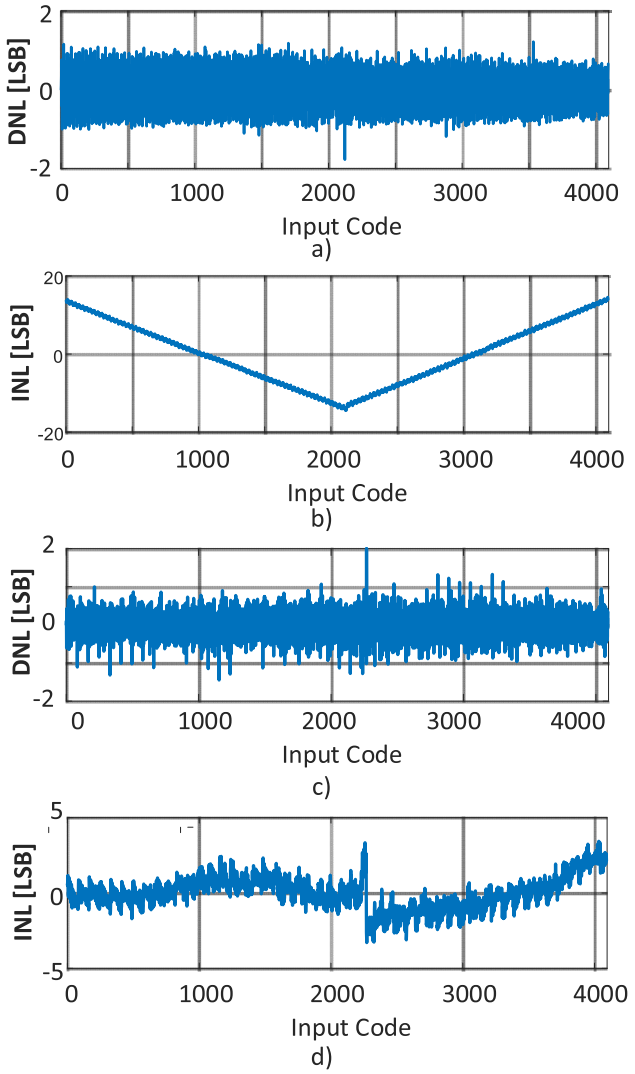

FIGURE 5. Static characterization of the proposed DAC_12 (operated at full resolution): a) DNL, b) non-calibrated INL, c) calibrated DNL (two-segment calibration), d) calibrated INL (two-segment calibration) vs. input code.

DNL of ±1LSBs (0.47 LSB), under two-segment calibration. The INL is expectedly piecewise-linear as shown in Fig. 5b. Without the proposed calibration, the maximum (RMS) INL error is expectedly larger, and equal to ±13 LSBs (2.2 LSB).

Based on the results of the dynamic characterization reported in Figs. 6a-b, DAC_12 achieves an SNDR of 72dB at low frequency, which corresponds to an ENOB of 11.6 bits. Moreover, both SFDR and THD exceed 85dB at low frequency. Compared with the DDPM DAC at the same resolution proposed in [29], DAC_12 presented in this paper achieves 2X higher sample rate at half area and 10% less power. The improvement is due to the avoidance of the overhead associated with the specific technique to achieve graceful degradation in [29], as appropriate to highlight the true potential of DDPM DACs (as opposed to aiming to relax system-level design by introducing graceful degradation against uncertain frequency and supply voltage).

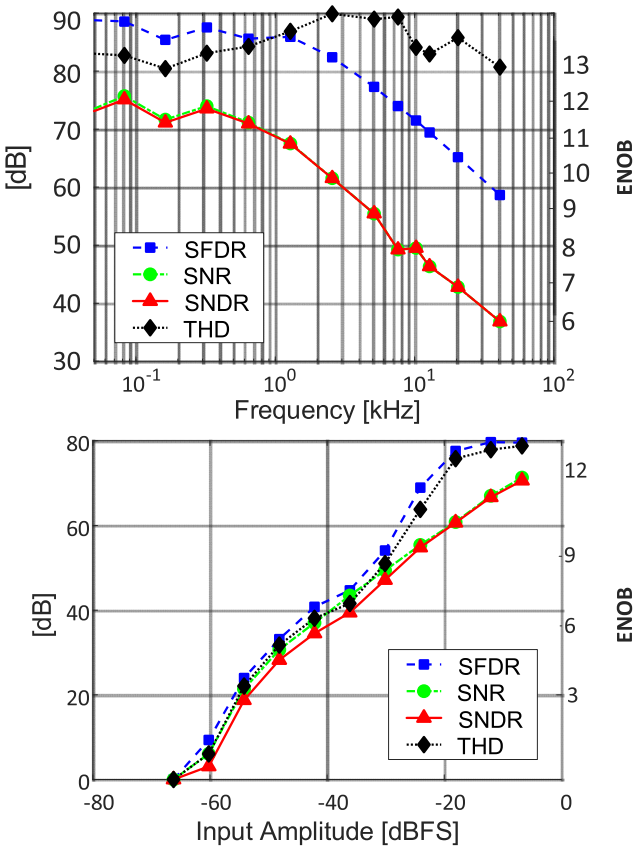

FIGURE 6. Dynamic characterization of the 12-bit DAC_12 operated at full resolution: a) SFDR, SNR, SNDR, THD vs. input frequency (1-kHz sine wave), b) SFDR, SNR, SNDR, THD vs. input amplitude (full-swing sine wave).

This results in a 7dB higher (i.e., better) power efficiency FOM [16], where the FOM is defined as:

$$FOM = 10\log_{10}\frac{2^{2ENOB} * BW}{P} \tag{8}$$

being BW the bandwidth and P the power consumption.

Compared with state-of-the-art DACs with comparable bandwidth and/or resolution ranges in Table 1, DAC_12 exhibits 52-5,180X lower area than [13]–[18]. For the sake of fairness, the comparison excludes the RC reconstruction filter, as it is not reported in prior art. Such area advantage is due to the simple architecture in Fig. 1, which avoids the need for the area-hungry interpolator, arithmetic and active analog circuitry needed by ΣΔ DACs. This area advantage further increases at finer technologies thanks to its digital architecture, which scales substantially faster than analog counterparts. Also, the avoidance of active analog circuitry makes the design effort minimal, i.e. in the order of 10 man-hours as opposed of more analog-intensive designs that typically require several hundreds of man-hours or more.

Regarding the DAC_16 design, its power consumption at nominal frequency f_{CLK} = 225MHz was measured to be 45μW. The results of its static characterization after eight-segment calibration are reported in Fig. 7, based on the eight-segment calibration in Section IVB. The RMS INL and

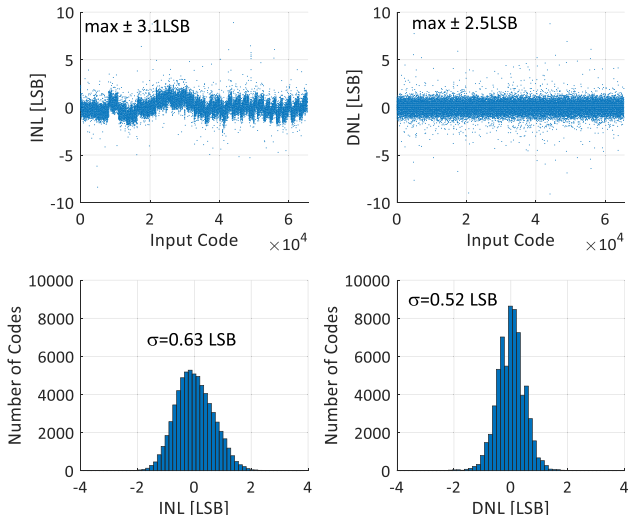

FIGURE 7. Static characterization of proposed 16-bit DAC_16 (die #1 under 8-segment calibration).

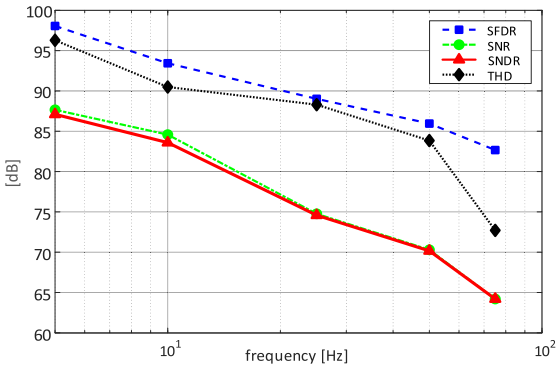

FIGURE 8. Dynamic performance of the proposed DAC_16 for a sinewave input of amplitude equal to 90% of the full-scale value, and 5-75Hz frequency.

DNL respectively are 0.63LSB and 0.52 LSB. Except for a very limited number of outliers (less than 20, i.e., 0.06% of input codes) exceeding ±2 LSB and always within ±9 LSB, the measured maximum INL is 3.15 LSBs and the maximum DNL is 2.5 LSBs.

The dynamic characterization of DAC_16 in Fig. 8 was performed on the same die under a sinewave input at 90% of full-scale amplitude with frequency in the 5-75Hz bandwidth. From this figure, the measured SFDR and THD are above 95dB, whereas SNR and SNDR are both 87.5dB at 5-Hz input, corresponding to 14.5 ENOB. A 20dB/dec ENOB degradation is shown at larger frequencies, as expected.

For completeness, the DAC_16 circuit was also tested in the presence of process, voltage and temperature (PVT) variations. Under die-specific calibration derived at 1V (i.e., at the cost of increased testing time), the measured static characteristics at supply voltages in the 0.9-1.1V range is reported in in Fig. 9a. This figure shows that such supply voltage fluctuations lead to a degradation in the RMS INL (DNL) of 0.27 LSBs (0.15 LSBs), compared to the nominal 1V supply. The DAC was also characterized over temperatures ranging

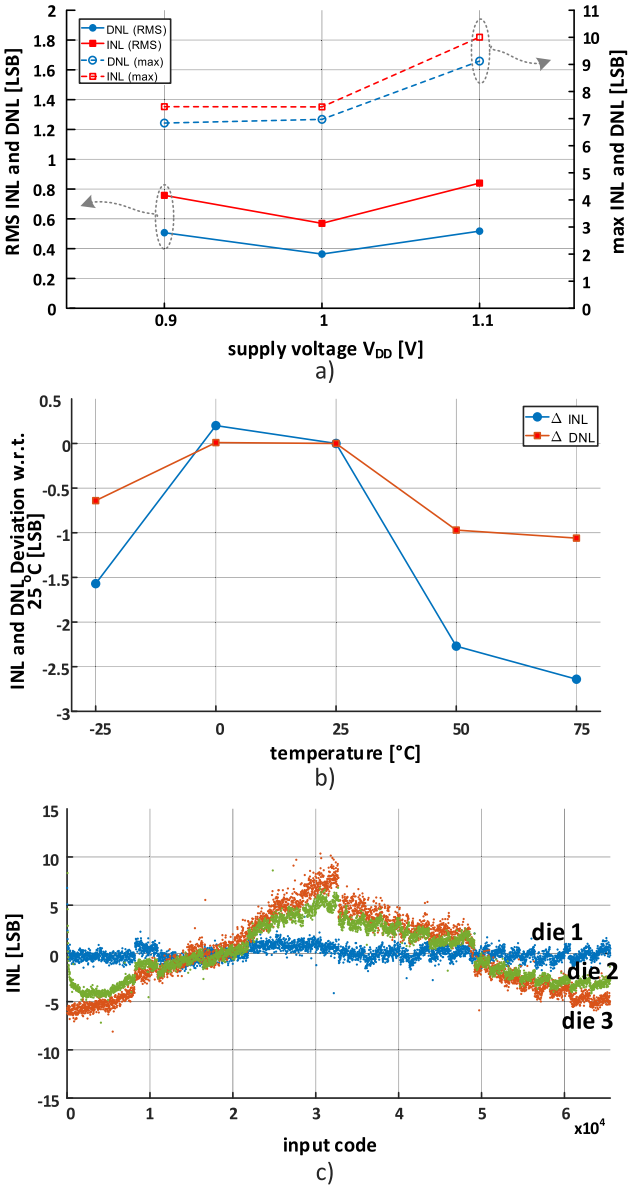

FIGURE 9. a) Calibrated max and RMS INL and DNL versus supply voltage, b) INL and DNL variation vs temperature, c) post-calibration performance across three dice, using the same calibration coefficients obtained from die #1 (offline calibration).

from −25°C to 75°C as shown in Fig. 9b. This figure shows that the deviation in the RMS value is 2.6LSB (1LSB), and the maximum INL (DNL) deviation from nominal temperature is 2.5LSB. A consistent 2.5X INL/DNL ratio is also observable over temperature, compared to room temperature, which indicates a very similar impact on INL and DNL.

To experimentally quantify the impact of die-to-die variations, the resulting static characterization was repeated over three dice. Conventional die-specific re-calibration of each die was confirmed to completely recover the nominal INL and DNL performance in all cases (results are hence omitted, as they are basically the same as Figs. 7-8). To quantify the resolution degradation due to the adoption of a simple offline calibration, Fig. 9c plots the static characterization in the

TABLE 1. Comparison with state-of-the-art DACs with comparable resolution and sample rate.

	This work		[29]	[34]	[33]	[32]	[31]	[30]	[18]	[13]
technology (nm)	40		40	110	180	45	180	600	350	350
category	fully digital (std. cell)		fully digital (std. cell)	analog	partially digital	partially digital	analog	analog	partially digital	analog
type	DDPM modulation-based		DDPM - based	Current steering	ΣΔ	ΣΔ	Current steering	R/2R	ΣΔ	Current steering
	DAC_12	DAC_16								
area (10^6 μm^2)	0.000270	0.000530	0.000500	0.117	0.10 [a]	0.16[a]	2.190	9.64	1.440 [a]	0.014[a]
area normalized to DAC_12	1	1.96	1.85	433	370	593	8,111	35,704	5,333	52
area (10^6 F^2)	0.17	0.33	0.31	9.7	3.1	79	67.6	26.8	11.7	0.11 [b]
resolution (bit)	12	16	12	12	N/A	18	16	20	16 [d]	9
sample rate (kS/s)	110	3.8	55	250,000	40 [f]	48 [f]	2,000	N/A	48 [f]	111
clock frequency (MHz)	450	255	225	250	6.25	3.072	2	N/A	3.072	N/A
DNL (LSB)	1	±1.5	±1	N/A	N/A	N/A	±0.8	±0.30	N/A	±0.8
INL w/ calib. (LSB)	±3	±8	N/A	N/A	N/A	N/A	N/A	±0.35	N/A	±1.6
INL w/o calib. (LSB)	±14	±3.1	±2	N/A	N/A	N/A	±4	N/A	N/A	N/A
supply voltage (V) (analog/digital)	1/1	0.8/0.8	1/1	3.3/2.5	1.8/ N/A	1.45/1.1	2.7	±10	0.8/0.8	3.3/3.3
min. supply voltage (V)	0.7	0.7	1	2.5	N/A	1.1	2.7	±10	0.7	3.3
SNDR (dB) peak	72	85	70	64 [d]	103 [c]	108 [c]	90	N/A	69	48 [d]
SNDR (dB) @ f_s/2	35	N/A	50	N/A	N/A	N/A	N/A	N/A	N/A	N/A
dynamic range (dB)	74	86	74	N/A	115 [c]	108 [c]	N/A	N/A	88	N/A
THD (dB)	85	95	72.2	N/A	N/A	104.6	N/A	N/A	N/A	N/A
SFDR (dB)	85	97.5	72.5	N/A	N/A	120	N/A	N/A	N/A	N/A
ENOB	11.6	14.5	11.3	10.3	16.8	17.6	16.8	N/A	11.2	8[d]
power (μW)	50.8	45	55	28,000	700[e]	875	1,620	84,000	2,600	33
power normalized to DAC_12	1	0.89	1.08	551	13.8	17.2	31. 9	1,654	51.2	0.65
FOM (dB)	160	163	153	158 [d]	174[d]	180 [d]	189	N/A	140	140 [d]
FOM_A (dB)	167	168	158	148	169	161	171	N/A	129	149

[a] As in prior art, area does not include the reconstruction filter (in the proposed DAC, it is the RC circuit in Figs. 1-3). In [18], only the digital sub-system is considered. [b] Area normalized to F^2 (F = process minimum feature size) is relatively constant across CMOS generations in digital architectures, and increases by slightly less than 2X in analog architectures. Hence, the area of [13] ported to 40nm is expected to translate into substantially larger area than this work, even though its normalized area is lower; [c] A-weighted; [d] based on text and figures; [e] analog power only, [f] twice the signal bandwidth for oversampled DACs.

three considered dice, using the same calibration coefficients obtained for die #1. In other words, the elimination of the testing time required by die-specific calibration results in an INL ranging from 0.9 to 11 LSB (average is 4 LSB), and a DNL ranging from 0.5 to 0.9 LSB (average is 0.7 LSB). The resulting linearity of the proposed DAC_16 under an offline calibration is still above 12 bits.

Compared with the DDPM DAC proposed by the same authors in [29], the introduction of the optimal sampling condition in Section II and die-specific piecewise-linear eight-segment calibration achieves 3.2 bit higher ENOB at only 6% increased area, 20% lower power consumption, and 30X reduced bandwidth. This results in an overall increase in the FOM by +10dB. At the lower 12-bit resolution of DAC_12, the impact of process, voltage and temperature variations was found to be insignificant, hence the related results are omitted (they are basically the same as Figs. 5-6). State-of-the-art DACs from the recent literature are summarized in Table 1. Compared to partially- and fully-digital DACs with comparable bandwidth and/or resolution, the proposed DAC_16 achieves 300X lower area compared to [32], 2,720X lower than [18], and 18,190X compared to [30]. The proposed DAC_16 has 19X lower power consumption compared to [32], 58X lower than [18], and 1,870X compared to [30]). Such reductions in area and power are achieved at the expense of a 12X reduction in the sample rate compared to [18] and [32], and 526X compared to [31], which is not an issue in DACs for on-chip calibration, being their output a DC signal. The favorable area-energy efficiency-performance of the proposed DACs is quantified by the area FOM

$$FOM_A = FOM + 10\log_{10}\frac{10^6}{A_F} \tag{9}$$

where A_F is the feature size-normalized area, which is lower than [31] and [33] only and it is only 3-4dB less than the highest reported in [31].

From the above comparison with the state of the art of DAC_16 and DAC_12, DDPM DACs are very well suited for cost-sensitive low-power systems with very low design effort, either for baseband signals at moderate resolutions (e.g., 12 bit), or for calibration purposes at high resolutions (e.g., 16 bit).

V. CONCLUSION

In this paper, standard cell-based Nyquist-rate DDPM DACs have been explored in terms of their limits and potential

for high resolution, while assuring very low area and design effort. To this aim, techniques to improve resolution have been introduced, including an optimal sampling condition to suppress spurious harmonics. Digital calibration has also been explored, showing that piecewise-linear techniques are sufficient to reach resolutions in the order of 16 bits.

To evaluate the effectiveness of these techniques, two DAC designs in 40nm CMOS have been demonstrated and experimentally characterized targeting moderate (12 bit) to relatively high resolution (16 bit). Both circuits were designed with a fully automated digital design flow based on standard cells, at a design effort in the order of only 10 man-hours (i.e., more than an order of magnitude lower than typical DAC designs). Their area was shown to be 370-5,333X smaller than prior partially-digital DAC architectures, and expectedly further smaller than conventional analog designs. Such area efficiency over partially-digital $\Sigma\Delta$ DACs is achieved thanks to the avoidance of interpolation, arithmetic and active analog circuitry. The power consumption of 45-50.8μW is equivalent to the lowest reported to date, and 2-3 orders of magnitude lower than other solutions. The power efficiency FOM of 160-163dB is in the middle of the range covered by prior art (i.e., between 140-189dB). Such performance is achieved while not requiring any passive element matching or static DC bias circuitry, as opposed to other state-of-the-art DACs.

Overall, this work shows that the introduction of simple techniques, such as an optimal sampling condition and lightweight digital calibration, make DDPM DACs very competitive in terms of area efficiency, power consumption and low design effort for a wide range of resolutions, as required by cost-sensitive applications and low-power constraints.

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