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Extending the Supercapacitor-Assisted Low-Dropout Regulator (SCALDO) Technique to a Split-Rail DC–DC Converter Application

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ABSTRACT The Supercapacitor-assisted low-dropout (SCALDO) regulator is a unique new DC-DC converter design approach with high end-to-end efficiency (ETEE), where a supercapacitor is used as a lossless voltage dropper in the series path of a linear regulator. This technique, in which the energy recovery happens at a very low frequency (typically in millihertz), with an efficiency multiplication factor in the range of 1.33 to 3, can be used in many different applications. For example, in a 12- 5V linear converter where the theoretical maximum efficiency is 41.67%, the SCALDO approach improves it to 83.33%. The SCALDO technique has been extended to multiple useful applications proving its versatility and has been identified as an entirely different approach compared to conventional switched capacitor converters. In this paper, we provide an in-depth discussion on the expansion of the SCALDO technique into a dual-polarity, split-rail DC power supply with high ETEE, high current, high slew-rate capability and other desirable features. It also presents the experimental results for a 12V to ± 5V prototype with steady-state performance, transient response capability, load/line regulation, and loss estimation.

INDEX TERMS DC-DC Converter, efficiency, low-dropout regulators, SCALDO regulator, split-rail converters, supercapacitors.

I. INTRODUCTION

Generating bipolar voltages from a single voltage level is an essential requirement in modern power electronics. A few established design approaches are available for designing dual-output DC-DC converters to satisfy this criterion such as switch-mode power supplies (SMPSs), switched capacitor converters and split-rail converters. Generally, SMPSs are the ideal candidates for dual-polarity circuits with high efficiency and high output current capability [1]–[3]. Nevertheless, their applications are limited due to the circuit-complexity, cost, output ripple, and electromagnetic interference (EMI) as reported in [4]. With the possibility of soft switching, SMPSs can reduce the dynamic losses and the EMI, though the unwanted ringing in the output voltage is one of the disadvantages of some designs [5].

Noise sensitive applications, such as medical equipment, portable devices, and industrial equipment, often use inductor-less topologies such as split-rail converters to produce bipolar voltages [6]. The concept of rail-splitting is based on the virtual ground where the input supply is divided into two halves with respect to this new voltage reference [7], [8]. For example, splitting of a 12V supply into ± 5V rails from a single battery cell with a virtual ground as the 0V reference (for the output rails) can be considered as a typical application. In such applications, the negative terminal of the battery is not a key requirement to be common for the operation of the downstream devices as they see the dual outputs with respect to the virtual ground. Many localized applications that vary from low current to high current such

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as op-amps, data-acquisition systems, liquid crystal displays (LCDs), audio-amplifiers, microprocessors, and small-motor drivers use virtual ground-based rail-splitters with fixed dual outputs [8], [9].

One of the simplest methods of generating split rails under a single voltage input is the use of capacitor voltage dividers [4], [10], [11]. Nevertheless, the drawbacks of the capacitor voltage dividers are the low-frequency noise, the drift in the voltage rails due to load imbalances and the tolerance of the capacitance [4], [11]. Switched capacitor converters (also known as charge pumps) are another conventional approach for rail-splitting [12], [13]. Nonetheless, the switched capacitor converters suffer from switching noise and voltage drifts. Also, they require additional hardware to reduce the output voltage ripple and to produce voltage regulation [14]. These charge pump converters are typically used in low current applications such as data-acquisition systems and low-power analog circuits.

Buffer circuits are also applied in split-rail applications such as audio-amplifiers and localized microprocessors due to their simplicity, better transient performance and low output noise [15]. Nevertheless, the high output impedance of the buffer circuits leads to low efficiency and they bring stability issues when the output loads are heavily capacitive [16].

Apart from the commercialized split-rail methods, non-conventional approaches can also be found in [4], [7], [8]. Some of these proposed structures have limited practical scope as a result of bulky components, low efficiency, complexity, low output current, and output noise problems. When these limitations are considered, it can be observed that most of the conventional and non-conventional split-rail approaches suffer from the poor transient response, low efficiency and low output current. The suppression of the output noise and the voltage regulation are also poor in some designs. Therefore, designing a split-rail converter with high output current capability, high efficiency, better dynamic response and superior voltage regulation will be beneficial in high current virtual ground applications such as audio-amplifiers, localized microprocessors, liquid crystal displays (LCDs), and small-motor drivers where conventional approaches have limited scope.

Given the above summary, extending the relatively newer design approach in SCALDO [17] to a split rail power supply was justifiable as a major research exercise. This paper provides an overview of the SCALDO technique in Section II, while Sections III to VII provide the essential details of how the SCALDO technique can be extended to a dual output variation. This method is known as the Dual-Output-SCALDO (DO-SCALDO) technique, in which the connected loads enjoy the useful benefits of a linear regulator such as low-noise and high-current slew rate, but with the major advantage of a high ETEE.

This technique can be applied to satisfy the requirements of many virtual ground applications such as amplifiers, localized microprocessors, liquid crystal displays (LCDs), and small-motor drivers.

II. THE BASIC CONCEPT OF THE SCALDO TECHNIQUE

A. SCALDO AS A NEW DC-DC CONVERTER DESIGN APPROACH

Well established DC-DC converter techniques are (i) linear regulators (ii) inductor-based switching converters and (iii) switched capacitor converters. They have their advantages and limitations, which are well summarized in many publications [18]–[21]. Linear regulators, despite their low ETEE, provide excellent output current slew rate, low complexity, low cost and very low noise. Given these useful characteristics, low-dropout regulators which are a special case of linear regulators are very commonly used in a myriad of portable products including newer cell phones; thus the production of LDOs has become a significant business for manufacturers of power management components [22], [23].

Moreover, the SCALDO regulator is a US patented technique [24] for designing high-efficiency, low noise and RFI/EMI free DC-DC converters based on the principle of using a very large capacitor such as a supercapacitor (SC) in the series path of a linear regulator. In this technique, a SC or an array of SCs is used as a near-lossless voltage dropper, and the charge balance of the capacitor is maintained based on an energy recovery technique with very low operating frequency. A wider New Zealand research team has worked on this subject over the years with significant outcomes as detailed in [24]–[30]. Its applications developed in New Zealand are now being continued in other countries such as South Korea [31], [32].

B. USE OF SUPERCAPACITORS FOR ENERGY RECOVERY

From a DC-DC converter designer's viewpoint, a SC can be described as approximately one million times larger capacitance compared to an electrolytic capacitor [30]. During the last 15 years, these devices have entered the passive component market with capacitance values from 0.1F to over 40,000F in single cells with DC voltage ratings from 2V to 5V [33]. Higher voltage capable SC modules are also available from 50F to 300F with voltage ratings over 200V in general, where low-voltage single cell devices are connected in series [33]. These devices and modules were originally developed as an alternative to rechargeable batteries or complementing battery packs for high power delivery [34]. Today, they are used in the automotive industry, power quality products including battery-less UPS systems, memory backup circuits, portable products and a myriad of other applications [35]–[38].

Table 1 compares the prices of single cell SCs from a Korean manufacturer, VINATech [39], with similar-volume can size of electrolytic capacitors from Farnell [40]. Given the cost and real estate implications in DC-DC converter designs, the SCs used in the SCALDO technique are economical and small devices of typically 0.2F to 300F capacitances. Therefore, the use of these small can size supercapacitors does not add extra cost to a DC-DC converter in general. In developing the SCALDO technique and its

TABLE 1. Comparison of prices of supercapacitors and electrolytic capacitors based on can sizes and quantities [source: vinatech, korea].

Can size (mm^2)	The unit price for 1k samples		The unit price for 100k samples	
	3V ELDC	Electrolytic	3V ELDC	Electrolytic
8×13	0.40 USD (1F)	0.18 USD (100uF/25V)	0.35 USD (1F)	0.15 USD (100uF/25V)
10×20	0.53 USD (5F)	0.24 USD (470 uF/35V)	0.48 USD (5F)	0.21 USD (470uF/35V)
10×30	0.60 USD (10F)	0.40 USD (1000uF/25V)	0.56 USD (10F)	0.38 USD (1000uF/25V)
16×25	1.60 USD (25F)	0.88 USD (4700uF/10V)	1.50 USD (25F)	0.83 USD (4700uF/10V)
18×40	1.80 USD (50F)	1.81 USD (4700uF/50V)	1.65 USD (50 F)	1.70 USD (4700uF/10V)

Note: Can size = diameter × height.
ELDC=Electric Double-Layer Capacitor.

extended topologies, the research team has considered the requirements of a low-cost DC-DC converter by employing smaller can size supercapacitor types with very low-speed switching devices together with low-dropout regulator ICs.

C. THE BASIC SCALDO CONFIGURATION

Fig. 1 depicts the simplified concept of the SCALDO regulator, where Fig. 1(a) and Fig. 1(b) are related to the two operating modes: charging and discharging phases. Four low-speed switches are used to transfer between these two modes, and more implementation details can be found in [26].

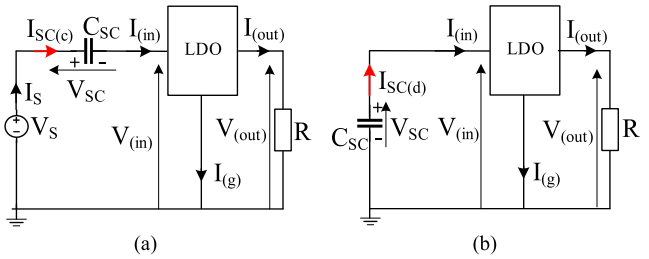

FIGURE 1. The fundamental circuit configuration of the SCALDO technique: (a) SC charging phase (b) SC discharging phase.

In Fig. 1 (a), the SC, the voltage source, and the LDO regulator are connected in series during the charging phase. For explanatory purposes, we assume that the SC is ideal, and it has zero equivalent series resistance (ESR). During the charging phase, the incremental voltage difference (Δv) across the SC is very small due to its extra-large capacitance (C_{SC}) when a finite current i(t) flows for a limited time (t) as depicted in (1).

$$\Delta v = \frac{1}{C_{sc}} \int_0^t i(t)dt \tag{1}$$

Therefore, the DC current of the circuit is not blocked within the duration of the charging phase, and the regulation of the LDO regulator is maintained for a finite amount of time.

In a well-designed LDO regulator, the ground pin current is nearly zero ($I_{(g)} \approx 0$); thus, the load current $I_{(out)}$ and the source current I_S are approximately the same. As the SC charges, the input voltage of the LDO regulator ($V_{(in)}$) starts to fall. The SC is kept in this position until $V_{(in)}$ reduces to the minimum working voltage (V_{min}) of the LDO regulator. If the resistance of the switches and the ESR of the SC are negligible, the voltage across the SC (V_{SC}) at the end of the charging cycle is approximately (V_S-V_{min}).

In the discharging phase, as illustrated in Fig. 1 (b), the starting voltage of the SC (V_S-V_{min}) must be higher than the V_{min} value, and this creates an operating condition requirement of $V_S > 2V_{min}$ for the basic SCALDO regulator [26], [27], [29] where the power supply voltage should be more than twice the minimum input voltage of the LDO regulator. The SC discharges until $V_{(in)}$ falls to V_{min} in this phase

In the SCALDO technique, the charge balance of the SC or the SC array is maintained, and the switching speed is very slow (typically in the range of millihertz to hertz only). In this simplest configuration, as the input source is disconnected during half the cycle time, the average input source current $I_{S(avg)}$ for a complete switching period becomes half the load current ($I_{(out)}/2$), and the ETEE (η_{SCALDO}) is multiplied by a factor of two as shown in (2) compared to the efficiency factor ($V_{(out)}/V_S$) of a linear regulator [41].

$$\eta_{SCALDO} \approx \frac{V_{(out)}I_{(out)}}{V_S I_{S(avg)}} = \frac{V_{(out)}I_{(out)}}{V_S\left(I_{(out)}/2\right)} = 2\frac{V_{(out)}}{V_S} \tag{2}$$

This simplified case is applied to the common example of a 12 to 5V SCALDO regulator, where one SC and four low-speed switches are used with the achievement of a theoretical ETEE of 83.33% from the case of 41.67%. In general, based on the input-output voltage difference, other SCALDO topologies have also been implemented with an array of SCs, but a discussion on those topologies is beyond the scope of this paper.

TABLE 2. Topological differences of switched capacitor converters and the SCALDO regulator.

Switched Capacitor Converters	The SCALDO Regulator
Capacitor-pair based voltage conversion is used.	A large capacitor acts as a lossless dropper element in the series path of a LDO regulator
The switching frequency is fixed (typically in the kilohertz range).	Variable frequency (typically in the millihertz range).
Load and line regulation are not precise, and additional regulators are required.	Precise load/line regulation due to the high-quality output regulation of a linear regulator.
Low output current (typically few hundreds of milliamperes).	Any load current in the range of mA to 10s of amps is possible.

As published in [42], the SCALDO concept is not a variation of the charge pump converters and Table 2 provides a summary of major differences. Generalized theory

and practical scope of the SCALDO technique are available in [25]–[27], [29].

D. PRACTICAL APPLICATIONS AND FURTHER ADVANCEMENT

Further development of the fundamentals of the SCALDO technique and its wider applications are available in [28], [30]. This technique is based on the loss-circumvention principle within a resistor-capacitor loop fed by a DC voltage source [43], and it has paved the path for a wider range of other new supercapacitor assisted (SCA) topologies such as SCASA, SCATMA, SCAHDI and SCALED [44]–[48].

Developments of the SCALDO technique and its wider applications are summarized here:

1) It is a very low-frequency DC-DC converter with similar efficiency to high-frequency switch-mode techniques.
2) Load always enjoys the low-noise, high slew-rate current capable output of a linear regulator stage.
3) The DC-UPS capability can be easily added to the converter by oversizing the SC [49].
4) There is no limit to the load current capability.
5) In the SCALDO technique, the required linear regulator can be either a single chip LDO regulator (for output currents up to about 3A) or a discrete transistor based high current linear regulator (with a small voltage drop across the series power semiconductor).

Applications of the SCALDO method and its derivative techniques are as follows:

1) High current DC power supplies with low noise output requirements [24].
2) DC power management systems for portable systems [28].
3) DC Microgrid applications [48], [50].
4) 48V DC power architecture requirements of the server power supply specified by Google [51].

It is important to highlight here that a very high current low-dropout regulator can be built easily by keeping a small voltage difference across the series power semiconductor (due to the availability of high current MOSFETs) of the linear regulator. For example, if a 5V regulator with 100A load current is required with a 5.2V average input voltage, the ETEE will be approximately 5V/5.2V (≈96%) which is very much better than similar capability inductor-based switchers. Since the charge-discharge capability of supercapacitors is large with the range of one to three hundred of amperes, placement of them in the series path of an LDO as near-lossless voltage droppers creates the practicality of building very high current SCALDO regulators.

Section III is focused on how the basic SCALDO technique can be extended into split-rail capability, without increasing the number of supercapacitors or low-speed switches used in the SCALDO concept. In several conference publications [17], [52]–[54], the authors have discussed the design aspects and proof-of-concept prototypes of the DO-SCALDO technique. Therefore, this paper exclusively explores the dynamic behavior, loss estimation, load/line regulation, and efficiency advantage along with a comparison with other split-rail topologies based on the experimental validation of a 12V to ± 5V proof-of-concept prototype. Also, the scope of this paper is limited to a split-rail converter with fixed output voltages which is the most common split-rail power supply in consumer electronics etc.

III. SPLIT-RAIL DO-SCALDO REGULATOR

Fundamentally, this DO-SCALDO technique is applicable in high current and virtual ground-based split-rail DC-DC converters where high efficiency, low noise, better dynamic response and superior voltage regulation are also some major concerns.

A. DESIGN CRITERIA

In the following section, we use a similar notation for the voltages, currents, and loads of the LDO regulator to Fig.1.

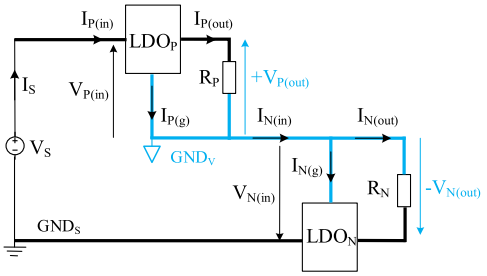

FIGURE 2. Two cascaded LDO regulators with dual-polarity outputs.

In developing the DO-SCALDO based split-rail DC-DC converter, a positive-rail LDO regulator (LDO_P) and a negative-rail LDO regulator (LDO_N) are connected in series as illustrated in Fig. 2, initially without any supercapacitor based subcircuit. The outputs of these two LDO regulators create dual-polarity output voltages with respect to the virtual ground (GND_V).

The relationship between the input voltages of the two LDO regulators and the current in each node of the circuit can be written as (3) and (4), respectively. The input current of each LDO regulator is the sum of its output current and the ground pin current according to the basic operation principles [41].

$$V_S = V_{P(in)} + \left|V_{N(in)}\right| \tag{3}$$

$$I_S = I_{P(in)} = I_{P(out)} + I_{P(g)} = I_{N(in)} = I_{N(out)} + I_{N(g)} \tag{4}$$

Since the above simple series circuit of two LDOs is based on a linear regulator pair with a common return, the voltage of the source should be greater than or equal to the sum of the minimum working voltages of the LDOs as defined in (5).

$$V_S \geq V_{P(\min)} + \left|V_{N(\min)}\right| \tag{5}$$

The simple circuit in Fig. 2 could work with outputs regulated, only if the load currents are approximately equal since the ground pin currents are small. In this situation, when

there is a mismatch in the load currents, the regulation is not possible. This problem can be solved by using a voltage-balancing circuit [4], [10], but with a loss of efficiency. The DO-SCALDO technique solves this fundamental problem with the added advantage of the higher ETEE, as shown in Fig. 3.

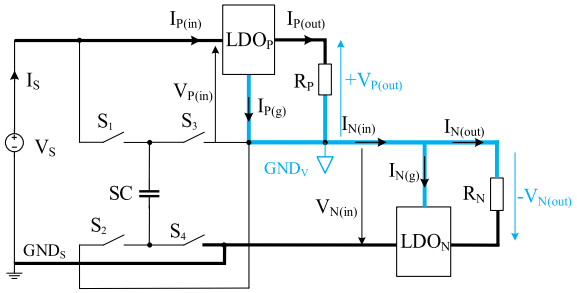

FIGURE 3. The proposed split-rail regulator built with the SCALDO technique.

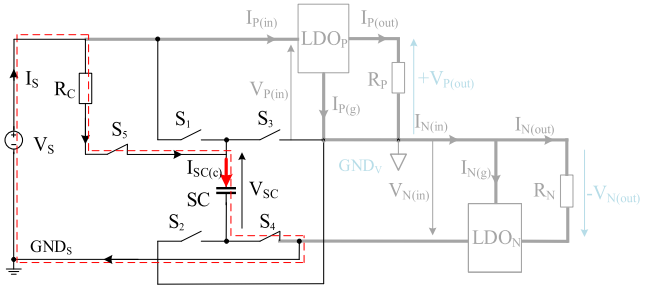

FIGURE 4. Initial charging mode.

In the proposed technique, the SC (considered ideal with zero ESR) is used as a lossless element to control the difference of the load currents. The charge balance of the SC is maintained throughout the switching cycles similar to the basic SCALDO technique. Two linear (LDO) regulators provide the voltage regulation with respect to the GND$_V$ despite their input voltages changing due to the charge balance. Therefore, the overall technique works with a high ETEE by the combined effect of the two linear regulators and the SC-assisted circuit in differential load current balancing. Four low-speed switches operate similar to the case in the basic SCALDO regulator.

The following theoretical conditions as per (6) to (8) should be maintained to achieve voltage-regulation.

$$V_{P(out)} = \left|V_{N(out)}\right| \tag{6}$$

$$V_{P(\min)} = \left|V_{N(\min)}\right| = V_{\min} \tag{7}$$

$$V_S \geq 2V_{\min} \tag{8}$$

The maximum voltage across the SC should be as per (9).

$$V_{SC(\max)} \geq V_S - V_{\min} \tag{9}$$

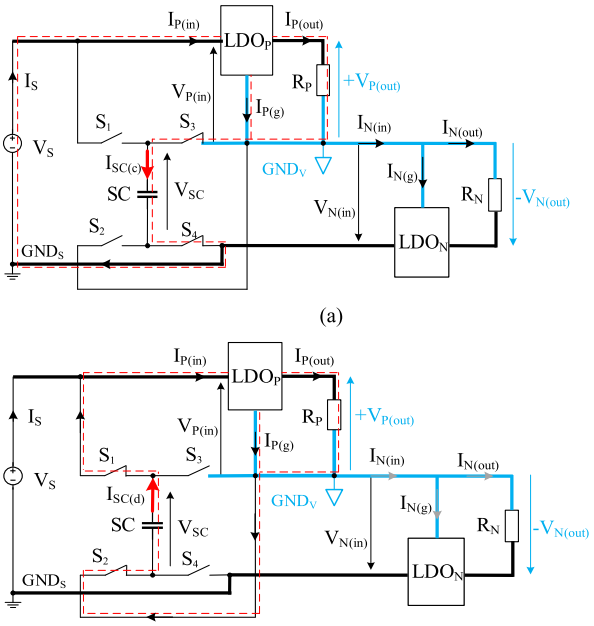

FIGURE 5. DO-SCALDO circuit operation when $I_{P(out)} > I_{N(out)}$: (a) Charging phase (b) Discharging phase.

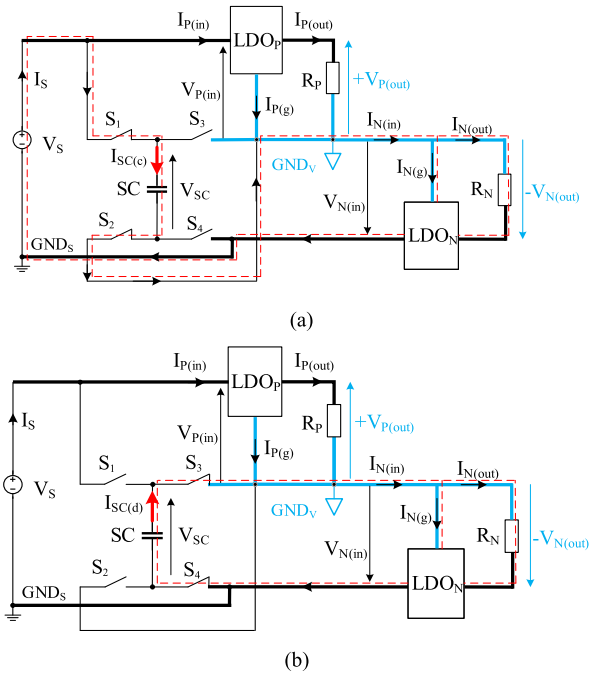

FIGURE 6. DO-SCALDO circuit operation when $I_{P(out)} < I_{N(out)}$: (a) Charging phase (b) Discharging phase.

B. OPERATING MODES

The circuit works based on four operating modes: (1) initial charging process, (2) load current of LDO$_P$ is higher than LDO$_N$ ($I_{P(out)} > I_{N(out)}$), (3) load current of LDO$_P$ is lower than LDO$_N$ ($I_{P(out)} < I_{N(out)}$), (4) equal load currents ($I_{P(out)} = I_{N(out)}$).

TABLE 3. Operational values for different phases of the split-rail DO-SCALDO circuit.

	Mode of Operation	Input source current	SC current	SC voltage at the end of the phase	Time duration of the phase
1	Initial charging process	$\approx \frac{V_S}{R_C} e^{-\left(1/R_C C_{SC}\right)}$	$\approx \frac{V_S}{R_C} e^{-\left(1/R_C C_{SC}\right)}$	$\approx V_{\min}$	$\approx R_C C_{sc} \ln(\frac{V_S}{V_S - V_{\min}})$
2	Charging phase ($I_{P(out)} > I_{N(out)}$)	$I_{P(out)}$	$I_{P(out)} - I_{N(out)}$	$V_S - V_{\min} - (2r_s + r_{sc})(I_{P(out)} - I_{N(out)})$	$\frac{C_{SC}[V_S - 2V_{\min} - 2(2r_s + r_{sc})(I_{P(out)} - I_{N(out)})]}{I_{P(out)} - I_{N(out)}}$
	Discharging phase ($I_{P(out)} > I_{N(out)}$)	$I_{N(out)}$	$I_{P(out)} - I_{N(out)}$	$V_{\min} + (2r_S + r_{SC})(I_{P(out)} - I_{N(out)})$	$\frac{C_{SC}[V_S - 2V_{\min} - 2(2r_s + r_{sc})(I_{P(out)} - I_{N(out)})]}{I_{P(out)} - I_{N(out)}}$
3	Charging phase ($I_{P(out)} < I_{N(out)}$)	$I_{N(out)}$	$I_{N(out)} - I_{P(out)}$	$V_S - V_{\min} - (2r_s + r_{sc})(I_{N(out)} - I_{P(out)})$	$\frac{C_{SC}[V_S - 2V_{\min} - 2(2r_s + r_{sc})(I_{N(out)} - I_{P(out)})]}{I_{N(out)} - I_{P(out)}}$
	Discharging phase ($I_{P(out)} < I_{N(out)}$)	$I_{P(out)}$	$I_{N(out)} - I_{P(out)}$	$V_{\min} + (2r_s + r_{sc})(I_{N(out)} - I_{P(out)})$	$\frac{C_{SC}[V_S - 2V_{\min} - 2(2r_s + r_{sc})(I_{N(out)} - I_{P(out)})]}{I_{N(out)} - I_{P(out)}}$
4	Equal loads ($I_{P(out)} = I_{N(out)}$)	$= I_{P(out)} = I_{N(out)}$	0	Does not change	Infinite (controller does not have to operate any switches)

*r_s = resistance of a single switch, r_{sc} = ESR of the supercapacitor, t = time.

1) INITIAL CHARGING PROCESS

The basic DO-SCALDO circuit shown in Fig. 3 could work only when the SC is precharged to a value close to half the power supply voltage. This process is done when the circuit is powered for the first time.

In a real-world application, in addition to the four switches shown in Fig. 3, an extra switch (S_5) is added to precharge the SC, as shown in Fig. 4. This switch and S_4 are turned on, and the charging circuit gets completed via resistor R_C, in such a way that the uncharged SC does not temporarily short circuit the input source. Once the SC charges slightly above V_{min}, the SC and LDO_N are connected in parallel, and the regular circuit operation is initiated by the controller.

2) LOAD CURRENT OF LDO_P IS HIGHER THAN LDO_N ($I_{P(out)} > I_{N(out)}$)

When the $I_{P(out)} > I_{N(out)}$ condition is met, the SC and LDO_N are connected in parallel to pass the difference of the load currents ($I_{P(out)}$- $I_{N(out)}$) into the supercapacitor. This process is achieved by closing the switches S_3 and S_4 as depicted in Fig. 5 (a). The switches S_1 and S_2 are kept open during this time, and the charging current becomes $I_{P(out)}$- $I_{N(out)}$. The flow of the charging current is shown in dashed lines in Fig. 5(a). During this phase, the input voltage of LDO_N($V_{N(in)}$) increases from the V_{min} value, the input voltage of LDO_P ($V_{P(in)}$) descends from the V_S-V_{min} value, and the input source current becomes approximately $I_{P(out)}$. The SC is kept in this position until $V_{P(in)}$ drops to V_{min}.

After the charging cycle, the SC is disconnected from the current position, and placed in parallel with LDO_P as illustrated in Fig. 5 (b). The input voltage of LDO_P and the SC voltage are approximately the same during this phase. The segmented lines in Fig. 5 (b) illustrate the flow of the discharging current of the SC. The input voltage of LDO_P continues to drop from the V_S-V_{min} value, and the input source current turns approximately $I_{N(out)}$ during this period. The discharging process is terminated when $V_{P(in)}$ becomes V_{min}.

3) LOAD CURRENT OF LDO_P IS lower THAN LDO_N ($I_{P(out)} < I_{N(out)}$)

When $I_{P(out)} < I_{N(out)}$, the circuit works in the exact opposite way compared to Mode (2). The SC charges in parallel to LDO_P and discharges in parallel to LDO_N as depicted in Fig. 6 (a) and Fig. 6 (b), respectively.

4) EQUAL LOAD CURRENTS ($I_{P(OUT)} = I_{N(out)}$)

If the load currents become equal, the current through the SC falls to zero. Since the voltage across the SC is kept always over V_{min}, the SC can be placed in parallel to any of the two inputs of the two LDO regulators. The current delivered by the input source and the load currents become almost the same. If the two load currents are zero, the circuit operation is governed by the difference of the ground pin currents of the two LDOs. In this case, the SC takes a long period to switch between the inputs of the LDOs.

C. CIRCUIT PARAMETERS

The analysis presented above considered the ideal models ignoring the ESR of the supercapacitor and the resistance of the switches. Table 3 summarizes the key parameters with respect to the four operating modes discussed above. The first-order model of the SC [55] which has an ideal capacitor in series with the ESR (in the range of 1 mΩ for devices higher than 1000F and approximately 50 to 10mΩ for smaller devices below 50F) is used to derive the operational values in Table 3. The ESR and the resistance of the switches come in series as the SC charges or discharges in Modes 2 and 3. Also, these two factors contribute to power losses of the converter (more details are given in Section V). The ground pin currents of the two LDO regulators are neglected for the simplicity of the analysis, and the constant load currents are considered except for Mode 1. In Mode 1, where the initial SC charging process occurs, the resistance of the switches and the ESR of the SC are neglected, since they are very small compared to R_C.

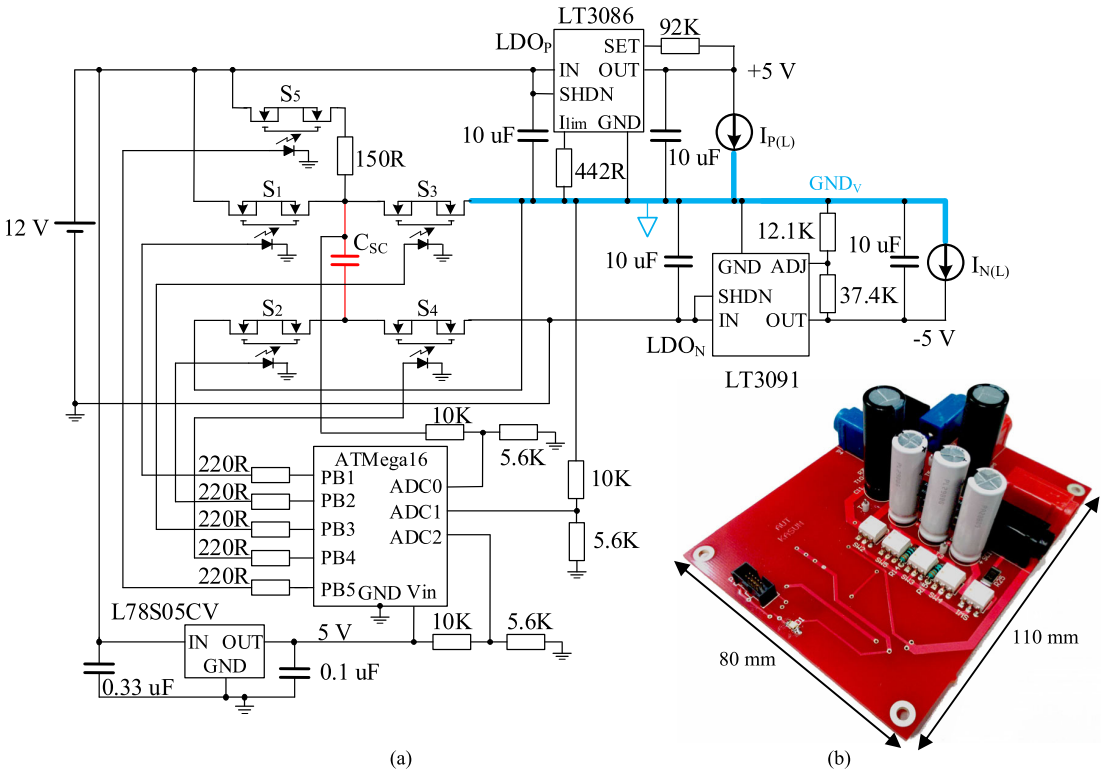

FIGURE 7. 12V to dual ±5V split-rail DO-SCALDO proof-of-concept prototype: (a) The schematic (b) The PCB.

TABLE 4. Summary of steady-state results.

Parameter		Mode 2		Mode 3		Mode 4	
		Charge	Discharge	Charge	Discharge	Charge	Discharge
$V_{P(in)}$		6.6V to 5.4V	6.6V to 5.4V	5.4V to 6.6V	5.4V to 6.6V	6V	6V
$V_{P(out)}$		5V	5V	5V	5V	5V	5V
$V_{N(in)}$		-5.4V to -6.6V	-5.4V to -6.6V	-6.6V to -5.4V	-6.6V to -5.4V	-6V	-6V
$V_{N(out)}$		-5V	-5V	-5V	-5V	-5V	-5V
I_{SC}		1A	1A	1A	1A	0A	0A
I_S		1130mA	130mA	1130mA	130mA	1030mA	1030mA
Cycle time	Measured	2.8s	2.8s	2.8s	2.8s	<< 1hr	<< 1hr
	Calculated	2.7s	2.7s	2.7s	2.7s	infinity	infinity

D. END-TO-END EFFICIENCY

Once the initial charging process is completed, the circuit operation can be in any of the Modes, 2, 3 or 4. The ETEE of the proposed regulator for Modes 2 and 3 (η) can be calculated considering the constant output currents and the zero net-charge accumulation in the SC.

$$\eta = \frac{(V_{P(out)}I_{P(out)} + |V_{N(out)}I_{N(out)}|)(t_c + t_d)}{V_S(I_{S(c)}t_c + I_{S(d)}t_d)} \quad (10)$$

where t_c, t_d, $I_{S(c)}$ and $I_{S(d)}$ are the time taken for the charging phase, the time taken for the discharging phase, the input source current in the charging phase and the input source current in the discharging phase, respectively. The two currents $I_{S(c)}$ and $I_{S(d)}$ depend on the operating state (as listed in Table 3), the control circuit current and the ground pin currents of the two LDOs.

At the steady state, t_c and t_d become equal. If the ground pin currents of the two LDO regulators and the control circuit current are neglected, the theoretical maximum ETEE of the proposed regulator can be obtained as:

$$\eta_{max} = (V_{P(out)} + |V_{N(out)}|)/V_S \quad (11)$$

In Mode 4, the SC neither charges nor discharges. Therefore, the approximate ETEE of the DO-SCALDO regulator equals the case in (11) in this mode.

IV. EXPERIMENTAL RESULTS

A. IMPLEMENTATION OF THE PROTOTYPE

A 12V to ±5V proof-of-concept prototype was built to validate the performance of the DO-SCALDO technique

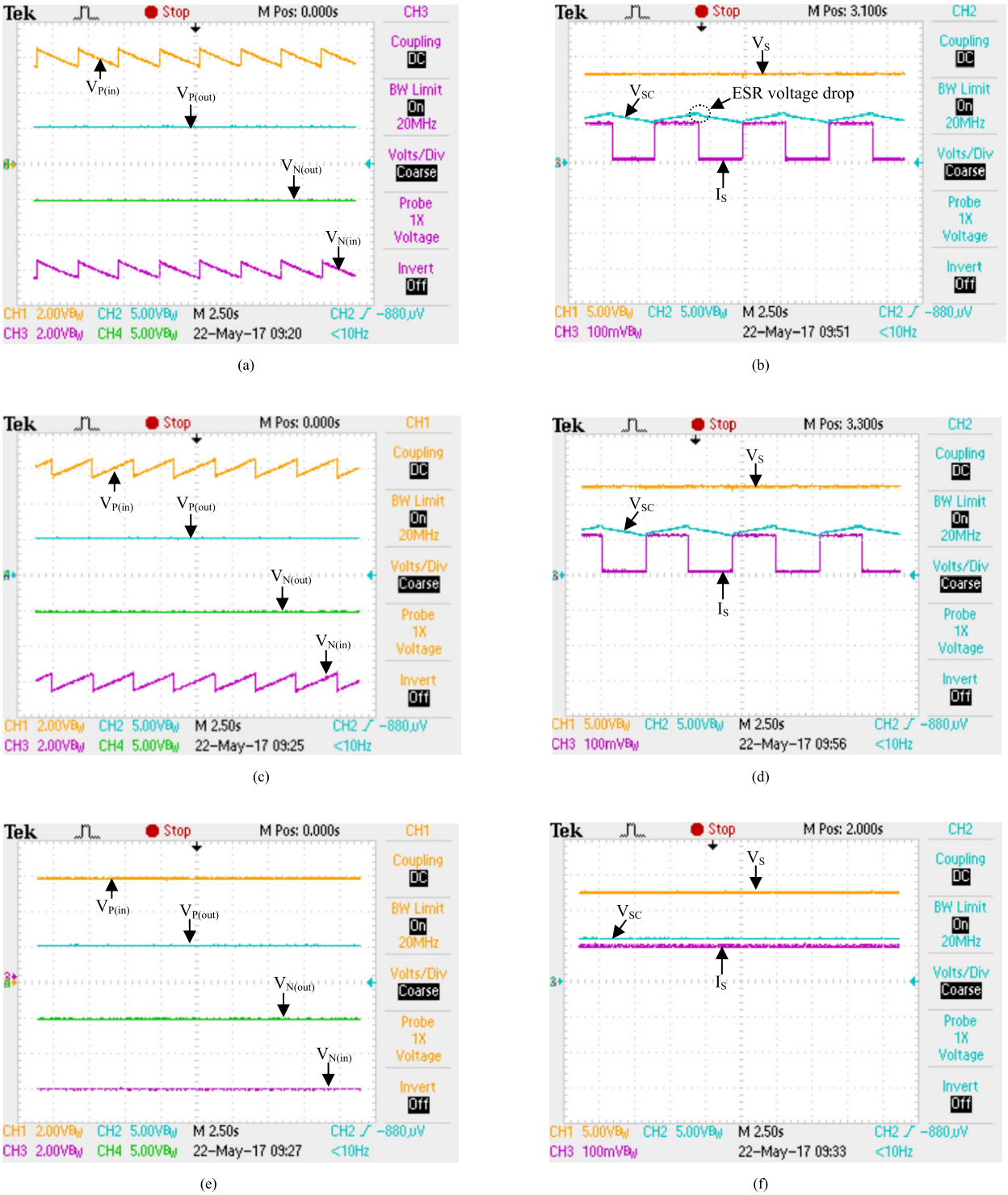

FIGURE 8. Steady-state performance: (a) and (b): Mode 2 when $I_{P(out)} = 1100$mA, $I_{N(out)} = 100$mA; (c) and (d): Mode 3 when $I_{P(out)} = 100$mA, $I_{N(out)} = 1100$mA; (e) and (f): Mode 4 when $I_{P(out)} = 1000$mA, $I_{N(out)} = 1000$mA. All the measurements were done with *DC coupling*: $V_{P(in)}$, $V_{N(in)}$: 2V/div, $V_{P(out)}$, $V_{N(out)}$, V_S, V_{SC}: 5V/div, I_S: 100mV/div, Time: 2.5s/div.

experimentally. The format of the experimental validation is built based on some recent work in the literature [56]–[58]. Two commercial LDO regulators (positive LDO: LT3086 and negative LDO: LT3091) were used with the maximum output currents adjusted to 1.5A. Fig. 7 (a) is the schematic and Fig.7(b) shows the PCB with all parts assembled into a working prototype. The required capacitance of the SC was 3.3F to keep the switching frequency less than 1Hz and to handle

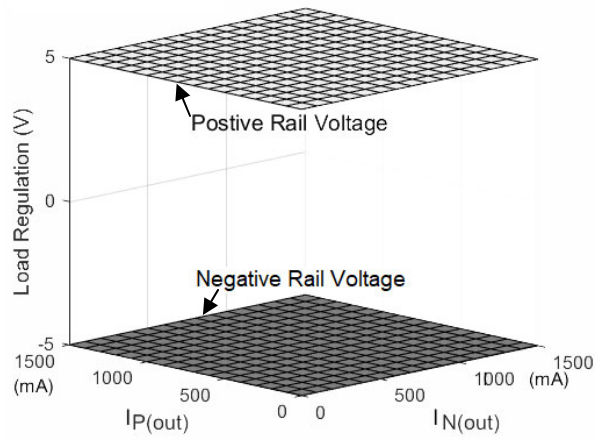

FIGURE 9. Load regulation of the prototype.

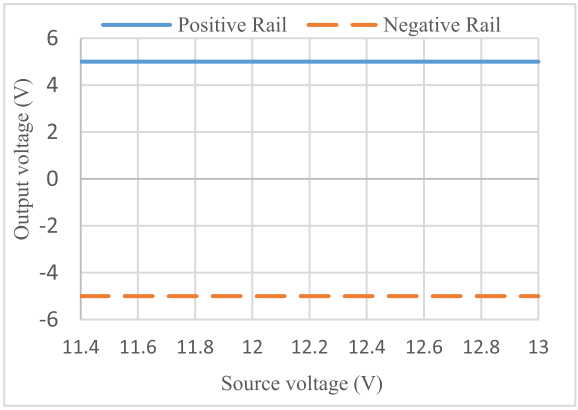

FIGURE 10. Line regulation of the prototype.

a maximum of 1.5A of differential load current. The electrically isolated inputs of the back-to-back MOSFET based switches (TLP3543: S_1-to-S_5 in Fig. 7(a)) were controlled with the aid of an Atmel ATMEGA16 microcontroller. The TLP3543 switches had a series resistance of 50mΩ each, and the ESR of the SC was 50mΩ.

The microcontroller unit (MCU) monitors the input source voltage, the input voltage of the LDO_N and the SC voltage through resistor dividers. The V_{min} value of the two LDO regulators was 5.4V. The input and output capacitors were applied according to the datasheet specifications to ensure the stability of each LDO regulator. Initially, the SC was charged up to 5.6V (through S_4, S_5 and 150R), and placed in parallel to LDO_N.

B. SYSTEM PERFORMANCE

1) STEADY-STATE PERFORMANCE

The resulting waveforms of the prototype for different output current levels are summarized in Fig. 8. The source current was measured using a current sensor of 100mV/A while keeping the input source voltage constant at 12V. The input and output voltages of the LDO regulators were measured relative to GND_V. The oscilloscope trace of $V_{N(in)}$ shows the inverted GND_V.

Table 4 summarizes the steady-state results. The two LDO regulators keep the voltage regulation with respect to the GND_V although their input voltages vary due to the energy recovery method of the SC switching network. Therefore, these results show that the DO-SCALDO method can offer better voltage regulation at the steady state.

2) LOAD AND LINE REGULATION

The load regulation of the prototype was tested for both rails at room temperature. The variation of the output voltage against the load current is displayed in Fig. 9. According to this diagram, the load regulation is 7μV/mA from 0 to 1.5A when the source voltage is 12V. This is quite an improvement compared to other inductorless split-rail topologies such as buffer circuits (e.g; 11 mV/mA for 0mA to 250mA in BUF634) and switched capacitor converters (e.g; 318mV/mA for 0mA to 11mA in MAX865) where the load regulation is poor at high output currents due to their high output impedance [13], [16], [59].

Line regulation of the prototype was also measured at room temperature with an input voltage range of 11.4V to 13V at a constant load current of 1.5A. The graph in Fig. 10 shows the line regulation. Again, compared to the buffer circuits and switched capacitor converters where the output voltages are unregulated [13], [15], this technique can keep the voltage regulation for a range of input voltages as shown in Fig. 10.

3) LOAD-TRANSIENT RESPONSE

First, the two individual LDO regulators were tested separately for the step load response before applying the SCALDO technique. This method keeps only the particular LDO regulator under test active while all the other parts of the circuit are isolated. The input voltage of the LDO regulator was set to 6V, and the load current was changed from 0mA to 500mA with a slew rate at about 10mA/μs. According to the test results of LDO_P (Fig. 11.(a)), the output ripple voltage of the rising edge and the falling edge of the load current are about 22mV and 29mV, respectively.

As the next step, the SCALDO operation was started and the two outputs of the split-rail regulator were tested separately for the same step load change. In the charging phase of LDO_P regulator (Fig. 11.(b)), the rising edge ripple and the falling edge ripple are around 18mV and 24mV, respectively. The differential load current of the rising edge passes through the SC and creates nearly 45mV across the SC. Similarly, in the falling edge of the load current, the SC voltage drops at about 45mV. Also, $V_{P(in)}$ tends to fall about 140mV during the rising edge, and it increases by the same amount in the falling edge. There is around 100mV difference between the change of V_{SC} and $V_{P(in)}$. This voltage drop is due to the resistance of the switches.

Furthermore, in the discharging phase of the LDO_P as displayed in Fig. 11 (c), the output voltage of the LDO_P drops about 19mV in the rising edge and hits about 26mV

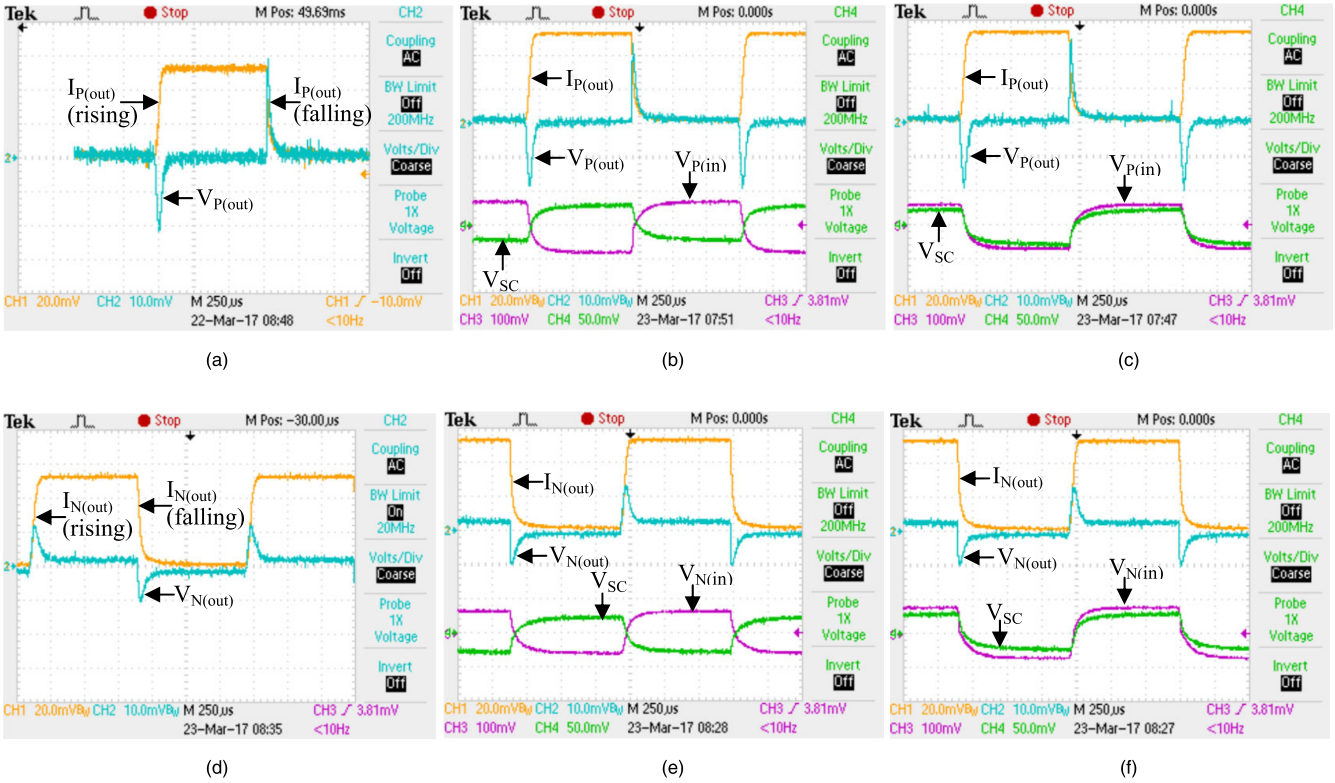

FIGURE 11. Transient response based on step-load test (a): LDO_P Only, (b) LDO_P in SC charging phase, (c) LDO_P in SC discharging phase, (d): LDO_N Only, (e) LDO_N in SC charging phase, (f) LDO_N in SC discharging phase. All the measurements were done with *DC coupling*: $I_{P(out)}$, $I_{N(out)}$: 20mV/div; *AC coupling*: $V_{P(out)}$, $V_{N(out)}$: 10mV/div, $V_{P(in)}$, $V_{N(in)}$: 100mV/div; Time: 250μs/div.

in the falling edge of the load current. Since the SC is in parallel to the LDO_P on this occasion, both the input voltage of the LDO_P and the voltage across the SC fall during the rising edge. The drop of the input voltage of LDO_P is around 130mV whereas the voltage drop across the SC is around 40mV. Similarly, throughout the falling edge of the transient load current, the input voltage of the LDO_P increases nearly 130mV, and the SC voltage rises at about 40mV. The corresponding voltage drop in the switches can be estimated as 90mV during this period. In addition, there is a roughly 140mV decrease in the $V_{P(in)}$ due to the transient load current. Nonetheless, the setting of the V_{min} value 150mV over the manufacturer-specified minimum input voltage of each LDO regulator ensures the continuous regulation during a maximum step load change.

Moreover, it is interesting to observe that the variation of the output voltage of the LDO_P is the same in all three cases of the step load test. Therefore, these observations imply that the proposed DC-DC converter can produce a similar response to a LDO regulator for a step load change. In other words, the load experiences the same quality DC output of a LDO regulator in the proposed design.

The load-transient responses of the LDO_N before and after the SCALDO operation are displayed in subplots (d), (e), and (f) in Fig. 11. These results further conclude that the negative output of the proposed split-rail regulator has a similar response to a negative LDO regulator for the step load test. In summary, the low-frequency operation of the SC along with the dual-polarity cascaded LDO regulator architecture brings an equivalent dynamic response to a LDO regulator. Given that the step-load response is a conventional test for the operational stability of a linear regulator, results shown in Fig. 11 imply that the DO-SCALDO regulator is stable, although the case of a SC switching configuration is used for energy recovery. The analytical work on the stability of this new technique will be presented in a future publication.

TABLE 5. Power losses of the DO-SCALDO circuit.

Loss factor	Calculated value (W)	Remarks
1 (Ohmic)	0.428	When the SC switching network is handling 1.5A differential current.
2 (Dynamic)	≈ 0	Due to the low-frequency operation
3 (Control unit)	0.3	When the control circuit consumes 25mA
4 (Voltage mismatch in Capacitors)	0.000003	Since the capacitance of an input capacitor is much smaller relative to the capacitance of the SC.
5 (LDO regulators)	1.161	Due to the heat dissipation across the series pass device and the power consumption due to the internal control circuit of the LDO

V. POWER LOSSES OF THE PROTOTYPE

Since the proposed split-rail DC-DC converter is derived from the basic SCALDO technique, the main losses are

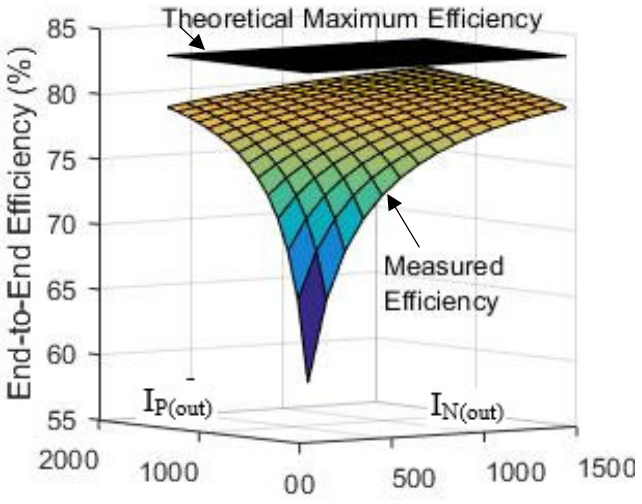

FIGURE 12. The end-to-end efficiency of the 12V to ± 5V split-rail regulator at rated input voltage.

similar to the losses inherited in the SCALDO design [25]. These losses are (1) Ohmic losses due to the switches and the ESR of the SC, (2) Dynamic losses, (3) Power consumption of the control circuit, (4) Energy loss due to the parallel connection of the capacitors with different voltages, and (5) Power losses in the LDO regulators. These losses are obtained at the rated input voltage (12V) for a maximum differential load current of 1.5A and summarized in Table 5.

When the above losses are considered, the calculated total power loss of the prototype is about 1.89W. This accounts for around 20% losses for the worst-case estimation at the rated supply voltage and the maximum differential load current.

VI. END-TO-END EFFICIENCY OF THE PROTOTYPE

According to (11), the maximum theoretical ETEE of the proposed split-rail regulator is about 83.3%. Fig. 12 depicts the measured ETEE of the proposed regulator at the rated input voltage. According to this graph, the maximum achievable efficiency is about 81% at maximum load current. The drop in the efficiency at low output current levels is due to the ground pin currents of the LDO regulators and the power consumption of the MCU.

Fig. 13 depicts the ETEE at different input voltages from 11.4V to 12.6V.

VII. SUMMARY OF THE DOMINANT DO-SCALDO CHARACTERISTICS

Some of the dominant parameters of the DO-SCALDO concept are listed in Table 6. The DO-SCALDO regulator offers voltage regulation, which is not available in buffer circuits and most of the charge pumps. Also, this regulator requires only a few components to build. The ETEE efficiency can reach to 86% if the supply voltage is dropped by 5% at rated output current.

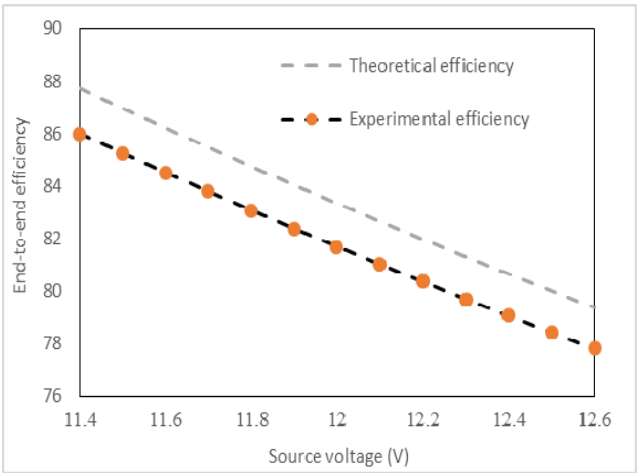

FIGURE 13. The end-to-end efficiency when the source voltage is adjusted to ± 5%.

TABLE 6. Basic features of the DO-SCALDO regulator.

Feature	DO-SCALDO (12V to ±5 V prototype)
Voltage Regulation	Regulated
Essential Components	2 LDOs, 4 input capacitors, 5 switches, Single Supercapacitor, a controller
Differential output current	1.5A (Proof-of-concept version) * Any load current in the range of mA to several 10s of amps is possible
Load Regulation	7μV/mA (0 to 1.5A, V_S = 12V)
Efficiency	Maximum 83.3% at rated input and reaches 86% if the supply voltage is dropped by 5%
Output noise	LDO_P : 40μV_{RMS} , and 300μV of SCALDO ripple LDO_N : 18μV_{RMS} and 100μV of SCALDO ripple
Maximum switching Frequency	360mHz (for 1.5A differential load current and 12V input)

A. HIGH CURRENT CAPABILITY

Conventional split-rail converters have limited output current capability due to their high output impedance. For example, the maximum load current capabilities of MAX865 and BUF634 are 20 mA and 250mA, respectively. Since the DO-SCALDO concept does not suffer from high output impedance, any load current can be achieved based on the current capability of the LDO regulators as they can be easily up-scaled to a very high current in the order of 10 to 50A. Similarly, the SCs used in this technique have ESR values

in the range of 50 to 100mΩ only, allowing them to be charged or discharged with currents in the order of tens of amperes. Therefore, the DO-SCALDO technique can be easily up-scaled to handle high load currents.

B. HIGH SLEW-RATE CAPABILITY

Better slew-rate performance is critical in applications where dynamic load changes are present such as localized micro-processors. Therefore, linear regulators in the form of LDOs are applied in the post-regulation stage in many DC-DC converters to achieve superior slew-rate performance. Since the DO-SCALDO regulator is designed based on cascaded LDO architecture, it can bring a faster dynamic load response from its dual polarity linear regulation stages. In the case of a non-linear load such as a DC motor fed by a high-frequency PWM supply with this dual-output regulator, it will have no issues since the current slew-rate capability of a LDO is very high.

C. LOW-NOISE CAPABILITY

Large time constants-based charge-discharge loops of the SCALDO technique create a lower switching frequency, which has the advantage of the RFI/EMI free output. When the load current reduces, or the size of the SC is increased the periods of the charge-discharge cycles increase, with no adverse effect on the regulation capability, since it is governed only by the LDO stages which are directly connected to the loads. While the lower range of the frequency variability is only on the input side, it has no direct impact on the voltage regulation [27]. This unique characteristic of the SCALDO method is mainly due to the attenuation of the switching ripple as the LDO regulators have a high ripple rejection ratio at low frequencies [60], [61]. Therefore, the DO-SCALDO regulator offers low noise operation compared to the well-known switched capacitor techniques (e.g: 10mV noise in MAX865 charge pump IC) which suffer from the high-frequency switching noise at the output.

The experimental results in Table 6 show that the maximum SC switching frequency of the 12 to ± 5V case is around 360mHz for 1.5A of differential load current at 12V input supply. In addition to the internal noise of the two LDO regulators, the amplitude of the low-frequency SC ripple that appears at the output of the positive LDO regulator is 300μV and it is about 100μV for the negative LDO regulator.

D. END-TO-END EFFICIENCY

Unlike the performance of the charge pump or buffer circuits where the efficiency falls when the load current is increased (e.g: MAX865: 60% efficiency in negative output at 18mA load current and 5V input), the DO-SCALDO regulator provides high efficiency at high output currents (86% at 1.5A differential load current and 11.4V supply voltage). The ETEE can also be improved at light loads by using the low quiescent current LDO regulators and replacing the MCU with low power logic gates and analog comparators designed to work for the same switching algorithm. Since the ETEE is mainly determined by the input/output voltage ratio as per (11), the switching frequency of the SC charge balance circuit has minimum influence on ETEE. Also, the selection of LDO regulators with very low dropout voltages (or design of discrete LDOs with minimum voltage headroom of their series-pass devices) and selection of switches with very low resistance can minimize the heat dissipation and improve the efficiency of the DO-SCALDO regulator significantly as shown in Table 5.

In summary, the DO-SCALDO is a new linear design approach which has all the useful characteristics of linear regulators such as high slew-rate capability, high output current and low noise with the added advantage of high efficiency. Many useful dual-output voltage combinations such as ±3V, ±1.8V can be achieved with the use of adjustable voltage LDO regulators in the DO-SCALDO concept.

VIII. CONCLUSION

This paper indicates that the basic SCALDO technique can be further extended to design a split-rail power supply with end-to-end efficiencies of around 81-86% for a case of 12V to ± 5V. The useful characteristics of the single-stage SCALDO technique are maintained in this dual-output version where the load enjoys the low noise and high slew-rate capable output of a set of LDO regulators. Since the switching frequency of the SC is in the millihertz range, the proposed design eliminates the need for RFI/ EMI filters. This DO-SCALDO technique can be further extended to high current outputs, by replacing the IC versions of LDOs, by high current discrete LDO regulators. Another potential unique application is a DO-SCALDO regulator with adjustable output voltages.

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