IEEE Access
Multidisciplinary Rapid Review Open Access Journal

Received July 8, 2019, accepted August 13, 2019, date of publication August 26, 2019, date of current version October 10, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2937444

Analog/RF Performance Investigation of Dopingless FET for Ultra-Low Power Applications

ANKIT SIROHI[1], CHITRAKANT SAHU[2], (Member, IEEE), AND JAWAR SINGH[1], (Senior Member, IEEE)

[1]Department of Electrical Engineering, Institute of Technology Patna, Patna 801106, India
[2]Department of Electronics and Communication Engineering, Malaviya National Institute of Technology at Jaipur, Jaipur 302017, India

Corresponding author: Jawar Singh (dr.jawar@gmail.com)

This work was supported by the Science and Engineering Research Board, Government of India, New Delhi, India, under Grant EMR/2016/004065.

ABSTRACT In this paper, we investigated the performance of a dopingless (DL) double gate field-effect transistor (DL-DGFET) for ultra-low power (ULP) analog/RF applications. It is observed that the source/drain metal electrode workfunction engineering in DL-DGFET yields improved analog/RF performance as compared to underlap inversion mode (IM) and junctionless (JL) DGFETs. The DL-DGFET exhibits superior electrostatic control, low threshold voltage variability, simpler fabrication process, and comparable ON state current as compared to IM- and JL-DGFETs. In addition, the DL-DGFET alleviates the inherent contradictory trade-off between gain and bandwidth by exhibiting the simultaneous improvement in intrinsic voltage gain (A_{vo}) and unity gain cutoff frequency (f_T). The well calibrated TCAD simulation results of the DL-DGFET show a minimum noise figure (NF_{min}) 1.27 times and 2.29 times less than the IM and JL-DGFET. At gate overdrive voltage of 0.1 V, the DL-DGFET achieves 5.08 times f_T and 5.86 times maximum oscillation frequency (f_{MAX}) along with 3.59 times A_{vo} in comparison to JL-DGFET. From simulation results, it is evident that the dopingless FET is a promising candidate for ultra-low power applications of analog and radio frequency (RF) domains.

INDEX TERMS Charge-plasma, doping-less, transconductance, minimum noise figure, ultra low power (ULP).

I. INTRODUCTION

The continuous downscaling of complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) has enabled tremendous improvement in the performance of digital systems. However, improved radio frequency (RF) figure-of-merit (FoM) has made CMOS technology attractive for system-on-chip (SoC) products too, where both analog/RF and digital circuits can be realized on the same integrated circuit. For low power applications, it is preferred to operate metal-oxide semiconductor FETs (MOSFETs) at power supply less than three times the threshold voltage [1]–[3]. Further, the major advantages of operating a DL-DGFET in low voltage regime are higher early voltage (V_{EA}) and higher transconductance generation factor (g_m/I_d).

The major challenges in nanoscale devices are short channel effects (SCEs) and stringent process requirements for formation of abrupt p-n junctions, which, limits their applicability for analog/RF applications [4]–[7]. The non-classical CMOS device structures, such as, underlap IM-DGFETs features high immunity to SCEs due to larger effective channel length (L_{eff}) [8]. The underlap optimization of IM-DGFET also shows good analog/RF performance but it requires a dual-spacer process and precise control of spacer width that makes fabrication process complex [9]–[11]. The junctionless FET (JL-FET) eliminates requirements of ultra sharp p-n junctions and its simple structure makes fabrication process easier [12]–[17]. However, highly doped JL-FETs suffer from increased sensitivity to device and technological

The associate editor coordinating the review of this manuscript and approving it for publication was Kalyan Koley.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

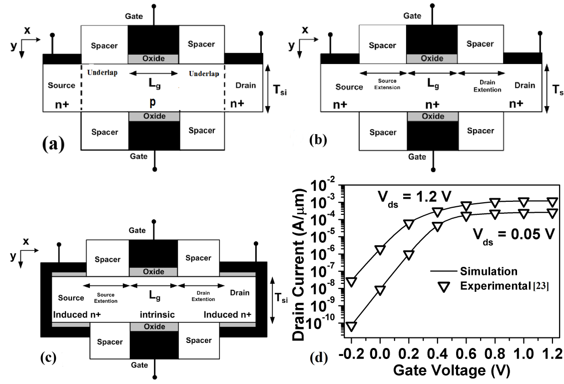

FIGURE 1. Schematic diagrams of (a) underlap IM-DGFET [8], (b) JL-DGFET, (c) DL-DGFET, and (d) calibration of simulated and experimental data for 30-nm abrupt source/drain junction IM-DGFET [31].

parameters variations due to random dopant fluctuations (RDFs) [18], [19].

The source/drain metal electrode workfunction engineering based dopingless (DL) double-gate FET (DL-DGFET) significantly overcomes the variability issues encountered in JL-FETs [20]–[24]. Furthermore, DL-DGFET offers advantages of both underlap MOSFET (improved analog/RF metrics) and JL-FET (low thermal budget and simpler fabrication process). We, therefore, report a systematic investigation of the analog/RF performance of DL-DGFET for ultra low power applications in comparison with underlap IM- and JL-DGFETs of equivalent geometry. The DL-DGFET shows 3.59 times improvement in intrinsic gain (A_{vo}) as well as 5.08 times improvement in cutoff frequency (f_T) over JL-DGFET. The noise conductance (g_n) is a quantity on which the noise figure directly depends [25], the DL-DGFET shows a g_n of 0.02 mS whereas the JL-DGFET offers a g_n of 0.07 mS at a frequency of 50 GHz which is significantly higher. Improvement in f_T and lower g_n is achieved because of higher transconductance (g_m). The enhanced FoMs of DL-DGFET are observed without making device structure complex along with better immunity towards variability as compared to counterpart devices reported previously [5], [9], [10].

II. DEVICE STRUCTURES AND SIMULATION METHODOLOGY

Fig. 1 shows the cross sectional view of (a) underlap IM-, (b) JL- and (c) DL-DGFETs. The underlap IM-DGFET consist of intrinsic channel doping of 10^{15} atoms/cm^3 with gate length (L_g) of 20 nm, oxide thickness (T_{ox}) of 1.7 nm, silicon fin thickness (T_{si}) of 10 nm, source/drain length (L_{sd}) of 30 nm and underlap length (L_{un}) of 15 nm. The source/drain implantation controlled lateral doping profile was conceived as a Gaussian distribution, and given by $N_{sd}(x) = N_{peak}\ exp(-x^2/\sigma^2)$, where N_{sd} is the source/drain doping concentration towards channel, x represents position along the channel (i.e. lateral diffusion from source/drain into the channel), and N_{peak} is the peak doping concentration at source/drain edge [1]. Here, σ is the lateral straggle of about 3 nm and N_{peak} is 10^{20} atoms/cm^3 at source/drain region. In previous study for 20 nm gate length of IM-DGFET, maximum analog/RF performance metrics were obtained for underlap design with $s/\sigma = 2.4$ (s = 15 nm) and it has better performance than highly doped JL device [26].

TABLE 1. Device simulation parameters for underlap IM, JL, and DL-DGFETs.

Parameters	Underlap IM	JL	DL
Silicon thickness, nm	10	10	10
Oxide thickness, nm	1.7	1.7	1.7
Channel doping S/D, cm^{-3}	10^{15}	10^{19}	10^{15}
S/D doping, cm^{-3}	10^{20}	10^{19}	10^{15}
Gate workfunction, eV	4.74	5.32	4.74
Gate length, nm	20	20	20
S/D extension, nm	15	15	15
S/D total resistance, Ω-μm	125	125	125

The simulation parameters for JL-DGFET are same as above except silicon film with uniform carrier concentration of 10^{19} atoms/cm^3. In DL-DGFET, to get carrier concentration of the order of 10^{19} atoms/cm^3 under source/drain region, hafnium metal (workfunction = 3.9 eV) is employed for source/drain contact electrodes [20]–[22], [24], [27]. The DL-DGFET has lateral as well as top contact over SiO_2 in source/drain region to induce constant electron plasma [20], [21], as shown in Fig. 1(c). The details of other device parameters are summarized in Table 1. The metal-semiconductor contacts are assumed to be ohmic contact for all devices. All devices are simulated with same external resistances to meet ITRS requirement for 45 nm technology node (with effective channel length 18 nm) [28]. For fair comparison of these devices, the threshold voltages (V_T) of these devices were optimized for common gate over drive voltage range. The V_T is estimated through double derivative method [29], and finally optimized V_T for IM-DGFET, DL-DGFET, and JL-DGFET, are 0.4 V, 0.4 V, and 0.35 V, respectively.

Device simulations were carried out using Silvaco ATLAS device simulator with default parameters of Silicon [30]. The simulation involves Lombardi mobility model along with Shockley-Read-Hall (SRH), Auger recombination models for minority carrier recombination. To determine density and active carrier lifetime, we have used incomplete ionization model. For calculation of noise parameters, we incorporated Hooges model for flicker noise calculation. Fig. 1(d) shows the calibration of our simulation results (for traditional abrupt source/drain junction IM-DGFET) with experimental data for 20 nm DGFETs [31]. We observed the transfer characteristics of all the three devices with gate overdrive voltage ($V_{OD} = V_{GS}$-V_T) ranging from -0.1 V and 0.1 V at drain voltage V_{DS} = 500 mV, as shown Fig. 2. The range of gate voltage (V_{GS}) taken for DL-DGFET and IM-DGFET is from 0.3 to 0.5 V and that for JL-DGFET is from 0.25 to 0.45 V.

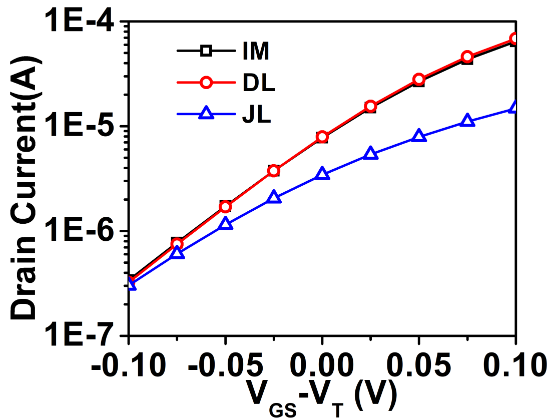

FIGURE 2. Transfer characteristics of optimized IM-, DL-, and JL-DGFET devices.

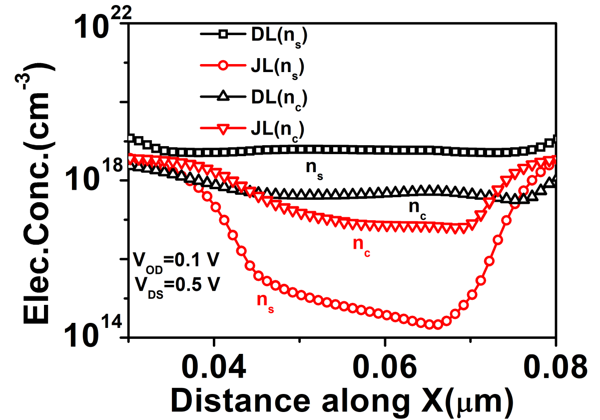

FIGURE 4. Electron concentration along the channel direction (x) for DL- and JL-DGFETs.

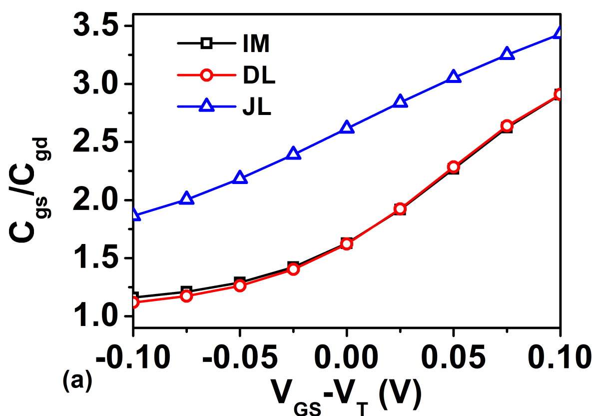

FIGURE 3. Variation of gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitance ratio as a function of gate overdrive voltage (V_{OD}) in IM-, DL-, and JL-DGFETs.

All three devices exhibit exponential rise in I_{DS} for a wide range of V_{OD} that signifies ultra low power applications of these devices.

A nanoscale MOSFET designed for ultra-low power analog/RF applications must have (a) better gate controllability on channel charges, and (b) minimum gate-to-drain feedback (Miller) capacitance. These qualities are generally expressed by a ratio of gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitance, a higher value of C_{gs}/C_{gd} means good control of the gate over the channel, which results in reduction in the Miller capacitance [32]. For a better gate controllability, ratio of C_{gs}/C_{gd} is observed as a function of V_{OD} for different DGFETs, as shown in Fig. 3. Simulation results indicate 1.17 times improvement in C_{gs}/C_{gd} of JL-DGFET over DL-DGFET at $V_{OD} = 0.1$ V. This improvement has resulted from longer effective channel length (L_{eff}) of JL-DGFET due to lateral extension of depletion width beyond the gate edges, as well as in JL-DGFET the concentration of electrons at the surface (n_s) is lower than that at the centre (n_c), as shown in Fig. 4 [26]. The electron concentration along the channel direction is calculated at $V_{OD} = 0.1$ V and $V_{DS} = 0.5$ V. The JL-DGFET shows higher electron concentration at the centre that signify bulk conduction in the device.

III. FOMS FOR ANALOG APPLICATIONS

Figure of Merits (FoMs) for analog performance of a DGFET can be described by: transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$), transconductance generation factor (g_m/I_{ds}), intrinsic gain ($A_{vo} = g_m/g_{ds}$), and early voltage ($V_{EA} = I_{ds}/g_{ds}$) [33]. Since, g_m influences the intrinsic voltage gain of a device, hence, considered as a key parameter for analog applications in the current study. The DL-DGFET exhibits 6.06 times (or 975.91 $\mu S/\mu m$) higher g_m than JL-DGFET (161.95 $\mu S/\mu m$) at V_{OD} of 0.1 V, as shown in Fig. 5(a). In JL-DGFET current flow in the bulk and it's small where as in DL-DGFET the conduction is spread out in silicon film i.e. volume accumulation this can be seen from Fig. 4, therefore, the JL-DGFET has smaller g_m. Also the incomplete ionization effect in JL-DGFET will reduce the mobility thereby reducing the current flow and g_m [21]. The lower transconductance generation factor (g_m/I_{ds}) implies decreased input drivability, hence, higher power dissipation in capacitive load circuits [8]. In Fig. 5(b), the DL-DGFET exhibits maximum g_m/I_{ds} followed by IM- and JL-DGFETs for ultra-low voltage region. The g_m/I_{ds} for DL-, IM-, and JL-DGFETs are $29.80V^{-1}$, $29.03V^{-1}$, and $19.29V^{-1}$, respectively, for V_{OD} of 0.0 V, and the same is summarized in Table 2. Hence, reduced power consumption in ultra low voltage regime makes DL-DGFET suitable for ultra-low power applications.

For analog circuit design, intrinsic voltage gain (A_{vo}) is another important design parameter expressed by the ratio of the transconductance to the drain conductance. The A_{vo} of DL-DGFET outperforms counterpart JL-DGFET device for entire V_{OD} range, as shown in Fig. 6(a). The (A_{vo}) for DL-DGFET is 3.6 times (or 44.84) higher than the JL-DGFET (i.e. 12.49) at $V_{OD} = 0.1$ V. The higher (A_{vo}) in DL-DGFET is due to improvement in g_m. The calculated g_{ds} as shown in Fig. 6(b) of DL-DGFET and JL-DGFET at $V_{OD} = 0.1$ V are 13.69 μS and 9.35 μS, respectively.

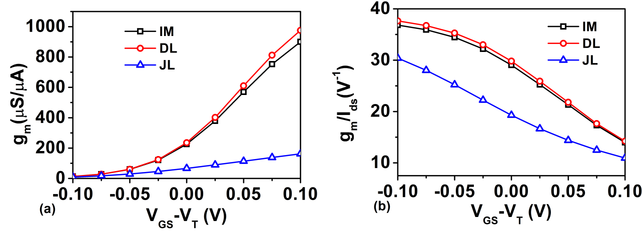

FIGURE 5. Variation of (a) transconductance (g_m), and (b) transconductance generation factor (g_m/I_{ds}) as a function of gate over drive voltage ($V_{gs} - V_T$) for IM-, DL-, and JL-DGFETs.

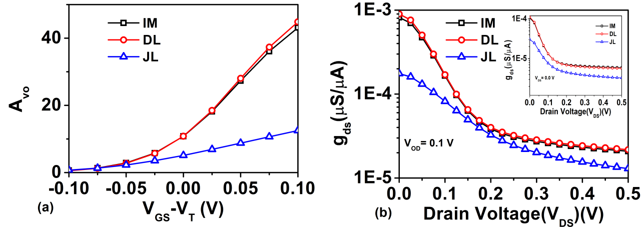

FIGURE 6. Variation of (a) Intrinsic voltage gain (A_{vo}) as a function of gate over drive voltage ($V_{gs} - V_T$) and (b) drain conductance (g_{ds}) as a function of drain voltage (V_{DS}) for IM-, DL-, and JL-DGFETs.

TABLE 2. Summary of analog FoMs.

-	V_{OD}=0.0 V V_{DS}=0.5 V			V_{OD}=0.1 V V_{DS}=0.5		
Parameters	JL	IM	DL	JL	IM	DL
A_{vo}	5.11	10.80	10.81	12.49	43.12	44.84
$g_m (\mu S/\mu m)$	66.26	225.52	235.36	161.95	899.92	975.91
g_m/I_{ds} (V^{-1})	19.29	29.03	29.80	10.93	13.97	14.22
-	V_{OD}=0.1 V V_{DS}=0.25 V			V_{OD}=0.1 V V_{DS}=0.5 V		
g_{ds} ($\mu S/\mu m$)	15.64	17.39	17.39	9.35	13.66	13.69
V_{EA} (V)	0.80	1.88	1.93	1.85	3.08	3.15
-	f=10 Hz V_{OD}=0.1 V			f=1000 Hz V_{OD}=0.1 V		
$S_{I_{ds,1/f}}$(a A^2/Hz)	50.21	216.89	252.42	2.52	2.16	2.52

Similarly, for V_{OD} = 0.0 V (see inset of Fig. 6(b)) the g_{ds} of DL-DGFET and JL-DGFET are 17.69 μS and 15.64 μS, respectively, the higher g_{ds} of DL-DGFET is the outcome of higher drive current which we have observed previously (in Fig 2). Further, early voltage (V_{EA}) is another important analog parameter and it was extracted by calculating the ratio of the drain current (I_{ds}) and the drain output conductance g_{ds} when all the devices are biased at a constant V_{OD}. One can see that IM- and DL-DGFETs have higher V_{EA} over JL-DGFET, as shown in Fig. 7. For V_{OD} = 0.1 V the value for V_{EA} is 3.15 and 1.85 V, and for V_{OD} = 0.0 V (see inset of Fig. 7) it's value is 1.93 and 0.8 V at V_{DS} = 0.5 V for DL-DGFET and JL-DGFET respectively. This improvement in V_{EA} is due to reduced electric field peak near drain end by 34.06%, can be seen in Fig. 8. These parameters are also summarized in Table 2.

Noise in analog circuits puts a lower limit in the detection of small signals as well as it limits the accuracy. We calculated

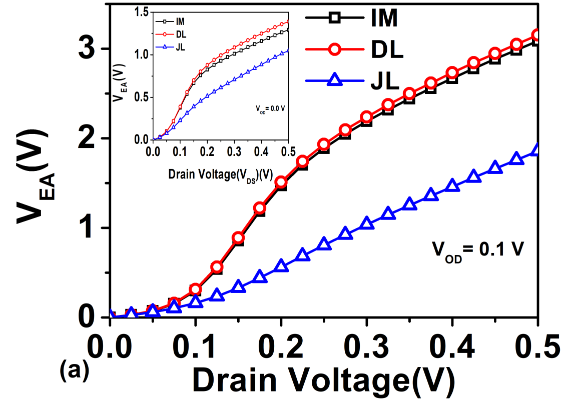

FIGURE 7. Variation of early voltage (V_{EA}) as a function of drain voltage (V_{DS}).

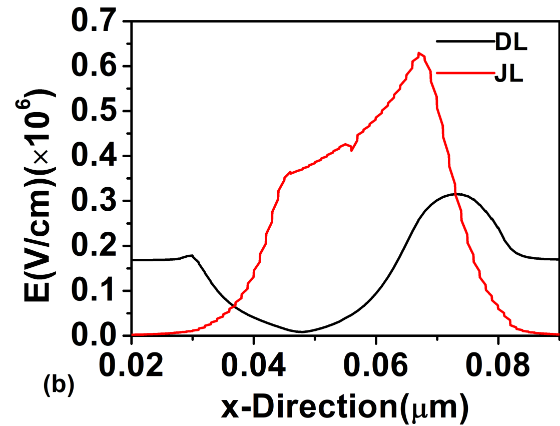

FIGURE 8. Variation of electric field at the center of the film along the channel direction (x) at V_{OD} = 0.1 V.

the current spectral density of flicker noise ($S_{I_{ds,1/f}}$) which is important for analog applications. The flicker noise spectral density is given by:

$$S_{I_{ds,1/f}} = \frac{q\alpha_H g_m^2}{fC_{ox}^2 WLQ_i} \quad (1)$$

where, f is the frequency, α_H the Hooge parameter, W and L is width and length of the channel and Q_i is the inversion charge [34], [35]. The quality of crystal and scattering mechanisms in semiconductor determines α_H that is responsible for mobility, in our case we have taken $\alpha_H = 1.8 \times 10^{-4}$ for desired fitting parameter which is close to the predicted ITRS road map for 45 nm technology node [36]. Fig. 9 shows the variation of flicker noise current spectral density with frequency for all the three devices at V_{OD} and V_{DS} of 0.1 V and 0.5 V, respectively. It can be seen that the DL-DGFET when compared with other devices, shows higher low-frequency noise, the reason being higher g_m. The current spectral density at 10 Hz for DL-DGFET and JL-DGFET is 252.42 $\times 10^{-18}$ and 50.21 $\times 10^{-18}$, respectively. Table 2 summarizes the analog FoMs of IM- , JL- and

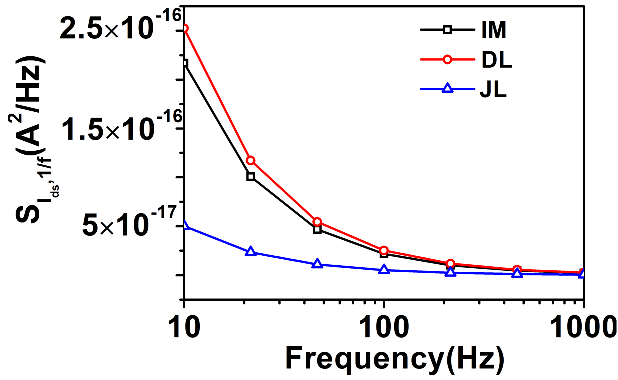

FIGURE 9. Noise spectral density ($S_{I_{ds,1/f}}$) on frequency at gate overdrive voltage of 0.1 V.

DL-DGFETs at gate over drive voltage of 0.0 and 0.1 V, and at a frequency of 10 Hz and 1000 Hz for $S_{I_{ds,1/f}}$.

IV. FOMS FOR RF APPLICATIONS

To compare RF performance, cutoff frequency (f_T), maximum oscillation frequency (f_{MAX}) and minimum noise figure (NF_{min}) were evaluated for IM-, JL- and DL-DGFETs. The f_T is an important FoM for high-speed digital applications, while f_{MAX} corresponds to the transit frequency at which maximum power gain available, a realistic parameter for microwave amplifiers. The f_T is a frequency when the current gain is unity, whereas the f_{MAX} is a frequency when power gain is unity. The NF_{min} is evaluated by dividing the signal-to-noise ratio at the input port to that of the output port and is a measure of high-frequency noise [33], [37]–[39]. The approximate values of these RF FoMs are given below [6]:

$$f_T \approx \frac{g_m}{2\pi C_{gs}\sqrt{1+(C_{gs}/C_{gd})}} \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{g_m}{2\pi C_{gg}} \quad (2)$$

$$f_{MAX} \approx \frac{g_m}{2\pi C_{gs}\sqrt{4(R_s+R_i+R_G)(g_{ds}+g_m(C_{gs}/C_{gd}))}} \quad (3)$$

$$NF_{min} = 1 + k_1 f C gs\sqrt{(R_G+R_s)/g_m} \quad (4)$$

where, k_1 is a fitting parameter, C_{gs}, C_{gd} and C_{gg} are the gate-to-source, gate-to-drain and total gate capacitances, respectively. The g_m and g_{ds} are the transconductance and output conductance, R_G, R_s and R_i are gate, source and channel resistances. Hence, f_T and f_{MAX} are largely depend upon the parasitic resistances and capacitances that are extracted from y-parameters computed using 2-D device simulator with small signal a.c. analysis and same is the case for NF_{min} [40], [41]. It is also matched numerically with equivalent non-quasi static (NQS) small signal model described in [42]. First, extrinsic parasitic components such as extrinsic gate-to-drain capacitance (C_{gde}), extrinsic gate-to-source capacitance (C_{gse}), source (R_s), and drain (R_d) resistances were extracted using total y-parameters at zero gate bias [41]–[43].

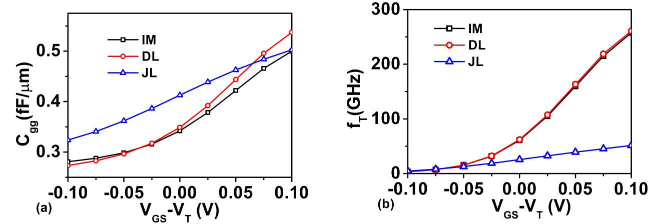

FIGURE 10. Variation of (a) total gate capacitance (C_{gg}) and (b) cutoff frequency (f_T) as a function of V_{OD} of IM-, DL- and JL-DGFETs.

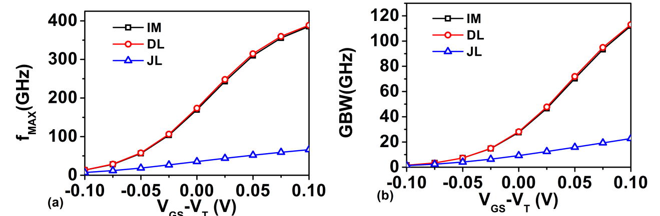

FIGURE 11. Variation of (a) maximum frequency of oscillation (f_{MAX}) and (b) gain bandwidth product (GBP) as a function of V_{OD} for IM-,DL- and JL-DGFETs.

Then above parameters are de-embedded to find internal y-parameters of channel (excluding series source/drain region), therefore, intrinsic gate to source/drain capacitances (C_{gs} and C_{gd}) and internal channel resistances (R_i) are extracted at $V_{OD} = 0.1$ V and $V_{DS} = 0.5$ V.

Total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$, where C_{gs} the gate-to-source capacitance and C_{gd} is the gate-to-drain capacitance) of the DL-, JL- and IM-DGFETs as a function of gate overdrive voltage is shown in Fig. 10(a). The C_{gg} comparison reveals that the JL-DGFET has lowest gate capacitance as compared to DL- and IM-DGFET. The C_{gg} of JL-DGFET is reduced by 1.18 times compared to DL-DGFET refer Table 3. The lowering of the gate capacitance is due to extension of depletion regions beyond the gate edges (underlap profile) along the channel direction that reduces internal fringing capacitance.

Fig. 10(b) shows dependance of f_T on V_{OD} for DL-, JL- and IM-DGFETs. It is clear that the f_T of DL-DGFET is higher than JL-DGFET. The reason for low f_T in the JL-DGFET is the increase of channel resistance due to incomplete ionization which reduces g_m this is not the case with DL-DGFET. As a result, DL-DGFET shows an increase in f_T with increase in gate voltage as shown in Fig. 10(b). Usually f_T is taken as 5-10 times the transistors operating frequency. Therefore, DL-DGFET has the potential to design radio-frequency integrated circuits (RFICs) operating up to 50 GHz approximately.

The f_{MAX} corresponding to unity power gain frequency which includes contribution from gate resistance can be seen in Fig. 11(a) with gate overdrive (V_{OD}) for DL-, JL- and IM-DGFETs. Normally f_{MAX} varies with thickness of the gate electrode, hence, it needs to be added to the gate-engineered MOSFET simulation model to predict the device behavior at a high frequency. The gate resistance R_G consists of two

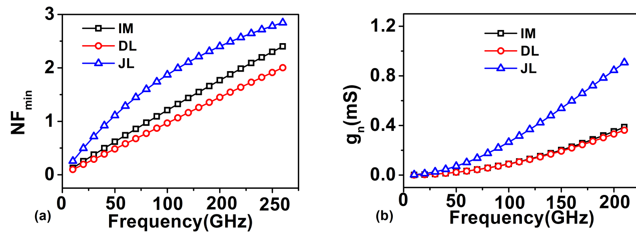

FIGURE 12. Variation of (a) Minimum noise margin NF_{min}. (b) Noise Conductance g_n of IM- DL- and JL-DGFETs as a function of frequency.

TABLE 3. Comparison of RF FoMs.

Gate Voltages	V_{OD}=0.0 V V_{DS}=0.5 V			V_{OD}=0.1 V V_{DS}=0.5 V		
Parameters	JL	IM	DL	JL	IM	DL
C_{gg} $(fF/\mu m)$	0.33	0.34	0.38	0.49	0.50	0.53
$f_T(\ GHz)$	25	61	62	51	257	260
$f_{MAX}(\ GHz)$	66	385	388	35	169	173
$GBP(GHz)$	9	27	28	22	112	113
Frequency	f=10 GHz V_{OD}=0.1 V			f=50 GHz V_{OD}=0.1 V		
NF_{min}	0.25	0.12	0.09	1.10	0.61	0.48
$g_n(\ \mu S)$	3.17	0.91	0.94	71.84	22.82	22.61

parts: (1) R_g contributed by gate electrode from gate material (metal/polysilicon); (2) the channel resistance R_i due to non-quasi-static (NQS) effect seen from the gate. In our simulation, molybdenum material of 20 nm length having R_g equals to 86.7 $\Omega.\mu$m is considered [6]. The values of R_S/R_D and R_i are obtained using y-parameter extraction [41], [43]. The DL device shows a 5.86 times increase in f_{MAX} than JL-DGFET. The DL-DGFET exhibits higher values of f_T, thereby, it has superior gain-bandwidth product (GBP) considering DC gain of 10 compared to its counterpart devices can be observed in Fig. 11(b). The DL-DGFET without any channel doping achieves nearly 5.13 times GBP as compared to JL-DGFETs. Hence, DL-DGFET can be a competitive contender for the mainstream MOSFET, and for ultra low power analog/RF applications.

Further, calculation of minimum noise figure NF_{min} Fig. 12(a) shows that DL-DGFET has NF_{min} 2.77 and 2.29 times less than JL-DGFET at 10 and 50 GHz frequency respectively. The reason is the higher g_m of DL-DGFET as compared to JL-DGFET and the same is the case for IM-DGFET. Meanwhile, the noise conductance (g_n) being the sensibility measure of noise figure is lower for DL-DGFET than JL-DGFET by 3.17 times as shown in Fig. 12(b).

Table 3 shows the RF performance metrics of IM-(abrupt S/D), JL- and DL-DGFETs at V_{OD} of 0.0 V and 0.1 V, for C_{gg}, f_T, f_{MAX} and GBP, and 10 GHz and 50 GHz for NF_{min} and noise conductance which shows DL-DGFET is superior for ultra low power applications in many aspects.

V. CONCLUSION

The potential of DL-DGFET for ultra-low power analog/RF applications is investigated in depth while considering various FoMs. A fair performance comparison of the DL-DGFET with its counter part devices was performed under uniform gate over drive voltages. The DL-DGFET shows significant enhancement in g_m, g_m/I_{ds}, A_{vo}, f_T and f_{MAX} above gate overdrive voltage of 0.1 V. Improvement in these FoMs is attributed from higher carrier mobility and reduced peak electric field at the gate edge near the drain. The DL-DGFET shows higher low-frequency noise whereas significantly enhance high-frequency noise performance the reason being higher g_m. Additionally, these improvements are observed without compromising the design simplicity (as in case of underlap devices) and performance metrics variability (as in case of JL devices). The results highlight new opportunities for realizing future ultra-low power analog/RF design with dopingless transistors.

REFERENCES

[1] V. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with gate-source/drain underlap," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 56–62, Jan. 2005.

[2] H. Kotaki, S. Kakimoto, M. Nakano, T. Matsuoka, K. Adachi, K. Sugimoto, T. Fukushima, and Y. Sato, "Novel bulk dynamic threshold voltage MOSFET (B-DTMOS) with advanced isolation (SITOS) and gate to shallow-well contact (SSS-C) processes for ultra low power dual gate CMOS," in *IEDM Tech. Dig.*, Dec. 1996, pp. 459–462.

[3] S. Chakraborty, A. Mallik, C. K. Sarkar, and V. R. Rao, "Impact of halo doping on the subthreshold performance of deep-submicrometer CMOS devices and circuits for ultralow power analog/mixed-signal applications," *IEEE Electron Device Lett.*, vol. 54, no. 2, pp. 241–248, Feb. 2007.

[4] R. T. Doria, M. A. Pavanello, R. D. Trevisoli, M. de Souza, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti, and J.-P. Colinge, "Junctionless multiple-gate transistors for analog applications," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2511–2519, Aug. 2011.

[5] R. K. Sharma and M. Bucher, "Device design engineering for optimum analog/rf performance of nanoscale DG MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 11, no. 5, pp. 992–998, Sep. 2012.

[6] A. Sarkar, A. K. Das, S. De, and C. K. Sarkar, "Effect of gate engineering in double-gate MOSFETs for analog/RF applications," *Microelectron. J.*, vol. 43, no. 11, pp. 88–873, Nov. 2012.

[7] N. Jain and B. Raj, "Analysis and performance exploration of high performance (HfO_2) SOI FinFETs over the conventional (Si_3N_4) SOI FinFET towards analog/RF design," *J. Semicond.*, vol. 39, no. 12, 2018, Art. no. 124002.

[8] K. Koley, A. Dutta, B. Syamal, S. K. Saha, and C. K. Sarkar, "Subthreshold analog/RF performance enhancement of underlap DG FETs with high-κ spacer for low power applications," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 63–69, Jan. 2013.

[9] A. Kranti, B. Rashmi, S. Burignat, J.-P. Raskin, and G. A. Armstrong, "Analog/RF performance of sub-100 nm SOI MOSFETs with non-classical gate-source/drain underlap channel design," in *Proc. Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2010, pp. 45–48.

[10] B. Anderson, A. Bryant, W. Clark, Jr., and E. Nowak, "Low capacitance FET for operation at subthreshold voltages," U.S. Patent 7 009 265, Jul. 3, 2006.

[11] A. Veloso, P. Matagne, E. Simoen, B. Kaczer, G. Eneman, H. Mertens, D. Yakimets, B. Parvais and D. Mocuta, "Junctionless versus inversion-mode lateral semiconductor nanowire transistors," *J. Phys., Condens. Matter*, vol. 30, no. 38, 2018, Art. no. 384002.

[12] J. Singh, A. K. Jain, and M. J. Kumar, "Realizing a planar 4H-SiC junctionless FET for Sub-10-nm regime using P^+ pocket," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 3209–3214, Jul. 2019.

[13] J. Singh and M. J. Kumar, "A planar junctionless FET using SiC with reduced impact of interface traps: Proposal and analysis," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4430–4434, Nov. 2017.

[14] D. Gola, B. Singh, J. Singh, S. Jit, and P. K. Tiwari, "Static and quasi-static drain current modeling of tri-gate junctionless transistor with substrate bias-induced effects," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2876–2883, Jul. 2019.

[15] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nature Nanotechnol.*, vol. 5, pp. 225–229, Feb. 2010.

[16] C.-H. Park, M.-D. Ko, K.-H. Kim, R.-H. Baek, C.-W. Sohn, C. K. Baek, S. Park, M. J. Deen, Y.-H. Jeong, and J.-S. Lee, "Electrical characteristics of 20-nm junctionless Si nanowire transistors," *Solid-State Electron.*, vol. 73, pp. 7–10, Jul. 2012.

[17] K. Biswas, A. Sarkar, and C. K. Sarkar, "Fin shape influence on analog and RF performance of junctionless accumulation-mode bulk FinFETs," *Microsyst. Technol.*, vol. 24, no. 5, pp. 2317–2324, May 2018.

[18] M. Aldegunde, A. Martinez, and J. R. Barker, "Study of discrete doping-induced variability in junctionless nanowire MOSFETs using dissipative quantum transport simulations," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 194–196, Feb. 2012.

[19] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, "Analysis of threshold voltage variability due to random dopant fluctuations in junctionless FETs," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 336–338, Mar. 2012.

[20] C. Sahu and J. Singh, "Charge-plasma based process variation immune junctionless transistor," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 411–413, Mar. 2014.

[21] C. Sahu and J. Singh, "Potential benefits and sensitivity analysis of dopingless transistor for low power applications," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 729–735, Mar. 2015.

[22] A. Lahgere, C. Sahu, and J. Singh, "PVT-aware design of dopingless dynamically configurable tunnel FET," *IEEE Trans. Electron Devices*, vol. 62, no. 8, pp. 2404–2409, Aug. 2015.

[23] N. Kamal, M. Panchore, and J. Singh, "3-D simulation of junction- and doping-free field-effect transistor under heavy ion irradiation," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 2, pp. 173–179, Jun. 2018.

[24] A. Kumar, C. Sahu, and J. Singh, "Subthreshold Analog/RF performance estimation of doping-less DGFET for ULP applications," in *Proc. IEEE Int. Conf. Emerg. Electron. (ICEE)*, Bengaluru, India, Dec. 2014, pp. 1–4.

[25] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide microwave field-effect transistors," in *Advances in Electronics and Electron Physics*, vol. 38. New York, NY, USA: Academic, Dec. 1975, pp. 195–265.

[26] D. Ghosh, M. S. Parihar, G. A. Armstrong, and A. Kranti, "High-performance junctionless MOSFETs for ultralow-power analog/RF applications," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1477–1479, Oct. 2012.

[27] B. Rajasekharan, R. J. E. Hueting, C. Salm, T. van Hemert, R. A. M. Wolters, and J. Schmitz, "Fabrication and characterization of the charge-plasma diode," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 528–530, Jun. 2010.

[28] C. Sahu and J. Singh, "Device and circuit performance analysis of double gate junctionless transistors at $L_g = 18$ nm," *J. Eng.*, vol. 2014, no. 3, pp. 105–110, Apr. 2014.

[29] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's," *Solid-State Electron.*, vol. 30, no. 9, pp. 953–968, Sep. 1987.

[30] *ATLAS Device Simulation Soft*, Silvaco Int., Santa Clara, CA, USA, 2012.

[31] M. Vinet, T. Poiroux, J. Widiez, J. Lolivier, B. Previtali, C. Vizioz, B. Guillaumot, Y. Le Tiec, P. Besson, B. Biasse, F. Allain, M. Cassé, D. Lafond, J.-M. Hartmann, Y. Morand, J. Chiaroni, and S. Deleonibus, "Bonded planar double-metal-gate NMOS transistors down to 10 nm," *IEEE Electron Device Lett.*, vol. 26, no. 5, pp. 317–319, May 2005.

[32] G. Dambrine, C. Raynaud, D. Lederer, M. Dehan, O. Rozeaux, M. Vanmackelberg, F. Danneville, S. Lepilliet, and J.-P. Raskin, "What are the limiting parameters of deep-submicron MOSFETs for high frequency applications?" *IEEE Electron Device Lett.*, vol. 24, no. 3, pp. 189–191, Mar. 2003.

[33] V. Passi and J.-P. Raskin, "Review on analog/radio frequency performance of advanced silicon MOSFETs," *Semicond. Sci. Technol.*, vol. 32, no. 12, 2017, Art. no. 123004.

[34] F. N. Hooge, "$1/f$ noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994.

[35] R. T. Doria, R. D. Trevisoli, M. de Souza, I. Ferain, S. Das, and M. A. Pavanello, "Low-frequency noise of nMOS and pMOS short channel junctionless nanowire transistors," in *Proc. IEEE Int. SOI Conf. (SOI)*, Oct. 2012, pp. 1–2.

[36] M. Haartman and M. Östling, *Low-Frequency Noise in Advanced MOS Devices*. Springer, 2007.

[37] C. H. Chen and M. J. Deen, "Direct calculation of metal–oxide–semiconductor field effect transistor high frequency noise parameters," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 16, no. 2, pp. 850–854, 1998.

[38] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2884–2892, Dec. 2001.

[39] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-26, no. 7, pp. 1032–1037, Jul. 1979.

[40] H. Fukui, "Design of microwave GaAs MESFET's for broad-band low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-27, no. 7, pp. 643–650, Jul. 1979.

[41] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. vol. 2. Oxford, U.K.: Oxford Univ. Press, 1999.

[42] S. Cho, K. R. Kim, B. G. Park, and I. M. Kang, "RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1388–1396, May 2011.

[43] X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu, "An effective gate resistance model for CMOS RF and noise modeling," in *IEDM Tech. Dig.*, Dec. 1998, pp. 961–964.

ANKIT SIROHI received the B.Tech. degree in electronics and communication engineering from the Birla Institute of Applied Sciences, Bhimtal, India, in 2013, and the M.Tech. degree in VLSI design from the ABV-Indian Institute of Information Technology and Management, Gwalior, India, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, IIT Patna, India.

CHITRAKANT SAHU received the B.E. degree in electrical and electronics engineering from Pt. Ravishankar Shukla University and the M.Tech. degree in electronics engineering from the University of Mumbai, Mumbai, India, in 2008. He is currently an Assistant Professor with the Malaviya National Institute of Technology at Jaipur, India.

JAWAR SINGH (SM'14) received the Ph.D. degree from the University of Bristol, Bristol, U.K., in 2010. He is currently an Associate Professor with the Indian Institute of Technology Patna, Patna, India. He holds two U.S. patents on SRAM cells. His current research interest includes exploration of classical and nonclassical device structures and their applications for CMOS enhancement or replacement. He was a recipient of the prestigious Indo-U.S. BHAVAN-2016 Fellowship.

• • •