IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received August 5, 2019, accepted August 15, 2019, date of publication August 26, 2019, date of current version September 6, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2937388

Bandwidth Enhancement of GaN MMIC Doherty Power Amplifiers Using Broadband Transformer-Based Load Modulation Network

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This work was supported in part by the European Union's Horizon 2020 Research and Innovation Program under the Marie Sklodowska-Curie Grant 713567, and in part by the Science Foundation Ireland (SFI) under Grant 13/RC/2077 and Grant 16/IA/4449.

ABSTRACT In this paper, we present a bandwidth enhancement technique for monolithic microwave integrated circuit (MMIC) Doherty power amplifiers (DPAs) in wireless transmitters. A broadband load modulation network is proposed by exploiting transformers and output-referred parasitic capacitances of the carrier and peaking transistors of DPA. The proposed network comprises two transformers that are used to improve frequency response of the load impedance presented to the carrier transistor at back-off and extend the DPA bandwidth. The network benefits from a unity transformation ratio and it can be readily realized by using edge-coupled microstrip transmission lines. Optimal coupling coefficients of the two transformers are determined based on bandwidth and insertion loss considerations. A proof-of-concept DPA is implemented in a 0.25-μm GaN MMIC process. It achieves 35–36 dBm output power, 42.8–48.7% drain efficiency at peak power and 24.4–31.6% at 6-dB back-off, over 4.5–6.0 GHz bandwidth. When excited by a 100-MHz 64-QAM signal with 8 dB peak-to-average power ratio (PAPR), the DPA exhibits 29.3 dBm average output power and 28.4% average drain efficiency, while the error vector magnitude (EVM) is −30.5 dB (3%) without any predistortion.

INDEX TERMS 5G, bandwidth enhancement, broadband, Doherty, GaN, integrated circuits, load modulation, MMIC, power amplifier (PA), transformer.

I. INTRODUCTION

The fifth generation (5G) of wireless networks is under advanced development and extensive research activities and trials are ongoing to achieve its targeted expectations. Small-cell base-stations are widely adopted to implement ultra-dense networks (UDNs) to meet the requirements of explosive data traffic in 5G. The energy efficiency of these devices is of paramount importance, which is primarily determined by the efficiency of RF power amplifiers (PAs) in the transmitter. The GaN technology with large power density and high efficiency is promising for such applications [1]. It also offers a potential for a higher-scale monolithic integration.

Spectrally efficient modulation schemes with large peak-to-average power ratio (PAPR) and wide bandwidth are employed to accommodate the 5G network speeds approaching tens of gigabits per second (Gb/s). The Doherty power amplifier (DPA) is an effective architecture to achieve high average efficiency in dealing with such signals [2], [3]. The conventional DPAs suffer limited bandwidth mainly arising from the load modulation network. Most notable bandwidth enhancement techniques developed for DPAs include modified characteristic impedance of transmission lines in the load modulation network, modified network for the peaking transistor, parasitic capacitance compensation, frequency response optimization, and dual-input DPA architecture [3]. However, most of these solutions are only applicable to discrete circuits. In monolithic microwave integrated circuit (MMIC) implementations, loss of passive components, limited characteristic impedance of transmission lines, and chip area limitations make most of these methods rather ineffective, and call for special techniques for MMIC DPAs.

The associate editor coordinating the review of this article and approving it for publication was Yuhao Liu.

Several GaN MMIC DPAs are reported in the literature [4]–[17], but most of them are narrow-band. A few broadband design approaches were developed for MMIC DPAs [12]–[14]. In [12], output networks of the carrier and peaking transistors are modified to maintain a low impedance-transformation ratio and hence the DPA could achieve a broad bandwidth. A drain efficiency (DE) of 48–62% is obtained at 7.6-dB back-off over 2.1–2.7 GHz (25%) bandwidth. However, the DPA is not fully integrated since the drain bias inductors are realized using bond wires. This contributes to wider bandwidth and higher efficiency of the DPA. In [13], a three-element network of transmission lines is proposed for integrated DPA implementations. A power-added efficiency (PAE) of 24–37% at 9-dB back-off is achieved over 6.8–8.5 GHz (22%) bandwidth. A power combining output network with asymmetric drain biases is presented in [14] to help with extending the DPA bandwidth. At 9-dB back-off, 31–39% PAE is measured over 5.8–8.8 GHz (42%) bandwidth.

In this paper, we propose a bandwidth enhancement technique for MMIC DPAs using a transformer-based load modulation network. We show that transformers can be effectively used in MMIC broadband amplifier design [18]–[20] and they can be realized as edge-coupled microstrip transmission lines in GaN process with benefits of broad bandwidth and low-loss. The transformer-based power combiners have been used for back-off efficiency enhancement [21] and in Doherty PA [22]. In those PA architectures, the transformer operates as a series voltage combiner that adds output voltages of the active PA cells. Here, we propose a load-modulation network using two transformers that improve frequency response of the impedance presented to the carrier transistor at back-off to extend the DPA bandwidth. In the proposed network, the circuit is transformed such that it can be realized using transformers with unity turn ratio and therefore can be implemented using the edge-coupled microstrip transmission lines.

This paper is structured as follows. In Section II, we describe the bandwidth enhancement technique for MMIC DPAs and present a circuit composed of transformers and output-referred parasitic capacitance of the transistors to provide the load modulation. The circuit design details are presented in Section III. The DPA's output network is realized using the proposed broadband load modulation circuit, while a meandered Lange coupler with broad bandwidth and compact chip area is adopted as its input network. Measurement results using continuous-wave (CW) and modulated signals are given in Section IV. Finally, conclusions are presented in Section V.

II. BANDWIDTH ENHANCEMENT OF MMIC DOHERTY PAS

A. BROADBAND LOAD MODULATION NETWORK ARCHITECTURE

A general DPA architecture is shown in Fig. 1, where the two two-port networks at the outputs of peaking and carrier amplifiers provide optimum impedances at the peak power and back-off. The carrier network is realized to operate as an impedance inverter, while the peaking network is mainly used to compensate output parasitic impedance of the peaking transistor. The output-referred parasitic capacitances of the transistors are usually absorbed into these networks. In the conventional DPA architecture, the carrier network is realized as a quarter-wavelength transmission line ($\theta_c = 90°$), while no explicit two-port network is used at the output of peaking amplifier ($\theta_p = 0$). Bandwidth of the DPA is usually limited by the narrow-band response of the load modulation network, e.g., the impedance inverter, especially at the output power back-off where the impedance transformation ratio is large.

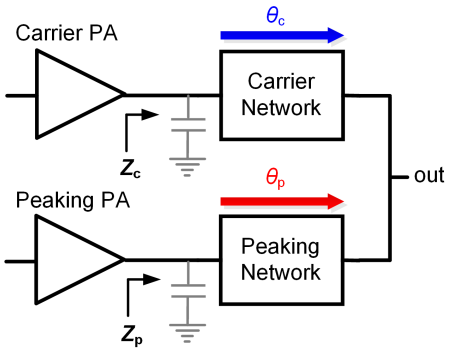

FIGURE 1. General DPA architecture.

A broadband DPA architecture can be developed by using the phase shift provided by the peaking network θ_p (at center of the band) as a design parameter. Assuming that the two networks are realized as transmission lines with a characteristic impedance of R_{opt} and the load impedance is given by $R_L = R_{opt}/2$, frequency response of the load impedance presented to the carrier network would be dependent on θ_p. It is shown that $\theta_p = 180°$ extends the bandwidth of the DPA [23].

This DPA architecture can be realized by using a cascade of two quarter-wavelength transmission lines as the peaking amplifier network (Fig. 2) [24], which can also be implemented by using lumped elements [25]. Moreover, it was shown that, to achieve broadband efficiency at both back-off and peak power, the characteristic impedance of the

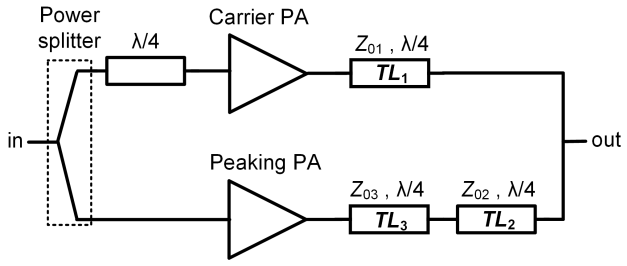

FIGURE 2. Broadband DPA architecture with half-wavelength peaking network.

transmission lines should be chosen as

$$Z_{01} = \frac{R_{opt}}{m} \tag{1}$$

$$Z_{02} = \frac{R_{opt}}{m\sqrt{m}} \tag{2}$$

$$Z_{03} = \frac{R_{opt}}{\sqrt{m}} \tag{3}$$

where $m = \sqrt{R_{opt}/2R_L}$ [26]. It is assumed that the carrier and peaking transistors have the same optimum load resistance R_{opt}. The impedance transformation ratio for TL_1 is derived as m^2 at peak power and $4m^2$ at 6-dB back-off, while for $TL_{2,3}$ it is given by m at peak power. Assuming that the impedance transformers are lossless, output power delivered to the load impedance at back-off would be the same as the available power from the carrier transistor. The carrier transistor can be fairly modeled as a current source in back-off (assuming that its output parasitic capacitance is included in the load modulation network), which delivers the output power of $P_{out} = Re[Z_{c,BO}]I_m^2/2$, where $Z_{c,BO}$ is the impedance presented to the carrier transistor at back-off and I_m denotes magnitude of the fundamental component of the drain current waveform. Bandwidth of the load modulation network at back-off can be defined based on 20% reduction in real part of the impedance, roughly corresponding to 1 dB drop in output power.

$$BW = \left(f \mid \frac{Re[Z_{c,BO}(f)]}{2R_{opt}} > 0.8\right). \tag{4}$$

In Fig. 3, real part of the impedance presented to the carrier amplifier at peak power and back-off is depicted for the conventional and broadband DPA architectures (assuming $m = 1$). The fractional bandwidth for a 20% reduction in real part of the impedance is included in the figure. The conventional DPA has a theoretically infinite bandwidth at peak power but a limited 38% bandwidth at back-off. Using the broadband DPA architecture, bandwidth at back-off is improved to 72% (i.e., by the factor of 1.89).

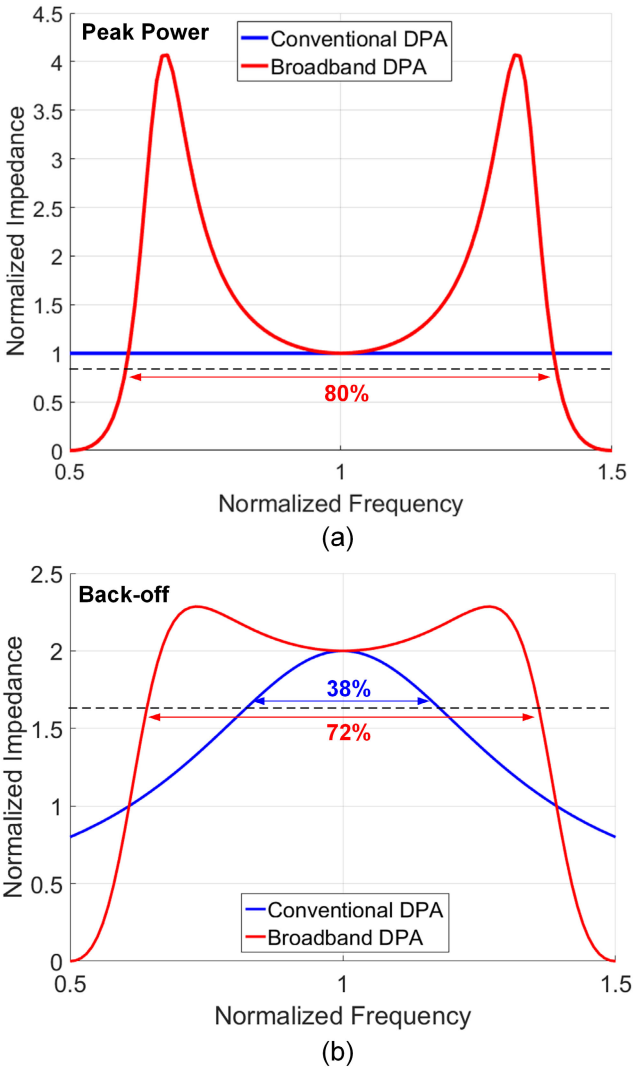

FIGURE 3. Comparison of real part of the impedance presented to the carrier amplifier at (a) peak power and (b) back-off in the conventional and broadband DPA architectures.

B. TRANSFORMER-BASED IMPEDANCE INVERTER

Conventionally, low-pass and high-pass equivalents of a transmission line, shown in Fig. 4, are used as impedance inverters in integrated-circuit DPAs. The circuit components should be selected as $L = Z_0/\omega_0$ and $C = 1/\omega_0 Z_0$ to approximate a quarter-wavelength transmission line of characteristic impedance Z_0. These circuits suffer from the following major limitations.

1) The required inductance can become very large, especially for GaN processes with high Z_0 (e.g., on the order of 100 Ω). Parasitic capacitances and losses of such large on-chip inductors can limit the DPA's bandwidth and efficiency.
2) The required capacitance is determined independently of the transistors' output-referred capacitances, $C_{o1,o2}$. These circuits can only be used when $C_{o1,o2} \leq C$, and so an extra capacitance maybe needed for balancing.

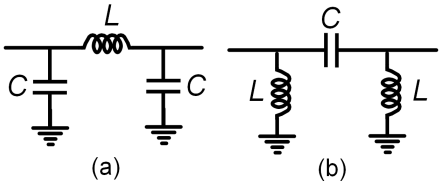

FIGURE 4. (a) Low-pass and (b) high-pass equivalent circuits of a quarter-wavelength transmission line conventionally used in DPAs.

3) The circuit of Fig. 4(a) does not include an element for the drain bias feed, while the circuit of Fig. 4(b) may need large inductances with wide metal width. Therefore, the drain bias feed is usually implemented using off-chip inductors or bond wires [10], [12].
4) These circuits can only be used in symmetric DPAs with equal C_{o1} and C_{o2}. In asymmetric DPAs, extra capacitors or inductors are needed to make the circuits symmetric. However, this limits the DPA bandwidth.

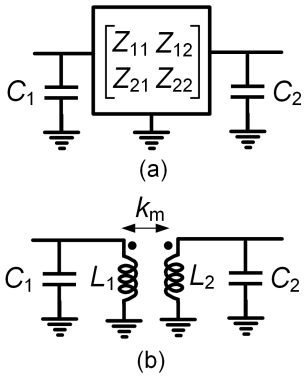

FIGURE 5. (a) General impedance inverter network including parasitic capacitances. (b) Transformer-based impedance inverter circuit.

A general impedance inverter network including the output-referred parasitic capacitances can be considered as in Fig. 5(a), where the two-port network is represented by its impedance parameters. This network is realized using linear and time-invariant passive components, thus it is reciprocal, and $Z_{12} = Z_{21}$. The impedance parameters of the network should be derived such that (along with C_1 and C_2) they constitute an impedance inverter. The transfer matrix of the impedance inverter network shown in Fig. 1 can be derived as

$$[T] = \begin{bmatrix} 1 & 0 \\ j\omega_0 C_1 & 1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega_0 C_2 & 1 \end{bmatrix}, \tag{5}$$

where *ABCD* denote the transfer parameters of the two-port network [27]. By equating this matrix with a transfer matrix of the quarter-wavelength transmission line given by

$$[T]_{\lambda/4} = \begin{bmatrix} 0 & jZ_0 \\ j\dfrac{1}{Z_0} & 0 \end{bmatrix}, \tag{6}$$

the *ABCD* parameters are derived as follows

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \omega_0 C_2 Z_0 & jZ_0 \\ j(\dfrac{1}{Z_0} - \omega_0^2 C_1 C_2 Z_0) & \omega_0 C_1 Z_0 \end{bmatrix}. \tag{7}$$

Using this representation, it can be shown that the impedance parameters of the two-port network are

$$Z_{11}(\omega_0) = \frac{(\omega_0 C_2 Z_0) jZ_0}{\omega_0^2 C_1 C_2 Z_0^2 - 1} \tag{8}$$

$$Z_{22}(\omega_0) = \frac{(\omega_0 C_1 Z_0) jZ_0}{\omega_0^2 C_1 C_2 Z_0^2 - 1} \tag{9}$$

$$Z_{12}(\omega_0) = Z_{21}(\omega_0) = \frac{jZ_0}{\omega_0^2 C_1 C_2 Z_0^2 - 1}. \tag{10}$$

This description is useful to synthesize a variety of circuit structures that can operate as the impedance inverter network.[1]

[1]This formulation can be used to analyze other circuits proposed in the literature as the impedance inverter [10], [13], [14].

Using (8)–(10), some important insights can be derived about the conditions that the two-port network of Fig. 5(a) should meet. First, we note that $Z_{11}(\omega_0)/Z_{22}(\omega_0) = C_2/C_1$, indicating that the two-port network should exhibit input and output impedances with the same frequency dependency, scaled by the ratio of the two parasitic capacitances. Furthermore, all impedance parameters have the same sign, which is dependent on $\omega_0^2 C_1 C_2 Z_0^2$. Assuming $\omega_0^2 C_1 C_2 Z_0^2 > 1$, all impedance parameters should be inductive. Based on these observations, we propose the transformer-based circuit shown in Fig. 5(b) as the impedance inverter. Using $Z_{11}(\omega_0) = j\omega_0 L_1$, $Z_{22}(\omega_0) = j\omega_0 L_2$, and $Z_{12}(\omega_0) = Z_{21}(\omega_0) = j\omega_0\, k_m \sqrt{L_1 L_2}$, the transformer's parameters are derived as

$$L_1 = \frac{C_2 Z_0^2}{\omega_0^2 C_1 C_2 Z_0^2 - 1} \tag{11}$$

$$L_2 = \frac{C_1 Z_0^2}{\omega_0^2 C_1 C_2 Z_0^2 - 1} \tag{12}$$

$$k_m = \frac{1}{\omega_0 \sqrt{C_1 C_2} Z_0}. \tag{13}$$

The transformer's turn ratio, $n_{tr} = \sqrt{L_1/L_2} = \sqrt{C_2/C_1}$, is dependent on ratio of the two parasitic capacitances. In the DPA, the width ratio of the peaking to carrier transistor is determined based on the desired output power back-off level for the efficiency peak, i.e., $W_p/W_c = N$, where the back-off level is $10\log_{10}(1+N)$ dB. As the parasitic capacitances are proportional to the widths of transistors,[2] the transformer's turn ratio is derived as $n_{tr} = \sqrt{N}$. For the case of symmetric DPA with a 6-dB back-off level, the transformer would have a unity turns ratio. Using (11)–(13), $L_{1,2}$ can be derived as

$$L_1 = \frac{k_m \sqrt{C_2/C_1}}{1 - k_m^2} \frac{Z_0}{\omega_0} \tag{14}$$

$$L_2 = \frac{k_m \sqrt{C_1/C_2}}{1 - k_m^2} \frac{Z_0}{\omega_0}. \tag{15}$$

Assuming that $C_2 = C_o$ and $C_1 = C_o/N$ (i.e., the output parasitic capacitance of the peaking transistor is denoted by C_o, which is N times larger than that of the carrier transistor), the total (summed) inductance is derived as

$$L_{T,TR} = \left(\sqrt{N} + \frac{1}{\sqrt{N}}\right) \frac{k_m}{1 - k_m^2} \frac{Z_0}{\omega_0}. \tag{16}$$

There is only one inductor in the low-pass impedance inverter network that is given by

$$L_{T,LP} = \frac{Z_0}{\omega_0}. \tag{17}$$

In order to make a fair comparison, it is assumed that in the case of high-pass circuit, the output parasitic capacitances

[2]Considering different biasing conditions of the peaking and carrier transistor, the ratio of their parasitic capacitances is not exactly equal to ratio of their widths. However, this is a minor effect, especially for the drain-source parasitic capacitances, and will be neglected in theoretical derivations.

of the transistors are compensated by extra parallel inductors $L_{p1} = N/\omega_0^2 C_o$ and $L_{p2} = 1/\omega_0^2 C_o$, which can be absorbed into the circuit inductance $L = Z_0/\omega_0$. Therefore, the total inductance is given by $L||L_{p1} + L||L_{p2}$, which can be expressed as

$$L_{T,HP} = \left(\frac{1}{1 + C_o/C} + \frac{N}{N + C_o/C}\right)\frac{Z_0}{\omega_0}. \tag{18}$$

The total inductance is dependent on the output parasitic capacitance $C_o/C = \omega_0 C_o Z_0$, and for $0 \leq C_o/C \leq 1$ it varies within 1–2× of Z_0/ω_0. Here, $C_o/C = 0.5$ is used in the simulations. In Fig. 6, the total inductance of the transformer-based impedance inverter is depicted versus the transformer's coupling coefficient. The results are shown for a symmetric DPA with $N = 1$. It is noted that for low coupling coefficients, the total inductance can be smaller than that of the conventional low-pass and high-pass circuits. This leads to a more compact chip area, which is important in MMIC implementations.

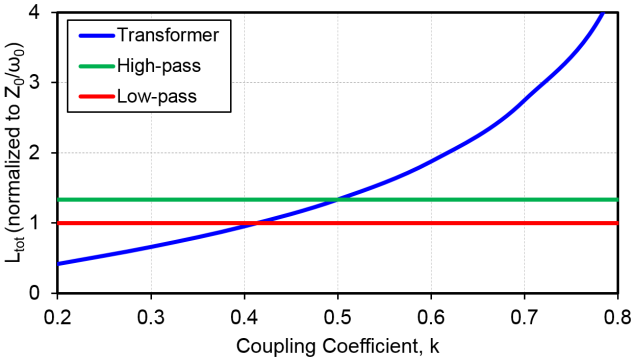

FIGURE 6. Comparison of the total inductance of the transformer-based impedance inverter [Fig. 5(b)] with conventional low-pass and high-pass circuits (Fig. 4).

Generally, the advantages of this circuit can be summarized as follows.

1) The required inductances can be smaller than in the conventional circuits.
2) Thanks to the three design parameters, L_1, L_2, and k_m, the required capacitances can be selected independently from the inductances. This allows the circuit to be realized without the need for extra capacitors.
3) The inductors can be used to provide a drain bias feed for the transistors.
4) The circuit can be used in asymmetric DPAs without the need for extra elements to balance the circuit.

C. LOAD MODULATION NETWORK FOR MMIC IMPLEMENTATION

For a MMIC implementation, the quarter-wavelength transmission lines of the broadband DPA architecture are replaced with their lumped-element equivalent circuits. By replacing $TL_{1,3}$ with the proposed transformer-based impedance inverter circuit of Fig. 5(b) and TL_2 with the high-pass circuit of Fig. 4, the load modulation network of the broadband DPA is obtained as shown in Fig. 7. The high-pass circuit is chosen so that the inductors L_3 can be absorbed into the transformers, leading to an even more compact circuit implementation. The drain bias voltage can be applied through the primary winding of the transformers.

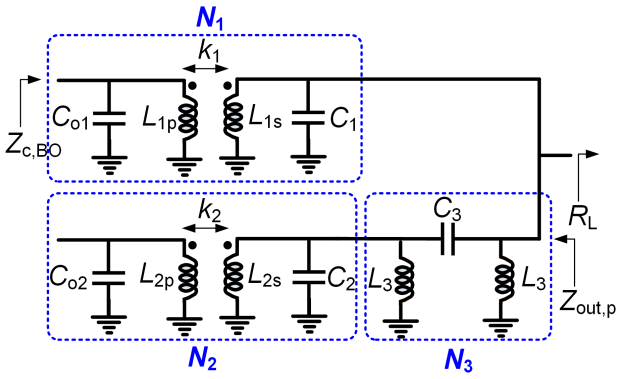

FIGURE 7. Transformer-based implementation of the load modulation network in the DPA with two-section peaking network.

We remap this circuit further such that it constrains the transformers to have only a 1:1 transformation ratio. These transformers can be implemented as edge-coupled microstrip transmission lines in MMIC processes, which usually feature wide bandwidth. As shown in Fig. 8, a transformer with a parallel inductor at its secondary winding can be transformed into a transformer with a unity transformation ratio and a series inductor at the primary. It can be shown that the elements of the two circuits can be related as

$$L = \frac{L_2 L_{par}}{L_2 + L_{par}} \tag{19}$$

$$L_{ser} = \frac{(1 - k^2)L_1 L_2 + (L_1 - L_2)L_{par}}{L_2 + L_{par}} \tag{20}$$

$$k' = \sqrt{\frac{L_1}{L_2}}k. \tag{21}$$

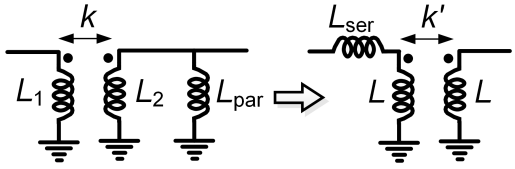

FIGURE 8. Circuit transformation used to simplify the transformer-based network.

Using this transformation, the load modulation network circuit is simplified as shown in Fig. 9, which is now more appropriate for a MMIC implementation. The circuit elements are calculated using (1)–(3), (11)–(13), and (19)–(21). There are two degrees of freedom in this system of equations which can be considered as the design parameters to maximize the bandwidth. We choose the coupling coefficients of the transformers $k_{1,2}$ as such design parameters.

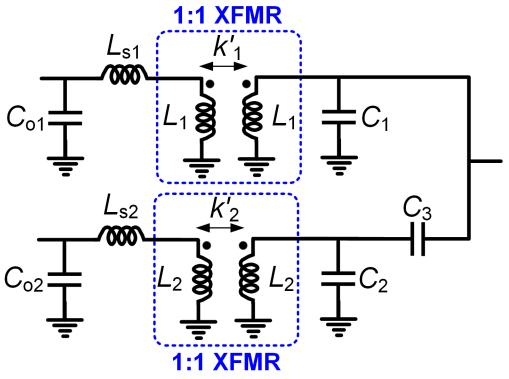

FIGURE 9. Simplified transformer-based load modulation network for MMIC implementation.

The impedance presented to the carrier amplifier at back-off $Z_{c,BO}$ can be derived using the circuit of Fig. 7. The two-port networks N_1–N_3 can be described by their impedance parameters. Using the input/output impedance of two-port networks in terms of their impedance parameters [27], $Z_{c,BO}$ is derived as

$$Z_{c,BO}(\omega) = Z_{11,N_1} - \frac{Z_{12,N_1}Z_{21,N_1}}{Z_{22,N_1} + R_L||Z_{out,p}} \tag{22}$$

where $Z_{out,p}$ is the output impedance of the peaking network given by

$$Z_{out,p} = Z_{22,N_3} - \frac{Z_{12,N_3}Z_{21,N_3}}{Z_{11,N_3} + Z_{22,N_2}}. \tag{23}$$

The impedance parameters of the networks N_1 and N_2 can be derived as ($i = 1, 2$)

$$Z_{11,N_i}(\omega) = \frac{x - x^3}{k_i^2/(1-k_i^2)x^4 - 2x^2 + 1 - k_i^2}\frac{j}{\omega_0 C_{oi}} \tag{24}$$

$$Z_{12,N_i}(\omega) = \frac{1/x}{k_i^2/(1-k_i^2)x^4 - 2x^2 + 1 - k_i^2}\frac{-j}{\omega_0 C_{oi}} \tag{25}$$

$$Z_{22,N_i}(\omega) = \frac{k_i^2(x - x^3)}{k_i^2/(1-k_i^2)x^4 - 2x^2 + 1 - k_i^2} j\omega_0 C_{oi} Z_{0i}^2, \tag{26}$$

and $Z_{21,N_i}(\omega) = Z_{12,N_i}(\omega)$, while for the network N_3

$$Z_{11,N_3}(\omega) = Z_{22,N_3}(\omega) = \frac{x - x^3}{1 - 2x^2} jZ_{03} \tag{27}$$

$$Z_{12,N_3}(\omega) = Z_{21,N_3}(\omega) = \frac{x^3}{1 - 2x^2} jZ_{03}, \tag{28}$$

where $x = \omega/\omega_0$ denotes the normalized frequency. Frequency response of the normalized impedance $Z_{c,BO}/R_{opt}$ is dependent on the transformers coupling coefficients and process-dependent parameters $\omega_0 R_{opt} C_{oi}$.

In Fig. 10, the real part of $Z_{c,BO}$ in the conventional and broadband DPA architectures is shown for different transformer coupling coefficients ($k_{1,2} = k$). The circuit parameters are assumed as $\omega_0 = 2\pi \times 5\,\text{GHz}$, $C_{o1} = C_{o2} = 0.4\,\text{pF}$, $R_{opt} = 100\,\Omega$, and $m = 1$ (i.e., $Z_{01,02,03} = R_{opt} = 2R_L$). In the broadband DPA, increasing the coupling coefficient k

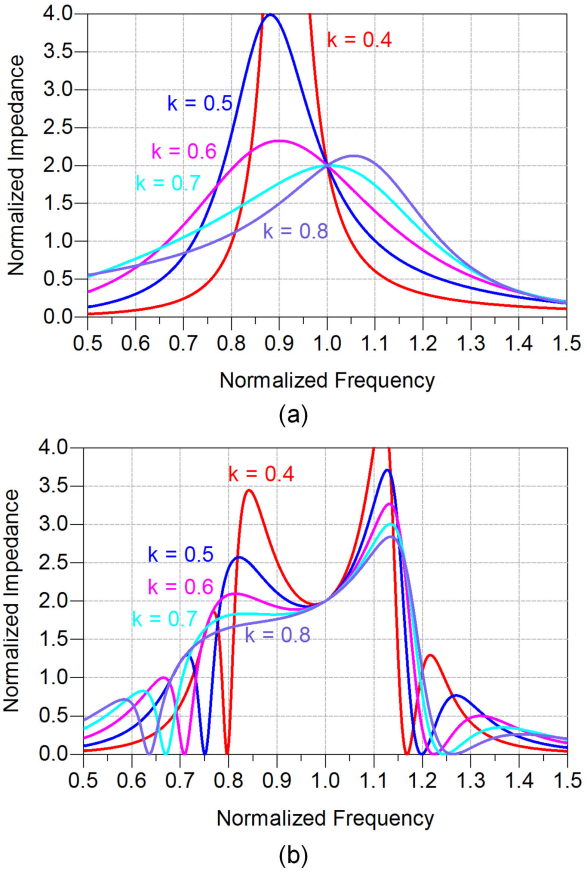

FIGURE 10. Real part of the impedance presented to the carrier amplifier at back-off for different transformer coupling coefficients: (a) conventional DPA and (b) broadband DPA. (The transformer coupling coefficient and the normalized impedance range are limited to practical values.)

causes its bandwidth to initially widen; but then it narrows for larger values of k (e.g., from 0.7 to 0.8). Therefore, the maximum bandwidth is achieved for moderate coupling coefficients (e.g., 0.6). In Fig. 11, fractional bandwidth of the conventional and broadband DPAs is plotted versus the

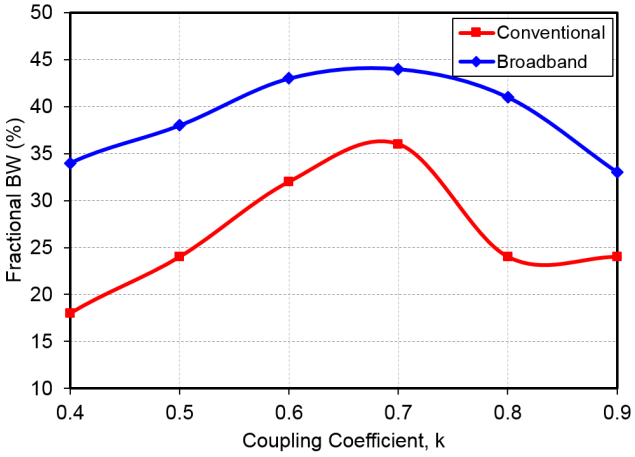

FIGURE 11. Fractional bandwidth of the conventional and broadband DPAs at back-off versus transformer coupling coefficient.

transformer coupling coefficient. For $k = 0.7$, fractional bandwidth of the broadband DPA is achieved as 44%.

Insertion loss of the load modulation network degrades efficiency of the DPA, especially at back-off where the impedance transformation ratio is larger. Assuming that all inductors have the same quality factor, Q, insertion loss of the conventional and broadband load modulation networks at back-off and center of the frequency band versus transformer coupling coefficient is shown in Fig. 12. The insertion loss is decreased with increasing the coupling coefficient. The broadband load modulation network exhibits much lower insertion loss for small coupling coefficients (e.g., $k \leq 0.5$), while its insertion loss is slightly higher for large coupling coefficients (e.g., $k \geq 0.7$).

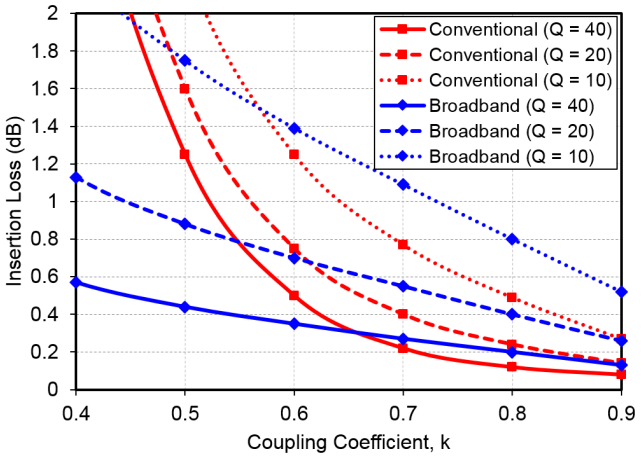

FIGURE 12. Insertion loss of the conventional and broadband load modulation networks at back-off versus transformer coupling coefficient, for different Q of inductors.

It should be noted that choosing a high coupling coefficient would lead to large total inductance (Fig. 6). Moreover, parasitic capacitive coupling between the primary and secondary of the transformer can degrade the bandwidth. Therefore, a moderate coupling coefficient (e.g., $0.6 \leq k \leq 0.8$) should be chosen to achieve wide bandwidth and low insertion loss while saving the chip area.

The two transformers have different roles in the load modulation network. The transformer of the carrier amplifier path transforms the load impedance into the optimum load impedance of the carrier amplifier at back-off, while the transformer in the peaking amplifier path mitigates effects of the parasitic capacitance of the peaking transistor on the DPA bandwidth. Therefore, their optimal coupling coefficients can be different. In Fig. 13, contours of the fractional bandwidth are shown versus the coupling coefficients (k_1, k_2). The maximum bandwidth is achieved for $0.6 \leq k_1 \leq 0.7$ and $0.7 \leq k_2 \leq 0.8$. In Fig. 14, contours of the insertion loss are shown versus (k_1,k_2). The insertion loss is mainly determined by k_1 and is almost independent of k_2. This is consistent with the fact that output power at back-off is delivered through the carrier path's transformer to the load resistance.

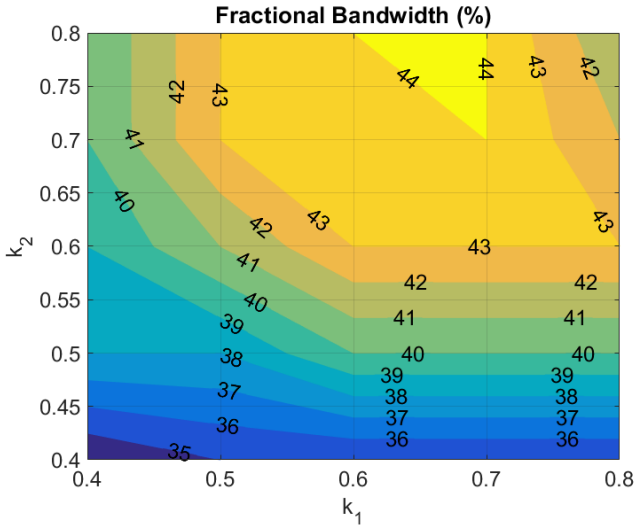

FIGURE 13. Fractional bandwidth of the broadband DPA at back-off versus coupling coefficients of the transformers.

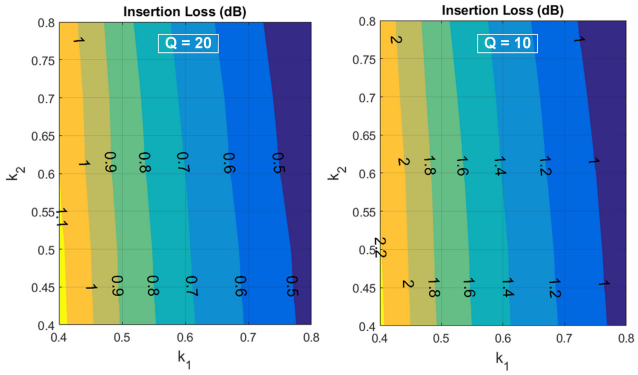

FIGURE 14. Insertion loss of the broadband load modulation network at back-off versus coupling coefficients of the transformers (for inductors' Q of 10 and 20).

In practice, the coupling coefficients should be optimized in the layout design where effects of the parasitic capacitances and resistances of the transformers are considered.

III. CIRCUIT DESIGN

In this section, we present circuit design of a broadband DPA using the proposed load modulation network. A symmetric DPA architecture with peak efficiency at 6-dB back-off is designed for a target frequency band of 4.5–6.0 GHz. The DPA circuit schematic is shown in Fig. 15.

A. OUTPUT NETWORK

The width of transistors in this 0.25-μm GaN MMIC process can be chosen to achieve an optimum load resistance of 100 Ω in order to simplify the output network of the DPA. The gate width of 8×75 μm leads to $R_{opt} \approx 100\,\Omega$. The drain-source parasitic capacitance is estimated as 0.4 pF. The process offers stacked double-metal transmission lines with total thickness of 5 μm over a 100-μm substrate. The coupling

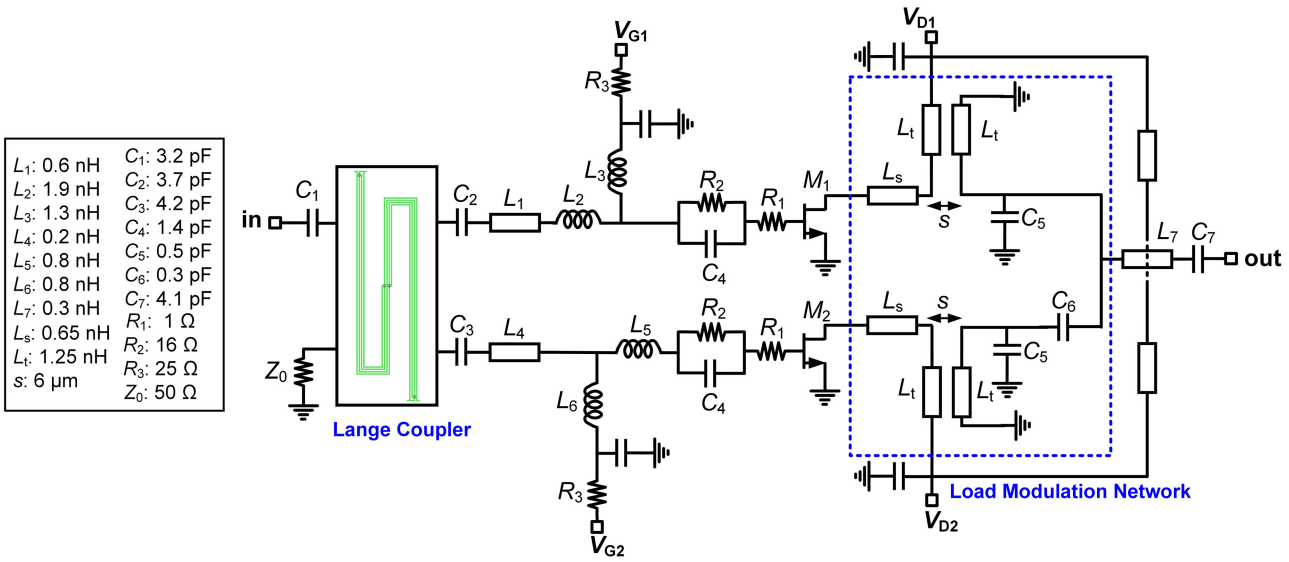

FIGURE 15. The DPA circuit schematic.

coefficient of two edge-coupled microstrip transmission lines versus their spacing is plotted in Fig. 16. The maximum coupling coefficient that can be achieved in this process is 0.7, which is limited by the 5 μm minimum spacing rule of metal layers.

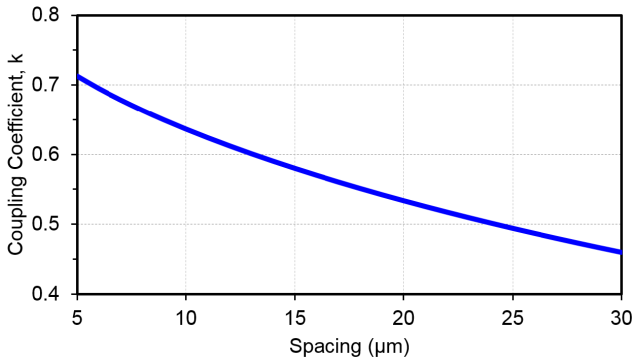

FIGURE 16. Coupling coefficient of the edge-coupled microstrip transmission lines versus their spacing in the GaN MMIC process.

The circuit of Fig. 9 is designed using the developed procedure and is optimized based on EM simulations. The coupling coefficient of the transformers is 0.64 (6-μm line spacing). The inductance values are extracted as $L_{s1,s2} = 0.52$ nH and $L_{1,2} = 1.12$ nH, while their quality factor is estimated as $Q_{s1,s2} = 26$ and $Q_{1,2} = 20$.

B. INPUT NETWORK

The input network of the broadband DPA architecture in Fig. 2 is composed of a power splitter and a quarter-wavelength transmission line providing a 90° phase shift. The input impedance of the amplifiers should be matched to 50 Ω. The power division and phase shift functions can be merged by using a quadrature hybrid circuit, e.g., a branch line coupler or Lange coupler. We use a Lange coupler for its broadband response and compatibility with MMIC. Standard Lange coupler includes quarter-wavelength transmission lines which in the targeted frequencies are too long to fit within the chip. We use a meandered structure, shown in Fig. 17, for a compact implementation. The physical dimensions w, s, d, and $l_{1,2}$ are tuned based on EM simulations to achieve the desired broadband performance. In this design, $l_1 = 1600$ μm, $l_2 = 1400$ μm, $d = 150$ μm, and $w = s = 10$ μm. Simulation results indicate that the Lange coupler provides 91°–93° phase shift with < 0.9 dB insertion

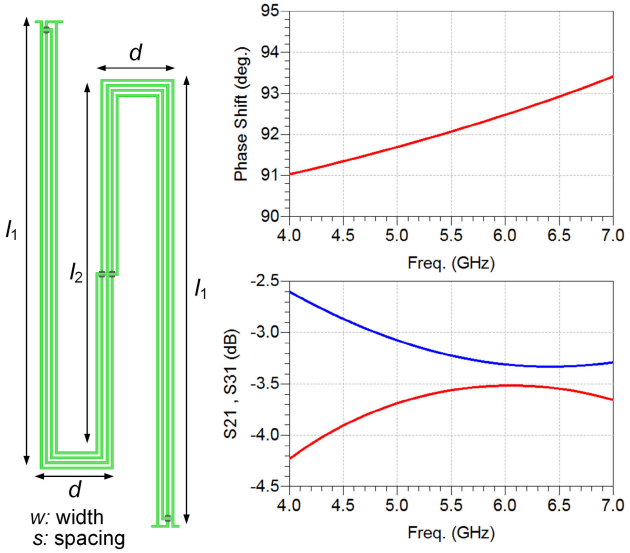

FIGURE 17. Physical structure of the meandered Lange coupler and its broadband phase and amplitude frequency responses.

loss, and 0.2–1.0 dB amplitude mismatch over 4.5–6.5 GHz bandwidth. Input matching networks of the transistors are realized using lumped and distributed circuit elements.

C. DPA SIMULATION RESULTS

The two drain bias pads of the DPA circuit in Fig. 15 are internally connected so that the DPA would need only one supply voltage, $V_D = 28$ V. The DPA is biased at $V_{G1} = -2.5$ V, $V_{G2} = -4.5$ V. Large-signal simulation results are shown in Fig. 18, where power gain and DE are plotted versus output power in the frequency band of 4.5–6.0 GHz. The efficiency behaves similarly as in the ideal DPA at the center of band, but it deviates at the edges of the band. At 5.5 GHz, DE is 50.6% at peak output power of 36.5 dBm, while degrading to 36.5% at 6-dB power back-off. The back-off efficiency enhancement over the class-B is 1.44, which is lower than that of the ideal DPA (i.e., 2). This is usual in integrated circuit implementations mainly due the limited bandwidth of the load modulation network, higher losses of the load modulation network at back-off, and nonzero current of the peaking transistor. The power gain is 7.5 dB at peak power and 9.0 dB at back-off.

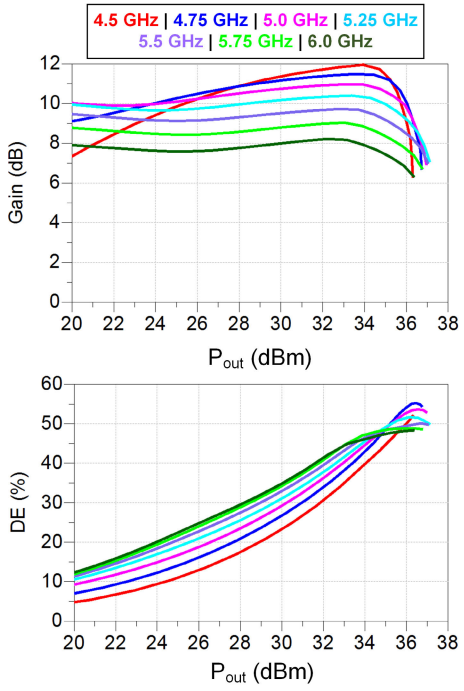

FIGURE 18. Simulated power gain and DE versus output power in the frequency band 4.5–6.0 GHz.

IV. MEASUREMENT RESULTS

The DPA is fabricated using the 0.25-μm GaN-on-SiC process from WIN Semiconductors. The chip shown in Fig. 19 occupies 3.0 × 2.8 mm^2 area. The chip is wire-bonded to a test printed circuit board (PCB). The transistors are biased at the 28-V drain voltage, while their gate voltages are adjusted based on the efficiency and linearity requirements.

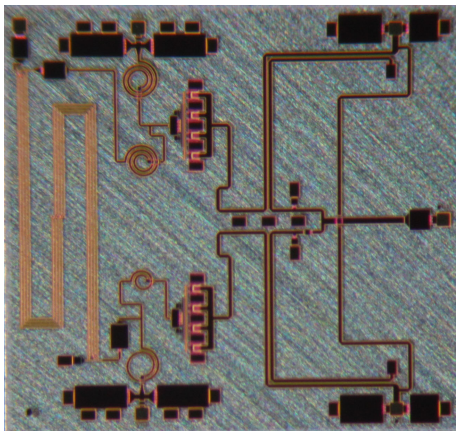

FIGURE 19. Chip micrograph (3.0 mm × 2.8 mm).

A. CW MEASUREMENTS

For CW measurements, the DPA is biased at $V_{G1} = -2.4$ V, $V_{G2} = -4.0$ V, and $V_D = 28$ V. The gate biases are tuned such that the DPA achieves the best back-off efficiency improvement. A driver amplifier is used at the input of the DPA to provide the required input power level. The measurements are performed up to 6 GHz due to the limited bandwidth of the driver stage.

In Figs. 20–22, the measured and simulated gain, DE, and PAE are shown versus output power. The measured maximum gain ranges from 7.6 dB to 11.6 dB. The peak output power measured at 2–3 dB gain compression is 35–36 dBm. DE is within the range of 42.8–48.7% at peak power and 24.4–31.6% at 6-dB back-off. PAE is measured at 31.8–40.7% at peak power and 22.5–27.6% at 6-dB back-off. The back-off efficiency enhancement over the class-B is within 1.22–1.62 (compared to 2 for an ideal DPA). In Fig. 23, measured DE and PAE are shown versus frequency at peak power and 6-dB back-off.

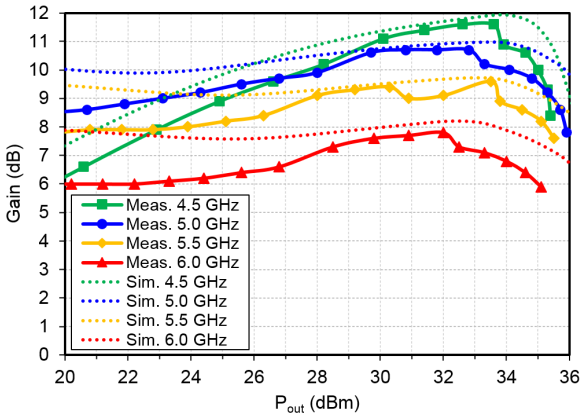

FIGURE 20. Measured and simulated gain versus output power.

B. MODULATED-SIGNAL MEASUREMENTS

In the modulated-signal measurements, a 64-QAM input signal with 100-MHz modulation bandwidth and 8.06 dB PAPR is applied to the DPA. In Fig. 24, the measured error vector

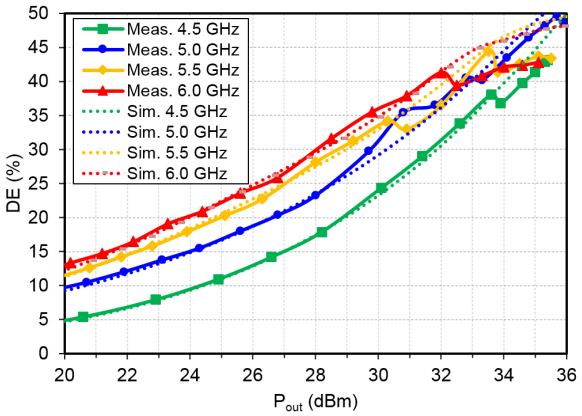

FIGURE 21. Measured and simulated DE versus output power.

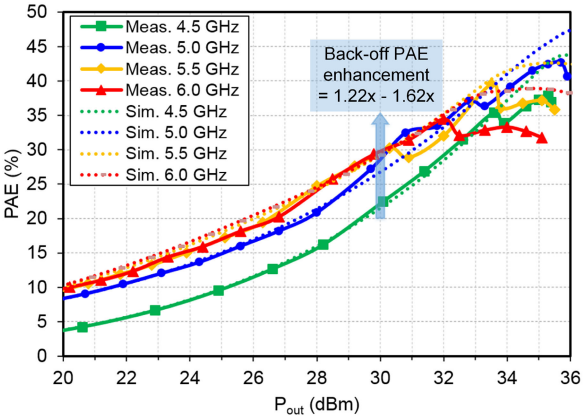

FIGURE 22. Measured and simulated PAE versus output power.

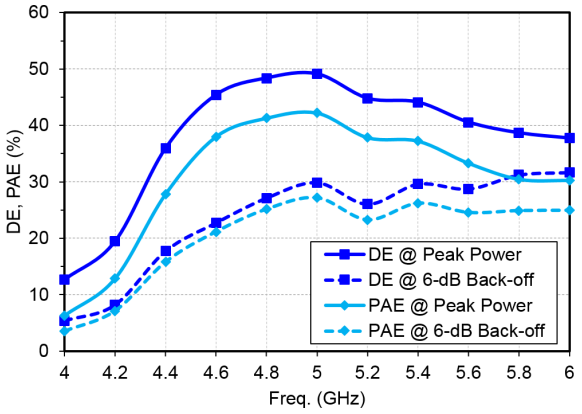

FIGURE 23. Measured DE and PAE versus frequency at peak power and 6-dB back-off.

magnitude (EVM), average PAE, and adjacent channel leakage ratio (ACLR) are shown versus the average output power for different gate bias voltages of the carrier transistor. Here, ACLR is reported as average of the relative power leakage into the lower and upper adjacent channels. The peaking transistor is biased at −4.0 V. It is observed that by choosing an appropriate gate bias voltage for the carrier transistor,

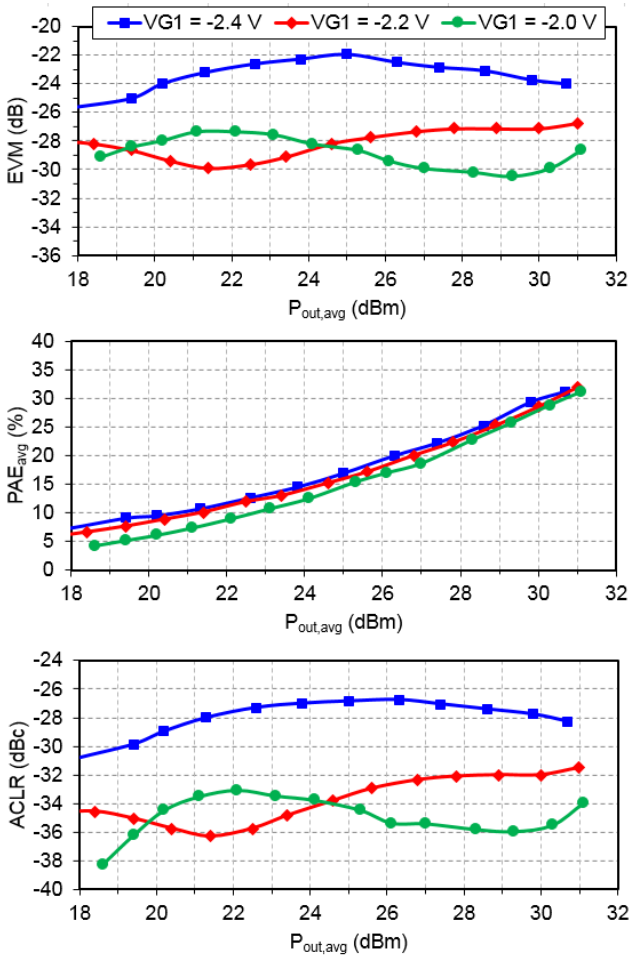

FIGURE 24. Measured EVM, average PAE, and ACLR versus average output power for different gate bias voltages of the carrier transistor. A 64-QAM signal with 100-MHz modulation bandwidth and 8.06 dB PAPR at 5.0 GHz is used in the test.

i.e., −2.0 V, EVM and ACLR can be improved by 4.6 dB and 5.7 dB, respectively. This has a negligible effect on the average efficiency. This feature is a result of the nonlinearity cancellation of the peaking and carrier transistors which are biased in the class-C and class-AB modes [28]. Using the gate bias of −2.0 V for the carrier transistor, EVM of −28.6 dB (3.7%), average PAE of 31.1 dBm, and −34 dBc ACLR can be achieved at 31 dBm average output power.

In Fig. 25, the measured output constellation and spectrum are shown for the 64-QAM input signal. The gate biases of the carrier and peaking transistors are respectively chosen as −2.0 V and −4.0 V. An EVM of −30.5 dB (3%) is achieved at 29.3 dBm average output power and 25.7% average PAE.[3]

C. PERFORMANCE COMPARISON

In Table 1, the performance of the designed DPA is compared with broadband GaN MMIC DPAs reported in the literature.

[3]It is noted that the EVM and ACLR are measured without using any predistortion. Further linearity improvements can be achieved by adopting digital predistortion (DPD).

TABLE 1. Comparison of broadband GaN MMIC Doherty power amplifiers.

	This Work	[12]	[13]	[14]	[15]	[16]	[17]
Bandwidth (GHz)	4.5–6.0	2.1–2.7	6.8–8.5	5.8–8.8	5.1–5.9	6.6–7.3	4.5–5.2
Fractional BW (%)	28.9	25.2	22.4	42.0	14.6	10.1	14.5
$P_{out,PP}$ (dBm)	35–36	40–41	34.5–35.5	35–36	36.0–38.7	38	40.4–41.2
DE @ PP (%)	42.8–48.7	—	—	—	—	—	55–63
PAE @ PP (%)	31.8–40.7	—	38–50	30–45	43.2–47.3	47.5	45–51
BO Level (dB)	6	7.6	9	9	6	7	6
DE @ BO (%)	24.4–31.6	48–62	—	—	—	—	47–50
PAE @ BO (%)	22.5–27.6	—	24–37	31–39	31.6–49.5	41	40–45
Gain (dB)	7.6–11.6	12–14	4–14	8.5–9	14.4–17.3	10	7–9
Modulation	64-QAM	LTE	256-QAM	256-QAM	64/256-QAM	—	LTE
Mod. BW (MHz)	100	10	10	20	80	—	40
PAPR (dB)	8	7.2	7.8	8.5	—	—	7.7
Carrier Freq. (GHz)	5.0	2.14–2.65	6.8–8.5	7.0	5.8	—	4.9
EVM (dB)	−30.5	—	—	—	−28/−32	—	—
$P_{out,avg}$ (dBm)	29.3	—	27.3–27.7	27.6	23.5/21.5	—	33.0
PAE_{avg} (%)	25.7	43–50	35–42	35.2	—	—	43
Chip Area (mm×mm)	3.0×2.8	2.65×1.9*	2.1×1.5	2.9×2.9	2.5×1.6	4.8×4.6	2.2×2.1
GaN Process (μm)	0.25	0.25	0.25	0.25	0.25	0.25	0.25

*Partially off-chip output matching network is realized using inductance of bond wires.

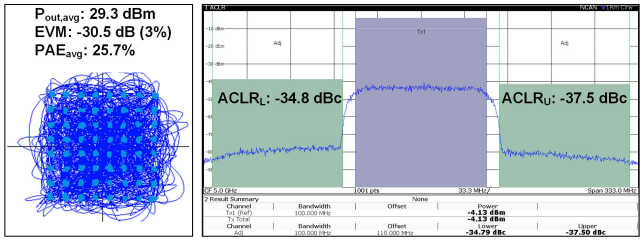

FIGURE 25. Measured output constellation and spectrum for a 64-QAM signal with 100-MHz modulation bandwidth and 8.06 dB PAPR at 5.0 GHz.

The bandwidth is defined based on the 1 dB drop in output power in cases where enough measured data is available. Our DPA reaches a wide fractional bandwidth of 28.9% thanks to the developed load modulation network. A wider bandwidth (42%) was only reported in [14], which was realized in TriQuint 0.25-μm GaN MMIC process, although it was tested with a maximum modulation bandwidth of only 20 MHz. The DPA efficiency is comparable with that in other designs. However, a low EVM of −30 dB has been achieved for a 64-QAM signal with wide modulation bandwidth of 100 MHz and PAPR of 8 dB. This can be compared with −28 dB EVM at center of the bandwidth reported in [15] for an 80-MHz 64-QAM signal. However, its average efficiency was not reported to make a comparison.

V. CONCLUSION

In this paper, we presented a bandwidth enhancement technique for monolithic microwave integrated circuit (MMIC) Doherty power amplifiers (DPAs). It was shown that a quarter-wavelength impedance inverter can be realized using two transformer-coupled microstrip transmission lines and output parasitic capacitance of transistors. The circuit was used to realize a broadband load modulation network for DPAs. This network includes two transformers that are used to improve frequency response of the load impedance presented to the carrier transistor at back-off and extend the DPA bandwidth. A proof-of-concept DPA, designed and implemented using a GaN MMIC process, achieved drain efficiency of 42.8–48.7% at peak power and 24.4–31.6% at 6-dB back-off, over the frequency band of 4.5–6.0 GHz (28.9% fractional bandwidth).

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