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A New Floating and Tunable Capacitance Multiplier With Large Multiplication Factor

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ABSTRACT This paper presents a CMOS floating and tunable capacitance multiplier with a very large multiplication factor. The proposed design uses CCII and OTAs designed using MOSFETs biased in subthreshold region to provide low power consumption and high multiplication factor. TANNER TSPICE simulation tool is used to confirm the functionality of the design in 0.18μm TSMC CMOS technology. The circuit is powered using $\pm$0.75V DC supply voltage. Simulation results indicate that the maximum multiplication factor is 3600 and the maximum error is 8.6%.

INDEX TERMS Impedance multiplier, filters, biomedical circuits, high multiplication factor, tunable.

I. INTRODUCTION

System integration has been a common practice over the years to satisfy the appealing of reducing the size of the devices and to achieve portability. In low frequency applications, such as biomedical circuits where large time constant is needed, large capacitors or resistors are needed which is impractical to implement in integrated circuits (ICs). The common approach for solving this issue is to use capacitance multiplier where small initial capacitance is scaled up using circuit that uses less chip area compared to direct implementation of passive components. Simulated capacitance can be grounded or floating depending on the intended application.

As the technology advances more transistors can be fabricated in a small area except for the passive elements. The impedance values of passive elements are still directly proportional to the silicon area. On the top of that, if a high value impedance is required for an example a 1.0nF capacitor, it will occupy 1mm^2 of silicon area in 0.18μm CMOS process technology [1]. This becomes impractical to fabricate in an IC chip because of the huge area required.

Capacitance multiplier is a useful technique where the integration of large time constant is required. Over the years, many circuits have been designed using different techniques [2]–[10], [10]–[15]. Temperature insensitive/electronically controllable floating capacitance simulators based on DV-CCTA is presented in [2]. This design uses two passive elements and consumes large power. A differential voltage current conveyor (DVCC) based floating capacitance multiplier designs are presented in [3] and [4]. The two designs have limited scaling factor, large bias current (100μA) and extra passive element. Another floating capacitance multiplier circuit using full-balanced voltage differencing buffered amplifiers (FB-VDBAs) is reported in [5]. It requires high bias current (50μA), has limited scaling factor and designed using BiCMOS technology. An electronically controllable capacitance multiplier circuit with temperature compensation utilizing OTA is presented in [6]. This design has a high multiplication factor; however, the OTAs are designed using BJT which is not preferable today. The design presented in [7] uses extra passive element which renders this design to have large silicon area. Tunable capacitance simulators using VDCC are reported in [8] and [9]. Both designs require extra passive elements which is not suitable in integrated circuits and the bias current is around 100μA which leads to high power consumption. Another design uses differential unity gain amplifier to implement a floating impedance scaling circuit [10]. It is a simple design, but it lacks the tunability for the multiplication factor since it depends on transistor aspect ratios. The designs presented in [11] and [12] have extra passive elements which will require large silicon area. Other designs in [13] and [14] uses large bias currents which lead to high power consumption. The design in [10] lacks the tunability.

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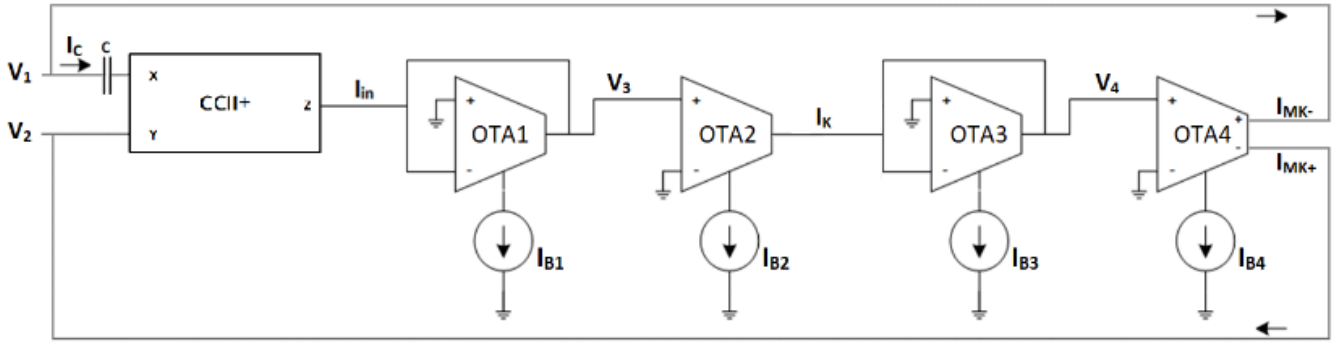

FIGURE 1. Proposed circuit for the floating capacitance simulator.

This paper presents a new CMOS floating and tunable capacitance multiplier with large multiplication factor low power consumption without using any extra passive elements.

II. PROPOSED CIRCUIT

The proposed floating capacitance multiplier is shown in Fig. 1, it consists of a CCII+ and two multiplication stages. The first stage of multiplication formed using of OTA1 and OTA2 while the second stage is formed using OTA3 and OTA4. The circuit diagram for the DO-OTA and OTA are shown in Fig. 2 and Fig. 3 respectively.

With reference to Fig. 1.

$$I_{in} = I_C \tag{1}$$

The voltage V_3 is given by:

$$V_3 = \frac{1}{g_{m1}} * I_{in} = \frac{2nV_T}{I_{B1}} * I_C \tag{2}$$

where n is the transistor slope factor, V_T is the thermal voltage and I_{B1} is the bias current for OTA1.

The current I_K is given by:

$$I_K = g_{m2}V_3 = \frac{I_{B2}}{I_{B1}} * I_C = K * I_C \tag{3}$$

where $K = I_{B2}/I_{B1}$ and I_{B2} is the bias current for OTA2. The voltage V_4 is given as.

$$V_4 = \frac{1}{g_{m3}} * I_K = \frac{2nV_T}{I_{B3}} * K * I_C \tag{4}$$

The output currents I_{MK+} and I_{MK-} are given as.

$$I_{MK+} = -I_{MK-} = g_{m4}V_4 = \frac{I_{B4}}{I_{B3}} * K * I_C = M * K * I_C \tag{5}$$

where $M = I_{B4}/I_{B3}$, the I_{B3} and I_{B4} are the bias currents for OTA3 and OTA4 respectively.

The total impedance Z_{eq} seen between the terminals V_1 and V_2 is given by:

$$Z_{eq} = \frac{V_1}{I_{MK-} + I_C} - \frac{V_2}{I_{MK-}} = \frac{V_1}{I_C\,(1 + M * K)} - \frac{V_2}{I_C * M * K} \tag{6}$$

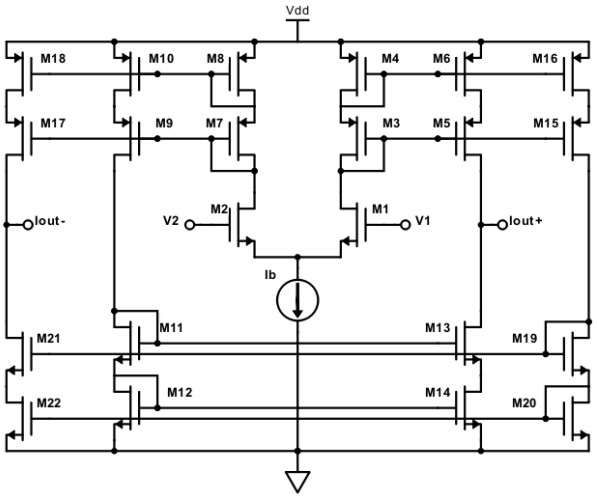

FIGURE 2. Circuit diagram for DO-OTA.

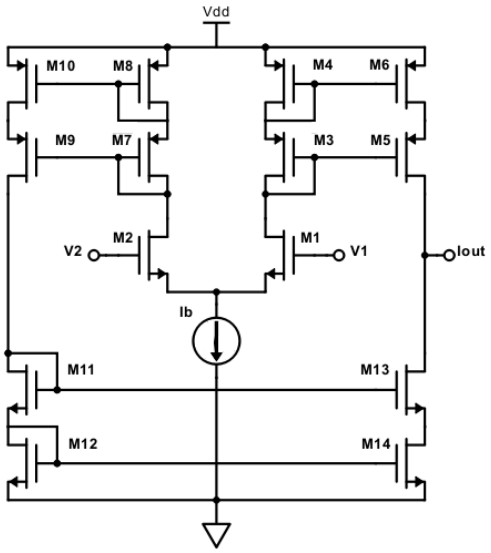

FIGURE 3. Circuit diagram for OTA.

Since $M * K \gg 1$, then equation (6) is written as:

$$Z_{eq} = \frac{V_1 - V_2}{I_C * M * K} \tag{7}$$

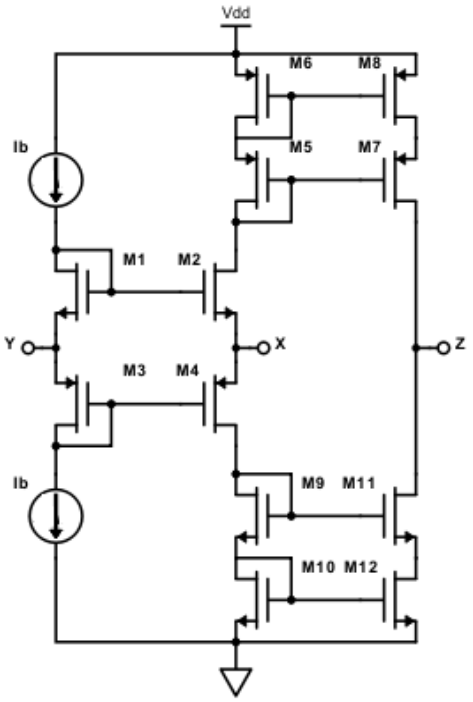

FIGURE 4. Circuit diagram for the CCII+.

The CCII+ internal circuit is shown in Fig. 4, and the function of the CCII+ is given as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{8}$$

From Fig 1, the current I_C is given as:

$$I_C = \frac{V_1 - V_2}{Z_C} \tag{9}$$

where Z_C is the impedance of the capacitor C. Combining equations (9) and (7). The total equivalent impedance is given by:

$$Z_{eq} = \frac{V_1 - V_2}{\frac{V_1 - V_2}{Z_C} * M * K} = \frac{Z_C}{M * K} \tag{10}$$

Replacing the impedances Z_C with 1/sC, equation (10) is written as:

$$Z_{eq} = \frac{1}{sC * M * K} \rightarrow C_{eq} = C * M * K \tag{11}$$

The relation in equation (11) describes a capacitance simulator with two scaling factors M and K and hence, high scaling factor can be achieved. The tuning capability is evident through the bias currents of the OTAs. The design is passive-less to ensure the ability to be fabricated using CMOS technology with less silicon area. All the transistors in this proposed design are biased to work in subthreshold region which results in a low power consumption.

The previous analysis and resulted equations were carried out based on the assumption that the CCII and OTA are ideal. In this section, the non-ideal effect of these blocks will be analyzed. For the CCII, the non-ideal relationship is shown in the following equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & R_X & 0 \\ 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{12}$$

where α is the voltage coefficient and β is the current coefficient. From the circuit in Fig 1, since the equivalent impedance of the capacitor is much higher than R_X, hence the $Z = 1/sC$ with C is equal 3pF results in a very low current I_X, so the effect of the second term will be neglected, so we conclude that:

$$V_X = \alpha V_Y \quad I_Z = \beta I_X \tag{13}$$

For OTA4, it is assumed that both the output currents are equal in magnitude, however, the non-ideal relation is given as:

$$I_{MK+} = \gamma I_{MK-} \tag{14}$$

Using the above non ideal relations, the equivalent impedance is given by:

$$Z_{eq} = \left(\frac{V_1 - \gamma V_2}{V_1 - \alpha V_2}\right) \frac{Z_C}{\gamma * \beta * M * K} \tag{15}$$

The percentage of error is:

$$\%\text{Error} = \left| \left(\frac{V_1/V_2 - \gamma}{V_1/V_2 - \alpha} \right) \beta - 1 \right| * 100 \tag{16}$$

As the modified CCII includes cascode current mirrors in the output stage, the current following error parameter β will be nearly 1, the same concept applies to OTA4s̀ γ parameter. A total error if 1.11% can be found if $V_1 = 10$mV, $V_2 = 1$mV, $\beta = 0.99$ and $\gamma = 0.98$ and $\alpha = 0.97$

III. SIMULATION RESULTS AND APPLICATIONS

The functionality of the proposed floating capacitance multiplier is confirmed using TANNER TSPICE simulator with 0.18μm TSMC CMOS technology. The bias currents I_b, I_{B1} and I_{B3} are set to 5nA. The bias current I_{B2} is kept at 300nA to keep the multiplication factor K = 60 and the bias current I_{B4} is swept from 5nA to 300nA to achieve a multiplication factor M from 1 to 60, and hence the total multiplication factor will be swept from 60 to 3600. The circuit is operated from $\pm 0.75V$ DC supply voltage. The initial capacitor C is 3pF. The expected capacitance range should be between 0.18nF to 10.8nF. The transistors aspect ratios used in simulation are listed in Table 1.

To verify the frequency range of the design, a plot of the simulated impedance of the proposed circuit and the theoretical value is shown in Fig. 5 for a total multiplication factor of 3600. It is evident from the plot that the working frequency range is between 1mHz and 5KHz. The scaled total capacitance values have been calculated for both the ideal and simulated results and are shown in Table. 2 and Fig. 6. It is clear that the maximum error is 8.5% when the scaling factor is 3600.

TABLE 1. The aspect ratios of the transistors for the proposed floating capacitance.

Block	Transistor	W/L
CCII	M1 – M4	1μm / 0.5μm
	M5 – M8	1.2μm / 0.3μm
	M9 – M12	0.9μm / 0.45μm
OTA	M1 – M2	15.0μm / 0.3μm
	M3 – M10	4.0μm / 0.8μm
	M11 – M14	3.8μm / 0.9μm
DO-OTA	M15 – M18	4.0μm / 0.8μm
	M19 – M22	3.8μm / 0.9μm

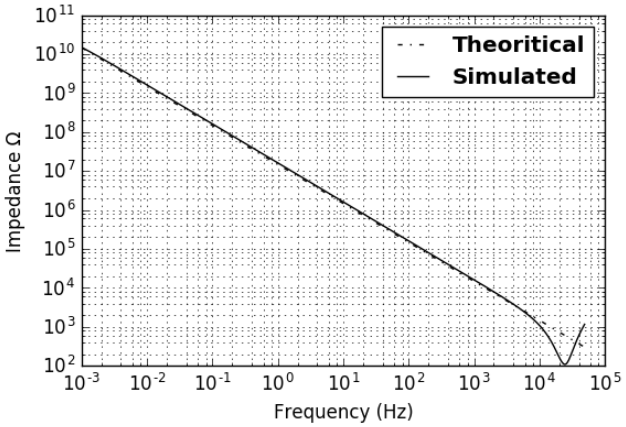

FIGURE 5. The impedance of the proposed floating capacitance simulator for M = 60 and K = 60.

TABLE 2. Capacitance deviation between the theoretical and simulated once at several multiplication factors.

M = 60		Expected value of Capacitance (nF)	Simulated value (nF)	% of Error
K	Multiplied Factor			
1	60	0.18	0.176	2.453
2	120	0.36	0.347	3.661
4	240	0.72	0.687	4.555
8	480	1.44	1.363	5.357
16	960	2.88	2.701	6.220
32	1920	5.76	5.341	7.268
60	3600	10.8	9.885	8.475

The power consumption recorded by the simulator is 2.301μW for a total multiplication factor of 3600 and 0.336μW for a total multiplication factor of 60.

Simulation results for temperature analysis was carried out. The temperature is swept from −25C° to 80C° in steps of 20C°. The simulation result for the equivalent impedance with total multiplication factor of 3600 is shown in Fig. 7.

It is evident that the total capacitance is insensitive to the temperature variation since all the temperature related parameters cancelled each other.

The performance of the proposed floating capacitance simulator is compared with previous works and is summarized in TABLE 3.

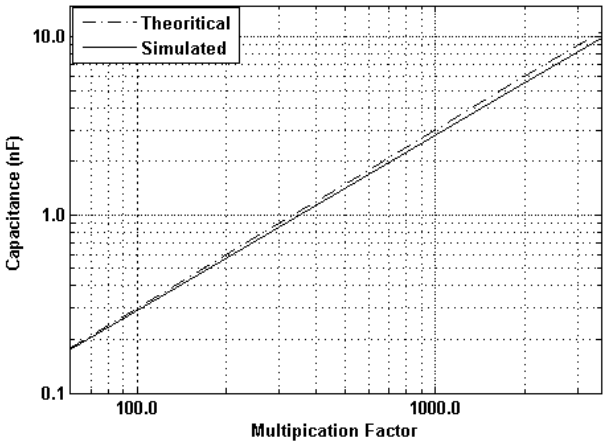

FIGURE 6. Variations between the simulated and expected values for the floating capacitance.

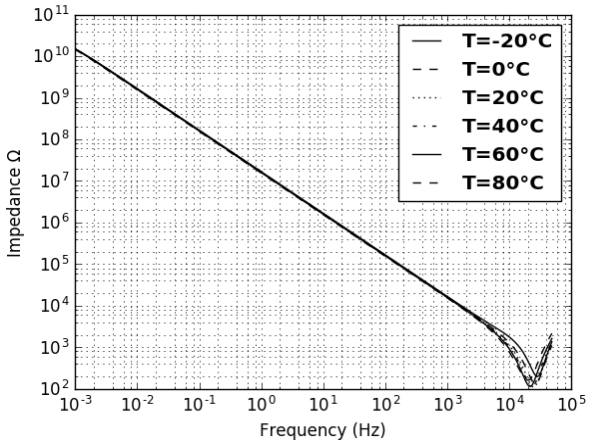

FIGURE 7. Simulation result for temperature analysis for multiplication factor of 3600.

To test the performance of the proposed floating capacitance simulator, a simple high-pass filter is used as illustrated in Fig 8. The resistance RH for the high-pass filter is 1MΩ. Plots of the frequency response of the filter using ideal and simulated capacitance for different multiplication factor is shown in figure 9. It is evident from the figure that the simualte and the ideal capciatnce are in close agreement.

The suitable applications for such tunable capacitors are biomedical ones, since biomedical signals are time records of biomedical events like heart movements or stimulated neuron. When biomedical signals are produces, an electric potential is generated that can be measured such as Electroencephalogram (EEG) and Electrocardiogram (ECG). Large amplification for such signals is necessary since the electric potential generated from the body is in range of micro to millivolt range. Pre-filtering is needed using analog filters to attenuate undesired high frequency noise as ECG signals occupy a frequency bandwidth 1mHz -100Hz while EEG occupy 10mHz – 30Hz17, hence the need of this work to design such filters.

TABLE 3. Performance comparison between the proposed circuit and previous ones.

Reference	Building Block	Type	Supply Voltage	Power Consumption	Technology	# of passive elements	Tunable?	Scaling Factor
[2]	DV-CCTA	F	±2.5V	NA	BJT	2	Yes	3
[3]	DVCC	F	±0.75V	1.29mW	0.13µm	2	Yes	20
[4]	DVCCTA	F	±2V	3mW	0.5µm	1	Yes	3
[5]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[6]	OTA	F	±2.5V	0.565mW	BJT	0	Yes	100000
[7]	OTA	F	NA	0.5µW	0.35µm	1	Yes	NA
[8]	VDCC	F	±0.45V	556µW	90nm	2	No	NA
[9]	VDCC	F	±0.9V	NA	0.18µm	2	Yes	NA
[10]	CMOS	F	±0.9V	53.2µW	0.18µm	0	No	50
[11]	CMOS	F	±3V	5.28mW	0.5µm	3	Yes	10
[12]	DVCC	F	±0.2.5V	NA	0.25µm	0	Yes	15
[13]	CBTA	F	±1.5V	43.3mW	0.25µm	2	NA	NA
[14]	FB-VDBA	F	±1V	NA	BiCMOS	0	Yes	3
[15]	CMOS	F	1.8V	5.94µW	0.18µm	0	No	50
Proposed Work	OTA CCII	F	±0.75V	2.030µW	0.18µm	0	Yes	3600

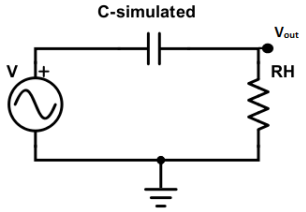

FIGURE 8. Simple high-pass filter.

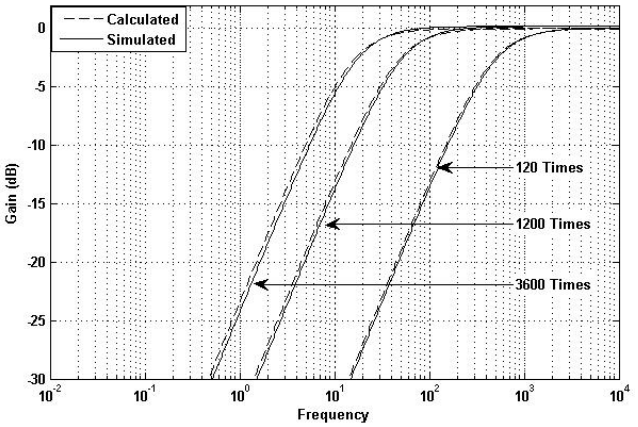

FIGURE 9. Simulation of the high-pass filter circuit with total scaling factor of 120, 1200 and 3600.

The tunable capacitors are needed in the amplification stage for controlling the gain of biomedical signals such as Chopper stabilization which is an established for suppressing offsets and drifts coming from neuro field potentials (NFP) [17]. Tunable capacitors are also needed in biomedical sensor interface as implants to measure and process NFP. This interface is called analog front-end (AFE) [18]. Tunable filters are achieved with tunable capacitors and are generally used in any typical data acquisition for biomedical signals [19].

IV. CONCLUSION

In this paper, a wide tunable floating capacitance multiplier design has been presented. The design utilizes two stages of multiplication. The circuit presented is having a wide tuning range with error less than 8.6% and is insensitive to temperature variations. Hence the major advantage of the proposed design over previous designs in terms of low power consumption, high accuracy, wide tunable range, high multiplication factor and small silicon area. The proposed design is suitable for low frequency applications which suits the biomedical applications, low frequency filters and oscillators where large time constant is required.

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