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A High Accuracy Weak Voltage LED Analog Dimming Method

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ABSTRACT A weak voltage analog dimming method for high precision light emitting diode (LED) current control with N-Bits analog static offset calibration (N-Bits ASOC), dynamic offset cancellation (DOC) and K-times dimming duty to voltage (KD2V) conversion is presented. The N-Bits ASOC circuit decreases the analog dimming error to $V_{OSMAX}/2^N - 1$ by pre-calibrating the error amplifier offset. Moreover, through a smart combination of KD2V circuits and DOC amplifier, the KD2V and DOC operational amplifier magnify the dimming reference and LED current sense voltage K-times, respectively, which reduces the residual dimming error K-times without any modification to the LED current sampling resistor. Based on the 0.18μm 5V/40V Bipolar-CMOS-DMOS (BCD) process, experimental results for a cell phone backlighting driver show that the analog dimming I_{LED} error reduces to 30μA at maximum 200mV LED current feedback voltage. This deviation mostly keeps constant through a dimming duty range of 0.5% to 100% and V_{IN} range of 2.7V to 5.5V. Furthermore, a 200-sample measurement data suggests that this method is effective even when dimming duty is smaller than 0.5% for mass production.

INDEX TERMS LED analog dimming, pulse width modulation (PWM) dimming, dynamic offset cancellation (DOC), analog static offset calibration (ASOC).

I. INTRODUCTION

The most widely used LED is the third generation solid state lighting source. Compared to cold cathode fluorescent lamps (CCFL) and others lighting sources (such as incandescent light bulbs, high intensity discharge lamps), LEDs are more efficient, smaller, safer, have longer lifespan, and provide flexible dimming method. Moreover, due to the nearly linear relation between forward current and LED luminance [1], current regulation becomes the most popular method to control LEDs' luminance [2], [3], whose performance is much better than that of the voltage regulation method.

Usually, the current regulation methods are divided into two categories. One is called Pulse Width Modulation (PWM) dimming control [4], [5]. It regulates the LEDs current stepping between zero and its maximum value with the LED switching off and on. Thus, the average current through the LED is linearly related to the duty cycle of the input dimming signal. The advantage of PWM is that it reaches high precision and achieves up to 50000:1 contrast [6], nevertheless, this approach suffers from electromagnetic interference (EMI) issues because of its high speed current transition [7], [8]. The other category is analog regulation, which is also called Amplitude Modulation (AM). In this method, the LED is always on. Its forward current is regulated linearly by the dimming signal duty cycle. This method can eliminate audio noise completely, reduce EMI, and achieve real brightness adjustment without flicker [8], [9].

Therefore, the analog regulation technology is used more and more widely in the field of low EMI and flicker free lighting. For example, to reduce the influence of LED backlighting on the performance of high-frequency electrical devices, the analog dimming method is used in mobile phone backlighting module [9], [10]. Fig. 1 is a typical topology for LEDs driver in mobile phone backlighting module [9], [11], [12].

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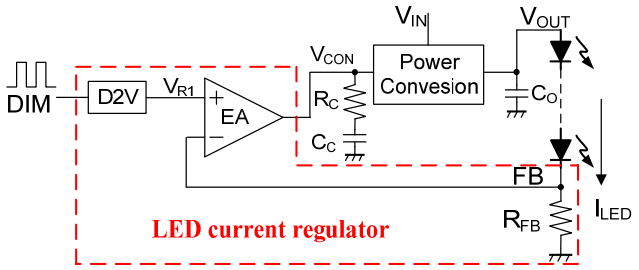

FIGURE 1. A typical block diagram for white LEDs driver in mobile phone backlighting module.

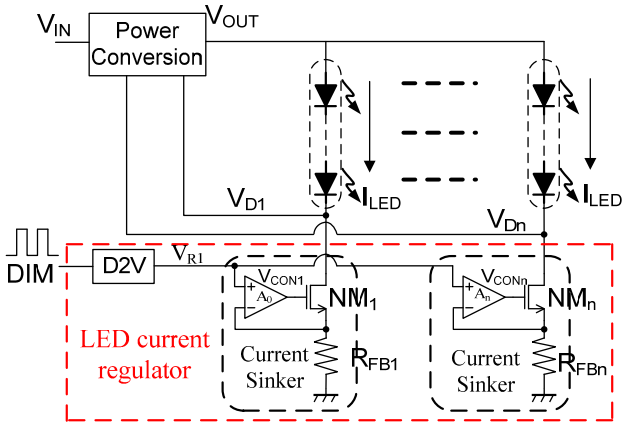

FIGURE 2. LED driver for medium-size LCD panel backlighting module.

This white LEDs driver consists of two parts: one is the voltage conversion circuit block, which boosts V_{IN} to V_{OUT} to provide the power for LEDs. The LED current regulator block is illustrated in the red dotted line rectangle. This block provides current regulation for LEDs.

Besides the application shown above, analog dimming methods are also commonly used for medium-size LCD panel backlighting modules. Fig. 2 is an extensively adopted topology for laptop, LCD monitor and medium-size LCD TV panel backlighting module [13]. In this application, multi-string LEDs are arranged to provide stronger luminance. In order to meet the light uniformity and accuracy, the driver needs high accuracy and precise matching of the current regulation for each string.

In Fig. 1 and Fig. 2, LED current regulators are marked in the corresponding red dotted line rectangle. In these blocks, the LEDs' current is controlled by the dimming voltage V_{R1} through the feedback loop, which consists of the current sense resistors (R_{FB}/R_{FB1} ~R_{FBn}) and error amplifiers (EA/A_0 ~A_n/NM_1 ~NM_n) and power conversion stage.

Based on the LED current regulation loop, the LED current can be formulated as follows:

$$I_{LED} = \frac{V_{FB}}{R_{FB}} = \frac{V_{R1} - V_{OS}}{R_{FB}} \tag{1}$$

where I_{LED} is the LEDs forward current, V_{FB} is the LEDs current feedback sense voltage, and R_{FB} is the LEDs' current sense resistor, V_{R1} is the output of D2V. It is a weak voltage signal without current output capability. The value is proportional to the dimming signal duty cycle D. V_{OS} is the offset voltage of the error amplifiers.

Based on equation (1), the V_{OS} severely impairs the precision of analog dimming, especially during small duty cycle applications. In order to obtain high efficiency, V_{R1} usually has a maximum value of 100mV~200mV. In the standard BCD process, EA/A_0 ~A_n V_{OS} 3σ statistical value reaches 5mV~10mV [14]–[16]. While the duty cycle D=100%, the dimming error is up to 5%. In a worse case, when the duty cycle D is 1%~5% and V_{OS} is close to or larger than the V_{R1} value, it can result in the brightness of the LED going out of control. Therefore, high-precision analog dimming can be achieved only by eliminating the error amplifiers V_{OS}.

There are many papers on offset voltage elimination technology. These methods are divided into two categories. One is the dynamic offset cancellation (DOC) technique, such as auto-zeroing [17]–[20], [30] and chopper [14], [21]–[23]. Auto-zeroing uses sampling-elimination technology to eliminate the offset voltage while the chopper uses high frequency modulation followed by bandwidth filter to decrease the offset voltage. The other one is the pre-calibration technique, which is to sample and compensate the offset voltage before the operational amplifier works while maintaining the offset voltage compensation state during normal operation, such as fuse trim [24] and circuit trim [25], [26]. The residual offset of pre-calibration accuracy is relatively higher. However, V_{R1} is a weak voltage signal and has no current output capability. Dynamic offset voltage cancellation techniques are not feasible in this analog dimming.

In this paper, a weak voltage analog dimming control method, which consists of a two-stage offset cancellation structure, is presented. In this approach, the first stage is composed of N-BITs analog static offset calibration operational amplifier (N-BITs ASOC OP2) to reduce the offset voltage of OP2 without any current load to the analog dimming signal. Furthermore, temperature compensation is introduced in this stage to reach a preset fixed error throughout the operating temperature. In the second stage, dynamic offset cancellation technology is applied to OP1 to achieve K-times attenuation of pre-calibrated residual error. By this mean, the weak voltage V_{R1} controls the LED current accurately, even during the small duty cycle of the input dimming signal (DIM).

This paper is organized as follows: Section II describes the proposed method principle; Section III presents the scheme and its circuit implementation; Section IV provides the experimental results; and Section V gives a conclusion for this method.

II. PRINCIPLE OF THE PROPOSED METHOD

The proposed analog dimming circuit architecture is shown as Fig. 3. This diagram is divided into three parts: 1) The Dimming signal (DIM) duty cycle to analog dimming voltage conversion block (KD2V). This block converts the DIM's duty cycle (D) into the analog voltage V_{R1}. 2) The N-BITs analog static calibration OP2 (N-BITs ASOC OP2).

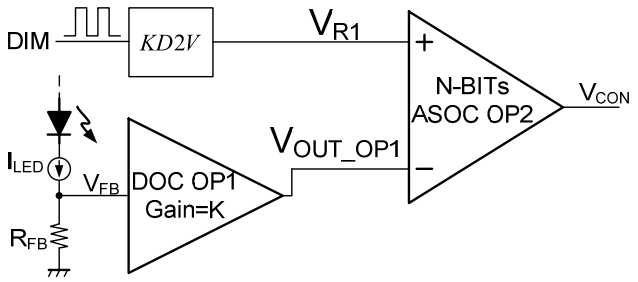

FIGURE 3. The topology of the proposed double offset cancellation structure for LEDs analog dimming.

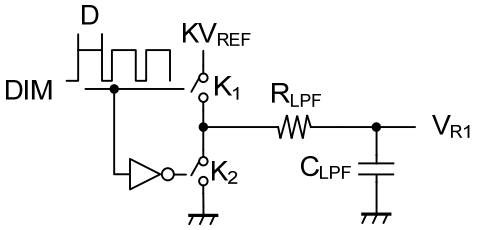

FIGURE 4. The topology of the proposed double offset cancellation structure for LEDs analog dimming.

The positive terminal of this amplifier is the analog dimming signal V_{R1}. The negative terminal connects to the signal V_{OUT_OP1}, and the output V_{CON} is directly used to control the LEDs power conversion, as the signals V_{CON}/V_{CON1} $\sim V_{CONn}$ in Fig. 1 and Fig. 2. 3) A feedback signal amplifier with K-times gain (DOC OP1 Gain=K). The dynamic offset elimination technique is used to reduce the input offset voltage of OP1, and the sense voltage V_{FB} generated from I_{LED} is accurately amplified by K-times. The output of OP1 (V_{OUT_OP1}) connects to the negative terminal of OP2, so that the equivalent residual offset voltage of N-BITs ASOC OP2 is further reduced to 1/K-times.

A. EXPLANATION OF KD2V BLOCK

KD2V block converts the DIM's duty cycle into the analog dimming voltage V_{R1}. The output analog voltage has a linear relationship with the DIM's duty cycle. This block consists of a typical RC low-pass filter, as shown in Fig. 4.

In Fig.4, the DIM is usually PWM signal for LED dimming, where D represents the duty cycle of the PWM signal high level. K_1 and K_2 are two analog switches. The R_{LPF}/C_{LPF} constitutes a low-pass filter. KV_{REF} is K-times of the maximum preset V_{FB}. When the DIM is at high level, switch K_1 is closed and K_2 is open, KV_{REF} charges C_{PLF} through R_{LPF}. When the DIM is at low level, switch K_1 is open and K_2 is closed, C_{LPF} discharges through R_{LPF}. After several cycles, V_{R1} is stable. Its average voltage is as follows:

$$V_{R1} = K \cdot D \cdot V_{REF} \tag{2}$$

where V_{R1} is the output voltage of KD2V, which is proportional to the DIM's duty cycle, and $D \cdot V_{REF}$ is the ideal value of V_{FB} when DIM's duty cycle equals to D. K is the multiply factor of V_{REF}. V_{REF} is the maximum preset V_{FB}.

From this formula, the converted output voltage V_{R1} is K-times of the ideal value of V_{FB} when DIM's duty cycle is D.

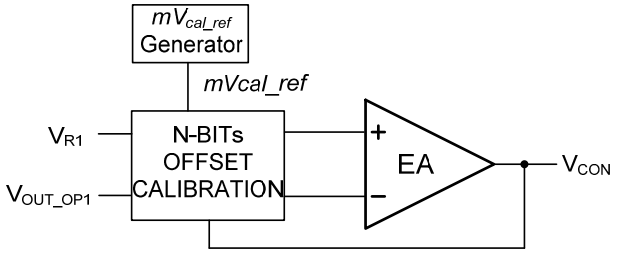

FIGURE 5. The structure of N-BITs analog static offset calibration (ASOC) OP2.

B. EXPLANATION OF N-BITS ASOC OP2 BLOCK

N-BITs ASOC OP2 block is an offset pre-calibration amplifier. Its structure is shown in Fig. 5, which consists of three units: N-BITS OFFSET CALIBRATION, Error Amplifier (EA) and mVcal_ref Generator, where mVcal_ref Generator generates the reference voltage for offset voltage calibration, the N-BITS OFFSET CALIBRATION realizes the N-BITs calibration function to reduce offset voltage of Error Amplifier (EA) and the Error Amplifier (EA) is the elementary error amplifier.

LED current control adopts close-loop regulation with high loop gain with OP2 providing this gain. Therefore, the voltage relationship between the two input terminals of OP2 is as follows:

$$V_{OUT\_OP1} = V_{R1} \frac{A_{DC\_LP}}{A_{DC\_LP} + 1} - V_{OS} \tag{3}$$

where V_{OUT_OP1} is the amplified LED current detection signal from OP1, and V_{OS} is the offset voltage of OP2. V_{R1} is the LED dimming signal, the value of which is controlled by LED dimming duty cycle. A_{DC_LP} is the loop gain of the LED current controller, which is much larger than 1. Therefore formula (3) can be expressed by formula (4):

$$V_{R1} - V_{OUT\_OP1} \approx V_{OS} \tag{4}$$

According to (3), the difference between V_{R1} and V_{OUT_OP1} is the OP2's offset voltage V_{OS}. The smaller V_{OS} reaches the more accurate the LED current precision gets. An N-BITs Analog-Static Calibration technique is proposed to decrease the V_{OS} significantly without additional current load to V_{R1}.

The N-BITs ASOC OP2 operates in two states, first in the offset voltage calibration stage, and then in the signal amplification state.

When N-BITs ASOC OP2 operates in the offset voltage calibration state, mVcal_ref Generator generates a reference voltage to compensate the offset voltage of the basic amplifier EA. In this stage, EA operates in the comparator mode

with very high gain. According to the output of the EA, the N-BITS OFFSET CALIBRATION circuit acquires the polarity of EA's initial offset voltage. Then, a compensation voltage opposite to the initial offset voltage is added to the input of the differential pair with the initial value setting to the minimum voltage generated by mVcal_ref. The EA output signal is detected again. If the output of the EA keeps the same logic state, the compensation voltage gradually increases with the step equaling to the minimum value generated by mVcal_ref until the EA output becomes the opposite logic status of the initial state. The cumulative compensation voltage is fixedly added to the differential pair input of the EA, then the offset voltage calibration stage is completed.

To ignore the V_{OS} temperature coefficient, the maximum residual error of N-BITs ASOC OP2 after calibration is in equation (4), which indicates that the residual error N-BITs ASOC OP2 can be decreased through increasing the N value.

$$V_{osres\_op2\_\max} = \frac{v_{os0\_\max}}{2^{N-1}}, \quad 0 < N \tag{5}$$

where Vosres_op2_max is the maximum residual error of N-BITs ASOC OP2. Vos0_max is the maximum offset voltage of OP2. This value is calculated according to the parameters provided by the manufacturer. N is the maximum digit of the offset voltage calibration. $\frac{v_{os0\_\max}}{2^{N-1}}$ is the minimum voltage generated by mVcal_ref.

Considering the influence of temperature, the maximum residual offset voltage can be revised to formula (6):

$$\begin{aligned} &V_{osres\_op2\_\max}(T) \\ &= \frac{V_{os0\_\max}(T_0)}{2^{N-1}} \\ &\quad + \frac{m}{2^{N-1}}(c - \Delta\beta/\beta)\, V_{T0}(T - T_0), \quad 0 < m < 2^{N-1} \end{aligned} \tag{6}$$

where,

Vos0_max (T_0): The maximum offset voltage at T_0 temperature.

m: The number of steps required for the offset calibration.

C: The temperature coefficient of the calibration voltage.

$\beta = \mu C_{ox} {}^{W}\!/_{L}$: The current factor of the MOSFETs.

$\Delta\beta$: The mismatch of current factor.

V_{T0}: The MOSFET threshold voltage at T_0.

In formula (5), the temperature coefficient of residual error voltage is zero if $c = \Delta\beta/\beta$. That is, the residual offset voltage does not alter with temperature. Substitute equation (6) into formula (4), the result is shown in equation (7):

$$V_{OUT\_OP1} \approx V_{R1} - \frac{V_{os0\_\max}(T_0)}{2^{N-1}} \tag{7}$$

Therefore, the residual offset voltage is smaller with an increasing N and does not change with temperature.

C. EXPLANATION OF DOC OP1 GAIN=K BLOCK

DOC OP1 Gain=K is an operational amplifier integrated dynamic offset cancellation technique. This amplifier close loop gain equals to K.

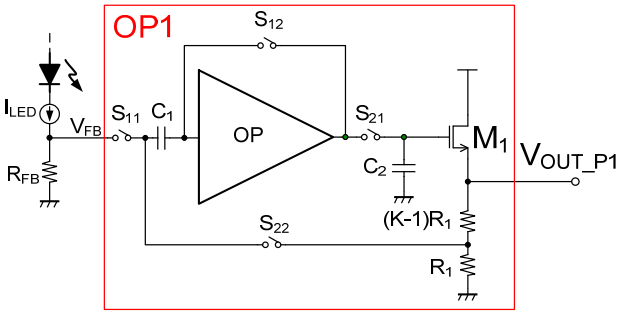

FIGURE 6. The structure of DOC OP1 with gain=K.

As shown in Fig. 3, this OP's input terminal connects to the LED current sense point V_{FB}. The output terminal V_{OUT_OP1} connects to the N-BITs ASOC OP2 negative input terminal. The V_{FB} has small equivalent output resistance with strong current drive capability. So the DOC technique is applied to get rid of the OP's offset voltage.

In this work, the OP1 circuit structure is shown in Fig 6. Considering the auto-zero residual error, OP1 output voltage signal is expressed as follows:

$$\begin{cases} V_{OUT\_OP1} = K\left(V_{FB} + V_{os\_res\_op1}\right) \\ V_{os\_res\_op1} = \frac{V_{os}}{A_1+1} + \frac{q_{inj\_S12}}{C_1} \end{cases} \tag{8}$$

where V_{OUT_OP1} is the output of OP1, K is the close loop DC gain of OP1, V_{FB} is the LED current feedback voltage, Vos_res_op1 is the residual offset voltage of OP1, Vos is the original offset voltage of OP, A_1 is the DC gain of OP, q_{inj_S12} is the combination of channel charge injection and clock feedthrough produced by switch S_{12}, C_1 is the capacitor for input voltage sample-hold.

From equation (8), the first item on the right side of the Vos_res_op1 equation can be neglected when $A_1 >> 1$, and the second item is induced by the switch S_{12} charge injection. There are multiple literatures [27]–[29] to decrease this value.

Combining equations (2) to (8), the LED current deviation is expressed in equation (9):

$$\begin{aligned} I_{ERR} &= I_{LED} - \frac{D \cdot V_{REF}}{R_{FB}} \\ &= -\frac{1}{R_{FB}}\left[\frac{V_{os0\_\max}(T_0)}{K \cdot 2^{N-1}} + \frac{V_{os}}{A_1 + 1} + \frac{q_{inj\_S12}}{C_1}\right] \end{aligned} \tag{9}$$

where, I_{ERR} indicates the deviation of LED current between the actual value and the ideal value. The intermediate and the rightmost equation of formula (8) indicate that this deviation is controlled by the circuit's electrical characteristic parameters and does not vary with the LED dimming duty cycle. From the final result of formula (8), the error consists of three items, $V_{os0\_\max}(T_0)/K \cdot 2^{N-1}$, $V_{os}/(A_1+1)$, q_{inj_S12}/C_1. These 3 items are analyzed separately as follows:

The first item is caused by the N-BITs ASOC OP2 residual error after the calibration stage. This value is very small. Furthermore, the residual error decreases to 1/K-times by OP1, which implies that the dimming error can be progressively

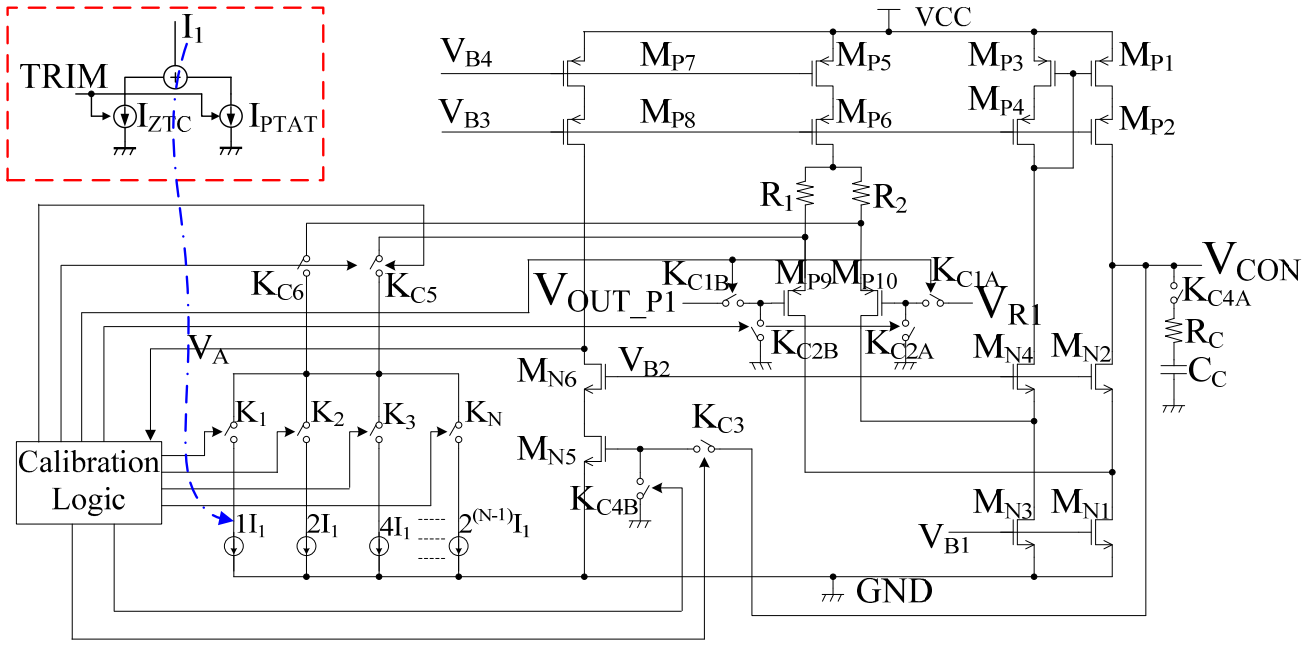

FIGURE 7. Circuits of N-BITs analog static offset calibration OP2.

reduced by increasing K. Assuming that the original offset $V_{OS0\_max}(T_0)$ equals to 5mV, N is 6, K is 6, the residual dimming error reduces to 2.6μA. Compared to the ideal LEDs' current, it's a tiny error that can be ignored even when D=1%.

The second one is caused by the offset voltage OP. The residual error caused by this offset reduces to $1/(A_1+1)$, where A_1 is the OP's open loop DC gain. The value can be up to 60dB or even larger, the actual dimming error induced by this item is about 0.5$\sim$1μA with OP's original offset voltage being 5$\sim$10mV.

The third one indicates the dimming error from OP1's channel charge injection and clock feed-through of the non-ideal switches. Several techniques have been developed over the years to minimize the imperfections, such as dummy transistor and complementary switches. The error can be decreased to less than 0.1mV [29]. Consequently, even when the dimming duty cycle D=1%, this adverse implication can be ignored.

In addition, from equation (8), the temperature coefficient of this residual error is almost zero. The first item in the middle bracket is the residual offset of N-BITs ASOC OP2. Because of the temperature compensation implementation for OP2 offset calibration voltage generation, thus, the residual offset of OP2 keeps constant through the operation temperature.

As the result of OP's high open loop A_1, the temperature coefficient caused by V_{OS1} is so small that it can be ignored. The error induced by q_{inj_S12} is determined by the switches' non-ideality. Obviously, clock feedthrough has a zero temperature coefficient, and the channel charge injection temperature relation can be shown as:

$$\frac{dq_{inj\_S12}}{dt} = -W_1 \cdot L_1 \cdot C_{ox} \frac{dV_{TH}}{dt} \tag{10}$$

where W_1 and L_1 is the S_{12} channel width and length respectively, C_{ox} is the gate capacitance per unit area, V_{TH} is the S_{12} threshold voltage. This item causes a temperature shift less than 1μV/°C. Assuming the temperature ranges from -40°C to 85°C, the error shift is about 0.165mV, which is much smaller than the DV_{REF} even at D=1%.

Comparing equation (1) with equation (9), the proposed approach reduces the dimming error substantially. When the EA's original offset is 5mV, the residual error decreases to less than 26μV with N=6 and K=6. Even considering the drift of this residual error to temperature, the value is less than 200μV.

Based on the above analysis, the proposed weak voltage analog dimming control method can significantly improve the analog dimming accuracy. It is valid over the operating temperature.

III. THE SCHEME AND CIRCUIT IMPLEMENTATION

This section mainly describes the circuit implementation of the weak voltage analog dimming control method. Because KD2V module uses conventional RC filter, it is easy to design. This work focuses on the circuit design of the N-BITs ASOC OP2 and DOC OP1 Gain=K.

A. THE CIRCUIT OF N-BITS ASOC OP2

The circuit of N-BITs ASOC OP2 is shown in Fig.7. In this circuit, I_1 and R_1/R_2 form mVcal_ref Generator. I_1 consists

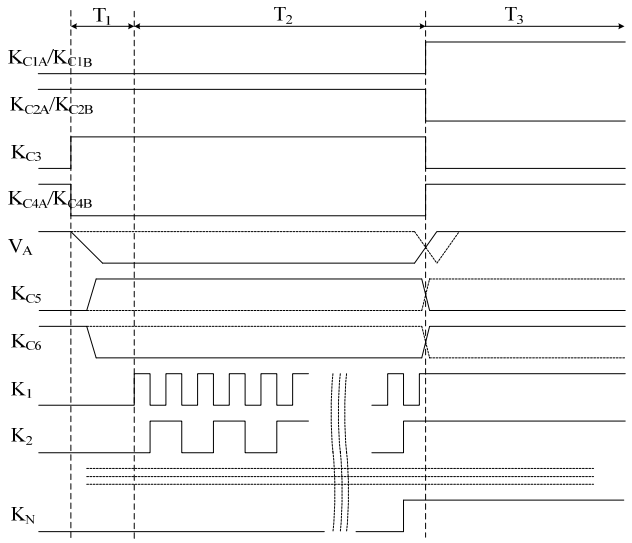

FIGURE 8. The timing sequence of the main control signals for the N-BITs ASOC input offset voltage calibration.

of zero temperature current I_{ZTC} and I_{PTAT}. The ratio between I_{ZTC} and I_{PTAT} is adjustable through the TRIM signal, while R_1/R_2 is a zero-temperature coefficient resistor.

In Fig. 7, M_{P1}-M_{P6}, M_{P9}/M_{P10}, and M_{N1}-M_{N4} and R_1/R_2 form a conventional folding op amp, which is the EA shown in Fig. 5. The trans-conductance of EA is mainly determined by R_1/R_2. The M_{P9}/M_{P10} form the input differential pair. The M_{P5}/M_{P6} provide a bias current for the M_{P9}/M_{P10}. The M_{N1}-M_{N4} and M_{P1}-M_{P4} form a classical folded-cascode structure. The output terminal is V_{CON}. R_C and C_C form a compensation network used to generate the zero/pole for controller loop compensation.

In Fig. 7, switches $K_{C1A}/K_{C1B}/K_{C2A}/K_{C2B}/K_{C3}/$ $K_{C4A}/K_{C4A}/K_{C4B}/K_{C5}/K_{C6}$, K_1-K_N and I_1-2(N-1)I_1, M_{N5}/M_{N6}, M_{P7}/M_{P8} and Calibration Logic form the N-BITS Analog Static Offset Calibration circuits to reduce the equivalent input offset voltage of EA without extra current load to the input voltage source.

In Fig. 7, the signals V_{B1}-V_{B4} are bias voltage to provide appropriate bias for different circuits. V_{OUT_P1} is K-times of V_{FB}. V_{FB} is the LED current feedback voltage and V_{R1} is the analog dimming reference voltage.

The working sequence of the N-BITs ASOC OP2 is shown in Fig. 8. The circuit works in three stages, namely the initial offset voltage polarity judgment stage (T_1 stage), the offset voltage compensation stage (T_2 stage) and the amplification stage (T_3 stage). These three stages of work are analyzed as follows:

1) INITIAL OFFSET VOLTAGE POLARITY JUDGMENT (T_1 STAGE)

In this stage, the EA's input signal is set to zero, which means that the gates of M_{P9}/M_{P10} are short to GND, K_{C1A} and K_{C1B} are open while K_{C2A} and K_{C2B} are short. Meanwhile, K_{C4A} and K_{C4B} keep open and K_{C3} keeps short. The output V_{CON} of EA is connected to the gate of M_{N5}. EA operates as a comparator. According to the logic state of V_A, the polarity of the initial equivalent offset voltage V_{OS1_EA} of EA can be determined.

The polarity of V_{OS1_EA} is positive if the output of V_A is at high logic level, which means that the threshold of M_{P9} is higher than that of M_{P10} ($V_{TH\_P9} > V_{TH\_P10}$). Then K_{C6} keeps close and K_{C5} keeps open, the current flowing through the switch K_{C6} generates voltage drop V_{KC6_R2} on R_2, which is used to compensate for the difference between V_{TH_P9} and V_{TH_P10}. The main control signals of the circuit are represented by the solid line in Fig. 8.

On the contrary, if the output of V_A is at low logic level, the polarity of V_{OS1_EA} is negative. V_{TH_P9} is less than V_{TH_P10}. At this time, K_{C6} is disconnected, K_{C5} is closed. The main control signals of the circuit are represented by the dotted line in Fig. 8.

Based on the previous approach, the initial polarity of V_{OS1_EA} can be acquired by the logical state of V_A to control the status of switches of K_{C5} and K_{C6}. During the T_1 stage, the N-BITs offset voltage compensation current control switches K_1-K_N keeps disconnected, and the current flowing through the switch K_{C5}/K_{C6} is still zero.

2) OFFSET VOLTAGE COMPENSATION STAGE (T_2 STAGE)

After the EA's original offset polarity is determined, this circuit enters the offset compensation stage. The timing sequences are illustrated in Fig. 8's T_2 stage. In this stage, the EA still keeps in comparator configuration, switches K_{C5}/K_{C6} keep previous state, and switches K_1-K_N turn ON/OFF to increase the offset compensation voltage step by step until the V_A logic state transition. During T_2 stage, the offset compensation voltage increases $V_{MAX}/2^{(N-1)}$ at each step, and V_{MAX} is the preset maximum offset compensation voltage, which is calculated based on the mismatch parameters from process foundry. Illustrated as in Fig. 7 and Fig. 8, the working process of T_2 stage is described as follows:

First, assuming that the output of V_A is logic low during T_1 stage, the polarity of V_{OS1_EA} is negative, K_{C6} keeps open and K_{C5} keeps close. Then, in the first step of compensation, switch K_1 is closed, and the offset compensation current flowing through the switch K_{C5} is I_1, the offset compensation voltage generated by the resistance R_1 is $V_{MAX}/2^{(N-1)}$. Then the Calibration Logic circuit checks V_A 's logic state again. If V_A still keeps low, switch K_2 is closed and K_1 is disconnected. The current flowing through the switch K_{C5} increases to two-times of I_1, while the voltage drop on the resistance R_1 increases to $2^*V_{MAX}/2^{(N-1)}$. If V_A 's level remains low, the compensation current increases step by step, and the increasing amount at each incremental step is I_1 until V_A 's level is reversed to the anti-phase logic state compared with that in T_1 stage. Then, the status of the switches K_1-K_N is locked, and the offset voltage compensation current remains.

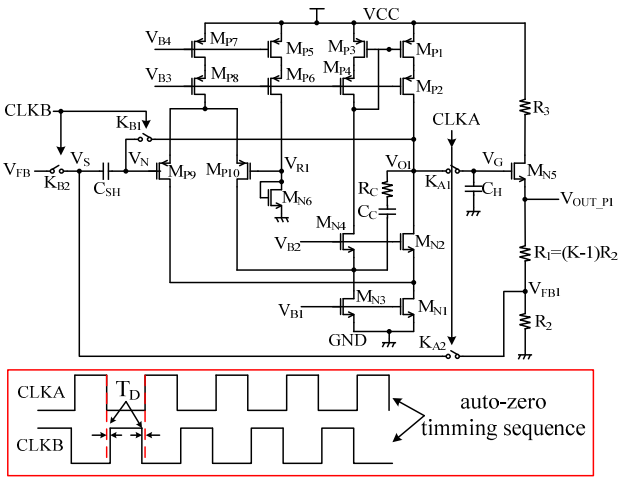

FIGURE 9. The FB K-times amplifier with auto-zero technical for OP's offset voltage cancellation, the loop gain is determined by the resistor ratio between R_1 and R_2; the timing sequence for switches $K_{A1}/K_{A2}/K_{B1}/K_{B2}$ is shown in the red line-frame.

Similarly, if V_A is at high level in stage T_1, then the input offset voltage polarity judgment switch K_{C6} is closed and K_{C5} opens. Then the compensation current control switches K_1-K_N are turned on/off step by step, which makes I_{KC6} increase gradually. When V_A changes from logic high to logic low state, the offset voltage compensation stage ends and switches K_1-K_N states are locked to keep the offset compensation voltage unchanged.

3) OFFSET COMPENSATION VOLTAGE HOLDING (T_3 STAGE)

At this stage, the offset compensation is fixed at T_2 stage, the EA returns to LED dimming control configuration. So, switches K_1-K_N and K_{C5}/K_{C6} maintain the states at the end of stage T_2, switches $K_{C2A}/K_{C2B}/K_{C3}$ change to open, $K_{C1A}/K_{C1B}/K_{C4A}/K_{C4B}$ are closed. Then, EA is again connected to the analog dimming control circuit as an N-BITs ASOC OP2, shown in Fig.3.

After these three stages, the N-BITs ASOC OP2's residual offset voltage is less than $V_{MAX}/2^{(N-1)}$. This value decreases as N increases.

B. DYNAMIC OFFSET CANCELLATION WITH K-TIMES LOOP GAIN OP1 (DOC OP1 GAIN=K)

The auto-zero technical is implemented in the DOC OP1 for offset cancellation to achieve an accurate K-times magnification of the LED current detection signal V_{FB}. The circuit structure is shown as Fig.9.

In Fig. 9, the folded-cascode op-amp is composed of M_{P1}-M_{P4}, M_{P7}-M_{P10}, M_{N1}-M_{N4} and R_1/R_2. The ratio amplification circuit consists of $M_{N5}/R_1/R_2$. R_1/R_2 controls the V_{FB} magnification ratio. M_{P9}/M_{P10} make up input differential pairs and M_{P7}/M_{P8} provides a bias current for the differential pairs M_{P9}/M_{P10}. M_{N1}-M_{N4} and M_{P1}-M_{P4} form a folding structure and the output terminal is V_{O1}; Capacitors C_H and MOSFET M_{N5}, resistors R_1-R_2 form ratio amplifier circuits. MOSFET $M_{P5}/M_{P6}/M_{N6}$ form a voltage bias circuit that provides appropriate DC operational points. Switches $K_{A1}/K_{A2}/K_{B1}/K_{B2}$, and capacitance C_{SH} work together forming an auto-zero offset cancellation circuit.

CLKA and CLKB are the non-overlapping clock signals for auto-zero switches controlling. The dead time is T_D, which is about 5nS to 10nS.

This circuit works in two stages. The first stage is the offset voltage sampling stage. In this stage, OP1 sets as the unit feedback topology, and its offset voltage is stored to C_{SH}.The second stage realizes offset cancellation. During this stage, the offset voltage stored on C_{SH} is subtracted from the input signal. The process can be analyzed as follows:

1) OFFSET VOLTAGE SAMPLING STAGE

During this stage, the signal CLKB is at logic high level and switches K_{B1}/K_{B2} are closed. Furthermore, the signal CLKA is logic low and switches K_{A1}/K_{A2} are disconnected. The folded-cascode OP is connected as a unit feedback gain configuration. The input signal V_{FB} is directly loaded at node V_S, which is one terminal of the sample-holding capacitance C_{SH}. The other terminal of C_{SH} is connected to the folded-cascode OP's output (negative input) terminal, so the offset voltage of this folded-cascode OP is sampled by C_{SH}. At this time, the voltage calculation formula can be shown as:

$$\begin{cases} V_N = V_{R1} + V_{OS1\_OP1} \\ V_{CSH} = V_{FB} - (V_{R1} + V_{OS1\_OP1}) \end{cases} \tag{11}$$

where V_N is the voltage of the non-positive input terminal of the OP, V_{R1} is the internal bias voltage of the OP, V_{OS1_OP1} is the offset voltage of the OP during the sampling stage, V_{CSH} is the voltage difference between the terminals of the offset sample-hold capacitor C_{SH}, V_{FB} is the feedback voltage of the resistor R_{FB}, which senses the LED forward current.

2) OFFSET VOLTAGE CANCELLATION STAGE

In the second stage, the signal CLKB is at logic low, the signal CLKA is at logic high, switches K_{B1}/K_{B2} are disconnected, and switches K_{A1}/K_{A2} are closed. At this time, the feedback voltage V_{FB} is connected to the node V_S, the other terminal of C_{SH} is connected to the OP's negative input terminal. According to the feedback loop of this OP, the voltage difference between two terminals C_{SH} and V_N are still maintained as in formula (11). Therefore, the voltage calculation formulas for V_{FB} and V_{FB1} are as follows:

$$\begin{cases} V_{FB1} = V_{FB} + (V_{OS2\_OP1} - V_{OS1\_OP1}) \\ V_{os\_op1\_res} = V_{OS2\_OP1} - V_{OS1\_OP1} \\ V_{OUT\_OP1} = \frac{R_1+R_2}{R_2} \cdot (V_{FB} + V_{os\_op1\_res}) \end{cases} \tag{12}$$

where V_{FB1} is the feedback voltage on the feedback resistor R_2, V_{OS2_OP1} is the offset voltage of the OP during the second operation stage, R_1 and R_2 is the feedback resistor network, V_{OUT_P1} is the output voltage of the OP, which is determined by V_{FB} and the ratio between resistor R_1 and R_2.

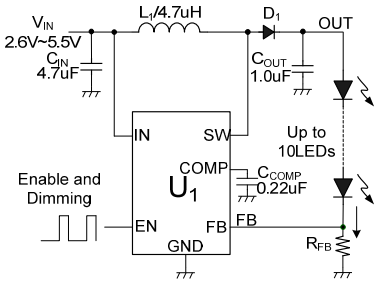

FIGURE 10. Typical application circuit of the proposed white LED driver.

From the V_{OUT1_OP1} calculation formula, it can be seen that the V_{OUT_OP1} is not the ideal V_{FB} K-times magnification due to OP1's residual error caused by the switch K_{B1} clock feed-through and charge injection.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed high precision analog dimming method was used in a small power white LED driver, which is used for small size liquid-crystal-display (LCD) panel backlighting. This driver was designed in a standard BCD process.

Based on 0.18μm 1.8V/3.3V/5V/40V BCD Process, a white-light LED driver is designed. In this chip, the input dimming signal is a digital PWM dimming signal, whose frequency ranges from 1KHz to 300KHz. The LED operates in DC current with the dimming duty cycle ranging from 1% to 100%. Under the analog dimming mode, the maximum output voltage of V_{FB} is 200 mV when the LED dimming signal is at 100% duty cycle. The minimum duty cycle of the dimming signal is 1%, and the V_{FB} DC average voltage is 1mV. This driving chip uses the proposed two-stage offset voltage elimination structure to achieve high-precision LED analog dimming control.

The typical application circuit of a white LED driver is shown in Fig. 10.

In Fig. 10, U_1 is a monolithic LED driver designed with boost structure. Its internal circuit is similar to Fig. 1. However, in the dimming module, the LEDs' forward current control circuit shown in Fig. 3 is adopted. U_1's key electrical parameters and external application components are shown as table 1.

This LED driver die size is 0.8mm×1.45mm. The proposed DOC OP1 and 5-BITs ANA-SC OP2 die size is 0.029mm^2 and 0.032 mm^2 respectively. Instead of DOC OP1, amplifiers with BJTs as OP1 are required in conventional analog dimming methods. Besides, an additional OP2 without offset cancellation is still needed. The die sizes of OP2 and BJT OP1 in conventional methods are about 0.01mm^2 and 0.012mm^2, respectively. Therefore, the proposed method needs an extra 0.039mm^2, which has little influence on the total cost. The microphotograph of this LED driver is shown in Fig. 11.

The oscilloscope test waveforms are shown in Fig 12. The test conditions are V_{IN} = 3.6V, the load is the single string

TABLE 1. Key electrical parameters and external application components.

Name	Descriptions	Value	Units
L_1	External inductor	4.7	μH
C_{IN}	Input capacitor	4.7	μF
C_{OUT}	Output capacitor	1.0	μF
C_{COMP}	Compensation capacitor	0.22	μF
F_{OSC}	Boost converter frequency	1.0	MHz
R_{FB}	LED current sense resistor	10	Ω
V_{FB}	Maximum regulation voltage	200	mV
D_{min}	Minimum dimming duty cycle	1	%

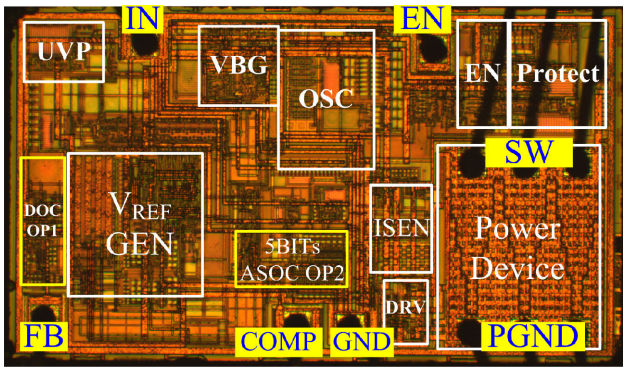

FIGURE 11. Microphotograph of the experimental white LED driver.

with 10LEDs series, the PWM dimming signal frequency on EN pin is 20KHz with the duty cycle at 0.5%, 5% and 50%.

In Fig. 12, CH1 is the input dimming signal. CH2 is OUT node voltage waveform with OUT being the top node of the LEDs string. CH3 is the VFB voltage. CH4 is LED forward current. In order to achieve higher precision, wire rounding method for current probe is used to obtain 10/5-times the LED current waveform during the measurement. Fig. 12A is dimming duty=0.5%, equivalent I_{LED} =0.12mA (with 10-times magnitude waveforms). Fig. 12B is D=5%, equivalent I_{LED} =1mA (with 5-times magnitude waveforms). Fig. 12C is D=50%, equivalent I_{LED} = 10mA (with 5-times magnitude waveforms). All of the LED current waveforms are DC shape. It's analog dimming mode.

In order to further find out the relationship between the I_{LED} and the input dimming duty cycle, the I_{LED} vs D graph is illustrated in Fig. 13A with the dimming duty cycle changing from 0.1% to 100%, while the details of D≤10% is shown in Fig. 11B.

In Fig. 13A, I_{LED} increases with the dimming duty cycle linearly when D changes from 0.1% to 100%. The deviation between the actual value and the idea I_{LED} is less than 0.1mA.

In Fig. 13B, the enlarged graph for D≤10% clearly shows that I_{LED} has a linear relationship with dimming duty cycle even when D is less than 1%. However, with the increasing

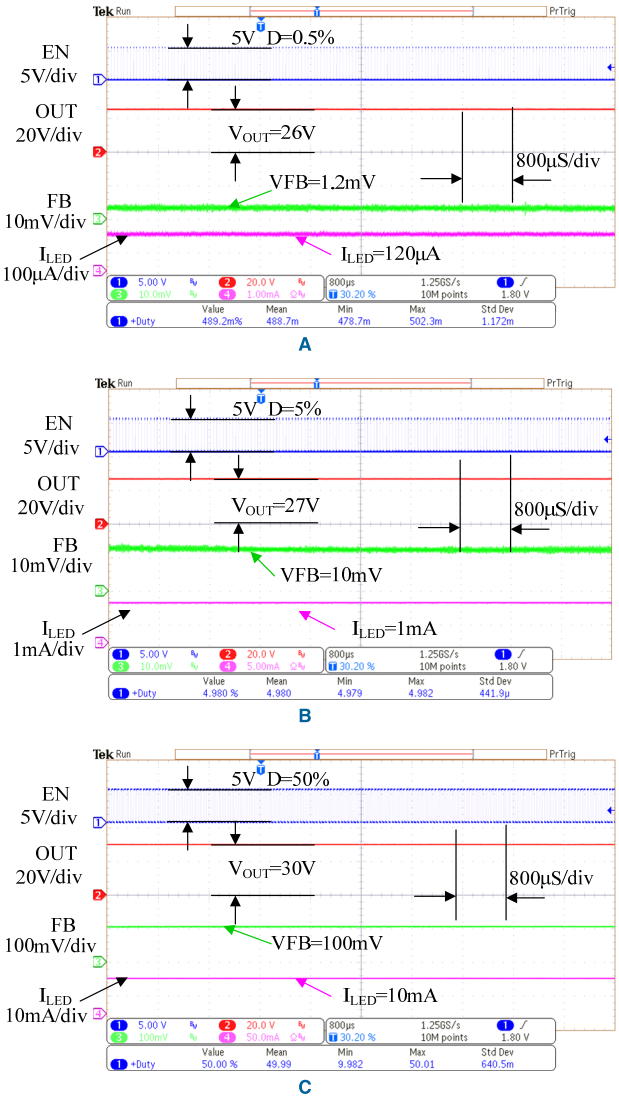

FIGURE 12. The white LEDs output waveforms with different PWM dimming duty cycle; A/B/C is PWM dimming duty cycle=0.5%/5%/50% output waveforms respectively, where CH1 is the PWM dimming signal, CH2 is the voltage at OUT node, CH3 is the voltage at FB node, CH4 is the 5-times LED forward current.

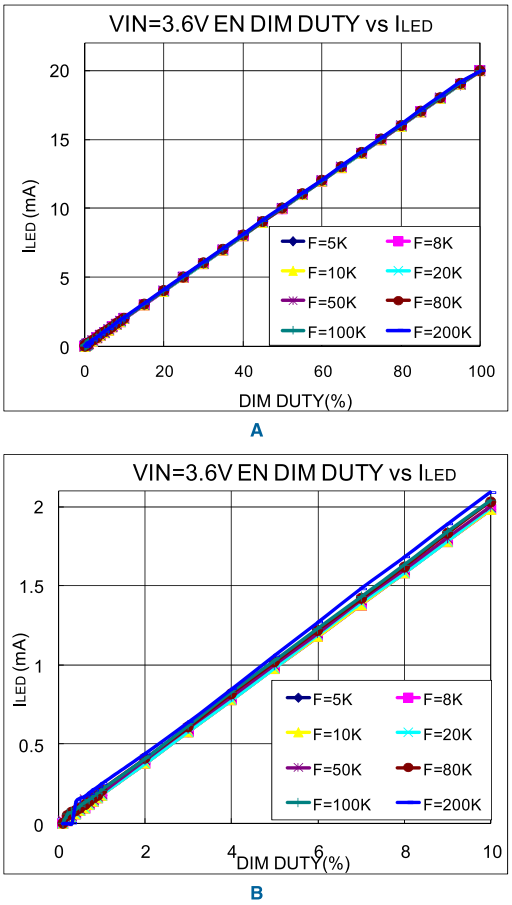

FIGURE 13. The graph of I_{LED} vs dimming duty cycle. A is the whole range drawing with D from 0.1% to 100%. B is the enlarged graph with D≤10%.

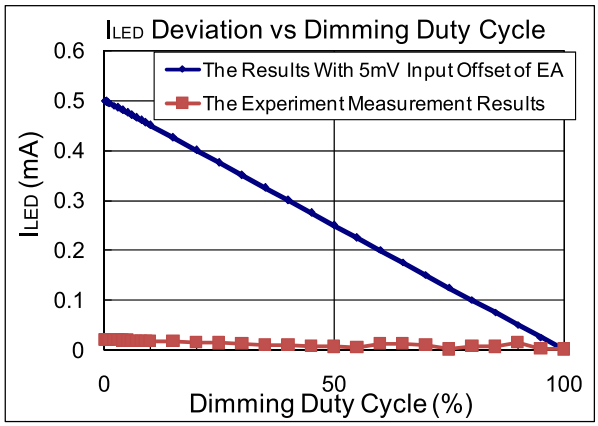

FIGURE 14. The I_{LED} deviation from the ideal value with dimming duty cycle range: 0.1% to 100%; the blue line is the data for EA with 5mV input offset voltage; the brown line is the presented method measurement.

of dimming frequencies, I_{LED} deviates more from the ideal value, as shown in the F=200KHz curve in Fig. 13B. This imperfection is caused by U_1's EN interface non-ideality, because the interface cannot completely replicate the dimming duty cycle to the internal KD2V block, especially in a small duty cycle.

The I_{LED} deviation comparison of the proposed method and the EA's input offset voltage being 5mV is illustrated in Fig. 14. The proposed method provides less than 30μA deviation and mostly keeps a constant error from the ideal I_{LED} with the dimming duty cycle ranging from 0.1% to 100%. On the contrary, the I_{LED} deviation grows larger as duty cycle becomes smaller. The maximum reaches 0.5mA at duty cycle being 0.1%.

Fig. 15 gives the relationship between I_{LED} and V_{IN} at different duty ratios with V_{IN} ranging from 2.7V∼5.5V. This graph shows that the I_{LED} precision is not affected by the operating power supply even at different dimming duty cycles. When D ranges from 0.5% to 10%, the I_{LED}

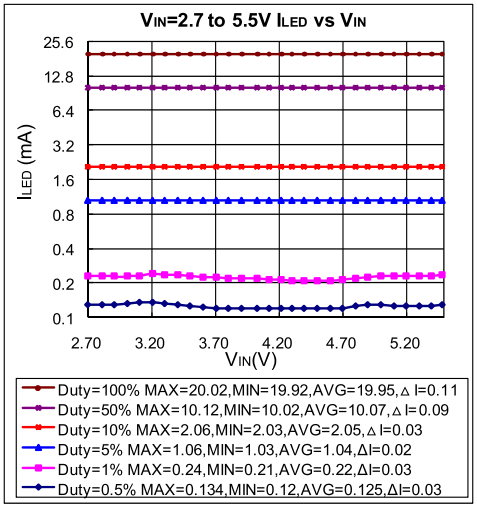

FIGURE 15. The LEDs forward current with V_{IN} ranging from 2.7V to 5.5V at different PWM dimming duty cycle.

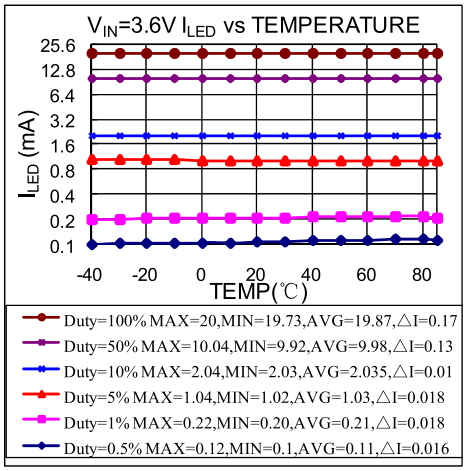

FIGURE 16. The I_{LED} vs PWM dimming duty cycle within temperature range: −40°C to 85°C.

vibration is about 30μA. So the equivalent V_{FB} vibration is about 0.3mV and the vibration without a clear regular pattern can be considered as measurement mistake. The similar phenomenon occurs with D=50%/100%, the I_{LED} variation is about 100μA, and the equivalent V_{FB} vibration is about 1mV with V_{FB} DC value at 100mV/200mV.

In order to further verify the change of the dimming method with temperature, I_{LED} is shown in Fig. 16. As the temperature increases from −40°C to 85°C, I_{LED} mostly keeps constant except when the vibration is induced by measurement mistake.

The I_{LED} of 200 samples was measured at room temperature with D=0.5% and D=1% (Fig. 17). Fig. 17A shows that the I_{LED} average is 0.11mA at D=0.5% with a mean of 0.017mA. Fig. 17B shows that the I_{LED} average is 0.2mA at D=1% with a mean of 0.015mA. These 200 samples data indicates that the experimental LED driver analog dimming precision is adequate for minimum dimming duty D=0.5%. It even supports D=0.3%.

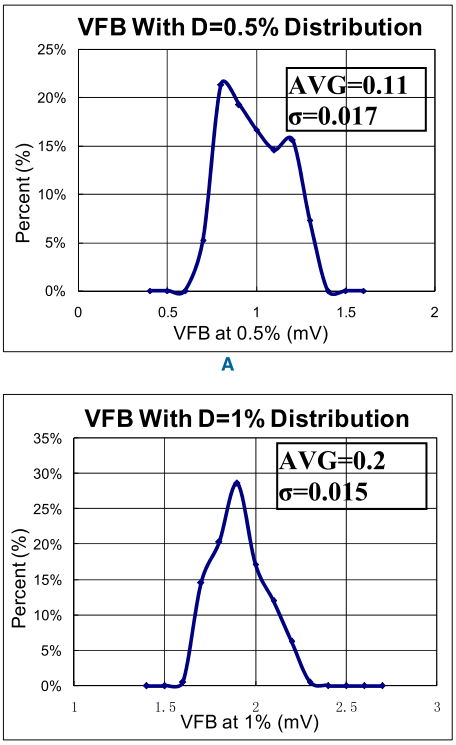

FIGURE 17. I_{LED} distribution within PWM dimming duty cycle is 0.5% and 1% with 200 samples. A is D=0.5%. B is D=1%.

TABLE 2. Comparison of the precision of analog dimming.

Reference	D_{MIN}	DIM Mode Analog or PWM	Variation
TPS54200/1	1%	Both	-0.1%~+0.4%
TPS61169	1%	Both	-
MP2341	2%	Analog	-
MP3312	1%	Analog	-
SGM3735	3%	Analog	-
[3]	5%	Analog	-
	2%	PWM	-
[5]	0.025%	PWM	-
[6]	0.02%	PWM	-
[8]	0.02%	PWM	-
	6%	Analog	-
This Work	0.5%	Analog	-0.2%~+0.2%

Table 2 shows the comparison of the minimum analog dimming duty and variation among commercial LED drivers, latest literatures and the proposed method. The presented work is 2 times better than that of the other LED drivers in analog dimming mode.

Furthermore, a chopper structure substitutes for the auto-zero technique to realize the DOC OP1 with Gain=K block for switches charge injection reduction. A smaller minimum dimming duty and a higher I_{LED} precision will be achieved.

V. CONCLUSION

In this paper, we have presented an accurate control method for a weak voltage analog dimming application. In this

method, by combining the temperature compensation for the calibration current reference, the N-Bits ASOC reduces the analog dimming error to $V_{OSMAX}/2^N-1$ throughout the PVT corner with dimming duty ranging from 0.5% to 100% and without any current load feeding to the weak dimming reference. What's more, with the same LED current sampling component, the DOC amplifier and KD2V can reduce the residual dimming error by K-times when working together. Compared with several current commercial products and latest literatures, this work exhibits half dimming error of the previous parts. Based on the statistical analysis of the test results of 200 samples, this method meets the technical requirements of mass production for high precision I_{LED} dimming.

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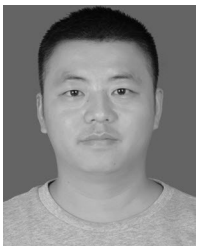

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