

Analysis and Verification of a New Photoelectric-Motivated Memristor Based on Avalanche Photo-Diode

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ABSTRACT This work reports a device based on photoelectric-motivated memristor. In this paper, the simulation model of photoelectric-motivated memristor was established, and we stimulated the memristive characteristics by this model. The device goes from the non-triggered state to the triggered state, then back to non-triggered state and we obtained the simulation results. Then the current curve and the voltage curve fit a hysteresis loop of this device. The results of this memristive characteristics are verified by the test of the real photoelectric-motivated memristor device. According to the memristive properties of this device, it can be used to study the memristor circuit integrated with avalanche photo-diode and signal processing circuit, and applied in neural network and a new type of photoelectric memory.

INDEX TERMS Photoelectric-motivated memristor, hysteresis loop, memristive characteristics.

I. INTRODUCTION

It has passed 37 years from the conception of memristor to the first realization of physical memristive device. The first device is a nanoscale TiO_2 memristor created by Strukov *et al.* [1]. With the deepening research on memristor, researchers had successively developed different memristive devices, such as ferroelectric memristor [2], ferroelectric tunnel memristor [3], light-emitting memristor [4], memristive diode bridge with LCR filter [5], [6], light sensitive memristor [7] and so on. Meanwhile, researchers had developed different models for memristor [8]–[10]. Depending on the applied bias voltage, the light sensitive memristor [7] charges or discharges the quantum dots, leading to reduction or increment the conductance. In this paper, the avalanche carrier memristor theory based on photoelectric-motivated memristor was established.

Lu Zhang *et al.* carried out a study on memristor and collected the measurement data of the real $\text{TiO}_2/\text{TiO}_{2-x}$ memristor device [11]. A memristor simulating $\text{TiO}_2\text{-TiO}_{2-x}$ validates a compact model of transition region motion based on classical ion transport theory. It is consistent with the static and dynamic switching characteristics of the simulation equipment. In this paper, a model of photoelectric-motivated memristor was simulated by Multisim software. The model

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verifies the memristive behavior by measuring the voltage of the resistor and the current values of this device. The model proves the voltage lags behind current and carries out actual tests to verify the simulation results of the model. Researchers also studied on human forgetting curve based on NiO memristor [12], and biological synaptic research applications. However, memristive devices made of nanomaterials are expensive. It is difficult to obtain commercial large-scale applications, and cannot be integrated on a large scale. Under this circumstance, a new type of photoelectric-motivated memristor was proposed, which has a low cost and is accessible for large-scale integration. This memristive device provides a reference for the large-scale integration of memristor and signal processing. This device also has a useful application prospect in both neural network [13], [14] and memory [15], [16].

II. PRINCIPLE ANALYSIS AND SIMULATION OF PHOTOELECTRIC-MOTIVATED MEMRISTOR

A. ANALYSIS OF PHOTOELECTRIC-MOTIVATED MEMRISTOR PRINCIPLE

When this devices are operated in the reverse bias state, there are 4 zones, namely, N, P, IN and M (N is the electron-type semiconducting region, P is the hole-type semiconducting region, IN is the intrinsic region, and M is the doubling region). Generally, the voltage drop in the N zone and the

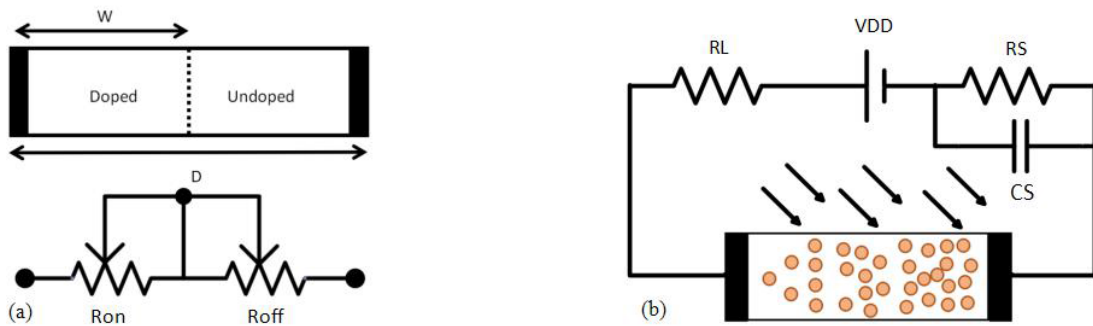


FIGURE 1. (a) Physical model of a memristor proposed by HP Lab; (b) conceptual geometry for a photoelectric-motivated memristor which based on Avalanche Photo-diode, RL is the quenching resistor, RS is the sampling resistor, CS is the bypass capacitor or parasitic capacitor.

P zone is ignored. Therefore, the voltage drop of the applied voltage is only in the IN region and the M region. When the photo-voltaic effect occurs in the device, the photo-generated carriers in the N and P regions can be ignored.

We can introduce a physical model for a two-terminal memristor developed by HP laboratory [1]. Within a section of its state variable w , its characteristics are consistent with the definition of an ideal memristor, as shown in Fig. 1(a). Doping is performed between the two pole metals, and the state of the device is controlled by the applied voltage. Assume that the thickness of the electrode removed by the device is D , and a region with a higher doping concentration is included, the resistance value is small, set to w , and the value of the doped region is $[0, D]$. The other part is a low doped region with a large resistance value. We can reflect the change in the resistance of the device by the change in w/D . When an external bias is applied, the boundaries of the doped and undoped regions will vary with changes in bias voltage. When $w/D = 1$, the entire device is a doped region, and the value of the memristor is R_{ON} . When $w/D = 0$, the device is an undoped region, and the resistance of the memristor is R_{OFF} .

This model can be used to describe a model for photoelectric-motivated memristor. When the relationship between voltage V and current I_A is a function related to the memristive value $M(q(t))$, there are two different resistance states of photoelectric-motivated memristor. If photoelectric-motivated memristor is in non-triggered state and then the conductive electrons or holes inside the photoelectric-motivated memristor are less. The photoelectric-motivated memristor conductivity is weak, and the device of the equivalent resistance is large, memristor value can be represented by R_{OFF} . When the device is in illumination, this device will be triggered by the light-generated carrier. When the device is in dark, this device will be triggered by noise. In both cases, avalanche effect can be triggered, resulting in carrier multiplication in the knot.

The device electron concentration or hole concentration is increased due to the avalanche effect in the device. Electron concentration or hole concentration promotes the conductivity of this photoelectric-motivated memristor, thus the

photoelectric-motivated memristor exhibits a small resistance under the triggered condition. According to equation (1), the memristive value $M(q(t))$ function changes and the value of I_A increases. Moreover, according to the law of conservation of energy, the external light or noise internally converted to carriers, and the carriers is multiplied by the avalanche effect further. The value of current I_A increases due to the avalanche multiplication effect in this device. In conclusion, if the device is in the triggered state of the external reverse bias voltage, the conductivity of the device is high, and the device of the equivalent resistance is small, memristor value can be represented by R_{ON} .

$$V = M(q(t)) * I_A \tag{1}$$

B. PHOTOELECTRIC-MOTIVATED MEMRISTOR MODEL SIMULATION

The APD (Avalanche photo-diode) passive quenching circuit [17]–[19] is used to validate memristive characteristics of photoelectric-motivated memristor. The photoelectric-motivated memristor of operating voltage is lower than the avalanche voltage, therefore the avalanche multiplication time produced by photoelectric-motivated memristor is quenched slowly than the SPAD (Single Photon Avalanche Diode Detector) avalanche multiplication time. The passive quenching of the photoelectric-motivated memristor only needs voltage drop in circuit. If there is a series resistor in the photoelectric-motivated memristor, the voltage drop of resistor rises gradually with the increase of the current I_A , which reduces the voltage drop in the IN and M region, thus slowing down growth rate of the avalanche. Finally, the growth and extraction rates are balanced, thus the stable state is formed. At this point, the current will not increase (or decrease), and the series resistance is provided a negative feedback function, which inclines to steady the vacillation of current level. Fig. 1(b) shows the memristive property circuit of the photoelectric-motivated memristor. The series resistor R_L causes the circuit a voltage drop to quench the avalanche. A capacitor C_S connected in parallel to the sampling resistor R_S of this quench circuit, is used to lag the value of the voltage

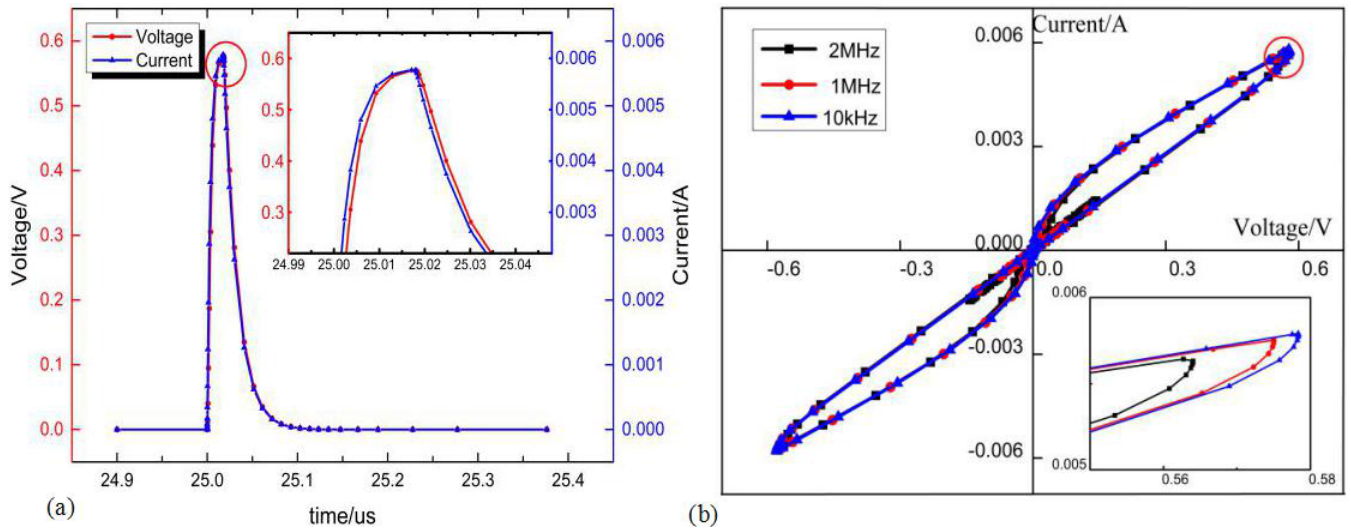


FIGURE 2. (a) Sampling resistor voltage (red line) and current (blue line) pulse waveform in 105 V bias; (b) I-V curve of photoelectric-motivated memristor anti-offset avalanche pulse fitting. The applied voltage is $V = 74.257 \sin(\pi f * t)$, when f is different, the tight hysteresis loop of I-V fit, $f = 10 \text{ kHz}$ tight hysteresis loop(blue line), $f = 1 \text{ MHz}$ tight hysteresis loop(red line), $f = 2 \text{ MHz}$ tight hysteresis loop(black line).

and form the I-V of the photoelectric-motivated memristor hysteresis loop.

When time of the avalanche effect in the photoelectric-motivated memristor is controlled by the light pulse, if the time of the light pulse exceeds the time of avalanche generation in the photoelectric-motivated memristor, the avalanche carriers in the photoelectric-motivated memristor cannot increase the current of the photoelectric-motivated memristor indefinitely. Thence, the current can be regarded as a fixed value. It shows that degree of avalanche in photoelectric-motivated memristor is affected by the external optical power, but the avalanche current cannot increase without restrictions. The dark count of photoelectric-motivated memristor is the other method provided by the test to validate memristive characteristics. Since the energy of the noise is disordered, the current generated by the avalanche effect is not a definite value. When an avalanche effect occurs under a dark count, the photoelectric-motivated memristor under this state will be quenched immediately. Also, Multisim is used to simulate the memristor characteristics when photoelectric-motivated memristor is under dark count. In order to match the actual measurement conditions, the dark count of photoelectric-motivated memristor is chosen to simulate the memristive characteristics.

C. SIMULATION RESULTS AND ANALYSIS

This work uses Multisim software to simulate photoelectric-motivated memristor triggered in light. The curve data is extracted under the condition of the applied reverse voltage $V = 74.257 \sin(\pi f * t)$ and frequency $f = 10 \text{ kHz}$. Fig. 2(a) shows the curves of current and voltage for this device. The quench time of avalanche voltage for the simulated photoelectric-motivated memristor is 18 ns, and the recovery time of avalanche voltage is 60 ns. The selected sampling

TABLE 1. The parameters of photoelectric-motivated memristor model.

Symbol	Quantity	Value
V	applied reverse voltage	74.257 V
R_S	sampling resistor	100 Ω
R_L	quenching resistor	120 k Ω
C_S	parasitic capacitor	25 pF
f	frequency of applied voltage	10 KHZ/1 MHz/2 MHz
V_{pulse}	pulse voltage of simulated photon	5 V
T_r/T_f	rise time/fall time of pulse voltage	10 ps/10 ps
T_w	pulse voltage width	60 ns

resistance is 100 Ω in the circuit. The peak value of avalanche pulse voltage for the simulated model is 580 mV and the avalanche pulse current is 5.8 mA. The avalanche time in this device is equal to the time for charging the photoelectric-motivated memristor. The charging process is a slow process due to the equivalent junction capacitance. Because of the existence of hysteresis behaviour in memristive devices, the voltage curve of the device lags behind the current curve under trigger state. When avalanche effect occurs in photoelectric-motivated memristor, the number of carriers increases in this device, resistance in the device decreases gradually. Then the conductivity increases gradually. Finally, the device is under the minimum resistance states when the number of carriers is in the majority. As the device is quenched, the number of carriers is gradually reduced. At the same time, the conductivity is also related to the applied bias voltage. When voltage of the device is high but below the avalanche voltage, the avalanche multiplication effect can form a larger avalanche current due to the increase of the external electric field, and the conductivity of the device is also larger.

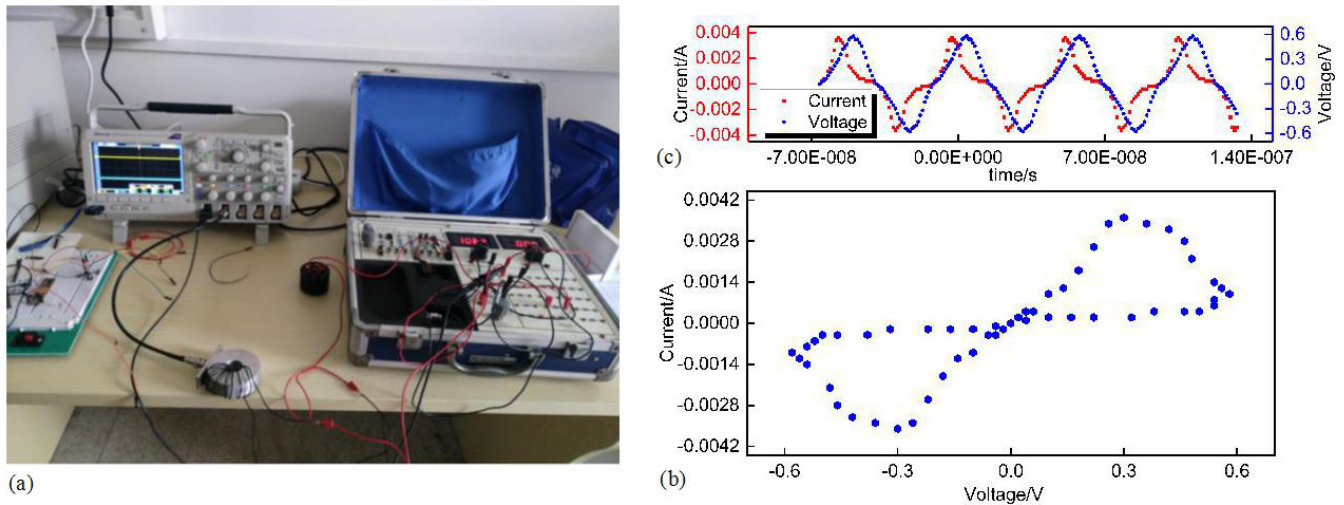


FIGURE 3. (a) Characteristic test platform for photoelectric-motivated memristor; (b) hysteresis loop of the tested photoelectric-motivated memristor; (c) sampling resistor voltage (blue line) and current (red line) of the tested photoelectric-motivated memristor in 105 V bias.

Fig. 2(a) shows the avalanche pulse curve of current and voltage. The value of the extracted current and voltage can be fitted to a hysteresis loop, such as the hysteresis loop shown in Fig. 2(b) in 10 kHz. This paper extracts the current curve and the sampling voltage curve at different frequencies of the photoelectric-motivated memristor. And the data of the extracted current and voltage is fit for a hysteresis loop. Then the characteristic curve of the photoelectric-motivated memristor is showed in Fig. 2(b). Fig. 2(b) shows the current curve and sampling voltage curve of photoelectric-motivated memristor when the frequency is 10 kHz, 1 MHz, and 2 MHz. When the frequency of the photoelectric-motivated device rises to 1 MHz, the part of hysteresis loop nearby the origin presents linear relation. When the frequency rises to 2 MHz, the linear length increases. In Fig. 2(b), comparing the side-lobe areas of three curves at different frequencies, the side-lobe area decreases as the frequency increases. When the frequency of the photoelectric-motivated rises to 1 MHz and 2 MHz, the hysteresis loop is approaching the origin fitted by photoelectric-motivated memristor, then the hysteresis loop moves to the highest position of the positive axis and the lowest of the negative axis, and making part of the curve linear. Moreover, the side-lobe area of the three hysteresis loops in Fig. 2(b) is getting smaller and smaller as the frequency increases. The curve of photoelectric-motivated memristor simulation accords with the definition of memristor proposed by Professor Chua, and it can be fitted to a hysteresis loop. At a certain frequency, the side-lobe area decreases as the frequency increases. Fig. 2(b) shows that the area of the hysteresis loop decreases with increasing frequency. Therefore, it can be inferred that when the frequency is increased to a certain extent, the last fitted hysteresis loop can shrink to a single-valued function.

III. TEST PLATFORM AND VERIFICATION ANALYSIS

Fig. 3(a) is the physical device for measuring memristive characteristic of the photoelectric-motivated memristor.

As showed in Fig. 3(a), the platform consists of three parts: A, B, and C. A is an oscilloscope, mainly used for pulse waveform display and pulse waveform data extraction. B is a photon detection experiment platform, providing a stable bias of photoelectric-motivated memristor. C is photoelectric-motivated memristor, and the device is AD500-8.

The tested device is AD500-8. The avalanche voltage value of this device is 120 V-130 V. This is to ensure that the tested photoelectric-motivated memristor works in the linear mode. When the device is under the external reverse bias voltage of 105 V, the sampling resistance voltage is 580 mV, the peak current of photoelectric-motivated memristor is 3.6 mA, and sampling resistance is 100 Ω in the circuit, it can be seen from the Fig. 3(c) that the peak voltage is significantly behind the peak current. Fig. 3(b) is compared with the hysteresis loop in Fig. 2(a), the actual test currently has an error of 2.2 mA due to the error of the test system. However, the frequency of the photoelectric-motivated memristor is out of control because the device is triggered by noise in the case of dark counting, and it is impossible to actually verify that the side-lobe area of hysteresis loop for photoelectric-motivated memristor decreases as the frequency increases. Based on the comparison between experiment and simulation, this paper finds that the two hysteresis loops are different. The difference is caused by the errors of the sampling voltage, sampling current, the quench time and the simulation recovery time. Although the hysteresis loop formed during simulation and testing is different, the corresponding current and voltage curves in the device can be fitted to form hysteresis loops.

IV. CONCLUSION AND PERSPECTIVES

In conclusion, this paper has established a memristive characteristics theory of the photoelectric-motivated memristor, the quenching circuit simulation of the photoelectric-motivated memristor, the quenching circuit test of the photoelectric-motivated memristor and verification of the

memristive property in this device. The I-V characteristic curve has been simulated by this model, and the test of the photoelectric-motivated memristor has been done. Due to the influence of the test instruments, the experimental results are merely similar to the simulation results. However, the extracted data of the I-V curve has confirmed the hysteresis behavior of the voltage-current and it can be fitted to the hysteresis loop. The photoelectric-motivated memristor has proved the general characteristics of the memristive device. Analyzing the change in the resistance value of the circuit, the research results have described memristive behavior of photoelectric-motivated memristor, and this device provides a reference for the large-scale integration of the memristor and the signal processing circuit.

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REFERENCES

- [1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
- [2] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, and J. Grollier, "A ferroelectric memristor," *Nature Mater.*, vol. 11, pp. 860–864, Sep. 2012.
- [3] D. J. Kim, H. Lu, S. Ryu, C.-W. Bark, C.-B. Eom, E. Y. Tsymbal, and A. Gruverman, "Ferroelectric tunnel memristor," *Nano Lett.*, vol. 12, no. 11, pp. 5697–5702, Oct. 2012.
- [4] A. A. Zakhidov, B. Jung, J. D. Slinker, H. D. Abruña, and D. G. Malliaras, "A light-emitting memristor," *Organic Electron.*, vol. 11, no. 1, pp. 150–153, Jan. 2012.
- [5] F. Corinto and A. Ascoli, "Memristive diode bridge with LCR filter," *Electron. Lett.*, vol. 48, no. 14, pp. 824–825, Jul. 2012.
- [6] B.-C. Bao, P. Wu, H. Bao, M. Chen, and Q. Xu, "Chaotic bursting in memristive diode bridge-coupled Sallen-Key lowpass filter," *Electron. Lett.*, vol. 53, no. 16, pp. 1104–1105, Aug. 2017.
- [7] P. Maier, F. Hartmann, M. R. S. Dias, M. Emmerling, C. Schneider, L. K. Castelano, M. Kamp, G. E. Marques, V. Lopez-Richard, L. Worschech, and S. Höfling, "Light sensitive memristor with bidirectional and wavelength-dependent conductance control," *Appl. Phys. Lett.*, vol. 109, no. 2, Jun. 2016, Art. no. 023501.
- [8] H. Tan, G. Liu, H. Yang, X. Yi, L. Pan, J. Shang, S. Long, M. Liu, Y. Wu, and R.-W. Li, "Light-gated memristor with integrated logic and memory functions," *ACS Nano*, vol. 11, no. 11, Oct. 2017.
- [9] A. G. Radwan, M. A. Zidan, and K. N. Salama, "HP memristor mathematical model for periodic signals and DC," in *Proc. 53rd IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2010, pp. 861–864.
- [10] Y. V. Pershin and M. D. Ventra, "SPICE model of memristive devices with threshold," *Radioengineering*, vol. 22, no. 2, pp. 485–489, Apr. 2012.
- [11] L. Zhang, Z. Chen, Y. J. Joshua, B. Wysocki, N. McDonald, and Y. Chen, "A compact modeling of $\text{TiO}_2\text{-TiO}_{2-x}$ memristor," *Appl. Phys. Lett.*, vol. 102, no. 15, Apr. 2013, Art. no. 153503.
- [12] S. G. Hu, Y. Liu, T. P. Chen, Z. Liu, Q. Yu, and L. J. Deng, "Emulating the ebbinghaus forgetting curve of the human brain with a NiO-based memristor," *Appl. Phys. Lett.*, vol. 103, no. 13, Sep. 2013, Art. no. 133701.
- [13] A. Fabien, E. Zamanidoost, and D. B. Strukov, "Pattern classification by memristive crossbar circuits using ex situ and in situ training," *Nature Commun.*, vol. 4, Jun. 2013, Art. no. 2072.
- [14] R. Guo, Y. Zhou, L. Wu, Z. Wang, Z. Lim, X. Yan, W. Lin, H. Wang, H. Y. Yoong, S. Chen, Ariando, T. Venkatesan, J. Wang, G. M. Chow, A. Gruverman, X. Miao, Y. Zhu, and J. Chen, "Control of synaptic plasticity learning of ferroelectric tunnel memristor by nanoscale interface engineering," *ACS Appl. Mater. Inter.*, vol. 10, no. 15, pp. 12862–12869, Mar. 2018.
- [15] M. N. Sakib, R. Hassan, S. N. Biswas, and S. R. Das, "Memristor-based high-speed memory cell with stable successive read operation," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 5, pp. 1037–1049, May 2017.
- [16] M. A. Lastras-Montañó and K.-T. Cheng, "Resistive random-access memory based on ratioed memristors," *Nature Electron.*, vol. 1, no. 8, pp. 466–472, Aug. 2018.
- [17] W. Wang, T. Chen, J. Li, and Y. He, "The research of high photon detection efficiency CMOS single photon avalanche diode," *Acta Photonica Sinica*, vol. 46, no. 8, Aug. 2017, Art. no. 0823001.
- [18] W. Xu, F. Chen, M. Chen, and Y. Xiao, "Characteristic analysis of avalanche photodetector based on equivalent circuit model," *Semicond. Optoelectron.*, vol. 32, no. 3, pp. 336–338 and 355, Jun. 2011.
- [19] X.-L. Jin, C. Can, and Y. Hong-Jiao, "Design and implementation of high performance single-photon avalanche diode in 180nm CMOS technology," *J. Infr. Millim. Waves*, vol. 37, no. 1, p. 30, Jun. 2018.



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