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Real-Time HIL Implementation of a Single-Phase Distribution Level THSeAF Based on D-NPC Converter Using Proportional-Resonant Controller for Power Quality Platform

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ABSTRACT In this paper a single-phase transformer-less hybrid series active filter (THSeAF) based on duo-neutral-point-clamped (D-NPC) converter to address distribution level power quality is proposed to investigate experimentally the efficiency of the hardware-in-the-loop (HIL) implementation for power electronics applications. This benchmark contributes to demonstrating the capability and efficiency of such real-time implementation for smart grid power quality (PQ) analysis which requires fast switching process with small sampling time. Such applications require the compensator to address major power quality issues related to a nonlinear load. This compensator presents an efficient and reliable solution for future grid applications to overcome voltage and current related issues as well as assisting the integration of renewables for a sustainable supply. The controller extracts voltage and current harmonics to be compensated. A proportional and resonant (P + R) regulator produces switching signals for the D-NPC converter. The paper demonstrates the reliability of the HIL simulation for power electronic applications assessing power quality related issues where a wide range of switching frequency is under study. A combination of simulation and real-time results are carried out to validate the performance and viability of the HIL implementation.

INDEX TERMS Duo-neutral-point-clamped (D-NPC) converter, hardware-in-the-loop, single-phase active filter, power quality of smart grid, real-time application.

I. INTRODUCTION

The HIL and Power-HIL (PHIL) are concepts quite established to study the behavior of systems with the fundamental 50 or 60 Hz. Regarding the limitation of the time-step imposed by the real-time (RT) simulators [1], it is challenging to study the behavior of high-frequency signals such as harmonics of a power system. In those cases the harmonics are not taken into account and are mostly out of scope of the study. The key objective of this paper is to investigate the potential and feasibility of HIL implementations for a power quality assessment implicating high frequency signals such as harmonics [2], [3]. This paper demonstrates the capability of pure HIL implementations for applications requiring as low as possible sampling times. The smart grid associated with the continuous increase of power electronic converters, drives, as well as domestic and industrial nonlinear loads has created a serious concern on the power quality of the future distribution power systems. The reason why, such implementations are becoming crucial and game changer tools especially for PQ studies. Moreover, with the electric vehicles (EV) market under considerable growth [4], it became essential to investigate their nonlinear behavior for the PQ purposes [5]. Moreover, in some existing North American EV charging stations, the cars are connected between two phases of the three-phase four-wire (3P4W) system, creating heavy unbalances.

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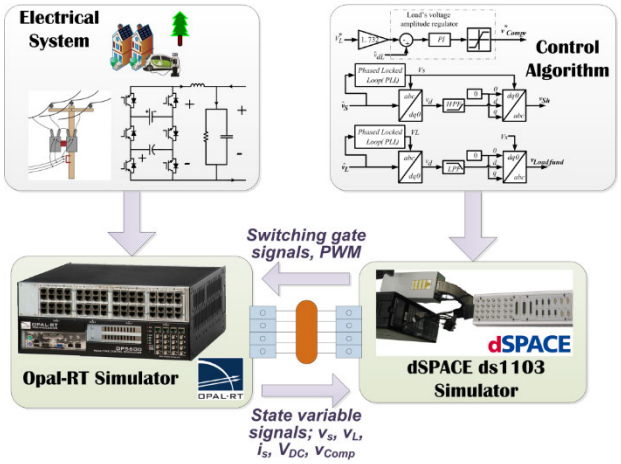


FIGURE 1. Hardware-in-the-Loop test bench realized in laboratory by means of two separate real-time simulators.

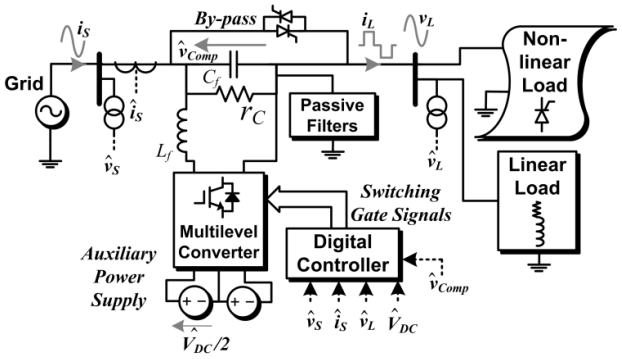


FIGURE 2. Electrical circuit connection with D-NPC-THSeAF connected in series implemented in the Opal-RT.

On the other hand, pushed by social efforts, governments start to investigate more on implementation of renewable energy sources, creating research and developments in this field [6], [7].

This multifunctional compensator will clean the harmonic pollution of current drawn by the nonlinear loads from the utility and, on the other hand, similar to a dynamic voltage restorer (DVR) it will eliminate voltage distortions from the point of common coupling (PCC) [8]. This compensator could inject or absorb active power during grid voltage variations to ensure high quality supply along with complete decoupling from polluted loads [9]. The application of multilevel converters for a single-phase THSeAF has been published in [10].

Meanwhile, with the improvement in HIL technologies, it is now possible to implement complex power electronics systems and testing them in a non-invasive condition [11], [12]. This allows the operator to test critical scenarios and perform faulty conditions to the electrical system without a power outage. In fact the power system and power electronics components are simulated on the Opal-RT real-time simulator and the controller is implemented in the dSPACE-1103 simulator. The two RT simulators are connected to each other, therefore, creating an HIL system [6] as shown in Figure 1 [13]. This paper uses new informatics development to address the new research challenges that are facing the power electronics converters in participating to the mitigation of pollution and enhancing the reliability of the grid [14], [15].

The efficient and affordable solution proposed in this paper uses a multilevel D-NPC configuration [16], [17] to reduce dc side voltage for low-level distribution system as demonstrated in Figure 2. The use of this device will facilitate the integration of energy storage systems and renewables for modern households [18]. The configuration does not necessitate the bulky series transformer which constitutes a key improvement for a cost-effective power quality enhancer [19].

The system shown in Figure 2 is implemented in a real-time Opal-RT simulator, while the controller is loaded on the dSPACE. This unit is then connected via isolated cables to the dSPCAE DS1103 which holds the control algorithm inside. The DS1103 receive via analog inputs the measured probes and after performing calculation it returns from the digital outputs, the control signals to the Opal-RT module. On the other hand, the Opal-RT simulator which emulates the electrical system receives the control signals by means of its Digital Inputs. The simulator returns the state variables of the system on its analog outputs. These signals are sent to the dSPACE. This closed-loop HIL is suitable to evaluate the performance of both the proposed electrical configuration and the control algorithm.

In fact, there exist numerous advantages in real-time simulation over offline simulation. The HIL implementation could be a step between the offline simulation and the prototype or industrial production process. The traditional production process is started by initial study, then pure offline simulation of the product in which various tests are performed for critical scenarios, followed by the prototype production where test and validations are made, and finally the mass production [20].

This process could be somehow very costly and expensive. The addition of the HIL test after the simulation process has been completed will help the developers and researchers to perform more advance quality tests and studying in depth the proper operation of each section; the controller (algorithm) and the power electrical system, separately. In this step it became much easier to evaluate the impact of numerous phenomenon on the ideal system; the delay time imposed by the measurement devices, the controller delay, the discretization of the controller implementation in the micro controller and much more. Especially, in offshore systems and marine engineering applications, electrical control systems and mechanical structures are generally developed and designed in parallel. Moreover, evaluation and testing of the control systems is only possible after integration. These will generally results in numerous errors that should be solved during the commissioning, with the high potential risks of human injuries, damaging costly equipment and higher operational delays as shown in the following comprehensive table. For this reason, in this special area, the HIL

TABLE 1. Comparison of the proposed HIL Platform for Power electronic applications.

Definition	Proposed HIL system	Off-line simulation	Power laboratory setup
Number of burden application type and their typology	Multiple	Multiple	Limited number
Spent development schedules time	Tight	Fastest	Over several month
Industrial production costs	Low	The Lowest	High
Quality and accuracy of testing	High	Low	Very High
Possibility of testing critical scenarios (Destructive physical analysis, DPA)	High	High	Very Low
Early process human factor	Low	Low	High
Usage in various disciplines	High	High	Low
Safety for equipment	High	High	Low
Power electronics applications	Moderate Switching Frequency	High Frequency	High Frequency
THD & Harmonic precision	Moderate	High	Most precise
Overall Cost	Moderate	Low	High

simulation is gaining widespread popularity and attention. The Table 1 illustrates the advantages of the HIL implementation for power electronics application over pure simulation techniques.

II. HIL ARCHITECTURE

A. ELECTRICAL SYSTEM CONFIGURATION

The electrical system depicted in Figure 2 is composed of a multilevel single-phase converter connected in series between the utility and the house entrance connected terminals. The transformerless hybrid series active filter is composed of a five-level D-NPC converter [17], [21] depicted in Figure 3, connected in series between the utility and the entrance of the building. An auxiliary supply is connected on the dc side. To filter high frequency switching harmonics, a passive filter is used.

A bank of tuned passive filters as shown in Figure 2 with F_5, F_7, F_{11}, and F_{HPF} described in Table 2, ensure a low impedance path for current harmonics. In this paper the studied system is implemented for a rated power of 5 kVA. To ensure a fast transient response with sufficient stability margins over a wide range of dynamic operations, the controller is implemented in a dSPACE real-time simulator as explained in the previous section. For an accurate real-time connection between the two simulators, an isolating card are used to adapt the In/Out of both modules. With system

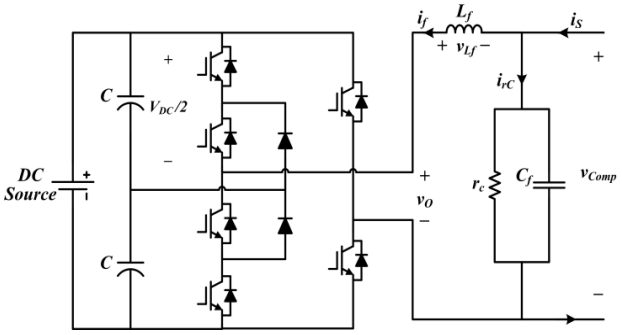


FIGURE 3. D-NPC converter topology implemented for the THSeAF compensator.

TABLE 2. HIL system parameters.

Symbol	Definition	Value
V_S	Line phase-to-neutral voltage	120 Vrms
f	System frequency	60 Hz
L_S	Supply equivalent inductance	150 µH
R, C	Non-linear load	8 Ω, 1000 µF
R, L	Linear load	6.5 Ω, 20 mH
Lf	Switching ripple filter inductance	2.5 mH
Cf	Switching ripple filter capacitance	0.5 µF
r_C	Switching ripple damping resistor	60 Ω
$Ts1$	Opal-RT Synchronous sampling time	42 µs
$Ts2$	dSPACE sampling time	36 µs
f_{PWM}	PWM frequency	4.63 kHz
F_5	Fifth order shunt passive filter	56µF, 5mH
F_7	Seventh order passive filter	14µF, 10mH
F_{11}	Eleventh order passive filter	6µF, 10mH
F_{HPF}	High-pass filter	2µF
K_P, K_r	Controller proportional and resonant gains	2.5, 10
ω_C	Cutoff frequency	5 rad/s
V_{DC}	dc auxiliary power supply voltage	100 V

parameters identified in Table 2, the compensator D-NPC converter is depicted in Figure 3.

On the DC side of the compensator, auxiliary dc-link energy storage components are installed at a reduced voltage level of 100V. The objective is to propose an efficient device capable of rectifying current related issues in smart grids which also provide sustainable and reliable voltage supply at the point of common coupling that define the entrance of residential or commercial buildings [22].

Using the circuit of Figure 2 showing the block diagram and model of equivalent house circuit connection with utility meters and D-NPC-THSeAF connected in series as shown in Figure 4, several critical scenarios such as grid distortion, sag or swell are simulated as illustrated in Figure 5. The D-NPC-THSeAF connected in series injects a compensating voltage which results in a drastic improvement of source current distortions and a cleaned load voltage.

In this work the approach to achieve optimal behavior during the time the grid is perturbed is implemented in the

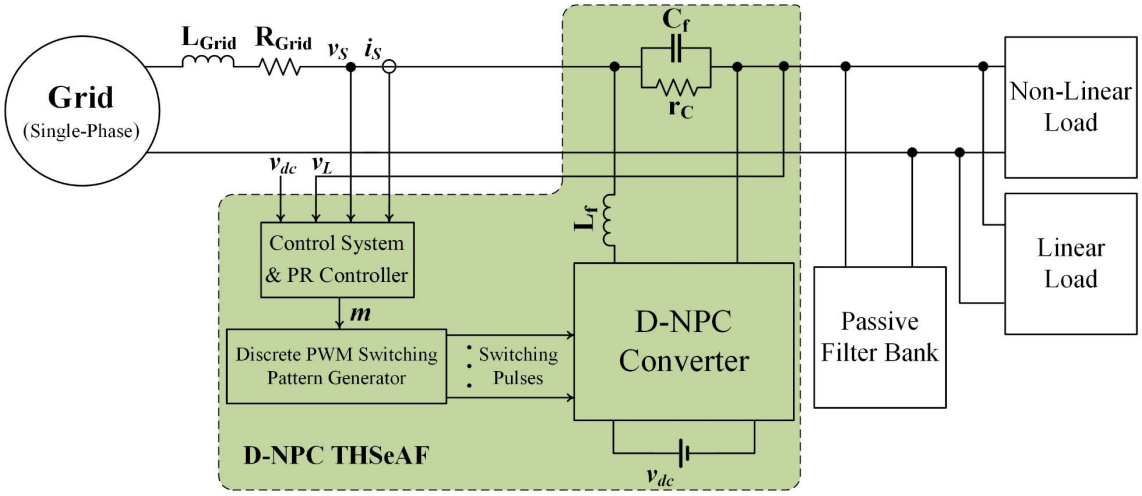


FIGURE 4. The offline simulation schematic diagram.

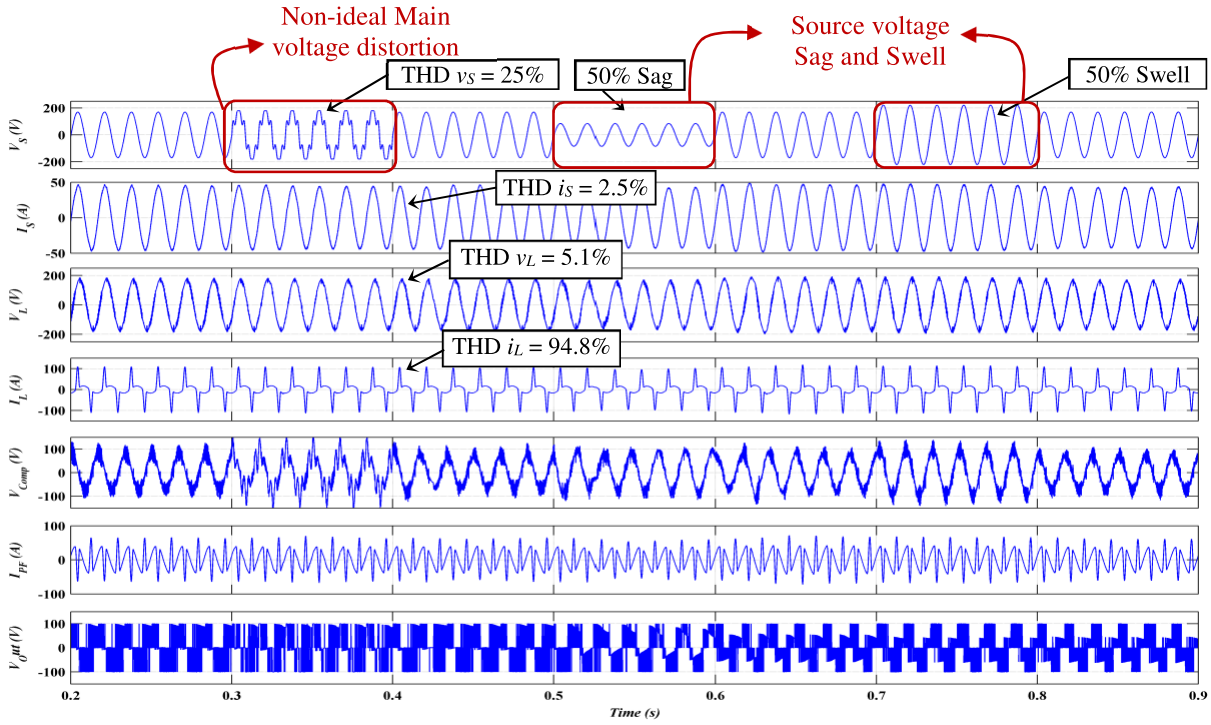


FIGURE 5. The results of simulation for the THSeAF compensating current harmonics and voltage regulation, during grid initiated distortions. (a) Source voltage v_S, (b) source current i_S, (c) load voltage v_L, (d) load current i_L, (e) active-filter voltage V_{Comp}, (f) Harmonics current of the passive filter i_{PF}, (g) Converter's output voltage V_{Out}.

controller [23]. The use of a passive filter is mandatory to compensate current issues and maintaining a constant voltage free of distortions at the load terminals with a higher power quality [24]. In order to make a brief comparison, the complete discrete and fixed step-size results of the Figure 4 are shown in Figure 5.

B. REAL-TIME PULSE WIDTH MODULATION (PWM)

The PWM technique is used to encode a continuous waveform into a pulsing signal. Although, this type of modulation seems attractive for encoding telecommunication information for transmission, its main use is in power electronic drives. In the PWM modulation a reference signal is compared to a fixed frequency carrier waveform as shown in Figure 6. The fixed PWM switching frequency has to be higher (at least 10 times higher) than the dynamics of the output voltage or current reference.

To make the resultant waveform to be as smooth as possible the switching of semiconductors have to be done several times a second up to tens of kilohertz (kHz) and well into

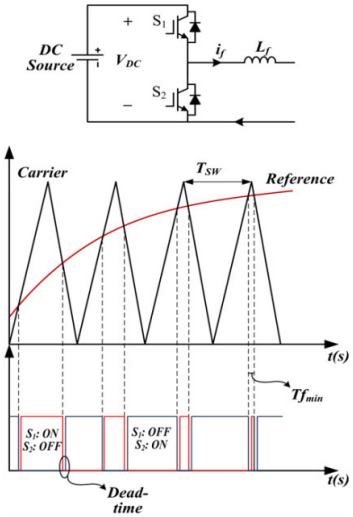


FIGURE 6. Practical considerations for a PWM to generate the Gate signals.

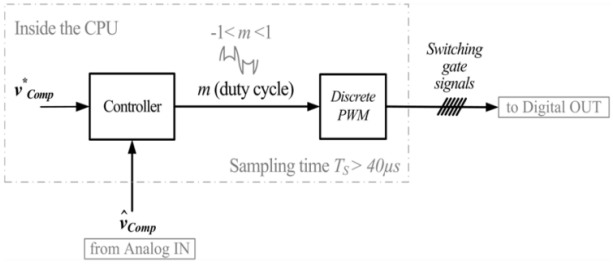


FIGURE 7. Real-time implementation block diagram of a PWM generated in the CPU.

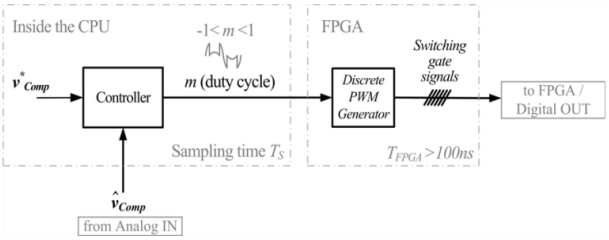


FIGURE 8. Real-time schematic of the PWM generated by the FPGA.

the hundreds of kHz in audio amplifiers and power supplies. A key advantage of the PWM is a low power loss in the switching devices. The reference signal is compared with a triangle waveform as shown in Figure 6 and when the latter is less than the former, the PWM signal is in low state where *S1* (the upper IGBT) is "*Off*" and *S2* (the lower IGBT of the arm) is "*On*", otherwise it is in the high state. This sequence could be any other combination of switches depending on the desired PWM state.

It is noteworthy to mention that the V_{Sh} and V_{Lh} are the harmonic portion of the source and load voltages respectively. In fact if one assume the Fourier decomposition of a waveform into $V = V_1(fundamental) + V_2 + V_3 + V_4 + \ldots V_n$ all the components excepted the fundamental one are considered as the V_h.

It should be noted that, there exists four key constraints to respect for a reliable experimental implementation. Based on the pre-defined sampling-time step for the controller (T_S), it is possible to tune the switching frequency (F_{SW}) and the dead-time (d_s) of the PWM according to the following constraints [25].

1) At first the lowest value that could be chosen for delay between the changing states of the PWM known as dead-time (d_S), is equal to the discrete Time-step T_s.

$$d_S \geq T_S \tag{1}$$

2) To have a marginally low accuracy for the PWM, the triangle waveform should have at least more than four sampling points. Consequently, the highest switching frequency for the PWM became, supposing no constraint from the semiconductor hardware, as follow:

$$F_{SW}\ (Hz) = \frac{1}{T_{SW}\ (s)} \leq \frac{1}{4T_S} \tag{2}$$

3) Consequently, the minimum time in which a state could be kept unchanged (Tf_{min}) will be greater than T_S. This is called the precision of the PWM generator.

4) The last limitation is the frequency of the reference signal should also be less than four times the carrier frequency.

$$F_{ref}\ (Hz) = \frac{1}{T_{modulation}\ (s)} \leq \frac{F_{SW}\ (Hz)}{4} = \frac{1}{4T_{SW}} \tag{3}$$

If a DSP or a digital controller with a sampling time of $40\mu s$ is used to implement the PWM generator according to the demonstration of Figure 6, the highest switching frequency that could be reached would be 6.250 kHz with regards to the preceding explanations.

Therefore, it can be deduced that the frequency of the reference signal as the input of the PWM should be less than 1.56 kHz equal to the 26th harmonic order. Even though, this will result in a marginal stable operation point in which it is became difficult to interpret experimental results accurately. When such low resolution frequencies are chosen, the aliasing phenomenon has a colossal influence on the obtained results. This limitation should be taken into account during an HIL or rapid control prototyping (RCP) implementation.

It has been experimented that with the dSPACE controller or the Opal-RT real-time simulators used in RCP application, the simplest case the sampling period could not go beyond 30 to 40 microseconds as shown in Figure 7. Consequently, if the PWM is generated inside the main CPU unit, it results in a low-profile performance for active filtering or any other application requiring fast switching abilities.

An alternative solution adopted is to implement the PWM generator outside the main CPU unit in a field programmable gate arrays (FPGA) as represented in Figure 8. This technique already available on dSPACE and Opal-RT modules allow reaching switching frequency up to 5 MHz, thanks to the FPGA fast sampling time of nano seconds. In an RCP

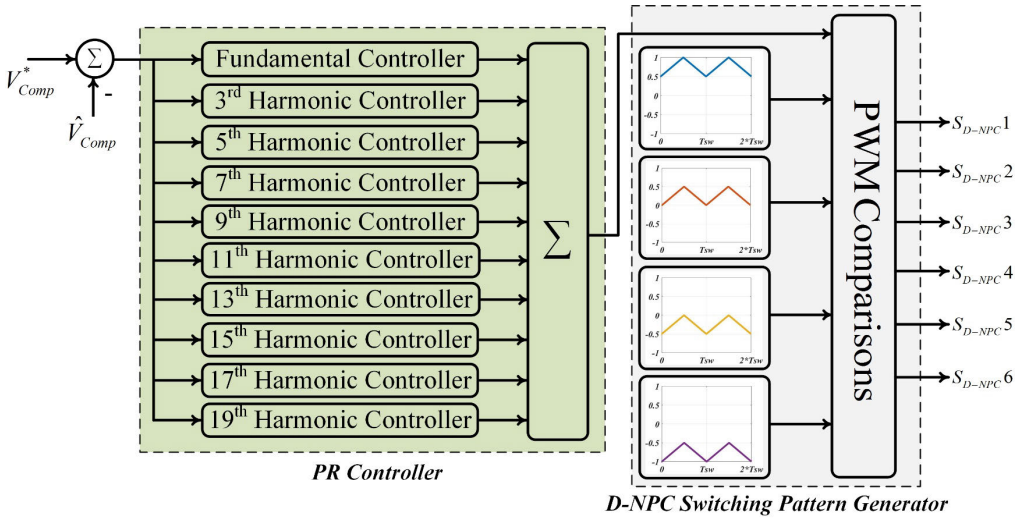


FIGURE 9. The discrete controller used in the offline simulation.

application this external PWM will operate independent of the CPU time-steps. Meanwhile, this is useless for an HIL, as the RT system digital input is limited by the simulator which implements the Electrical system.

The controller shown in Figure 9 is implemented in the HIL platform used in the dSPACE and the electrical system in the Opal-RT simulator.

The result of the simulation at T_s of 36μs which is close to the HIL one, is shown in Figure 10. The result combines different scenarios within a time frame of less than one second [26]. They are obtained exactly with the same parameters illustrated in Table 2, and those used for the HIL implementation. These results are used for the comparison and reliability validation of the HIL application.

III. MODELING AND ALGORITHM OF THE SINGLE-PHASE MULTILEVEL-THSEAF

A D-NPC THSeAF configuration is considered in this paper in order to avoid current harmonic pollution along the power line caused by a single-phase diode bridge rectifier load, followed by a Capacitor C_{NL} in parallel with a resistor R_{NL}.

The second order differential equation between the compensating voltage and the duty cycle is expressed as

$$C_f \frac{d^2 v_{Comp}}{dt^2} + \frac{1}{r_C}\frac{dv_{Comp}}{dt} + \frac{1}{L_f} v_{Comp} = \frac{V_{DC}}{L_f} m + \frac{di_S}{dt} \quad (4)$$

This model has been used in developing the converter controller and its stability analysis. The D-NPC THSeAF considered in this work is taking advantage of the 5L D-NPC converter to reduce passive components rating while, delivering a high-quality compensating voltage. The reference signal applied to the P + R regulator is created by two detection block taking care of the voltage and current issues respectively as presented in the following control diagram. In this RCP application, the whole controller is implemented in the dSPACE module, where the controller is run on a fixed time step size determined in the core of the paper in Table 2. The output signals of the controller are the switching gate signals produced over the digital output of the real-time simulator.

The controller is composed of two loops, the controller outer-loop is composed of two parallel section based on a notch filter harmonics extraction technique. The first part is dedicated to load voltage regulation and added to a second part which compensates the source current harmonics. The controller demonstrated in the diagram of Figure 11, restores a stable voltage at the load PCC terminals, while compensating for current harmonics and reactive power. In the source current regulation block, the notch filter extracts magnitude of the fundamental and its phase degree, leaving harmonics and the reactive component. The control gain G representing the impedance of the source for current harmonics, should be enough to clean the grid from current harmonics fed through the non-linear load. For a more precise compensation of current harmonics, the source and load voltage harmonics should also be considered in the algorithm.

The source and load voltages together with the source current are considered as system input signals. The Single-phase discrete phase-locked loop (PLL) was used to obtain the reference angular frequency synchronized with the source utility voltage (ω_s). Furthermore, the v_{comp_i} contains a fundamental component synchronized with the source voltage in order to compensate for the reactive power. The gain G representing the resistance for harmonics converts compensating current into a relative voltage. The generated reference voltage v_{comp_i} required to clean source current from harmonics.

$$v_{comp\_i} = +Gi_{Sh} - v_{Lh} + v_{Sh} \quad (5)$$

Hereby, as voltage distortion at the load terminals is not desired, the voltage sag and swell should also be investigated to indirectly maintain the voltage magnitude at load side equal

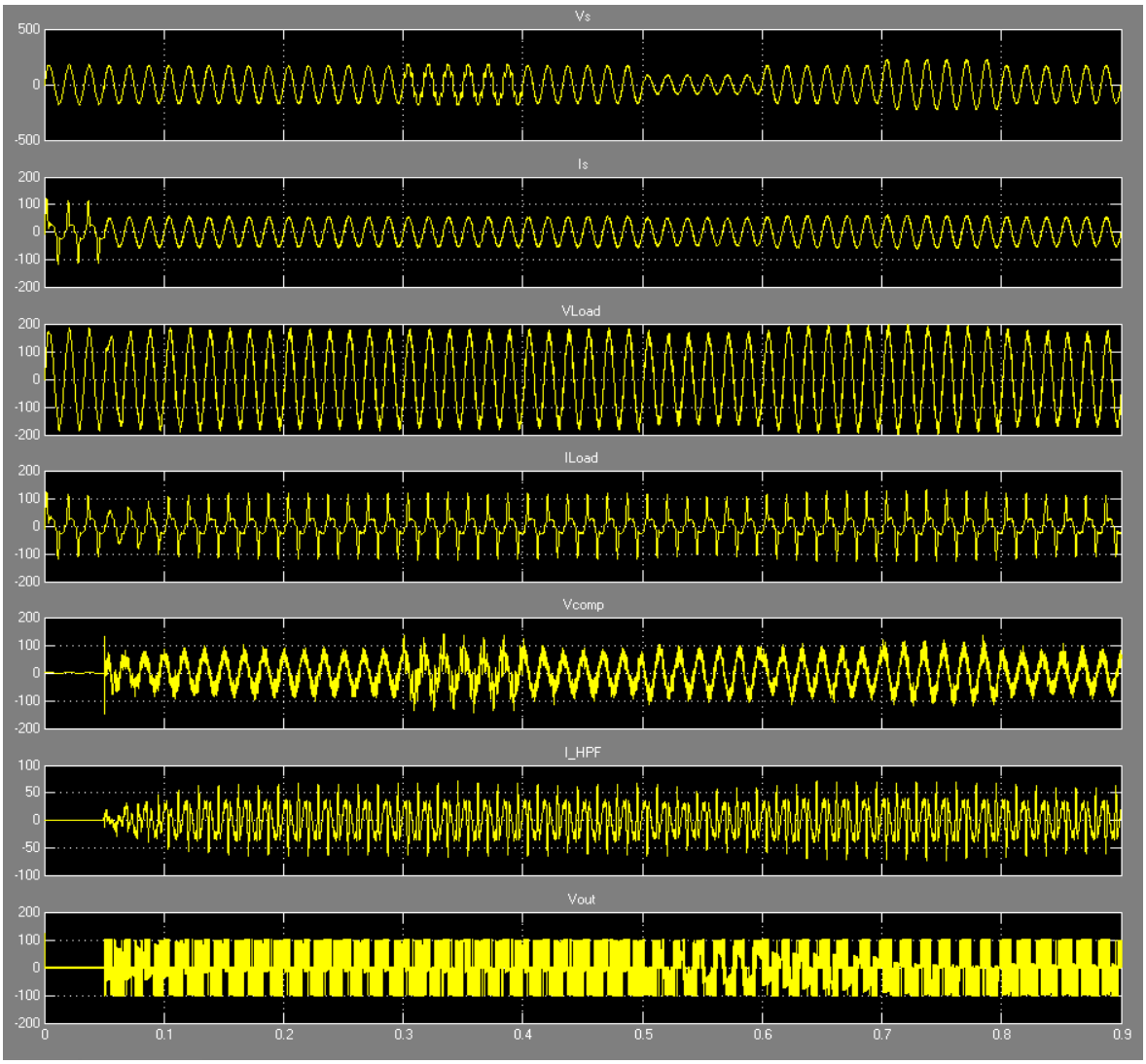


FIGURE 10. The offline simulation result.

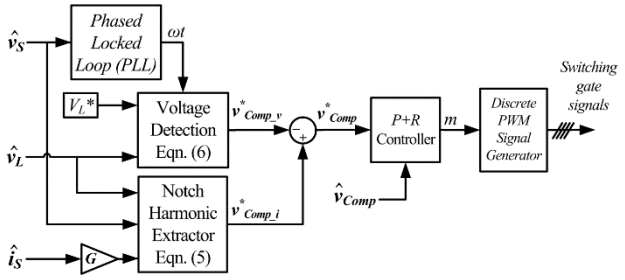


FIGURE 11. Control system scheme for the P + R Controller of single-phase D-NPC THSeAF.

to the reference V_L^* defined by the operator.

$$v_{comp\_v} = \left[k_p\left(V_L^* - \hat{V}_L\right) + k_i \int \left(V_L^* - \hat{V}_L\right) \cdot d_t\right] sin(\omega_L t) \tag{6}$$

where k_p and k_i are respectively the proportional and integrator gains of the PI regulator and $\hat{V}_L$ is the magnitude of $\hat{v}_L$. The final compensating voltage reference is obtained by combination of the stated components related to current issues and voltage issues.

$$v^*_{comp} = -v_{comp_v} + v_{comp\_i} \tag{7}$$

The inner-loop is made with the P + R approach to generate duty cycle required by IGBTs to commutate and produce desired compensating voltage. The transfer function of the controller with a multi-resonant property is given by:

$$G_{P-R}(s) = K_P + \sum_{h=1,3,5,7,\ldots}^{n} \frac{2K_{rh} \cdot \omega_C \cdot s}{s^2 + 2\omega_C \cdot s + (h \cdot \omega)^2} \tag{8}$$

where h is the harmonic order, K_p and K_{rh} are gains, and h. ω is the resonant frequency and ω_C is the cutoff frequency. Their values are depicted in Table 2.

To implement the controller in the digital simulator the transfer function should be obtained by discretization via numerical integration. To obtain the discrete equivalent of a

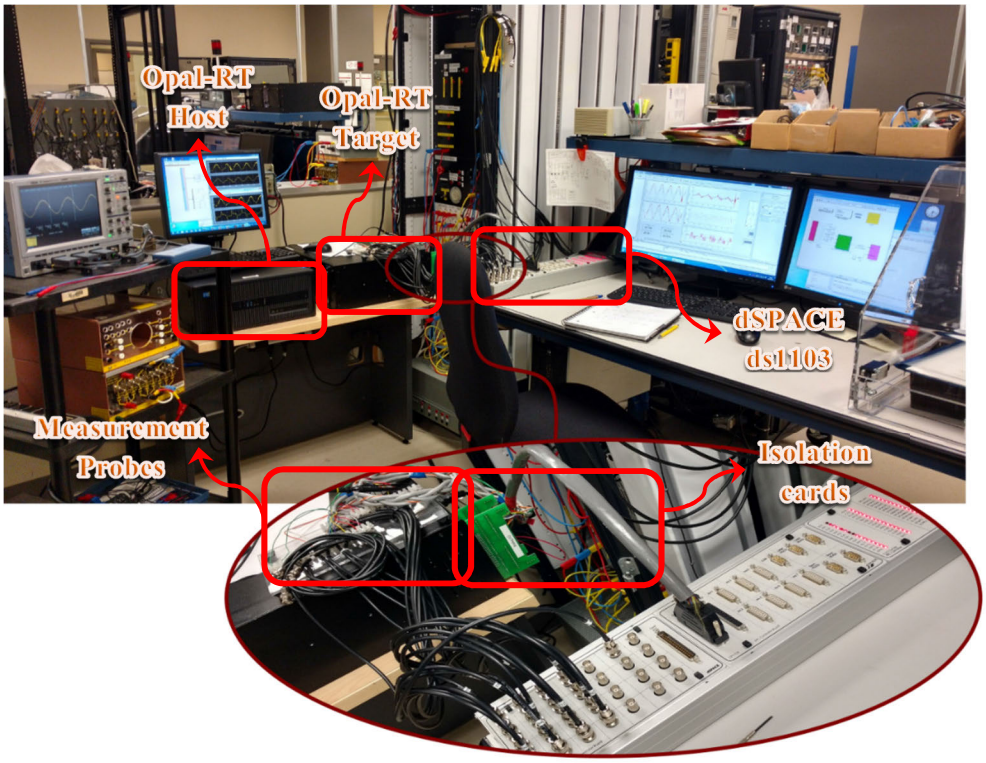


FIGURE 12. Laboratory setup used for HIL experiments.

transfer function via numerical integration, one should apply appropriate numerical integration techniques depending on the sensitivity and stability requirements to the system differential equation [27].

The P + R controller function is then calculated, where z is the variable in the z-domain and T is the sampling time constant also known as step-time T_S in Matlab environment.

The gains should be chosen depending on the sampling time imposed by the digital controller, and the behavior of the system itself. In a general rule; the more the sampling time T has a smaller value, the more the chance to reach a stable system is observed.

IV. EXPERIMENTAL HIL RESULTS

To validate the study various scenarios similar to those effectuated in the simulation are performed on the laboratory prototype realized according to explanations of section II.

Figure 12 shows the setup components with parameters described in Table 2. The setup is connected as explained in section II. The Opal-RT real-time simulator, the dSPACE Simulator along with connections dedicated for the HIL applications are noticeable in the picture. The controller strategy implemented in this paper is based on a Proportional plus resonant controller to generate IGBT's gate signals.

The electrical system is implemented on the Opal-RT simulator as shown in Figure 13(a), while the controller is implemented on the dSPACE as the interface is shown in Figure 13(b). The system is discretized on both simulators and running on two different time-steps.

The previous figure shows the way the model is split into multiple sections to reduce the calculation implemented in each core of the CPU. As well as the PWM generator implemented in the external chip for the dSPACE.

The Figure 14 shows the produced voltage sources by the Opal-RT and capture by an external Oscilloscope to validate the connections between two simulators during normal operating conditions and during a distortion of the grid voltage supply with harmonics.

The HIL setup allows performing experiments exactly as with a physical setup, with all its challenges and fine tunings. Meanwhile, after the setup and models are ready, this setup allows performing extremely dangerous scenarios such as faults and online variation of parameters.

The platform gives the possibility of performing fine adjustment of the control parameters and configuration as if

$$G_{P+R}(z) = K_P + \sum\nolimits_{h=1,3,5,7,\ldots}^{n} \frac{2K_{rh}\cdot\omega_C\cdot z^2\cdot T - K_{rh}\cdot\omega_C\cdot T}{\left(1+\omega_C T+(h\omega T)^2\right)z^2+\left(\frac{(h\omega T)^2}{2}-2\right)z+1-\omega_C T+\frac{(h\omega T)^2}{4}} \tag{9}$$

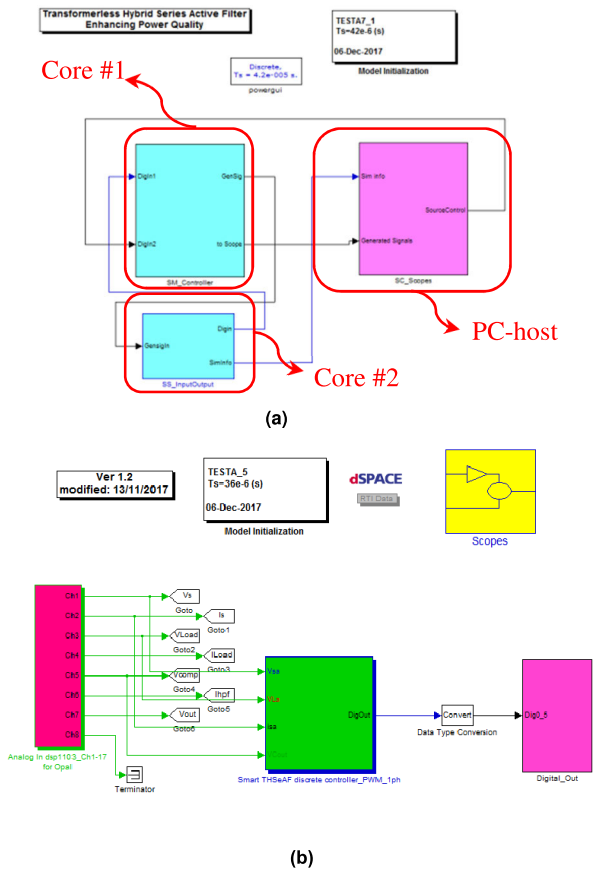


FIGURE 13. The HIL implemented models on multiple CPU's Cores and FPGA. (a) The electrical system implemented in the Opal-RT. (b) The controller running on the dSPACE.

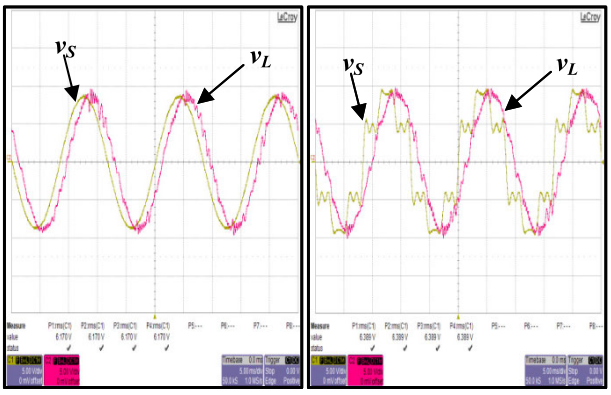


FIGURE 14. Experimental waveforms. (a) Under normal operation. (b) Grid distorted conditions.

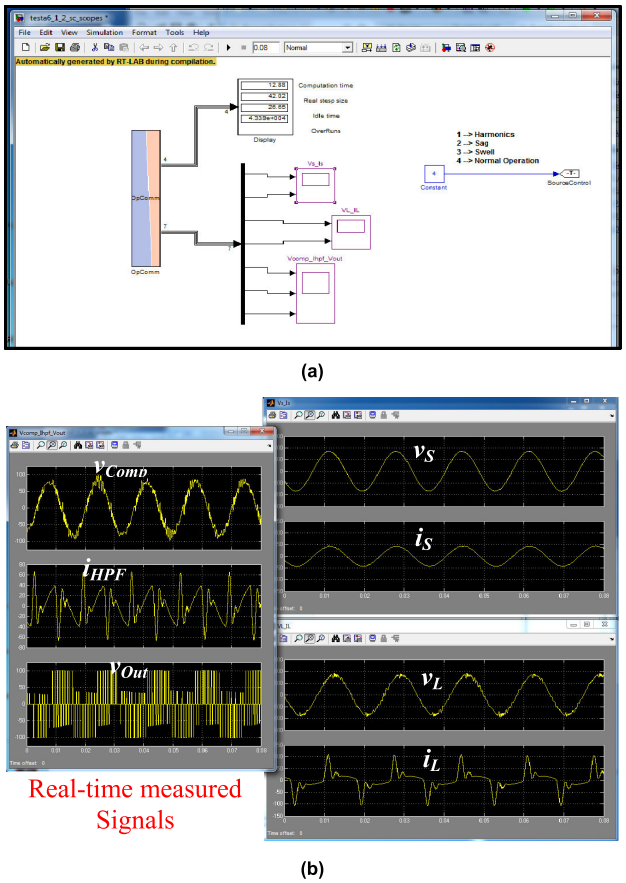


FIGURE 15. Experimental HIL waveforms of the Opal-RT during normal operation. (a) Real-time interface console. (b) Voltage v_S [100V/div], source current i_S [50A/div], load PCC voltage v_L [100V/div], load current i_L [50A/div].

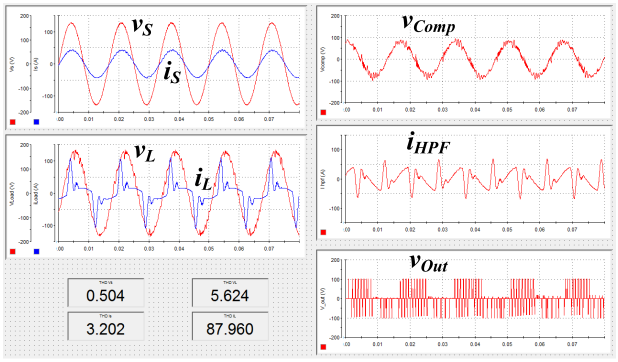


FIGURE 16. The real-time experimental results on the dSPACE ControlDesk.

it was connected to a physical system. The only limitation of the system is imposed by the discrete sampling time imposed by the real-time simulator which hosts the electrical system. The Figure 15 illustrates the system under normal conditions at the stable operating point.

Experimented HIL results illustrate high fidelity towards simulations. Similar to previously demonstrated results, the compensator connected in series to the system compensates the current and voltage related issues instantaneously as demonstrated in the Figure 15. The THSeAF is preventing load current distortions with a high THD to flow into the utility and correcting the power factor. The load voltage THD could be reduced to the desired value by performing a fine-tuning of the shunt passive filter which indirectly contributes to the voltages quality as explained in the previous section. This is a one-time tuning independent of other parameters of the system.

It is also possible to observe on the dSPACE ControlDesk the same waveforms while the controller is performing

TABLE 3. Laboratory HIL measured value and power flow analysis.

Measures	Load		Grid Utility (Source)	
	Voltage (V), V_L	Current (A), I_L	Voltage (V), V_S	Current (A), I_S
Fund. (rms)	121	31	120	32
THD (%)	5.6	88	0.5	3.2
Active power, P (kW)	3.34		3.8	
Reactive power, Q (kvar)	-1.7		-0.54	
Power, S (kVA)	3.75		3.84	
Power Factor, PF	0.89		0.99	
Compensator, THSeAF	S_{Comp}= + 460W + j 1158var			

its regulation task shown in Figure 16. With regards to the chosen time steps and the PWM frequency as well as the passive filter ratings, the load voltage contains 5.6% of THD as calculated by the online FFT module developed for a real-time calculation implemented in the dSPACE controller. Nevertheless, this does not compromise the reliability of the HIL implementation for a power quality analysis platform.

The power flow and THD of measured values are summarized in Table 3 for the case demonstrated in Figure 16. As presented in Table 3, the compensator is absorbing 460 W and 1.16 kVAR. The active power is stored in an energy storage element to be used for regulating the load voltage at its nominal magnitude.

To emulate the behavior of the system under voltage distortions caused by the grid, a harmonic source has been added to the Simulink model implemented in the Opal-RT module. This function operates similar to a programmable voltage supply, able to generate all kinds of harmonics or sags and swells online and during the real-time tests.

The Figure 17 shows worst circumstances in which the utility voltage becomes distorted with THD of 28%. The compensator should prevent these voltage distortions caused by the grid to appear at the loads terminals while cleaning the grid current from the harmonic pollution of the load. The response of the system depicted in Figure 17 is similar to experimental results performed on a 5kVA laboratory prototype. This illustrates the high impact that HIL testing could have on the development process of devices devoted to power quality issues. By far the ease of producing such anomalies to study the system gives a breakthrough tools to researchers and scientific developers.

Moreover, it is noted that the PLL is of great importance in single phase applications and should be suitable for a real-time and discrete implementation. The developed PLL used in this work is able to detect zero crossing events even during source voltage distortion as reference while tuned low-pass filters are employed to filter distortions, and extracting the fundamental.

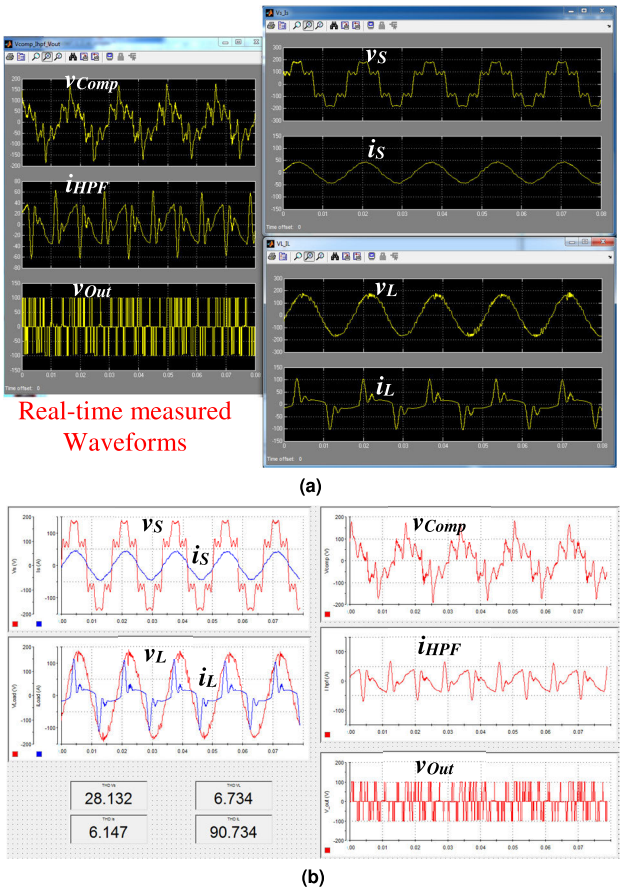


FIGURE 17. The HIL measured waveforms and harmonic THD under non-sinusoidal grid voltage. (a) Opal-RT produced state variables. (b) dSPACE ControlDesk captured waveforms; Source voltage v_S [100V/div], source current i_S [50A/div], load terminal voltage v_L [100V/div], load current i_L [50A/div], THSeAF voltage v_{Comp} [100V/div], passive filter current i_{HPF} [100A/div], converters Output voltage v_{Out} [100V/div].

As demonstrated in the simulation during a distortion or sag and swell in the grid voltage, the compensator delivers a clean and regulated voltage supply at the load PCC entrance.

During a grid voltage sags, the compensator regulates the load voltage magnitude, compensates current harmonics and corrects the power factor as shown in Figure 18. These figures show possible cases in which the THSeAF could face during the worst scenario requiring compensation of the load voltage harmonics and a 50% sag of the supply voltage. During such sturdy sag, the DC energy storage system should supply the required active power to maintain a regulated voltage across the load terminals.

On the other side, the grid supply could be faced with a solid overvoltage or swell. The realized HIL platform allows easily the study of such circumstances a well. In Figure 19, the source voltage has a 33% voltage swell. As one can observe the load voltage stays regulated at the nominal rating. The exceeding energy is absorbed by the storage system. The presented results are practically similar to those obtained by the laboratory power prototype. This allows the study of such

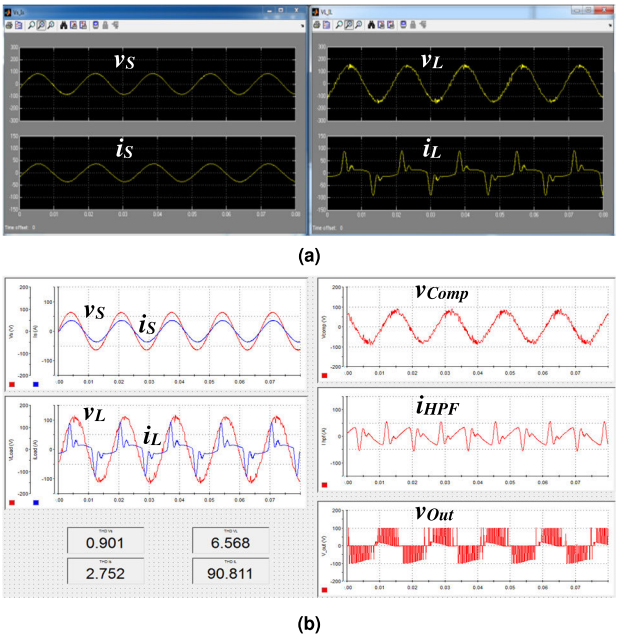


FIGURE 18. The experimental waveforms during supply sag. (a) Opal-RT generated state variables. (b) dSPACE ControlDesk measured waveforms.

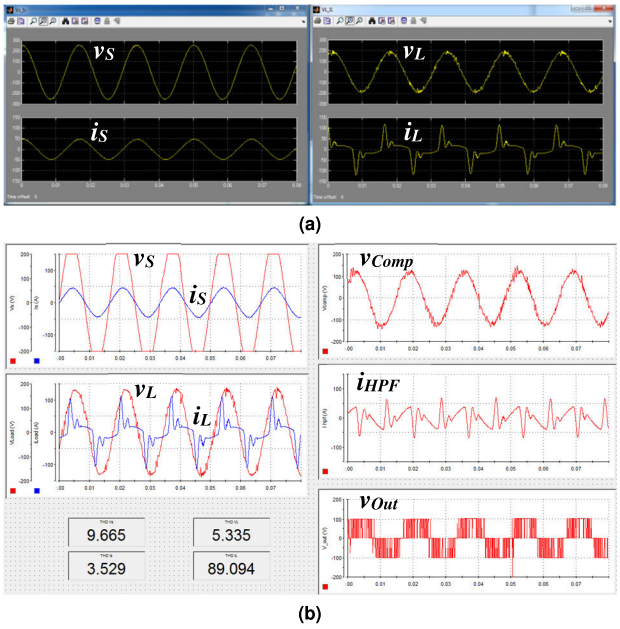


FIGURE 19. Experimental HIL waveforms during supply swell. (a) Opal-RT generated state variables. (b) dSPACE ControlDesk measured waveforms.

critical cases without the worry of a collapse or electrical threat.

To illustrate the feasibility of HIL platform for power electronics applications, a harmonics analysis and comparison between the offline simulation and the HIL setup results are performed. First, results of the HIL are compared with the offline simulation with the same sampling time. Then, they are compared to a simulation that uses a much smaller sampling time, meaning the precision of the simulation is increased.

TABLE 4. THD comparison of the proposed HIL platform and the pure offline simulation.

Total harmonic distortion, THD (%)	Offline Simulation	HIL implementation	Precisions / Tolerance
Source current (i_S)	3.48	3.2	5.18 E-5
Load voltage (v_{Load})	7.1	5.62	8.7 E-5
Load current (i_{Load})	74.2	87.9	2.6 E-3

Figure 20 shows the simulation results for the offline simulation with sampling T_s of 36μs. It shows the results of the THD and FFT analysis of the waveform for the source current i_S, the load voltage V_L, and the load current i_L. The results show the THD values are quite similar to those obtained values by the HIL setup, shown in the core of the paper, even though, the offline simulation does not include the one sampling delay and those associated to the input and outputs measurements. The results of Figure 20 demonstrate that the HIL real-time implementation for power electronics is a fairly true image of an offline simulation with similar conditions. The Table 4 summarizes the observed results.

Where T_{S1} is the Opal-RT Synchronous sampling time for 42 μs, the T_{S2} dSPACE sampling time with 36 μs, and the T_S Offline simulation step-time which is 36 μs.

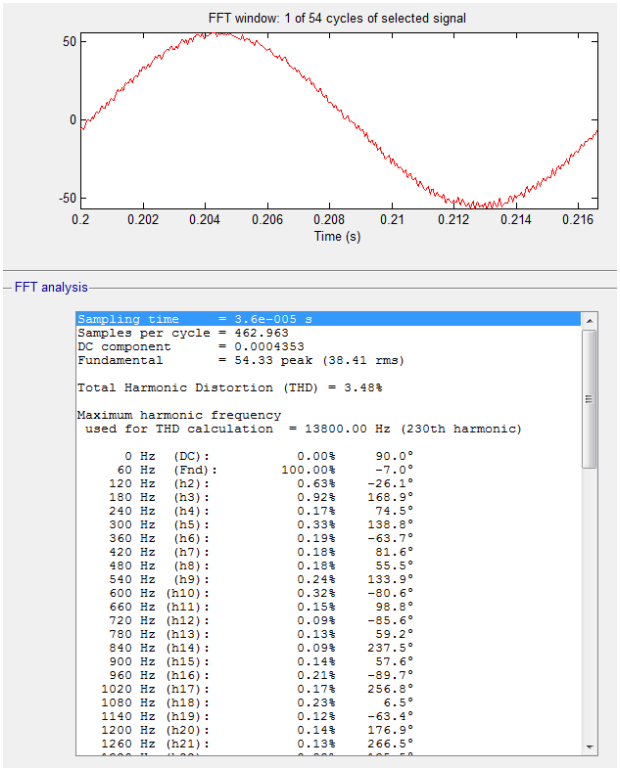
The configuration parameters of the simulation which are not included in the Table are as follow;

1) Solver type: Fixed-step, discrete (non continuous state)
2) Unconstraint periodic sample time

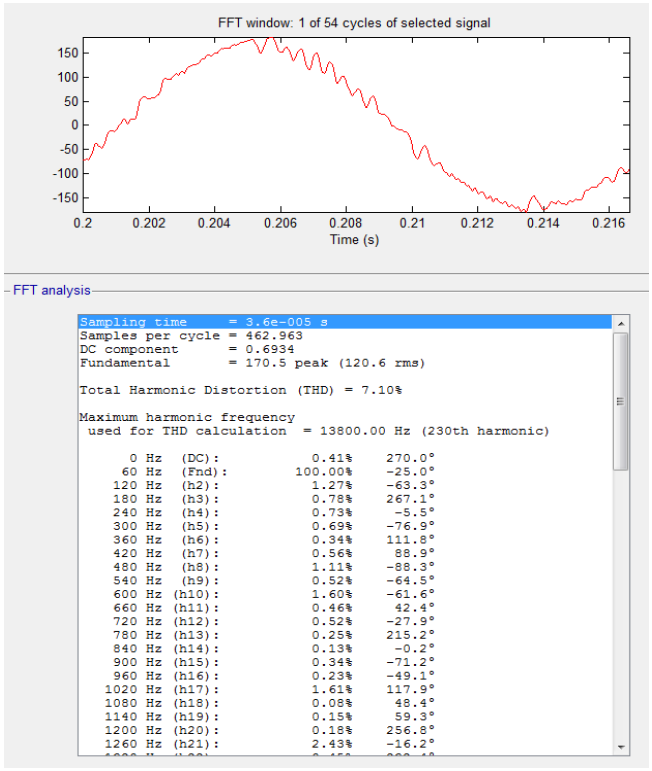
By considering the fact that there exist multiple influences in the simulation process for the HIL implementation, starting by the delay, noises, etc., the results are quiet impressive compared to the offline simulation.

However, it is for sure, possible to reproduce exactly the HIL response in simulation by including all the delays and any interference. This is an extremely complex and time spending task, which is out of the scope of this paper. Meanwhile, as far as the results shows, this replication of the offline simulation is behaving very close to the theoretical study. Also some parameters should be taken into account, the FFT analyzer used in the offline simulation take advantage of a continues iteration, meanwhile the RT model, implemented for the HIL platform is using an FFT developed for discrete by running at a fixed step time of 36μs. All these parameters influence the results. However, for the Power electronic applications with a switching frequency of less than 5kHz, the HIL platform is giving over acceptable results. Furthermore, it allows developers to perform various critical tests, improve their controller, and adjust their electrical components, without destroying power equipment and/or electrical control boards.

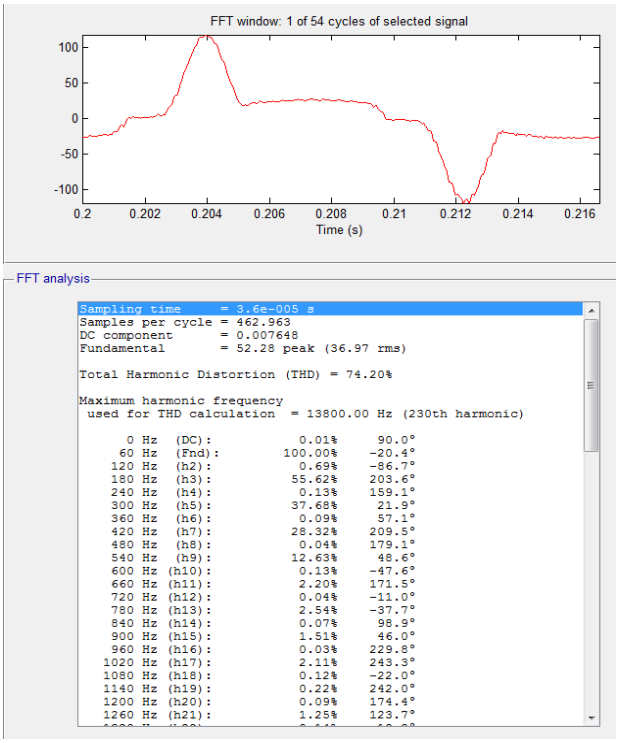
In the next step, to demonstrate the viability of the previous results, the offline simulation is performed at a much smaller step time with a high precision. The results of



(a)



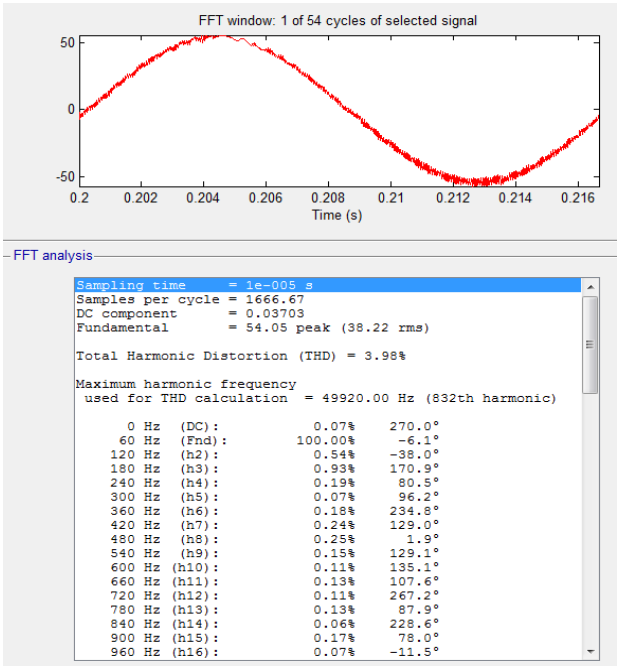
(b)



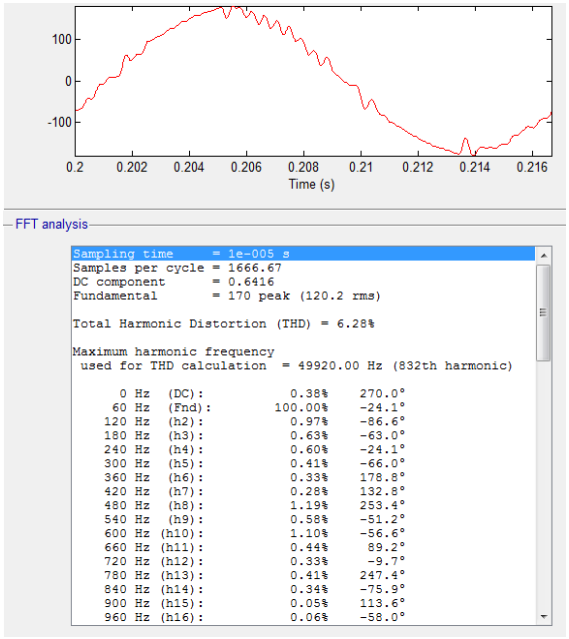
(c)

FIGURE 20. The THD and harmonic analysis of the offline simulation ($T_S = 36\mu$s); (a) the source current, (b) the load voltage, (c) the load current.

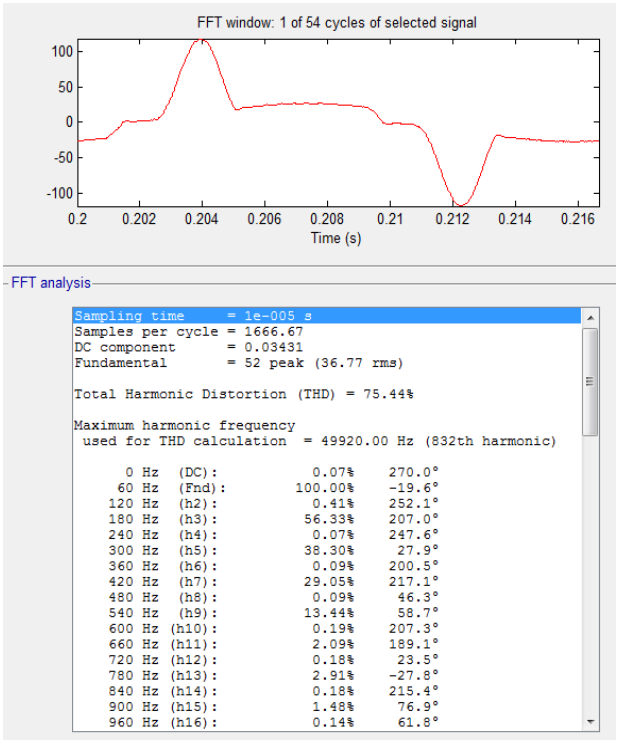
Figure 21 show a high fidelity between the two simulations, and the HIL implementation afterwards. The THD values stays in an acceptable margins for the 10μs, 36μs, and the HIL setup. As explained in previous sections, the auxiliary



(a)



(b)



(c)

FIGURE 21. The THD and harmonic analysis of the offline simulation ($T_S = 10\mu s$); (a) the source current, (b) the load voltage, (c) the load current.

DC source, similar to a UPS, provides necessary amount of power to maintain the supply at the load terminals despite variation in the utility voltage magnitude. The bidirectional DC source should exchange power with an auxiliary feeder or energy storage to maintain the DC voltage at a constant value.

V. CONCLUSION

The power electronic devices are constantly proliferating into the smart grid and a wide range of other applications. Therefore, the necessity of performing a profound study of a system before its industrial consideration is becoming essential. The high-promoting HIL platform could be engaged between the

final production of a power prototype or controller. It is quite more reliable than the simple offline simulation and could improve without doubt the feasibility of any proposed configuration or controller. This also allows developers to test and fine-tune their controllers or control parameters. It permits modifying and adapting the components of the electrical system and ratings before the experimental physical power implementation. In this paper, the HIL benchmark was presented to implement a 5L D-NPC-THSeAF to improve the power quality of a system. The novelty of the proposed configuration includes application of HIL for power quality improvement in a single residential building that may result to the enhancement of the global power system. Moreover, a P + R controller was employed in the 5L D-NPC-THSeAF to improve the dynamic and static performance of the proposed D-NPC-THSeAF. The experimental results depicted in the paper were similar to experimental results performed on a laboratory prototype. This illustrates the high impact that HIL testing could have on the development process of devices devoted to power quality issues. Therefore, it is demonstrated that the proposed configuration and P + R controller can regulate and improve the load voltage and when connected to a renewable auxiliary DC supply, the topology is able to counteract actively to the power flow in the system similar to a UPS. Having a constant and distortion-free supply at load PCC, illustrated that the active compensator responds well to source voltage variations. The proposed compensator configuration along with its controller was simulated and experimentally validated on an HIL platform.

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