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# Dual-Independent-Output Inverter for Dynamic Wireless Power Transfer System

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**ABSTRACT** In this paper, a dual-independent-output inverter, which consists of four power switches, one inductor, and one capacitor, is proposed for segmented-track dynamic wireless power transfer (DWPT) system. It can generate two independently controllable outputs and operate in four output states, to drive two primary tracks independently. Moreover, the voltage gain ranges of both outputs of the proposed inverter are wider than that of a voltage-fed full-bridge inverter (VFFBI). These features enable the inverter to replace conventional VFFBI with less number of power switches and higher redundancy than the existing multi-output inverters to realize on-demand driving of the same number of primary tracks so as to simplify the design and control of the system. First, the topology and operating principle of the proposed inverter are introduced, and two output voltages are analyzed. Second, load voltage in different output states are analyzed, based on which the steady-state modulation strategy, output state switching strategy, and parameters of the proposed inverter are designed. Further, the soft switching state of the proposed inverter is also analyzed. Finally, a Matlab/Simulink simulation and an experimental setup are implemented to verify the correctness of the theoretical analysis and the feasibility and superiority of the proposed inverter.

**INDEX TERMS** Dynamic wireless power transfer (DWPT), segmented primary track, dual-independent-output inverter, operating mode.

## I. INTRODUCTION

Magnetic coupling wireless power transfer (MC-WPT) technology can realize the contactless power transfer based on the principle of electromagnetic induction coupling [1]–[3]. It has been widely applied in various fields such as smart home appliances, biomedical implants, consumer electronics, and transportation [4]–[8]. For some movable electrical equipment such as electric vehicles, robots, and logistics sorting trolley [9]–[12], dynamic wireless power transfer (DWPT) technology can realize the real-time power supply during the movement, hence increase the endurance mileage and reduce the dependence on battery packs.

Generally, according to the topology of the transmitter, DWPT system can be divided into two categories. One is the single-track power supply mode [13]–[15] which is suitable for short-distance system. The other is the segmented-track power supply mode which is suitable for long-distance system. There are mainly two kinds of driving modes in segmented-track power supply mode. One is the single-inverter driving mode as shown in Fig. 1(a) [16]–[18], where multiple primary tracks are driven by a single inverter. Track switching circuits are employed to switch primary tracks. In [17], a single-inverter DWPT system based on multi-paralleled LCC networks was proposed. All primary tracks are excited by a sole inverter, and power in all primary tracks can be distributed automatically without track switching circuit, which simplifies the control and makes the system cost-effective. However, current regulation circuits are needed to reduce the currents in standby primary tracks. Moreover, single-inverter driving mode requires high capacity for the inverter and has low redundancy, so it is not preferred for long-distance system. The other is the multi-inverter driving mode as shown in Fig. 1(b) [2], [19], [20] where each primary track is driven by an independent inverter. The power capacity for inverters is relatively low and the

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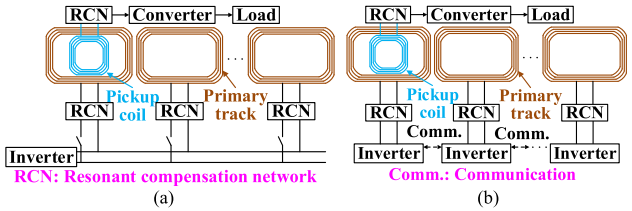


**FIGURE 1.** Diagram of segmented-track DWPT system with (a) single-inverter and (b) multi-inverter driving modes.

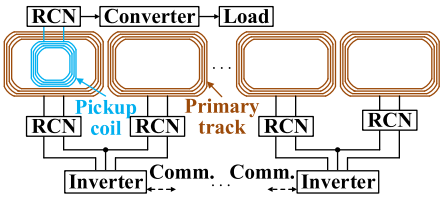


**FIGURE 2.** Diagram of DWPT system based on the proposed inverter.

system has high scalability and redundancy, which makes this driving mode more suitable for long-distance system than the single-inverter driving mode. However, it requires a large number of inverters, which increases system cost and maintenance difficulty. Moreover, communication and synchronous control between inverters [21] are required to realize fast and smooth switching of primary tracks and to improve the stability of load power during the switching process. A large number of inverters will increase the complexity of the system. In [22], a multiplexing LCC module was proposed to reduce the number of inverters by 50%. However, the two primary tracks that are connected to one inverter cannot be driven simultaneously.

Aiming at the large number of required inverters in the multi-inverter driving mode, some multi-output inverters have been proposed and analyzed. In [23] and [24], a multiple legs inverter (MLI) which consists of one common leg and $n$ selectable legs was proposed for driving $n$ primary tracks. Compared with the voltage-fed full-bridge inverter (VFFBI), the MLI can drive the same number of primary tracks with nearly half number of power switches. However, the current stress of the common leg is the sum of that of all selectable legs, and the power loss in the common leg will be higher. In [25], a single-inductor multi-output inverter (SIMOI) was proposed for driving multiple primary coils which can achieve a small number of inductors and power switches, high power density and scalability, and independent controllability for each output. However, the switching frequency of the main power switch is proportional to the number of outputs, and the output power is low. In [26], a variable-topology multi-output inverter (VTMOI) was proposed for multi-load system. It is similar to the MLI in topology but different in control. However, the independent controllability for each output is poor. The common feature of the existing multi-output inverters is that they all contain common modules. Although one inverter can drive more than two primary tracks, the power capacity of the common module will be higher. More importantly, the fault of the common module will affect the drive of all primary tracks that are connected to one inverter.

In this paper, a dual-independent-output inverter, which consists of four power switches, one inductor, and one capacitor, is proposed. It can generate two independently controllable outputs whose voltage gain ranges are wider than that of the VFFBI. According to the number of primary tracks that need to be driven simultaneously, it can operate in a total of four output states: dual-output, first-output, second-output, and none-output. These features enable the proposed inverter to replace conventional VFFBI driving the same number of primary tracks independently with less number of power switches than the existing multi-output inverters so as to simplify the driving circuits, the cooling equipment, and the control algorithm, and further reducing the high-frequency electromagnetic interference caused by the switching process of power switches. The diagram of DWPT system based on the proposed inverter is shown in Fig. 2. It can be seen that the fault of one proposed inverter only affects the driving of two primary tracks, while the other tracks can still be driven. Therefore, the proposed inverter also has the advantage of higher redundancy than the existing multi-output inverters.

The rest of this paper is organized as follows: In section II, the topology, operating principle, and characteristics of two output voltages of the proposed inverter are introduced and analyzed, and then the inverter is compared with the existing multi-output inverters. In section III, load voltage in the pickup side in different output states of the proposed inverter are analyzed in detail, based on which the steady-state modulation strategy and output state switching strategy are designed. In section IV, parameter design and the soft switching state of the proposed inverter are analyzed. In section V, a Matlab/Simulink simulation and an experimental setup are implemented, and simulation and experimental results are presented to verify the proposed inverter. Finally, the conclusion is presented in section VI.

## II. PROPOSED DUAL-INDEPENDENT-OUTPUT INVERTER

### A. TOPOLOGY

The topology of the proposed dual-independent-output inverter for DWPT system is shown in Fig. 3. It can be seen that the proposed inverter consists of four power switches $S_1$-$S_4$ along with their body diodes$D_{S1}$-$D_{S4}$, a choke inductor $L$, and an energy storage capacitor$C$. Two LCC RCN, which are composed by $L_{f1}$, $C_{f1}$, $C_{p1}$ and $L_{f1}$, $C_{f1}$, $C_{p1}$, and perform as current sources [17], [27] at resonant frequency, are adopted in the primary side. $L_{p1}$ and $L_{p2}$ are two primary tracks. In the pickup side, $C_s$ is utilized to compensate the pickup coil $L_s$. $R$ is the equivalent load resistance. $M_1$, $M_2$, and $M_{12}$ are mutual inductances between $L_{p1}$ and $L_s$, $L_{p2}$ and $L_s$, and $L_{p1}$ and $L_{p2}$, respectively. $u_{in}$ and $i_{in}$ are input voltage and input current of the proposed inverter, respectively. $i_L$ and $i_C$ are currents flowing through $L$ and $C$, respectively. $u_C$ is the voltage of $C$. $u_1$ and $u_2$ are two output

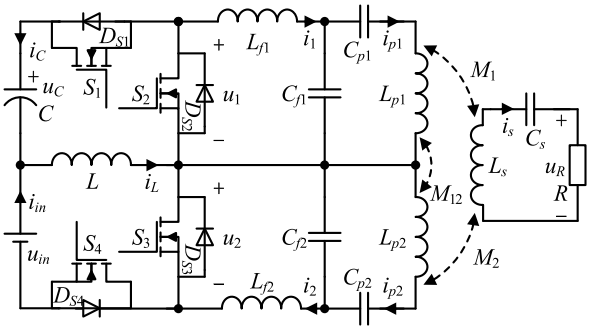


**FIGURE 3.** Topology of the proposed inverter for DWPT system.

voltages of the proposed inverter, while $i_1$ and $i_2$ are two output currents. $i_{p1}$ and $i_{p2}$ are the currents in two primary tracks. $i_s$ is the load current, and $u_R$ is the load voltage. In the following analysis, unless otherwise specified, all currents are positive in the direction indicated by the arrows in Fig. 3, and all voltages are positive at the end where the symbol '+' is located.

### B. OPERATING PRINCIPLE

Define $u_b$ as

$$u_b = u_C + u_{in}. \tag{1}$$

The proposed inverter can operate in four output states: dual-output, first-output, second-output, and none-output. Define $f_s$ as the operating frequency, the operating waveforms of the proposed inverter in four output states are shown in Fig. 4, where $T = 1/f_s$ is the operating cycle and $t_d$ is the dead time to prevent the bridge arm from being shoot-through.$D$ is the duty cycle of energy storage of $L$, and $D_1$ and $D_2$ are duty cycle of $u_1$ and $u_2$, respectively. It is noted that $i_1$ and $i_2$ are not sinusoidal waves due to the impedance characteristics of the LCC network under high order harmonics [28]. In the following analysis, the dual-output state is taken as an example to analyze the proposed inverter. To simplify the analysis, the following assumptions are made: (1) $L$ and $C$ are ideal devices without internal resistance, and $C$ is large enough to make $u_c$ approximately constant; (2) both on-resistance and on-voltage of $S_1$-$S_4$ are zero; and (3) the pickup side is replaced by the reflected impedances $Z_{r1}$ and $Z_{r2}$. The equivalent circuits of all operating modes of the proposed inverter in the dual-output state are illustrated in Fig. 5, where the direction indicated by each arrow is the actual direction of the corresponding current at the beginning of the operating mode. One cycle operating of the proposed inverter can be divided into eight modes as follows:

1) Mode 1: 0-$t_1$ (Fig. 5(a)). At time 0, $S_1$ is turned on, the operating cycle begins. $L$ is connected in parallel with $C$ through $S_1$ and $S_2$, so $i_L$ decreases linearly. During this interval, $u_1 = 0$ and $u_2 = u_b$.
2) Mode 2: $t_1$-$t_2$ (Fig. 5(b)). At time $t_1$, $S_4$ is turned off, $D_{S3}$ is turned on, and $u_{in}$ stops injecting energy. During this interval, $u_1 = u_2 = 0$ and $i_L$ continues to decrease linearly.

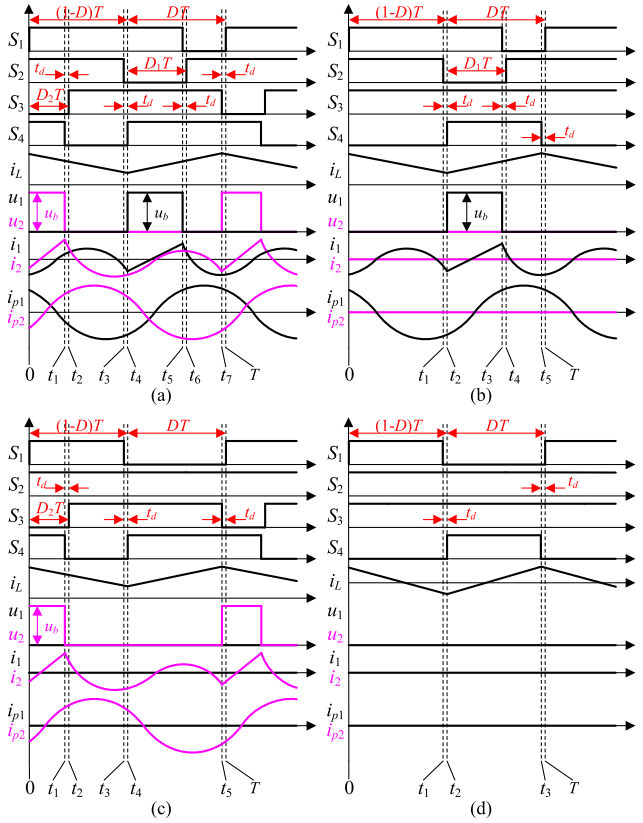


**FIGURE 4.** Operating waveforms of the proposed inverter in (a) dual-output, (b) first-output, (c) second-output, and (d) none-output states.

3) Mode 3: $t_2$-$t_3$ (Fig. 5(c)). At time $t_2$, $S_3$ is turned on. During this interval, $u_1 = u_2 = 0$ and $i_L$ continues to decrease linearly.
4) Mode 4: $t_3$-$t_4$ (Fig. 5(d)). At time $t_3$, $S_2$ is turned off and$D_{S2}$ is turned on. During this interval, $u_1 = u_2 = 0$ and $i_L$ continues to decrease linearly.
5) Mode 5: $t_4$-$t_5$ (Fig. 5(e)). At time $t_4$, $S_4$ is turned on, and $D_{S2}$ is turned off. $L$ begins to store energy through $S_3$ and $S_4$, so $i_L$ begins to increase linearly from the minimum value. During this interval, $u_1 = u_b$ and $u_2 = 0$.
6) Mode 6: $t_5$-$t_6$ (Fig. 5(f)). At time $t_5$, $S_1$ is turned off and $D_{S2}$ is turned on. $C$ is disconnected, so $u_C$ remains unchanged. During this interval, $u_1 = u_2 = 0$ and $i_L$ continues to increase linearly.
7) Mode 7: $t_6$-$t_7$ (Fig. 5(g)). At time $t_6$, $S_2$ is turned on, and $C$ is still disconnected. During this interval, $u_1 = u_2 = 0$ and $i_L$ continues to increase linearly.
8) Mode 8: $t_7$-$T$ (Fig. 5(h)). At time $t_7$, $S_3$ is turned off and $D_{S1}$ is turned on. $L$ is connected in parallel with $C$ through $S_2$ and $D_{S1}$, so $i_L$ begins to decrease linearly from the maximum value. During this interval, $u_1 = 0$ and $u_2 = u_b$. At time $T$, $S_1$ is turned on, the next operating cycle begins.

It can be seen from Fig. 4 that in the first-output state, $S_3$ is turned on to keep the second output at zero; in the

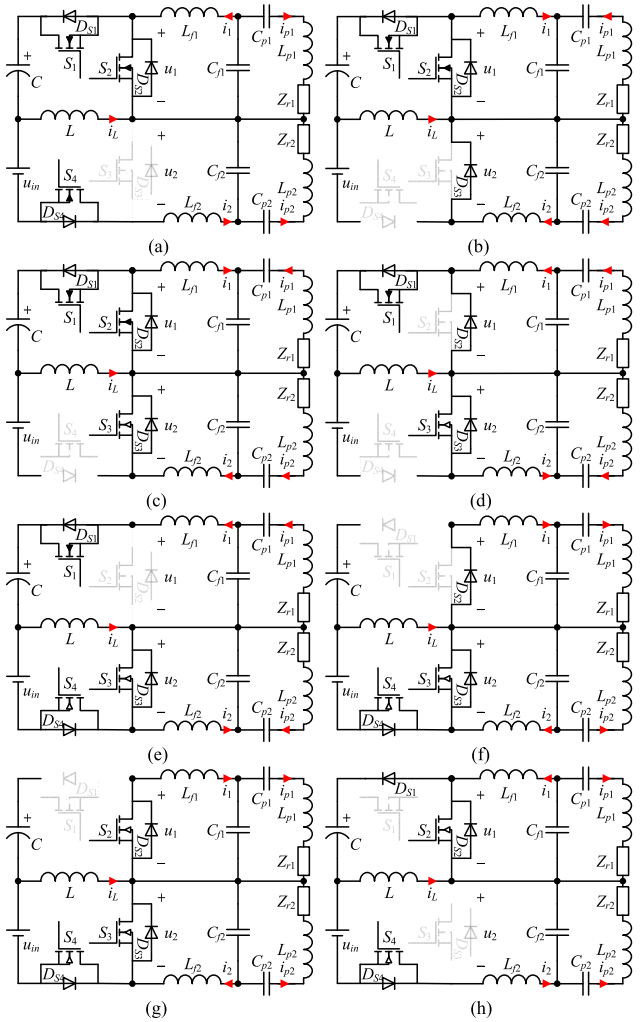


**FIGURE 5.** Equivalent circuits of all operating modes in the dual-output state. (a) 0-$t_1$, (b) $t_1$-$t_2$, (c) $t_2$-$t_3$, (d) $t_3$-$t_4$, (e) $t_4$-$t_5$, (f) $t_5$-$t_6$, (g) $t_6$-$t_7$, and (h) $t_7$-$T$.

second-output state, $S_2$ is turned on to keep the first output at zero; and in the none-output state, both $S_2$ and $S_3$ are turned on to keep both outputs at zero. It is worth noting that in the none-output state, the inverter actually operates in the standby state, so $u_C$ and $i_L$ are not zero. When the inverter starts to output, the time of entering the steady state can be shortened, thus increasing the effective operating time of the inverter. Finally, the switching logic of $S_1$-$S_4$ in four output states are shown in TABLE 1, where $D_d = t_d/T$.

### C. OUTPUT VOLTAGES

According to Fig. 4, the relationships that should be satisfied between $D$, $D_1$, and $D_2$ are

$$D_1 \le D \quad \text{and } D_2 \le 1 - D. \tag{2}$$

As can be seen from Fig. 4(a), $t_d$ is much smaller than $T$, so it can be neglected for simplifying the analysis. In time interval 0-$t_4$, the inductor voltage $u_L$ equals to $U_C$, while in time interval $t_4$-$T$, $u_L$ equals to $U_{in}$. In steady state, the

**TABLE 1.** Switching logic of $S_1$-$S_4$ in four output states of the proposed inverter.

| | | Dual-output | First-output | Second-output | None-output |
|---|---|---|---|---|---|
| $S_1$ | Duty cycle | 1-$D$+$D_1$-$D_d$ | 1-$D$+$D_1$-$D_d$ | 1-$D$-$D_d$ | 1-$D$-$D_d$ |
| | Phase | 0 | 0 | 0 | 0 |
| $S_2$ | Duty cycle | 1-$D_1$-$D_d$ | 1-$D_1$-$D_d$ | 1 | 1 |
| | Phase | (1-$D$+$D_1$)$T$ | (1-$D$+$D_1$)$T$ | - | - |
| $S_3$ | Duty cycle | 1-$D_2$-$D_d$ | 1 | 1-$D_2$-$D_d$ | 1 |
| | Phase | $D_2T$ | - | $D_2T$ | - |
| $S_4$ | Duty cycle | $D$+$D_2$-$D_d$ | $D$-$D_d$ | $D$+$D_2$-$D_d$ | $D$-$D_d$ |
| | Phase | (1-$D$)$T$ | (1-$D$)$T$ | (1-$D$)$T$ | (1-$D$)$T$ |

volt-second balance of $L$ can be expressed as $U_{in}DT = U_C(1-D)T$, and hence$U_C$ and $U_b$ can be derived as

$$U_C = \frac{DU_{in}}{1-D}, \quad U_b = \frac{U_{in}}{1-D}. \tag{3}$$

As shown in Fig. 4(a), in time interval $t_4$-$t_6$, $u_1$ equals to $U_b$, while in time interval 0-$t_4$ and $t_6$-$T$, $u_1$ equals to 0. In time interval 0-$t_2$, $u_2$ equals to $U_b$, while in time interval $t_2$-$T$, $u_2$ equals to 0. Therefore, the Fourier series of $u_1$ and $u_2$ thus can be expressed as

$$\begin{cases} u_1 = U_b D_1 + \dfrac{\sqrt{2}U_b}{\pi} \displaystyle\sum_{n=1}^{\infty} \left[ \frac{\sqrt{1-\cos 2n\pi D_1}}{n} \sin\left(n\omega t + \varphi_{1n}\right) \right] \\ u_2 = U_b D_2 + \dfrac{\sqrt{2}U_b}{\pi} \displaystyle\sum_{n=1}^{\infty} \left[ \frac{\sqrt{1-\cos 2n\pi D_2}}{n} \sin\left(n\omega t + \varphi_{2n}\right) \right] \end{cases} \tag{4}$$

where $\omega = 2\pi/T$, $\varphi_{1n} = 2n\pi D + \arctan(\cot(n\pi D_1))$, and $\varphi_{2n} = \arctan(\cot(n\pi D_2))$.

According to(4), the fundamental component of $u_1$ and $u_2$ in phasor form can be expressed as

$$\begin{cases} \dot{U}_{11} = U_{11}\angle\varphi_{11} = \dfrac{U_{in}\sqrt{1-\cos 2\pi D_1}}{\pi\,(1-D)}\angle\varphi_{11} \\ \dot{U}_{21} = U_{21}\angle\varphi_{21} = \dfrac{U_{in}\sqrt{1-\cos 2\pi D_2}}{\pi\,(1-D)}\angle\varphi_{21}. \end{cases} \tag{5}$$

As can be seen from(5), when $U_{in}$ and $D$ are determined, $U_{11}$ is only related to $D_1$, and $U_{21}$ is only related to $D_2$. Therefore, $U_{11}$ and $U_{21}$ can be controlled independently. The voltage gain can be defined as

$$G_{vj} = U_{j1}/U_{in}\ (j = 1, 2). \tag{6}$$

Fig. 6 shows $G_{v1}$ versus $D$ and $D_1$. It can be seen that when $D \le 0.5$, $G_{v1}$ is positively correlated with $D_1$; and when $D > 0.5$, $G_{v1}$ reaches the peak value at $D_1 = 0.5$. Fig. 7 shows $G_{v2}$ versus $D$ and $D_2$. It can be seen that when $D \le 0.5$, $G_{v2}$ reaches the peak value at $D_2 = 0.5$; and when $D > 0.5$, $G_{v2}$ is positively correlated with $D_2$. Moreover, both $G_{v1}$ and $G_{v2}$ can be higher than 1, which is higher than that

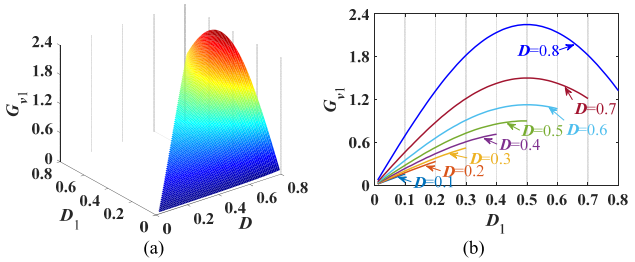


**FIGURE 6.** $G_{v1}$ versus $D$, and $D_1$. (a) 3-D curve, (b) 2-D curve.

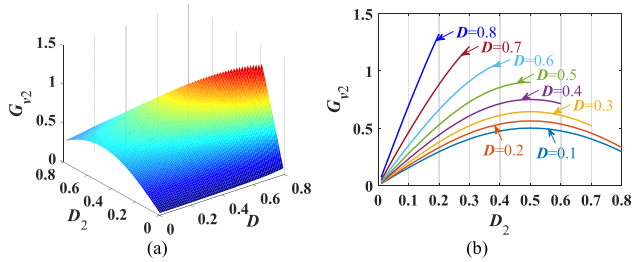


**FIGURE 7.** $G_{v2}$ versus $D$ and $D_2$. (a) 3-D curve, (b) 2-D curve.

of the VFFB. Then the value of $G_{v1}$ and $G_{v2}$ can be specified as (7) and(8), respectively.

$$\begin{cases} 0 \le G_{v1} \le \dfrac{\sqrt{1-\cos 2\pi D}}{\pi\,(1-D)}, & D \le 0.5 \\ 0 \le G_{v1} \le \dfrac{\sqrt{2}}{\pi\,(1-D)}, & D > 0.5. \end{cases} \tag{7}$$

$$\begin{cases} 0 \le G_{v2} \le \dfrac{\sqrt{2}}{\pi\,(1-D)}, & D \le 0.5 \\ 0 \le G_{v2} \le \dfrac{\sqrt{1-\cos 2\pi D}}{\pi\,(1-D)}, & D > 0.5. \end{cases} \tag{8}$$

### D. COMPARISON WITH THE EXISTING MULTI-OUTPUT INVERTERS

The comparison results of the proposed inverter with the existing multi-output inverters ([23]–[26]), the VFFBI, and the voltage-fed half-bridge inverter (VFHBI) in terms of the number of semiconductors, the number of capacitors and inductors, and the maximum voltage gain for driving N primary tracks are shown in TABLE 2. It can be seen that except for the SIMOI and the VFHBI, the number of power switches in other topologies is larger than that in the proposed inverter. However, the SIMOI contains N + 1 diodes, while the proposed inverter does not. Moreover, the switching frequency of the main power switch in the SIMIO is proportional to the number of outputs, which will lead to higher switching loss. The deficiency of the VFHBI is that its maximum voltage gain is only 0.45, while that of the VFFBI, the MLI, and the VTMOI is 0.9, and that of the SIMOI and the proposed inverter is higher than 0.9. Another common disadvantage of the existing multi-output inverters not shown in the table is that they all contain common modules, which will reduce the system redundancy. Based on the above analysis, the proposed inverter can replace the VFFBI to drive the same number of primary tracks independently with less number of power switches and higher redundancy than the existing multi-output inverters, which can reduce the design and control difficulty of DWPT system.

**TABLE 2. Comparison of the proposed inverter with the existing multi-output inverters for driving N primary tracks.**

| | Num. $S$ | Num. $D$ | Num. $C$ | Num. $L$ | Max gain |
|---|---|---|---|---|---|
| VFFBI | 4N | 0 | 0 | 0 | =0.9 |
| VFHBI | 2N | 0 | 0 | 0 | =0.45 |
| MLI [23], [24] | 2N+2 | 0 | 0 | 0 | =0.9 |
| VTMOI [26] | 2N+2 | 0 | 0 | 0 | =0.9 |
| SIMOI [25] | N+1 | N+1 | 0 | 1 | >0.9 |
| Proposed | 2N | 0 | N/2 | N/2 | >0.9 |

It can be seen that one proposed inverter requires one inductor and one capacitor, which seems to increase its volume and cost, and affect its reliability. However, for power switches, both the driving circuits and the cooling equipment are necessary, which will also increase the volume and the cost. Moreover, the heat dissipation design of power switches is more complex than that of capacitors and inductors, which will increase the design difficulty of the inverter. Although power switches can serve longer than capacitors, they fail more easily than capacitors. Therefore, capacitors and inductors do not necessarily bring disadvantage from the point of view of practical application.

## III. OPERATING STRATEGY OF THE PROPOSED INVERTER

### A. LOAD VOLTAGE IN THE PICKUP SIDE

In this part, the load voltage and power in the pickup side in single-output and dual-output states will be analyzed, which will guide the operating strategy design of the proposed inverter, and the parameter design and soft switching state analysis in the next section.

In DWPT system, the parameters of all primary sides are generally equal [17], [23], that is, $L_{f1} = L_{f2} = L_f$, $C_{f1} = C_{f2} = C_f$, $C_{p1} = C_{p2} = C_p$, and $L_{p1} = L_{p2} = L_p$ in this paper. Then the resonant angle frequency of the system can be expressed as

$$\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{L_f C_f}} = \frac{1}{\sqrt{(L_p - L_f)\,C_p}} = \frac{1}{\sqrt{L_s C_s}}. \tag{9}$$

where $f_0$ is the resonant frequency of the system.

#### 1) DUAL-OUTPUT STATE

As shown in Fig. 4(a), the phases of $i_{p1}$ and $i_p$ are almost in the opposite direction, which will cause power cancellation between the two primary tracks, resulting in zero load power. Therefore, in practical system, it is necessary to connect the second LCC network in the opposite direction to make $i_{p1}$ and $i_p$ in phase. In theoretical analysis, $u_2$, $i_2$, and $i_{p2}$ should

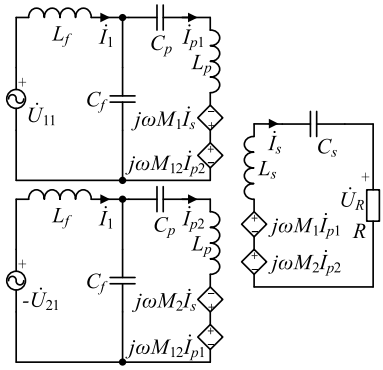


**FIGURE 8.** Equivalent circuit of the system.

be dealt with in their opposite directions, then the equivalent circuit of the system can be shown in Fig. 8.

By applying Kirchhoff's Voltage Law (KVL) in Fig. 8, one can obtain

$$\begin{bmatrix} \dot{U}_{11} \\ \dot{U}_{11} \\ -\dot{U}_{21} \\ -\dot{U}_{21} \\ 0 \end{bmatrix} = \begin{bmatrix} Z_f & -1/j\omega C_f & 0 & 0 & 0 \\ j\omega L_f & Z_p & 0 & j\omega M_{12} & -j\omega M_1 \\ 0 & 0 & Z_f & -1/j\omega C_f & 0 \\ 0 & j\omega M_{12} & j\omega L_f & Z_p & -j\omega M_2 \\ 0 & -j\omega M_1 & 0 & -j\omega M_2 & Z_s + R \end{bmatrix} \times \begin{bmatrix} \dot{I}_1 \\ \dot{I}_{p1} \\ \dot{I}_2 \\ \dot{I}_{p2} \\ \dot{I}_s \end{bmatrix} \tag{10}$$

where $Z_f = j\omega L_f + 1/j\omega C_f$, $Z_p = j\omega L_p + 1/j\omega C_p$, and $Z_s = j\omega L_s + 1/j\omega C_s$.

When $\omega = \omega_0$, the currents can be derived as

$$\begin{cases} \dot{I}_1 = \dfrac{\omega_0 M_1^2 \dot{U}_{11} - (\omega_0 M_1 M_2 + jM_{12}R)\,\dot{U}_{21}}{\omega_0 L_f^2 R} \\ \dot{I}_2 = \dfrac{-\omega_0 M_2^2 \dot{U}_{21} + (\omega_0 M_1 M_2 + jM_{12}R)\,\dot{U}_{11}}{\omega_0 L_f^2 R} \\ \dot{I}_{p1} = \dfrac{\dot{U}_{11}}{j\omega_0 L_f}, \dot{I}_{p2} = \dfrac{-\dot{U}_{21}}{j\omega_0 L_f}, \dot{I}_s = \dfrac{M_1\dot{U}_{11} - M_2\dot{U}_{21}}{L_f R}. \end{cases} \tag{11}$$

The load voltage in the pickup side can be derived as

$$\dot{U}_R = \dot{I}_s R = \left(M_1\dot{U}_{11} - M_2\dot{U}_{21}\right)/L_f. \tag{12}$$

It can be seen from (12) that if the phase of $\dot{U}_{11}$ and $\dot{U}_{21}$ are opposite, $\dot{U}_R$ can reach the maximum value. Then the relationship between $\varphi_{11}$ and $\varphi_{21}$ should be

$$\varphi_{11} - \varphi_{21} = \pi. \tag{13}$$

To improve the stability of power supply in DWPT system, the two primary track currents are generally desired to be equal. By combining(5) with(13), the relationships between $D$, $D_1$, and $D_2$ can be derived as

$$D = 0.5, \quad D_2 = D_1 \text{ or } D_1 = D,\ D_2 = 1 - D. \tag{14}$$

Then the load voltage and power can be rewritten as

$$\dot{U}_R = (M_1 + M_2)\,\dot{U}_{11}/L_f, \quad P_o = \left|\dot{U}_R\right|^2/R. \tag{15}$$

#### 2) SINGLE-OUTPUT STATE

In the first-output state, $\dot{U}_{21} = 0$, then (11) can be rewritten as

$$\begin{cases} \dot{I}_1 = \dfrac{M_1^2\dot{U}_{11}}{L_f^2 R}, \quad \dot{I}_2 = \dfrac{(\omega_0 M_1 M_2 + jM_{12}R)\,\dot{U}_{11}}{\omega_0 L_f^2 R} \\ \dot{I}_{p1} = \dfrac{\dot{U}_{11}}{j\omega_0 L_f}, \quad \dot{I}_{p2} = 0, \dot{I}_s = \dfrac{M_1\dot{U}_{11}}{L_f R}. \end{cases} \tag{16}$$

It can be seen from(16) that $\dot{I}_{p2}$ is zero in the first-output state, then the load voltage can be derived as

$$\dot{U}_R = \dot{I}_s R = M_1\dot{U}_{11}/L_f. \tag{17}$$

Similarly, $\dot{I}_{p1}$ should be zero in the second-output state, then the load voltage should be

$$\dot{U}_R = \dot{I}_s R = -M_2\dot{U}_{21}/L_f. \tag{18}$$

### B. STEADY-STATE MODULATION STRATEGY

According to(14), there are two kinds of relationships between $D$, $D_1$, and $D_2$ in the dual-output state: ① $D = 0.5$, $D_2 = D_1$; and ② $D_1 = D$, $D_2 = 1 - D$. As can be seen from Fig. 6 and Fig. 7, ② has a wider output voltage range than ①. Moreover, by substituting ① and ② into TABLE 1, ② can make $S_1$ and $S_4$ keep 'ON' state, which can reduce the switching loss and electromagnetic interference of the proposed inverter. Therefore, ② is selected as the steady-state modulation strategy.

In the first-output state, different ($D$, $D_1$) can generate the same $G_{v1}$ according to Fig. 6. As can be seen from Fig. 4, the voltage stress of all power switches is $U_b$ which is positively related to $D$. It is necessary to set reasonable ($D$, $D_1$) to reduce the voltage stress. According to(7), when $D = D_1 = 0.5$, $G_{v1} = 0.9$, then the steady-state modulation strategy can be set as follows: when $G_{v1} \le 0.9$, set $D \le 0.5$ and $D_1 = D$; and when $G_{v1} > 0.9$, set $D > 0.5$ and $D_1 = 0.5$. Similarly, in the second-output state, the steady-state modulation strategy can be set as follows: when $G_{v2} \le 0.9$, set $D \le 0.5$ and $D_2 = 0.5$; and when $G_{v2} > 0.9$, set $D > 0.5$ and $D_2 = 1 - D$. In the none-output state, set $D_1 = D_2 = 0$.

### C. OUTPUT STATE SWITCHING STRATEGY

As the pickup coil moves, the inverter needs to switch the output state accordingly. To improve the stability of switching processes, a delay-switching strategy is designed in this paper. The flow chart of the designed output state switching strategy is shown in Fig. 9, and the operating waveforms of switching processes are shown in Fig. 10.

Take the closing process of the first output in Fig. 10(a) as an example for analysis, where the falling edge of $S_{t1}$ means the closing of the first output. At time $t_1$,

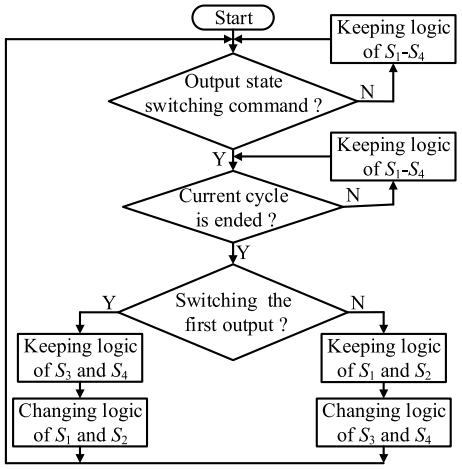


**FIGURE 9.** Flow chart of the designed output state switching strategy.

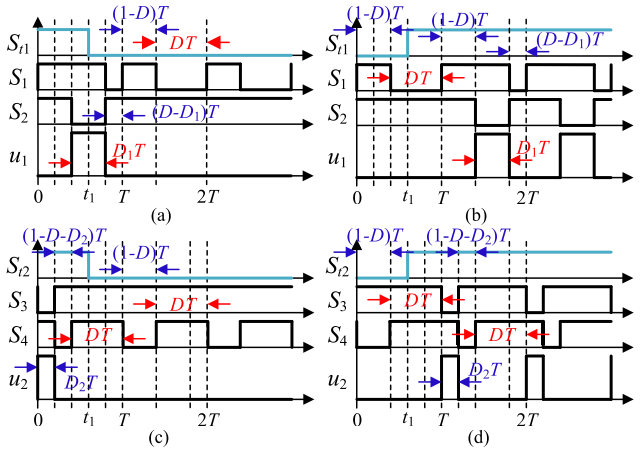


**FIGURE 10.** Operating waveforms of processes of (a) closing the first output, (b) opening the first output, (c) closing the second output, and (d) opening the second output.

the inverter receives the command of closing the first output, but the current operating cycle has not ended yet, thus $S_1$-$S_4$ will keep current switching logic unchanged. At time $T$, the next operating cycle begins. $S_2$ is turned on to keep $u_1$ at zero. Meanwhile, the switching logic of $S_1$ is adjusted, and the switching logic of $S_3$ and $S_4$ remains unchanged making no effect on the second output. Then the inverter repeats the new switching logic to decrease $i_{p1}$ to zero gradually.

The switching of the second output can be realized by adjusting the switching logic of $S_3$ and $S_4$, while keeping the switching logic of $S_1$ and $S_2$ unchanged.

## IV. PARAMETER DESIGN AND SOFT SWITCHING STATE OF THE PROPOSED INVERTER

### A. PARAMETER DESIGN

#### 1) DESIGN OF $L$

Assuming that there is no power loss in the system, input power of the inverter and load power can be expressed as

$$P_{in} = P_o = U_{in} I_{in} = U_{in} (I_L - I_C) \tag{19}$$

where $I_{in}$, $I_L$, and $I_C$ are the mean values of $i_{in}$, $i_L$, and $i_C$, respectively. In steady state, $I_C = 0$, then $I_L$ can be derived as

$$I_L = I_{in} = P_o / U_{in}. \tag{20}$$

When both $S_3$ and $S_4$ are turned on, $i_L$ increases linearly, so the ripple of $i_L$ is

$$\Delta i_L = U_{in} DT / L. \tag{21}$$

Then $i_L$ can be expressed as

$$i_L = \begin{cases} i_{L-\max} - U_C t / L, & 0 \le t \le (1-D)T \\ i_{L-\min} + U_{in}(t - (1-D)T)/L, & (1-D)T \le t \le T. \end{cases} \tag{22}$$

where $i_{L-\max} = I_L + \Delta i_L/2$ and $i_{L-\min} = I_L - \Delta i_L/2$ are the maximum and minimum values of $i_L$, respectively.

The ripple coefficient of $i_L$ can be expressed as

$$r_{iL} = \frac{i_L}{I_L} = \frac{U_{in}^2 DT}{P_o L}. \tag{23}$$

Define $r_{i-\max}$ as the maximum allowable ripple coefficient of $i_L$. $r_{iL} \le r_{i-\max}$ should be satisfied when $P_{o-\max}$ is obtained at the maximum duty cycle $D_{\max}$, then $L$ needs to satisfy

$$L \ge \frac{U_{in}^2 D_{\max} T}{r_{i-\max} P_{o-\max}}. \tag{24}$$

The position of the pickup coil where $P_{o-\max}$ is obtained can be determined according to the design of the magnetic coupler. When the position is in the common power supply area of two primary tracks, the calculation can be carried out by(15), otherwise, by(17) or(18).

#### 2) DESIGN OF $C$

When $S_4$ is turned off, $C$ enters the charging state and $i_C = i_L$. When both $S_3$ and $S_4$ are turned on, $C$ enters the discharging state. The longest charging time of $C$ is (1-$D$)$T$, then by using(22), the ripple of $u_C$ can be calculated as

$$\Delta u_C = \frac{1}{C} \int_0^{(1-D)T} i_L dt = \frac{P_o (1-D) T}{C U_{in}}. \tag{25}$$

By combining(25) with(3), the ripple coefficient of $u_C$ can be expressed as

$$r_{uC} = \frac{u_C}{U_C} = \frac{P_o (1-D)^2 T}{U_{in}^2 DC}. \tag{26}$$

Define $r_{u-\max}$ as the maximum ripple coefficient of $u_C$. $r_{uC} \le r_{u-\max}$ should be satisfied when $P_{o-\max}$ is obtained at $D_{\max}$, then $C$ needs to satisfy

$$C \ge \frac{P_{o-\max} (1 - D_{\max})^2 T}{r_{u-\max} U_{in}^2 D_{\max}}. \tag{27}$$

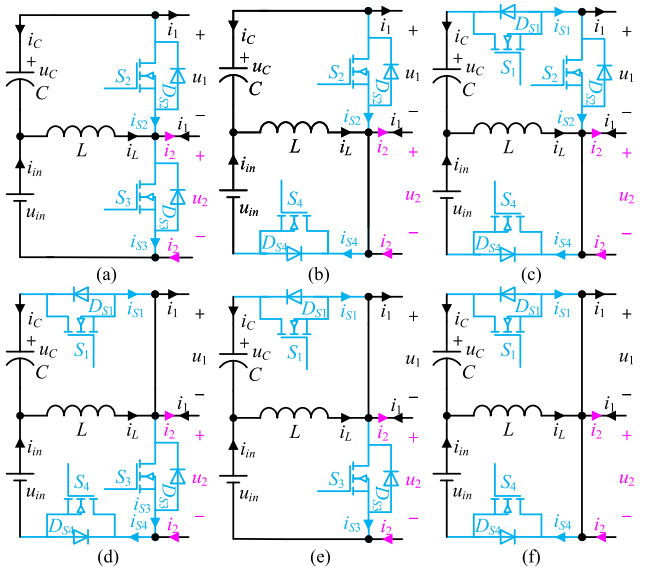


**FIGURE 11.** Equivalent topologies of the proposed inverter in (a) dual-output state, (b) first-output state, $D < 0.5$, (c) first-output state, $D > 0.5$, (d) second-output state, $D < 0.5$, (e) second-output state, $D > 0.5$, and (f) none-output state.

### B. SOFT SWITCHING STATE

Based on the designed steady-state modulation strategy in section III, the equivalent topologies of the proposed inverter in four output states are shown in Fig. 11, where $i_{S1}$, $i_{S2}$, $i_{S3}$, and $i_{S4}$ are currents flowing through $S_1$, $S_2$, $S_3$, and $S_4$, respectively. Take the dual-output state in Fig. 11(a) as an example to explain the achievement of soft switching. In Fig. 11(a), $S_2$ and $S_3$ are switched in the complementary way. If $i_{S2} > 0$ when $S_2$ is turned off, $i_{S2}$ will transfer from $S_2$ to $D_{S3}$ because $i_L$, $i_1$, and $i_2$ can't mutate, then $u_2$ will decrease to zero. Therefore, $S_3$ can achieve zero voltage (ZVS) turn on at the end of the dead time. If $i_{S2} < 0$ when $S_2$ is turned off, $i_{S2}$ will transfer from $S_2$ to $D_{S2}$ to keep $u_1$ at zero, so $S_2$ achieves ZVS turn off. To get the soft switching states in different output states, it is necessary to derive the expressions of $i_1$ and $i_2$. According to(11), the fundamental components of $i_1$ and $i_2$ can be expressed as

$$\begin{cases} i_{11}(t) = \sqrt{2}\dfrac{U_{11}\sqrt{X^2+Z^2}}{\omega_0 L_f^2 R}\sin\left(\omega_0 t + \varphi_{11} + \arctan\dfrac{Z}{X}\right) \\ i_{21}(t) = \sqrt{2}\dfrac{U_{11}\sqrt{Y^2+Z^2}}{\omega_0 L_f^2 R}\sin\left(\omega_0 t + \varphi_{21} + \arctan\dfrac{Z}{Y}\right) \end{cases} \tag{28}$$

where $X = \omega_0 {M_1}^2 + \omega_0 M_1 M_2$, $Y = \omega_0 {M_2}^2 + \omega_0 M_1 M_2$, and $Z = M_{12}R$.

Under high order harmonics, the impedance of $C_f$ is much smaller than that of the series connection of $C_p$, $L_p$, and $Z_r$. Therefore, the LCC network can be simplified to a LC series circuit [28] as shown in Fig. 12 under high order harmonics, where high order currents mainly flow through $C_f$ rather than $C_p$, so $i_{p1}$ and $i_{p2}$ are sinusoidal waves. The impedance

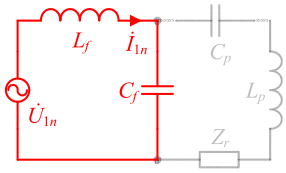


**FIGURE 12.** Equivalent circuit of the LCC network under high order harmonics.

of the LCC network under $n$th harmonic can be expressed as

$$Z_{1n} = jn\omega_0 L_f + \frac{1}{jn\omega_0 C_f} = jZ_c\frac{n^2-1}{n} \tag{29}$$

where $Z_c = \omega_0 L_f = \sqrt{L_f/C_f}$ and $n \geq 2$. Then the $n$th harmonic of $i_1$ and $i_2$ can be expressed as

$$\begin{cases} i_{1n}(t) = \sqrt{2}\dfrac{U_{1n}}{|Z_{1n}|}\sin\left(n\omega_0 t + \varphi_{1n} - \dfrac{\pi}{2}\right) \\ i_{2n}(t) = \sqrt{2}\dfrac{U_{1n}}{|Z_{1n}|}\sin\left(n\omega_0 t + \varphi_{2n} - \dfrac{\pi}{2}\right) \end{cases} \tag{30}$$

where $U_{1n}$ and $U_{2n}$ are root mean square (RMS) of $n$th harmonics of $u_1$ and $u_2$, respectively. They can be calculated from(4). Then the total expressions of $i_1$ and $i_2$ can be written as

$$i_1(t) = i_{11}(t) + \sum_{n=2}^{\infty} i_{1n}(t), \quad i_2(t) = i_{21}(t) + \sum_{n=2}^{\infty} i_{2n}(t) \tag{31}$$

The high order currents in (31) explain the cause of the distortion of $i_1$ and $i_2$. In the dual-output state, $S_2$ is turned on at time 0 and turned off at time (1-$D$)$T$, while $S_3$ is switched in complementary with $S_2$. In time interval 0-(1-$D$)$T$, $i_{S2}$ = $i_2$-$i_1$-$i_L$, while in time interval (1-$D$)$T$-$T$, $i_{S3} = i_L + i_1$-$i_2$. Then the turn off currents $i_{S2\text{-}off}$ and $i_{S3\text{-}off}$ can be written as

$$\begin{cases} i_{S2-off} = (i_2 - i_1)|_{t=(1-D)T} - i_{L-\min} \\ i_{S3-off} = i_{L-\max} + (i_1 - i_2)|_{t=0}. \end{cases} \tag{32}$$

Similarly, in the first-output state, $i_{11}(t)$ and $i_{21}(t)$ can be derived from (16), then the turn off currents $i_{S1\text{-}off}$, $i_{S2\text{-}off}$, and $i_{S4\text{-}off}$ can be expressed as

$$\begin{cases} i_{S1-off} = i_1|_{t=(1-D+0.5)T}, & D > 0.5 \\ i_{S2-off} = -i_1|_{t=(1-D)T} - i_{L-\min} & \\ i_{S4-off} = i_{L-\max} + i_1|_{t=0}, & D < 0.5 \\ i_{S4-off} = i_{L-\max}, & D > 0.5. \end{cases} \tag{33}$$

In the second-output state, the turn off currents $i_{S1\text{-}off}$, $i_{S3\text{-}off}$, and $i_{S4\text{-}off}$ can be expressed as

$$\begin{cases} i_{S1-off} = -i_{L-\min}, & D < 0.5 \\ i_{S1-off} = i_2|_{t=(1-D)T} - i_{L-\min}, & D > 0.5 \\ i_{S3-off} = i_{L-\max} - i_2|_{t=0} & \\ i_{S4-off} = i_2|_{t=0.5T}, & D < 0.5. \end{cases} \tag{34}$$

**TABLE 3. Main system parameters.**

| Parameters | Values | Parameters | Values |
|---|---|---|---|
| $U_{in}$/V | 100 | $L_p$/μH | 100 |
| $L$/μH | 250 | $L_s$/μH | 130 |
| $C$/μF | 250 | $C_s$/nF | 26.97 |
| $L_f$/μH | 30 | $R$/Ω | 10 |
| $C_f$/nF | 116.86 | $M_{12}$/μH | 5.7 |
| $C_p$/nF | 50.09 | $f_0, f_s$/KHz | 85 |

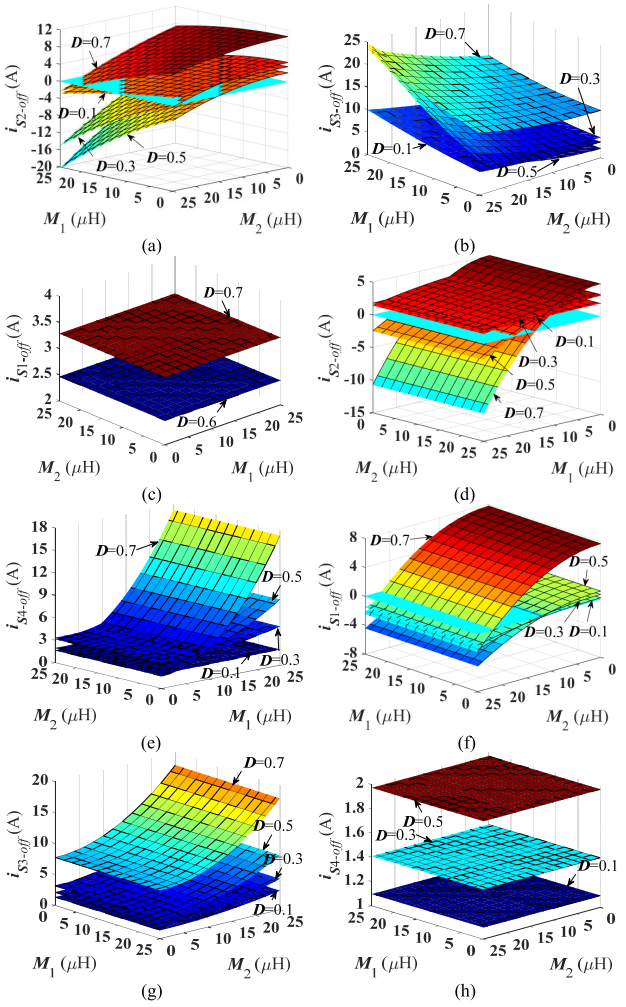


**FIGURE 13.** (a) $i_{S2\text{-}off}$ and (b) $i_{S3\text{-}off}$ in the dual-output state, (c) $i_{S1\text{-}off}$, (d) $i_{S2\text{-}off}$, and (e) $i_{S4\text{-}off}$ in the first-output state, and (f) $i_{S1\text{-}off}$, (g) $i_{S3\text{-}off}$, and (h) $i_{S4\text{-}off}$ in the second-output state versus $M_1$ and $M_2$ at different $D$.

Since there is no output power in the none-output state, its soft switching state will not be analyzed in this paper. Based on (32)-(34), turn off currents in the three effective output states versus $M_1$ and $M_2$ at different $D$ are plotted in Fig. 13. The main system parameters are listed in TABLE 3. It can be seen from Fig. 13(a) that $i_{S2\text{-}off}$ decreases from positive to negative with the increase of $M_1 + M_2$, which means that small $M_1 + M_2$ leads to the ZVS turn on of $S_3$ in

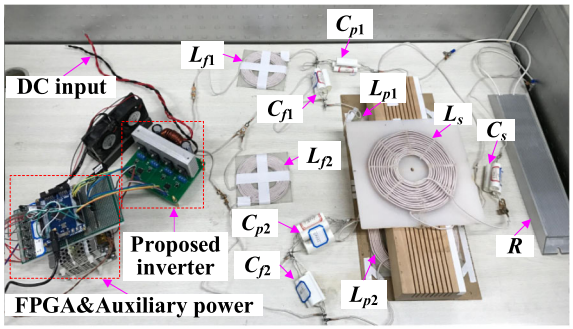


**FIGURE 14.** Experimental setup.

dual-output state, while large $M_1 + M_2$ leads to the ZVS turn off of $S_2$. In Fig. 13(b), $i_{S3\text{-}off}$ is always positive, which means that $S_2$ can always achieve ZVS turn on in the dual-output state. Fig. 13(c)-(e) indicate that the soft switching state in the first-output state is independent of $M_2$. $S_1$ and $S_2$ can always achieve ZVS turn on because $i_{S1\text{-}off}$ and $i_{S4\text{-}off}$ are always positive. Small $M_1$ leads to ZVS turn on of $S_4$, while large $M_1$ leads to ZVS turn off of $S_2$. Fig. 13(f)-(h) indicate that the soft switching state in the second-output state is independent of $M_1$. When $D < 0.5$, based on the topology in Fig. 11(d), $S_1$ and $S_3$ can always achieve ZVS turn on because $i_{S3\text{-}off}$ and $i_{S4\text{-}off}$ are always positive. Small $M_2$ leads to the ZVS turn on of $S_4$, while large $M_2$ leads to the ZVS turn off of $S_1$. When $D > 0.5$, based on the topology in Fig. 11(e), $S_1$ can always achieve ZVS turn on because $i_{S3\text{-}off}$ is always positive. Small $M_2$ leads to the ZVS turn on of $S_3$, while large $M_2$ leads to the ZVS turn off of $S_1$.

## V. SIMULATION AND EXPERIMENTAL RESULTS

To verify the proposed inverter and the theoretical analysis, a DWPT system based on the proposed inverter is simulated in MATLAB/Simulink. Moreover, an experimental setup is implemented as shown in Fig. 14. Main parameters of the system are listed in TABLE 3. The designed $D_{\max} = 0.7$, $r_{i-\max} = 40\%$, and $r_{u-\max} = 5\%$. The FPGA (EP2C5T144C8N) controller is used to generate four logic signals with different duty cycles and phases, which are converted by two isolated dual-channel gate drivers into pulse voltages with appropriate amplitudes, to drive $S_1$-$S_4$. Meanwhile, two switching signals $S_{t1}$ and $S_{t2}$ that were defined in Fig. 10 are inputted into the FPGA to switch the output state of the proposed inverter. The schematic diagram of the magnetic coupler is shown in Fig. 15(a), and the measured mutual inductances versus the relative position $x$ between the pickup coil and primary tracks are shown in Fig. 15(b). It can be seen that $M_1$ and $M_2$ reach peak value at $x = -7.5$cm and 7.5cm, respectively. $M_1 + M_2$ is relatively symmetric, while $M_{12}$ is constant.

As shown in Fig. 15(b), when $-3.75\text{cm} < x < 3.75\text{cm}$, both$M_1$ and $M_2$ are less than $M_1 + M_2$. Therefore, when the pickup coil moves from $x = -15$cm to 15cm, $x = -15$cm, $-3.75$cm, 3.75cm, and 15cm are selected as the

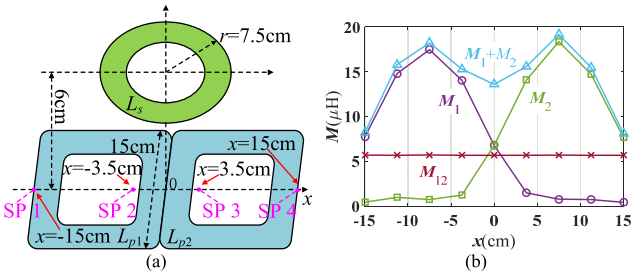


**FIGURE 15.** (a) Schematic diagram and (b) measured mutual inductances versus $x$ of the Magnetic coupler.

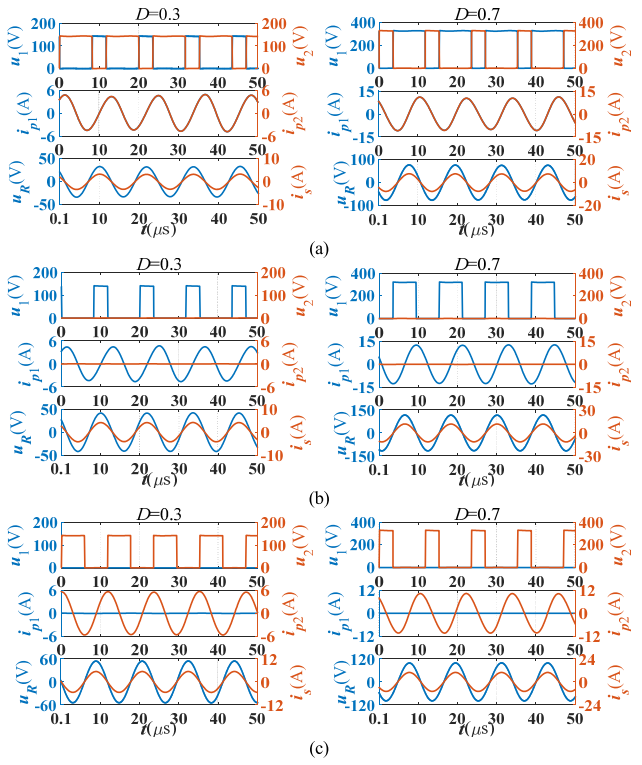


**FIGURE 16.** Simulation waveforms in the primary and pickup sides in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.3$ and 0.7.

switching points (SP) of the none-output to the first-output state, the first-output to the dual-output state, the dual-output to the second-output state, and the second-output to the none-output state, respectively.

When $x = 0$, $-7.5$cm, and 7.5cm, the proposed inverter operates in the dual-output, first-output, and second-output states, respectively. The simulation and experimental waveforms in the primary and pickup sides in the three output states when $D = 0.3$ and 0.7 are shown in Fig. 16 and Fig. 17, respectively. It can be seen that the simulation and experimental values of $U_b$ are about 140V and 330V when $D = 0.3$ and 0.7, respectively. While the theoretical values of $U_b$ are 142.8V and 333.4V, respectively. They are basically consistent. In the dual-output state, both the simulation and experimental results show that $u_1$ and $u_2$ are complementary.

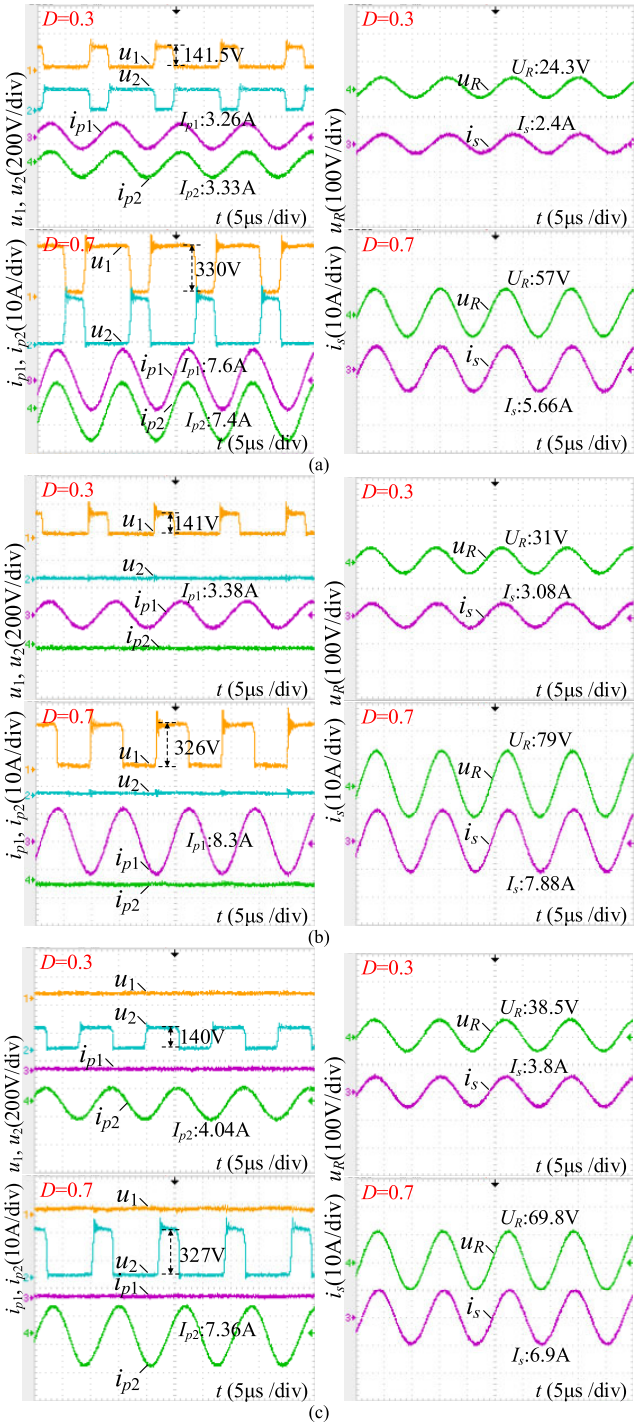


**FIGURE 17.** Experimental waveforms in the primary and pickup sides in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.3$ and 0.7.

According to the values of $I_{p1}$ and $I_{p2}$, $U_{11}$ ($= U_{21}$) can be calculated as about 53.4V and 121.8V when $D = 0.3$ and 0.7, respectively. In the first-output state, $u_2$ in both the simulation and the experiment keeps at zero. $U_{11}$ can be calculated as about 54V and 144.2V when $D = 0.3$ and 0.7, respectively. In the second-output state, $u_1$ in both the simulation and the

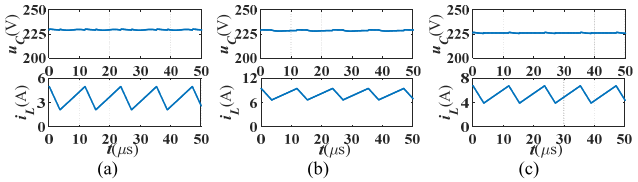


**FIGURE 18.** Simulation waveforms of $u_C$ and $i_L$ in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.7$.

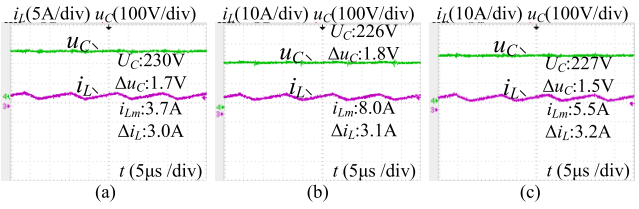


**FIGURE 19.** Experimental waveforms of $u_C$ and $i_L$ in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.7$.

experiment keeps at zero. $U_{21}$ can be calculated as about 64.7V and 117.9V when $D = 0.3$ and 0.7, respectively. In the dual-output state, both the simulation and experimental results show that $i_{p1}$ and $i_{p2}$ are almost the same and in phase. The minor error in the experiment is mainly caused by the inherent error between two LCC networks. The above results verify the correctness of the theoretical analysis, the independent controllability and gain characteristics of two outputs, and the feasibility of the designed steady-state modulation strategy. As can be seen from the pickup side, when $D = 0.7$ and $x = -7.5$cm, $u_R$ in the first-output state is the largest, thus this point is selected for the inverter parameter design.

Fig. 18 and Fig. 19 show the simulation and experimental waveforms of $u_C$ and $i_L$ in the three output states when $D = 0.7$. It can be seen from Fig. 19 that in the first-output state, $U_C = 226$V, $\Delta u_C = 1.8$V, $I_L = 8$A, and $\Delta i_L = 3.1$A, then $r_{uC} = 0.8\%$ and $r_{iL} = 38.75\%$. The results meet the designed requirements of $r_{uC} < 5\%$ and $r_{iL} < 40\%$, which indicates the reasonableness of the value of $L$ and $C$. The simulation results shown in Fig. 18 show good agreement with the experimental results shown in Fig. 19, verifying the theoretical analysis.

Fig. 20 shows the experimental switching waveforms of power switches in three effective output states when $D = 0.3$ and 0.7, where the dead time $t_d$ is set to 300ns, and $u_{S1}$, $u_{S2}$, $u_{S3}$, and $u_{S4}$ are voltages of $S_1$, $S_2$, $S_3$, and $S_4$, respectively. As can be seen from Fig. 20(a), before $S_2$ is turned on, $u_{S2}$ has decreased to zero due to the turn off of $S_3$, so $S_2$ can achieve ZVS turn on. Similarly, before $S_3$ is turned on, $u_{S3}$ has decreased to zero due to the turn off of $S_2$, so $S_3$ can achieve ZVS turn on. In Fig. 13(a), it is calculated that $S_3$ can achieve ZVS turn on if $M_1 + M_2 < 24\mu$H at $D = 0.3$, and $M_1 + M_2 < 45\mu$H at $D = 0.7$, respectively. In Fig. 15(b), $M_1 + M_2$ at $x = 0$ is about 13.6$\mu$H, so the experimental

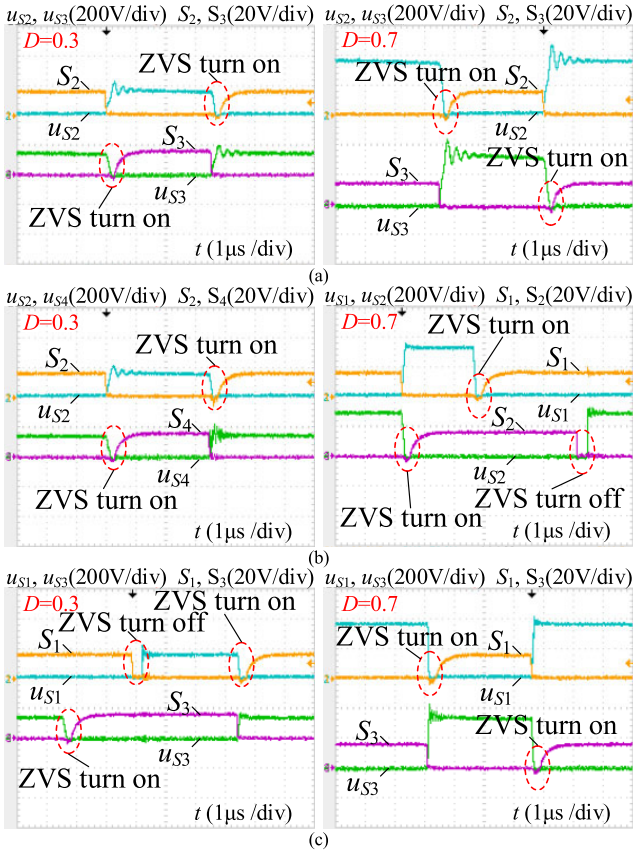


**FIGURE 20.** Experimental switching waveforms of power switches in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.3$ and 0.7.

soft switching state is consistent with the theoretical analysis. Similarly, as can be seen from Fig. 13(b), at $x = -7.5$cm, $S_2$ and $S_4$ can achieve ZVS turn on when $D = 0.3$, while $S_1$ can achieve ZVS turn on and $S_2$ can achieve ZVS turn on and turn off when $D = 0.7$. Further, at $x = 7.5$cm, $S_1$ can achieve ZVS turn on and turn off and $S_3$ can achieve ZVS turn on when $D = 0.3$, while $S_1$ and $S_3$ can achieve ZVS turn on when $D = 0.7$.

Fig. 21 shows the experimental waveforms in the primary side during the output state switching processes when $D = 0.5$. As can be seen from Fig. 21(a) and (b), when the two outputs are opened respectively, the corresponding primary track current will generate a short overshoot and then quickly enter the steady state. In Fig. 21(c) and (d), when the two outputs are closed respectively, the corresponding primary track current will decrease to zero quickly. Moreover, the closing and opening of each output don't affect the voltage of the other output. Although there are some oscillations to $i_{p1}$ and $i_{p2}$, the amplitudes are small and the durations are short, which do not affect the operation of the inverter. In general, the output state switching processes are smooth, and there are no high voltage and current spikes. All switching processes can be completed within 1ms, which means the proposed inverter has a fast output state switching speed and is suitable for DWPT system.

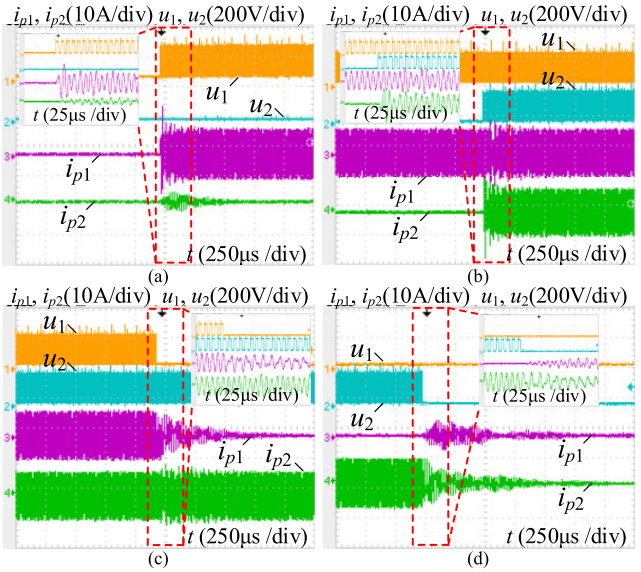


**FIGURE 21.** Experimental waveforms in the primary side during switching processes of (a) the none-output to the first-output state, (b) the first-output to the dual-output state, (c) the dual-output to the second-output state, and (d) the second-output to the none-output state when $D = 0.5$.

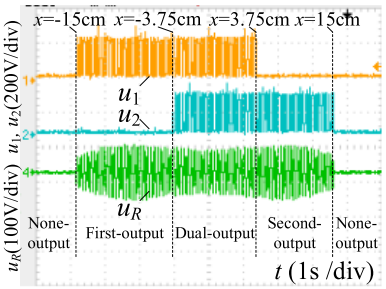


**FIGURE 22.** Experimental waveforms of $u_1$, $u_2$, and $u_R$ during the process of the pickup coil moving from $x = -15$cm to 15cm when $D = 0.5$.

Fig. 22 shows the experimental waveforms of $u_1$, $u_2$, and $u_R$ during the process of the pickup coil moving from $x = -15$cm to 15cm when $D = 0.5$. It can be seen that with the movement of the pickup coil, the output states of the proposed inverter are switched sequentially, and the envelop of $u_R$ is smooth without mutation and spike, which means that the proposed inverter can achieve smooth and stable dynamic wireless power supply.

Fig. 23 shows the experimental waveforms of load variation in three effective output states when $D = 0.5$. In this experiment, the load resistance $R$ is suddenly raised from 10Ω to 15Ω and then suddenly decreased back to 10Ω. As shown in Fig. 23, in all three output states, $u_1$, $u_2$, and $u_R$ can keep constant when $R$ varies, except for $i_s$. Moreover, all transition time is within 200$\mu$s, which means that the proposed inverter has a fast dynamic response performance.

Define $\eta$ as system efficiency. Fig. 24 shows $P_o$ and $\eta$ versus duty cycle $D$ in three effective output states. As can be seen from Fig. 24(a), when $D < 0.5$, $P_o$ in the first-output state is lower than that in the second-output state.

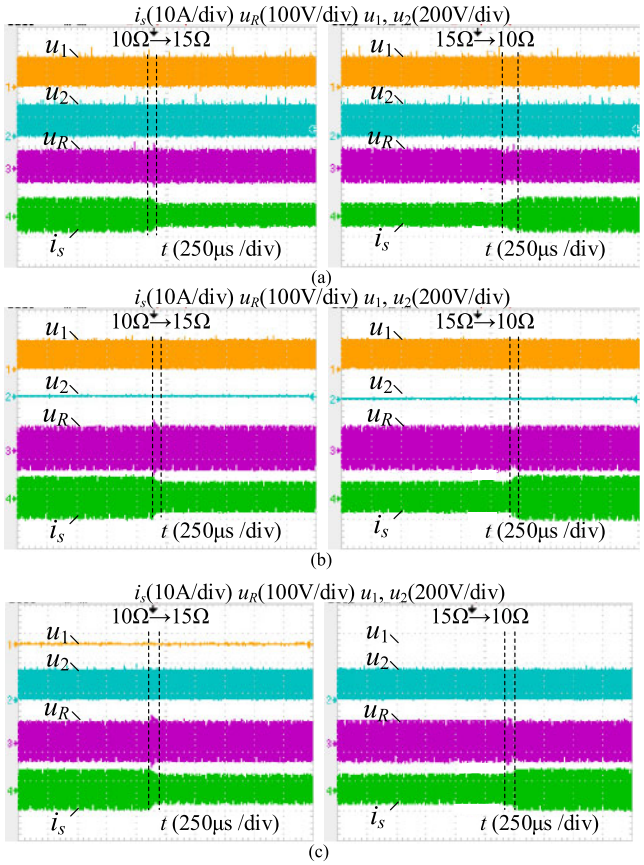


**FIGURE 23.** Experimental waveforms of load variation in (a) $x = 0$, the dual-output state, (b) $x = -7.5$cm, the first-output state, and (c) $x = 7.5$cm, the second-output state when $D = 0.5$.

When $D > 0.5$, $P_o$ in the first-output state is higher than that in the second-output state, and the $P_{o-\max}$ is 700W. In the three output states, when $D$ is small, $\eta$ in the first-output state is the largest, while $D$ is large, $\eta$ in the second-output state is the largest, and the maximum value is 88%.

The comparison results of the proposed inverter with the existing multi-output inverters in terms of the output power, the system efficiency, and the output switching time are shown in TABLE 4. As can be seen from TABLE 4, except for the MLI, both the output power and system efficiency of the VTMOI and the SIMOI are lower than that of the proposed inverter. However, the system efficiency of the MLI was not mentioned. In term of the output switching time, the experimental switching waveforms of the MLI were given but the switching time was not mentioned. For the SIMOI, there was no relevant theoretical analysis or experimental results. The switching time of the VTMOI is 2.5ms, which is longer than that of the proposed inverter. In general, the proposed inverter is more efficient and more suitable for DWPT system.

To better understand the proposed inverter, the power loss distribution in all components when $P_o = 700$W is measured and calculated as shown in Fig. 25. It can be seen that the switching loss of $S_1$-$S_4$ and loss in $L$ are the major

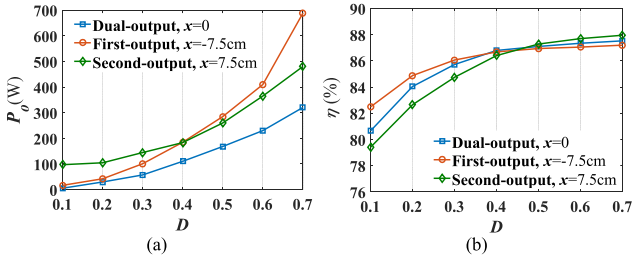


**FIGURE 24.** (a) $P_O$ and (b) $\eta$ versus $D$ in three effective output states.

**TABLE 4.** Comparison of the proposed inverter with the existing multi-output inverters.

| | Output power | System efficiency | Output switching time |
|---|---|---|---|
| MLI in [23] and [24] | 5.6kW | Not mentioned | Not mentioned |
| VTMOI in [26] | 17.3W | 85% | 2.5ms |
| SIMOI in [25] | 6W | 84.5% | Not mentioned |
| Proposed | 700W | 88% | <1ms |

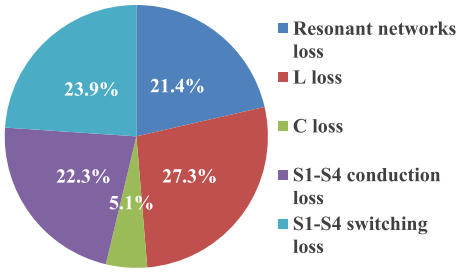


**FIGURE 25.** Power loss distribution in all components when $P_O$ = 700W.

contributors to total power loss, optimization of which can be the research focus in the future.

## VI. CONCLUSION

Aiming at the large number of required inverters in DWPT system with multi-inverter driving mode, this paper proposes a dual-independent-output inverter, which consists of four power switches, one inductor, and one capacitor. It can generate two independently controllable outputs to replace conventional VFFBI to realize on-demand driving of the same number of primary tracks with less number of power switches and higher redundancy than the existing multi-output inverters, which can simplify the design and control of the system. The experimental results show that each output of the proposed inverter can achieve fast and smooth switching and dynamic response without affecting the other output, which are more suitable for DWPT system of high moving speed. In all the three effective output states of the proposed inverter, there are always some power switches that can achieve soft switching. The system efficiency maintains at a high level as the pickup coil moves along primary tracks, and the maximum value can reach 88%, which is higher than the state of art.

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