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A Programmable Single-Phase Multilevel Current Source Inverter

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ABSTRACT The conventional single-phase multilevel current source inverters suffer from the high count of switches for increasing the levels. Therefore, how to generate more levels with reduced-count of switches is attractive. In this paper, a programmable single-phase current source inverter is presented. It can achieve the programmable level output with only five switches. Different from the existing single-phase reduced-count multilevel inverters, it has the advantages of a simple structure and programmable level output. Finally, the simulation and experimental tests are carried out. And, the experimental results verify the effectiveness of the proposed programmable multilevel inverter.

INDEX TERMS Current source inverter, single-phase inverter, multilevel inverter.

I. INTRODUCTION

In recent years, the renewable energy utilization is developed in a rapid pace, such as wind and solar energy power generation. As an interface between the renewable energy and grid, the inverter is a necessity. In general, it can be divided into the voltage-source inverter and the current-source inverter. So far, the research on topology, control methods, modulation strategies of the voltage source inverter is extensive. However, the current source inverter has not been well explored. With development of the wide-bandgap semiconductor devices, the current source inverter has been attracted more and more attentions [1]. The current source inverter is attractive for future industrial applications [2]–[5]. Compared to the voltage source inverter, it has the advantages of high reliability, long life, the inherent current limiting capability and excellent quality of output waveform [6]. In fact, it has been used in industrial application such as the uninterrupted power supply system from GE [7], electric aircraft power system [8], photovoltaic power system [9], wind power generation system [10], flexible AC transmission system [11], high voltage direct current transmission system from ABB [12], and so on.

The converter topology is the attractive topic of power electronics technology. For the single-phase multilevel current source inverters, they can be generally divided into two categories. One is the directly constructed type, and the other is the modular combined type. The classification of conventional single-phase multilevel current source inverters (SPMCSI) topologies is shown in Fig. 1 and the further details about each topology will be discussed in section II.

Basically, the conventional multilevel inverters suffer from the high count of switches for increasing the levels [13]–[17]. Therefore, how to generate more levels with reduced-count of switches is attractive. In general, the multiple switches, inductors, diodes, or dc current sources are needed for the traditional single-phase multilevel current source inverters. In order to overcome the abovementioned limitation, a programmable single-phase current source inverter is presented in this paper. Furthermore, the proposed topology doesn't have the inductance current sharing issue compared to the traditional SPMCSI.

The rest paper is organized as follows. Section II presents a brief review of traditional single-phase multilevel current source inverters. Section III presents the proposed programmable inverter and its modulation strategy and parameters design. The simulation and experimental results are provided in Section IV and Section V, respectively. The conclusion is reached in Section VI.

II. BRIEF REVIEW OF SPMCSI

A. DIRECT-CONSTRUCTED TOPOLOGIES

The feature of directly constructed topologies is that the multiple switches and inductors (or current sources) are used, and

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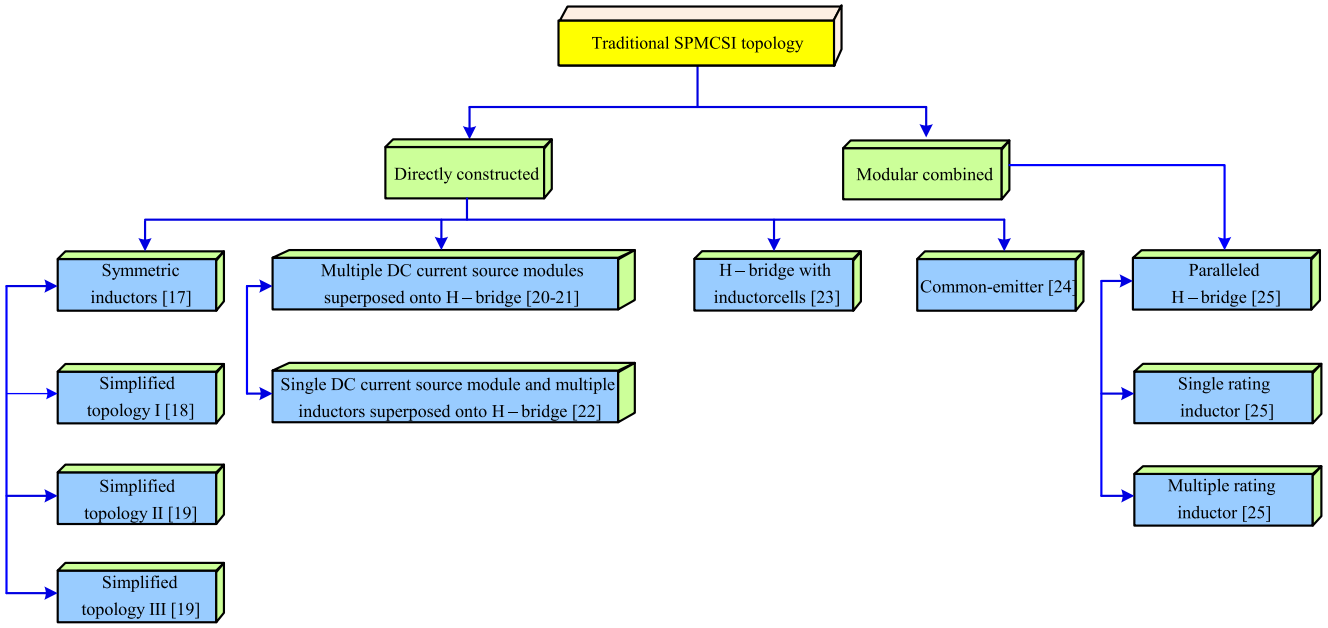

FIGURE 1. Classification of single-phase multilevel current source inverters (SPMCSI).

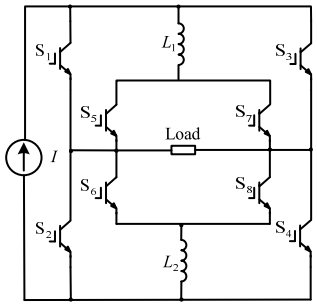

FIGURE 2. Symmetric inductors topology.

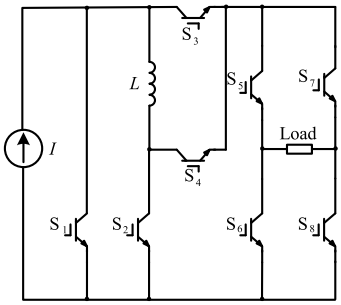

FIGURE 3. Simplified topology I.

there is no multi-module parallel connection at the AC side. A typical directly constructed topology is proposed in [18]. The topology adopts a symmetrical structure and any of two switches connected to the same point of the sharing inductor are complementary ones. The disadvantage of this topology is that the number of switches and the number of inductors are relatively large. For each additional level, four switches and two diodes need to be added.

In order to reduce the number of switches and inductors, many interesting simplified topologies are proposed based on the Fig. 2. The simplified topologies are named as the simplified topology I [19], simplified topology II [20] and simplified topology III [20], which are shown in Fig. 3, Fig. 4, and Fig. 5, respectively.

Compared with Fig. 2, one switch is reduced in the simplified topology I, and only one inductor and two switches are needed for each additional level. The simplified topology is a two-stage structure. The front-stage is an inductor shunt structure and multiple levels are realized. The latter-stage is an H-bridge structure to realize the current commutation.

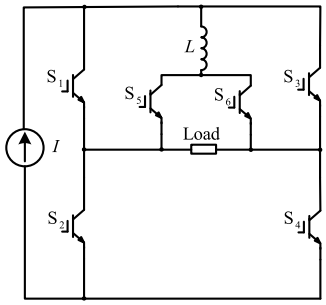

FIGURE 4. Simplified topology II.

The simplified topology II and the simplified topology III are presented in [20]. Two switches and an inductor are reduced in the simplified topology II and III. Compared with Fig. 2, only one inductor and two switches are needed for each additional level.

To further reduce the number of switches, another directly constructed single-phase multilevel current source inverter is

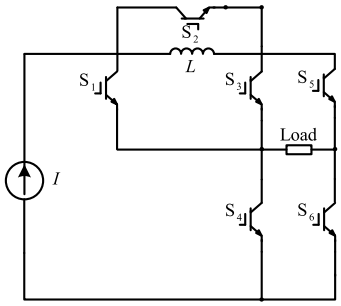

FIGURE 5. Simplified topology III.

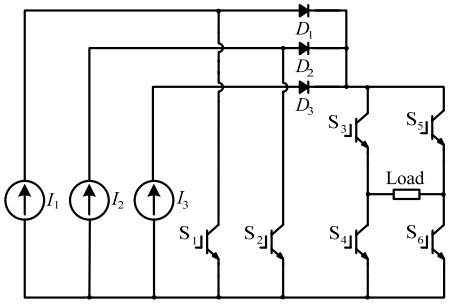

FIGURE 6. Multiple DC current source modules superposed onto H-bridge SPMCSI topology.

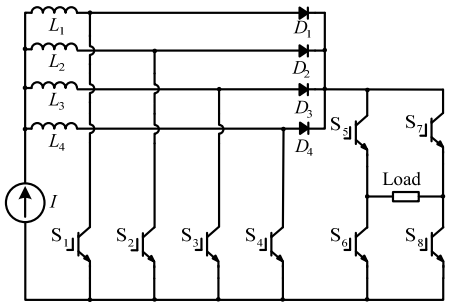

FIGURE 7. Single DC current source module and multiple inductors superposed onto H-bridge SPMCSI topology.

proposed in [21], [22]. As shown in Fig. 6, only one current source and one switch are needed for each additional level. But multiple current sources with identical characteristics are needed in this topology. A similar topology is presented in [23]. Multiple inductors are used instead of current sources as shown in Fig. 7. But the current imbalance issue exists in this topology.

When the switches are not connected to the common emitter, multiple separate auxiliary power units are required. In order to reduce the complexity of the drive circuit, a common-emitter SPMCSI topology is proposed in [24] which is shown in Fig 8. The advantage of this topology is that only one auxiliary power unit is needed, but multiple current sources are required.

The SPMCSI topologies with inductive shunting are expected to achieve equal sharing of inductor current. Most of these topologies rely on switch symmetry to control the

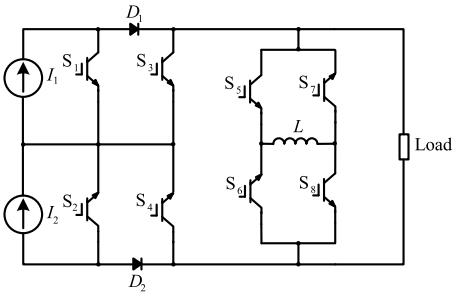

FIGURE 8. Common-emitter SPMCSI topology.

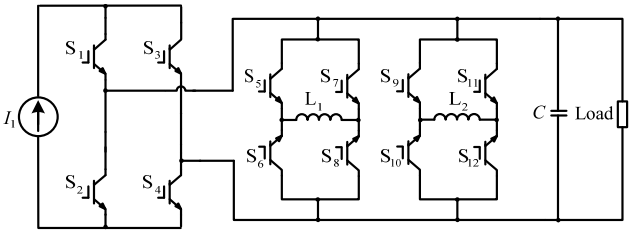

FIGURE 9. H-bridge with inductor cells SPMCSI topology.

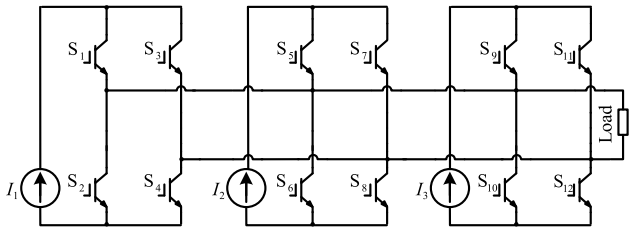

FIGURE 10. Paralleled H-bridge SPMCSI topology.

magnitude of the inductor current. The current imbalance issue exists in these topologies which will reduce the quality of the output waveform of the converter and affect the stability of the system. In [25], an H-bridge combined inductance cell topology is presented, as shown in Fig.9. The H-bridge with inductor cells topology is also a two stage topology. The front-stage is a conventional H bridge structure to achieve pulse width modulation and current commutation. The latter-stage is multiple inductance cells. The intermediate level can be achieved by controlling the current of the inductance cells.

B. MODULAR-COMBINED TOPOLOGIES

The feature of the modular combined SPMCSI topologies is that multiple H-bridge cells are connected in parallel at the AC side to form the multi-level and the number of levels can be expanded flexibly, as shown in Fig. 10. Three typical modular combined topologies are proposed in [26].

The paralleled H-bridge topology consists of three independent single phase H-bridge cells connected in parallel and the independent current source is used in each cell. The single rating inductor SPMCSI can be achieved by two single rating

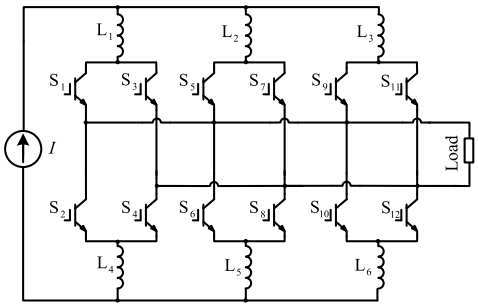

FIGURE 11. Single rating inductor SPMCSI topology.

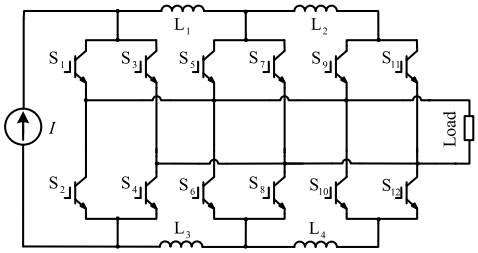

FIGURE 12. Multiple rating inductor SPMCSI toplology.

inductor cells as shown in Fig. 11. Similar to the single rating inductor SPMCSI, the two rating inductor cells can form a SPMCSI as shown in Fig. 12.

In summary, the conventional single-phase multilevel current source inverters suffer from the high count of switches for increasing the levels. Therefore, how to generate more levels with reduced-count of switches is attractive. A new single-phase current source inverter will be presented in the next section.

III. PROPOSED TOPOLOGY

A. OPERATION PRINCIPLE

In order to overcome the abovementioned problem, a new single-phase multilevel current source inverter is proposed, as shown in Fig. 13. Different from the existing single-phase reduced-count multilevel inverters, it has the advantages of a simple structure and programmable level output. Firstly, the input current is regulated with the switch of S in Fig. 13. The average output current is a function of duty cycle and input current, as shown in (1), where I_{ave} is the average output current, I_{dc} is the input current, T_{off} and T_{on} are the turn-off and turn-on times, respectively, and D is the duty cycle for the switch of S.

$$I_{ave} = \frac{T_{off}}{T_{on} + T_{off}} I_{dc} = DI_{dc} \tag{1}$$

Different from the existing idea, the duty cycle is not constant, but controlled as an n-level function. And then the corresponding n-level waveform is transformed by a synchronized H-bridge. In this way, the programmable level output can be achieved with only five switches.

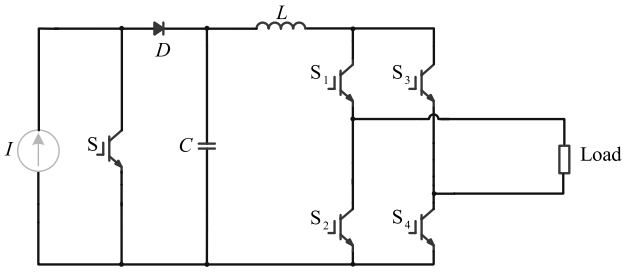

FIGURE 13. Proposed single-phase multilevel current source inverter.

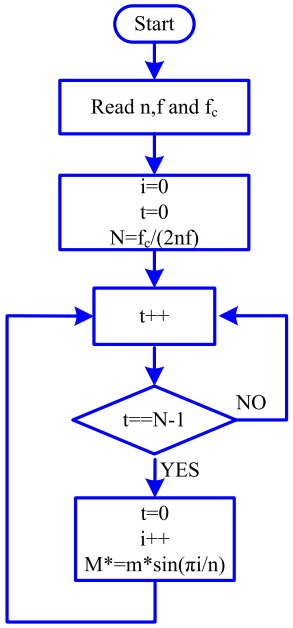

FIGURE 14. The flowchart to get the piecewise constant sinusoidal fashion modulated wave m*.

B. MODULATION STRATEGY

In order to get an arbitrary level output, the piecewise constant sinusoidal fashion as the modulated wave should be gained. The flowchart to generate the varying the modulated wave m* is shown in Fig. 14 and described step by step as follows.

First step: initialize the value of n, f and f_c, where n is the number of the output levels, f is the frequency of the output and f_c is the interrupt frequency of the microcontroller unit.

Second step: initialize variables t and i and calculate the variable N according to the relationship of the value of n, f and f_c where $N = f_c/(2nf)$ where t, i and N are the variables.

Third step: the variable t is increased by 1.

Forth step: If the variable t is less than N−1, return the third step.

Fifth step: If the variable t is equal to N−1, the variable t is set to zero, the variable i is increased by 1 and the modulated wave m* is generated by setting M* equals to m* sin(π i/n), where m is the modulation ratio. Then, return the third step.

After getting the piecewise constant sinusoidal modulated wave m* from Fig. 14, the drive signals can be gained

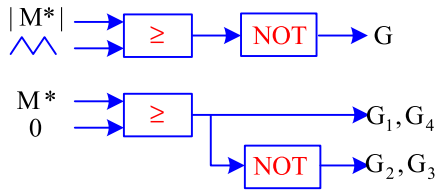

FIGURE 15. Modulation strategy of the proposed SPMCSI topology.

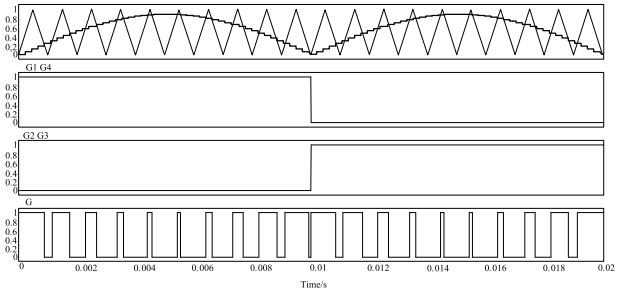

FIGURE 16. The modulation waveform of the proposed SPMCSI topology.

according to the Fig. 15. If the modulated wave after taking absolute value is lower than the carrier, the G is high. If not, the G is low. And in the positive half cycle of the modulated wave, the G_1 and G_4 is high, the G_1 and G_4 is low in the other half cycle of the modulated wave. The logical of G_2, G_3 and G_1, G_4 is opposite. The related waveform is shown in Fig.16.

According to the above analysis, the proposed SPMCSI works in the following four working states.

First mode: In this mode, switches S_1 and S_4 are turned on, whereas switches S, S_2 and S_3 are turned off, as depicted in Fig. 16 (a). The input current is dived into two parallel branches and the capacitor is charged by I_{dc} during this period.

Second mode: In this mode, switches S, S_1 and S_4 are turned on, whereas switches S_2 and S_3 are turned off, as depicted in Fig. 16 (b). The input current is short by S and the diode is reversed due to the capacitor voltage. The capacitor is discharged during this period.

Third mode: In this mode, switches S_2 and S_3 are turned on, whereas switches S, S_1 and S_4 are turned off, as depicted in Fig. 16 (c). The input current is dived into two parallel branches and the capacitor is charged by I_{dc} during this period.

Fourth mode: In this mode, switches S, S_2 and S_3 are turned on, whereas switches S_1 and S_4 are turned off, as depicted in Fig. 16 (d). The input current is short by S and the diode is reversed due to the capacitor voltage. The capacitor is discharged during this period.

In the second and fourth modes, the current source is in short-circuit state, which is not allowed in voltage source converters. However, the short circuit state is an important state for the impedance source converters and current source converters, described in [27]–[29].

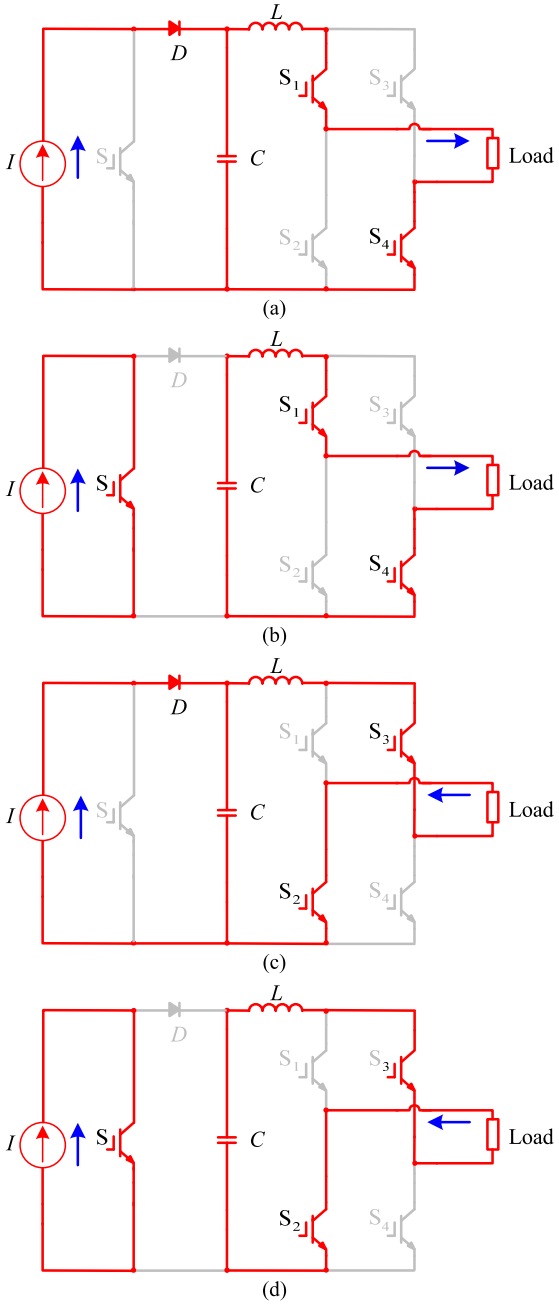

FIGURE 17. Working states of the proposed SPMCSI (a) First mode; (b) Second mode; (c) Third mode; (d) Fourth mode.

C. PARAMETERS DESIGN

The CL filter of the current type converter can filter out the high order harmonic in the output current. In order to achieve better filtering, it is necessary to design the CL filter. The transfer function of CL filter can be expressed as

$$G(s) = \frac{1}{LCs^2 + rCs + 1} \tag{2}$$

It can be seen that the CL filter is a second order transfer function. The cut-off frequency and damping ratio of the CL

TABLE 1. Simulation parameters.

Component	Value
current source	10 A
Filter capacitance	9.4 μF
Filter inductance	250 μH
load	10 Ω
Switching frequency of S	40 kHz
Switching frequency of S_1-S_4	50 Hz

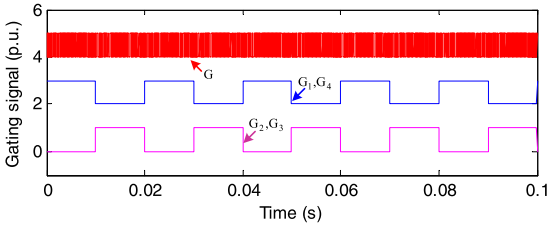

FIGURE 18. Gate pulses for the switches of the proposed topology.

filter are

$$\begin{cases} f_0 = \dfrac{1}{2\pi\sqrt{LC}} \\ \xi = \dfrac{r}{2}\sqrt{\dfrac{C}{L}} \end{cases} \tag{3}$$

Since the high order harmonic of the AC current is mainly concentrated at the switching frequency and its integral multiple, the cut-off frequency should be much smaller than the switching frequency. At the same time, the cut-off frequency should be much larger than the fundamental frequency in order to ensure that the fundamental component is transmitted without attenuation. The cut-off frequency can be selected as shown in (4). In addition, the suitable damping ratio should be selected in order to suppress resonance.

$$10f_g < f_0 < 0.5f_{sw} \tag{4}$$

IV. SIMULATION

In order to test the performances of the proposed single phase multilevel current source inverter, a series of simulations have been done in Matlab/Simulink®2013a. The simulation parameters are listed as follows which have been shown in Tab. 1. The input current source is set to 10 A. The filter capacitance is set to 9.4 μF. The filter inductance is set to 250 μH. The switching frequency of S is set to 40 kHz and the switching frequency of $S_1 - S_4$ is set to 50 Hz, respectively. The load is set to 10 Ω.

Using the parameters from Tab.1, the simulations have been done. The gate pulses for the switches of the proposed topology are shown in Fig. 18. It can been seen from Fig. 18, only the switch S works in high frequency conditions and the other four switches work in low frequency conditions. Therefore, the proposed topology has low switching loss.

The Fig. 19 to Fig. 27 show the simulation results under different conditions. Fig. 19 gives out the output voltage and load current of the nine-level SPMCSI. Related waveforms

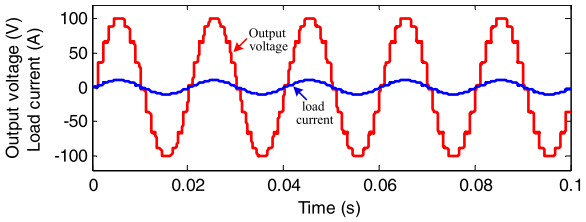

FIGURE 19. 9-level output voltage and load current.

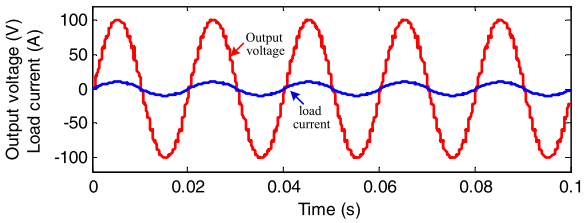

FIGURE 20. 15-level output voltage and load current.

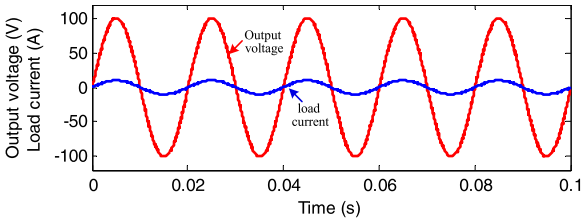

FIGURE 21. 200-level output voltage and load current.

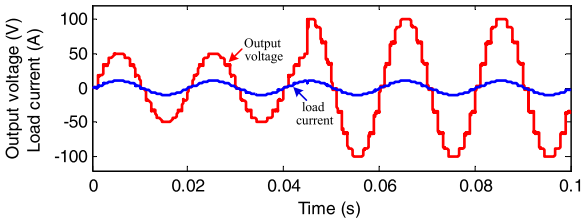

FIGURE 22. 9-level output voltage and load current under load changes.

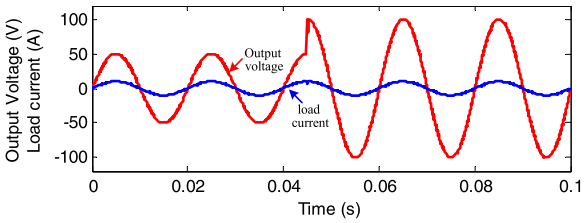

FIGURE 23. 200-level output voltage and load current under load changes.

of 15-level SPMCSI and 200-level SPMCSI are shown in Fig. 20 and Fig. 21, respectively. Fig. 22 and Fig. 23 give out related waveform of 9-level and 200-level SPMCSI under load changes from 5 Ω to 10 Ω suddenly, respectively. It can be seen from Fig. 22 and Fig. 23, the output voltage changes with the load and the output exhibits current sourece characteristics. Furthermore, the total harmonic distortion (THD)

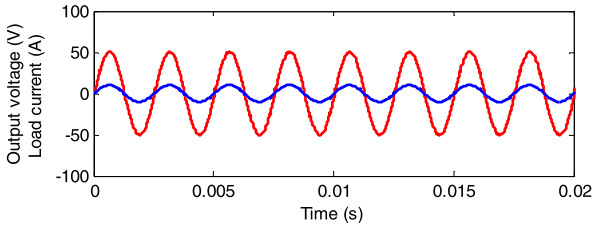

FIGURE 24. 200-level and 400 Hz output voltage and load current.

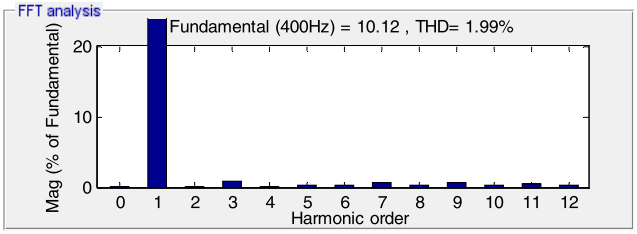

FIGURE 25. The FFT analysis of the output current.

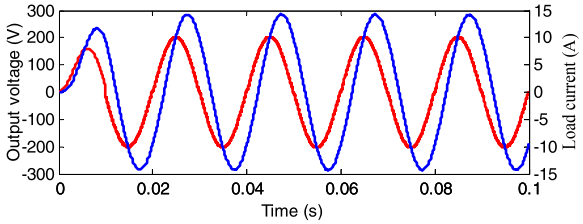

FIGURE 26. 200-level output voltage and load current under R-L load conditions.

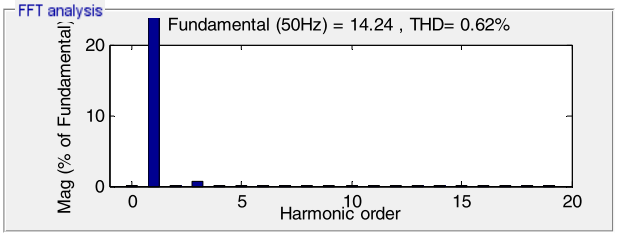

FIGURE 27. FFT analysis of the output current under R-L load conditions.

TABLE 2. THD of different levels.

No. levels	THD
5	16.48
7	11.16
9	8.18
11	7.05
15	4.21
45	1.29
200	0.80

of output current is calculated by the FFT Analysis tool of Simulink. The THD of output current under different level conditions is listed in Tab. 2. It can be seen form Tab. 2 that the better output waveform can be obtained as the number of levels increases.

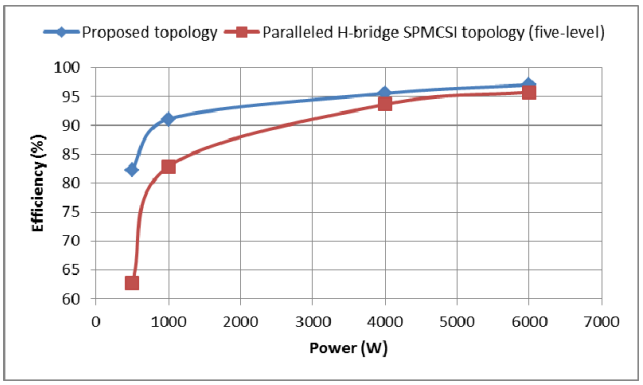

FIGURE 28. Efficiency of the proposed topology and the paralleled H-bridge SPMCSI topology.

Normally, the frequency of output current is 50 Hz. If the level of the output current is high, for example the 400 Hz in the field of aviation, the switching frequency of S_1-S_4 should also be set to 400 Hz. Although a better output waveform can be obtained, the efficiency will decrease because of switching loss, if the switching frequency of S is higher. The simulation for 200-level and 400 Hz output is carried out. The load is set to 5 Ω and the switching frequency of S_1-S_4 is set to 400 Hz. The other simulation parameters are the same as Tab. 1. From Fig.24 to Fig. 25 it can be observed that the sinusoidal output waveform can be obtained when the required frequency and level of the output current are both high. The 40 kHz for the switching frequency of S is enough to meet the IEEE standard, if the required frequency and level of the output current are both high.

The simulation and the corresponding experiment under R-L load conditions have been done. The R load is set to 10 Ω and the L load is set to 30 mH. The other simulation parameters are the same as Tab. 1. Fig. 26 shows the waveform of 200-level SPMCSI under R-L load conditions. And the FFT analysis of the output current is shown is Fig. 27. It can be seen from Fig. 26 and Fig. 27, the proposed topology works well under R-L load conditions.

The conventional single-phase multilevel current source inverters suffer from the high count of switches for increasing the levels. The proposed topology can achieve the programmable level with only five switches. The switching power loss of the proposed topology is comparatively low for the two reasons as follows. First it has lower count of switches. Second, only one power semiconductor switch is operating at high frequency and the rest (four power semiconductor switches of H-bridge) are operating at fundamental frequency. Hence, the proposed topology has high efficiency compared with the conventional multilevel inverters. The efficiency of the proposed topology and the paralleled H-bridge SPMCSI five-level topology is shown in Fig. 28. It can be seen from Fig. 28 that the proposed topology has higher efficiency than the traditional SPMCSI.

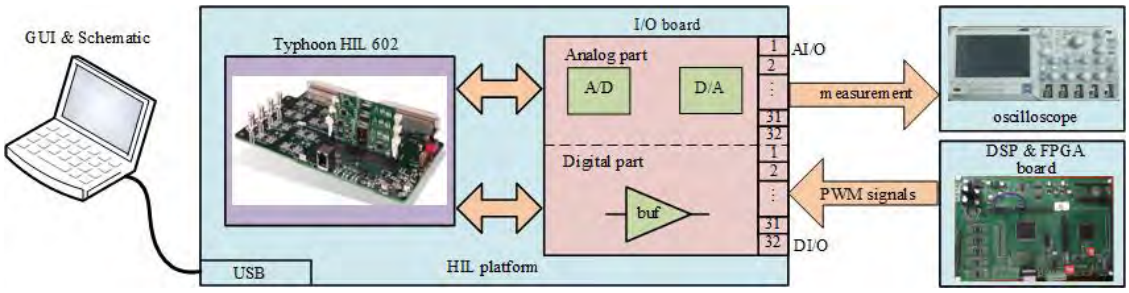

FIGURE 29. HIL emulator hardware description.

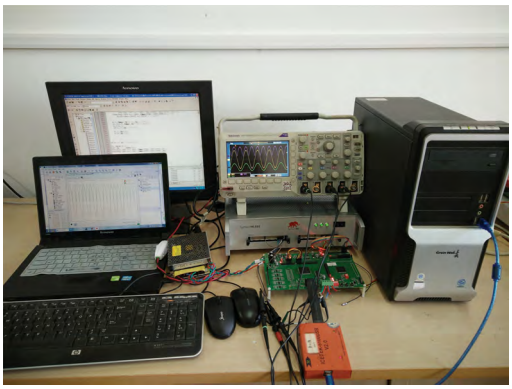

FIGURE 30. Photograph of experimental prototype.

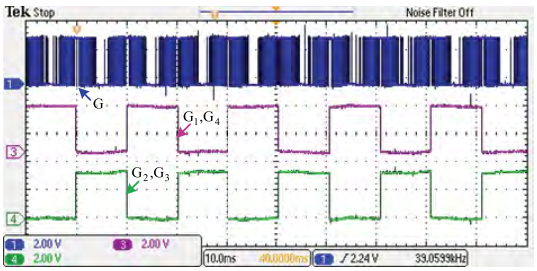

FIGURE 31. Gate pulses for the switches of the proposed topology.

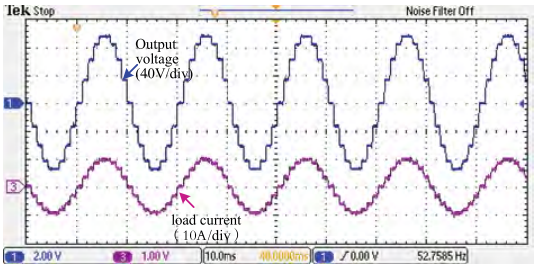

FIGURE 32. 9-level output voltage and load current.

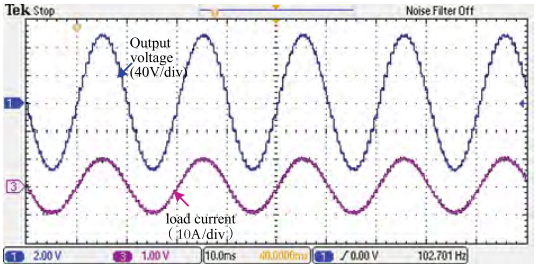

FIGURE 33. 15-level output voltage and load current.

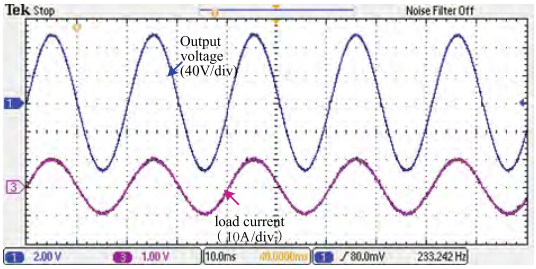

FIGURE 34. 200-level output voltage and load current.

V. EXPERIMENTAL VERIFICATION

In order to further verify the effectiveness of the proposed inverter, the corresponding experiment is carried out on the Typhoon HIL 602 device. The experimental parameters are consistent with the simulation parameters which are shown in Tab. 1. The general hardware architecture of Typhoon HIL 602 is shown in Fig. 29. The communication between Typhoon and the computer is achieved through an USB link. Typhoon HIL 602 provides 32 digital inputs and 32 analog outputs. The digital inputs are used to receive PWM signals and the analog outputs are used to transfer the inner signals for measurement. The PWM signals are generated with TMS320F28335 DSP and Xilinx XC6SLX9 FPGA board. The photograph of experimental prototype is given in Fig. 30.

The gate pulses for the switches of the proposed topology are shown in Fig. 31. The Fig. 32 to Fig. 37 show the simulation results under different conditions. Fig. 31 gives out the output voltage and load current of the nine-level SPMCSI. Related waveforms of 15-level SPMCSI and 200-level SPMCSI are shown in Fig. 33 and Fig. 34, respectively. Fig. 35 and Fig. 36 give out related waveform of 9-level and 200-level SPMCSI under load changes from 5 Ω to 10 Ω suddenly, respectively. Furthermore, the related waveform 200-level SPMCSI under R-L load conditions is shown

TABLE 3. Comparison of proposed topology with traditional spmcsi topologies.

Topology	Level	Switch	Diode	Inductor	Source
Symmetric inductors [17]	5	8	0	2	1
Simplified topology I [18]	5	8	0	1	1
Simplified topology II [19]	5	6	0	1	1
Simplified topology III [19]	5	6	0	1	1
Multiple dc current source modules with H-bridge [20-21]	7	6	3	0	3
Single dc current source and multiple inductors with H-bridge [22]	9	8	4	4	1
Common-emitter [23]	5	8	2	1	2
H-bridge with inductor cells [24]	9	12	0	2	1
Paralleled H-bridge [25]	7	12	0	0	3
Single rating inductor [25]	7	12	0	6	1
Multiple rating inductor [25]	7	12	0	4	1
Proposed inverter	Programmable	5	1	1	1

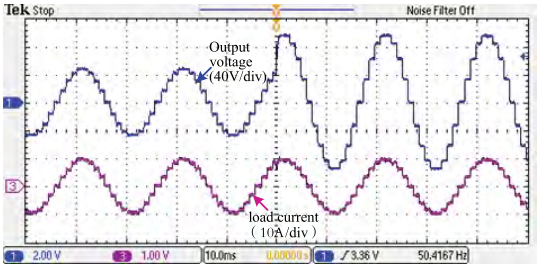

FIGURE 35. 9-level output voltage and load current under load changes suddenly conditions.

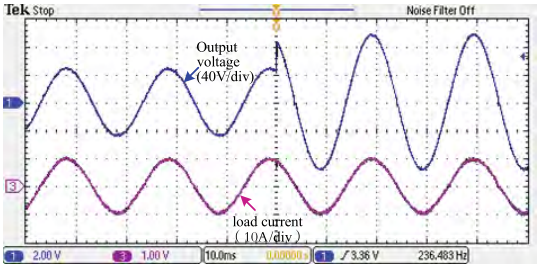

FIGURE 36. 200-level output voltage and load current under load changes.

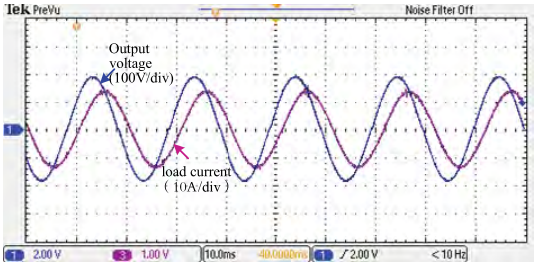

FIGURE 37. 200-level output voltage and load current under R-L load.

in Fig. 37. It can be observed that there is a good agreement between simulink results and experimental ones.

VI. CONCLUSION

The main contribution of this paper is to present a new programmable single-phase multilevel current source inverter. Different from the existing single-phase multilevel inverters, it can achieve the programmable level output with only five switches. The comparison with the existing topologies in Tab. 3 demonstrates the advantages of the proposed inverter.

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