IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 18, 2019, accepted July 14, 2019, date of publication July 29, 2019, date of current version August 19, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2931562

A Novel Switched-Capacitor Converter With High Voltage Gain

HONGYANG XIE AND RUI LI, (Member, IEEE)
Key Laboratory of Control of Power Transmission and Conversion, Ministry of Education, School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China

Corresponding author: Rui Li (liruiqd@sjtu.edu.cn)

This work was supported in part by the National Key Research and Development Project under Grant 2018YFB1500702, and in part by the National Natural Science Foundation of China under Grant 51777124.

ABSTRACT In this paper, a novel topology of switched-capacitor converter is proposed. Compared with the existing switched-capacitor topologies, such as the Dickson-based switched-capacitor converter or the ladder switched-capacitor converter, it limits both voltage stress and current stress of components under lower level, which reduces the volume of capacitor banks and the conduction loss. These characteristics can help high-power density and high-efficiency design, especially in high-voltage-gain applications. The phase shift modulation strategy corresponding to the proposed switched-capacitor converter is also presented in this paper. With phase shift modulation, voltage gain can be adjusted as continuous value. The voltage regulation ability makes up the defect of conventional switched-capacitor converters, and the ZVS operation of all the switching devices is also achieved with the proposed modulation method so that the WBG devices can play more strength in the converter with higher switching frequency. The derivation of the circuit topology and phase shift modulation will be introduced in this paper. The steady analysis and performance comparison will prove the advantage of the proposed converter. A 600-W prototype is built, and the experiment results are presented to validate the proposed converter.

INDEX TERMS High-voltage-gain converter, switched-capacitor converter, high power density, high efficiency, phase shift modulation, voltage regulation ability, zero-voltage switching (ZVS).

I. INTRODUCTION

Nowadays, high-voltage-gain DC-DC converters [1] are required in many industrial fields, such as solar photovoltaic system, data center, battery formation and so on [2], [3]. An isolated converter is typically applied in these applications to connect two different voltage rates. However, switched-capacitor converters (SCC) attract more considerable attention because of its magnet-less feature. The SCC realizes high voltage gain by changing the topologies of a series of capacitors instead of transformers that used in isolated converters. And the energy is stored in capacitors rather than magnetic materials. Without bulky magnetic components like inductor and transformer and incidental magnetic loss, SCC can easily achieve high power density and high efficiency and is within the trend of high frequency and integration.

The development of SCC experiences three major stages. First, the rudiment of SCC came from voltage multiplier, which utilizes diode and capacitor network to generate high voltage pulse like Cockcroft-Walton voltage multiplier and Marx Generator. Then, from 1970s, Ladder SCC [27]–[29]

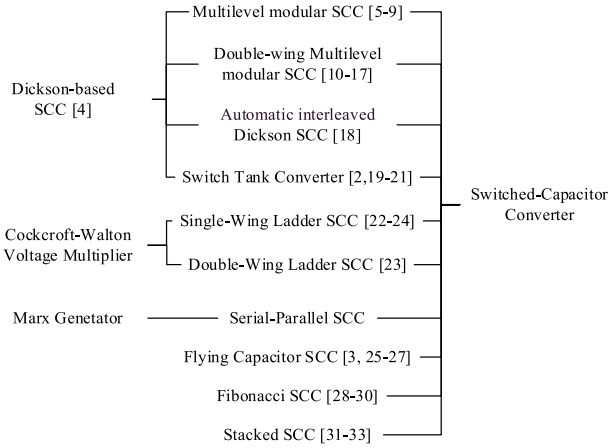


FIGURE 1. Review of switched-capacitor converter.

The associate editor coordinating the review of this manuscript and approving it for publication was Yijie Wang.

and serial-parallel SCC are invented by replacing the diodes in the voltage multiplier with MOSFET. New SCC topologies are also proposed, such as Dickson SCC [4] and Fibonacci SCC [27]. The Dickson SCC eliminates unexpected voltage drop in Ladder SCC caused by parasitic capacitance. And Fibonacci SCC can realize the highest voltage gain with the least components among all kinds of SCCs. In this period, SCC is mainly applied as integrated power source for other chip with low power. At present, SCC begins to broaden its application, as various kinds of SCC topologies are continuously proposed, like multilevel modular SCC [5]–[9], double-wing multilevel modular SCC [6], [10]–[16], flying capacitor SCC [3], [24]–[26] and stacked SCC [30]–[32]. These novel SCCs are more suitable for high power application from hundreds of watts to kilos of watts in industrial fields.

To play a more important role as a high-voltage-gain converter, SCC is supposed to achieve higher efficiency and higher power density, which almost depends on the loss of switching device and the volume of capacitor banks. Therefore, the voltage stress and current stress of switching device and the voltage stress of capacitor should be the optimization objects [33], [34]. Current stress directly determines the conduction loss and with lower voltage stress, device with lower conduction resistance can be utilized. As for capacitor, voltage stress restricts its minimum volume. Different topologies will cause different voltage and current stress distribution on components. For example, although the Fibonacci SCC can easily realize high voltage gain, the voltage and current stress on switching device and capacitor both increase rapidly with the voltage gain, so Fibonacci SCC can take its advantages in low power application but not in high power stages.

The Dickson-based SCC becomes more popular in these years. Many new converters like multilevel modular SCC, double-wing multilevel modular SCC and switching tank SCC [2], [18]–[20] are all based on the topology proposed by Dickson in 1970s. In Dickson SCC, the voltage stress of switching device never exceeds twice of low side voltage no matter how high the voltage gain is. And the current stress is evenly shared by all switching devices, so the conduction loss is also acceptable. The defect of Dickson SCC is that the voltage stress of capacitor rises linearly with the high side voltage, which means larger capacitor banks should be used in high voltage applications.

Another kind of SCC like Ladder SCC is based on the topology proposed by Cockcroft-Walton. This kind of SCC limits the capacitor voltage stress at low side voltage, so it can achieve higher power density. However, the current stress is not even and will increase linearly with voltage gain, which reduces the efficiency of the converter.

There are also some improvements of basic SCC. For example, the double-wing multilevel modular SCC cuts the increasing voltage stress of capacitor by half, but the non-command-ground characteristic restricts its range of use. It is suggested that there is an inner contradiction among the voltage stress and current stress of switching device and capacitor in existing SCCs. Therefore, it is meaningful to combine the advantages of Dickson-based SCC and Ladder SCC to achieve both high efficiency and high power density, especially in high-voltage-gain application.

Besides, there are some inherent disadvantages of SCC. First, the voltage gain of SCC is fixed by its circuit structure like a transformer, which makes it not suitable for wide-voltage-range applications and have poor voltage regulation ability. Second, the absence of inductor means that the transient current is out of control. At start-up process the charging current will be sharp and large. And if the capacitor voltage is not balanced when devices switch, current spike will also appear. Third, the devices operate in hard-switching, which causes EMI noise and switching loss. It's important to achieve soft-switching so that the switching frequency can be increased.

The key to avoid these shortcomings is inserting some inductors in basic SCC. The additional inductors have low inductance at the level of nanohenry, so these inductors can be applied as stray inductor or air-core inductor which still keeps magnet-less characteristic of SCC. This kind of SCCs that utilizing few inductors are also called hybrid SCC. With the help of inductors, the current spike can be choked. And with the ability of controlling current, several modulation strategies are proposed to improve the performance of SCC.

Resonant SCC such as resonant multilevel modular SCC [5], [6], [8] applies inserting inductors and original capacitors to make up resonant loops. The switching frequency is equal to the resonant frequency. Therefore, in each switching state, the current drops to zero at the end of the state. The resonant SCC realizes ZCS operation and can reduce the inductance and capacitance by increasing switching frequency. However, the resonant SCC still has fixed voltage gain. Besides, if wide-band-gap devices like SiC and GaN are applied in the converter, the switching-off loss will automatically vanish because of the WBG device's zero-tail-current characteristic. Therefore, it is more helpful to achieve zero-voltage-on.

Phase shift modulation strategy is first applied to SCC by Hideaki Fujita in flying capacitor SCC [39]. Then this strategy is developed to be used in multilevel modular SCC and double-wing multilevel modular SCC [9], [13], [40], [41]. By shifting one group gate signal with a certain phase from another, two new switching states are added to the basic SCC switching sequence to achieve ZVS operation. Besides, the energy delivery through the converter in one switching period can be controlled by the shift phase so that the output voltage can be also controlled by the phase to realize adjustable voltage gain and voltage regulation ability. However, the existing phase shift method is not applicable for all kinds of SCCs, such as ladder SCC. And the input current of power supply has a rapid change when circuit state switching, which requires a larger input capacitor bank.

This paper proposes a novel topology of switching-capacitor converter. The new topology combines the advantage of Dickson-based SCC and ladder SCC. The voltage stress and current stress can both be limited under certain

level, so the proposed converter can indeed achieve high efficiency and high power density in high-voltage-gain applications. Then the corresponding phase shift modulation strategy is also proposed to realize ZVS operation and voltage regulation ability. The second section will first introduce the circuit configuration and basic operation principle. Then the phase shift strategy and how ZVS operation can be realized will be exhibited in section III. The quantitative analysis of the converter will be presented in the section IV and will compare with other SCCs. At last section, experiment result will be given out to validate the proposed topology and modulation method.

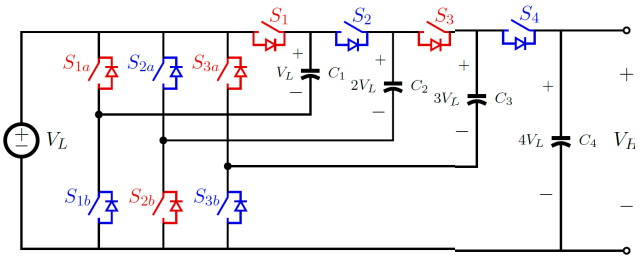


FIGURE 2. Dickson-based SCC.

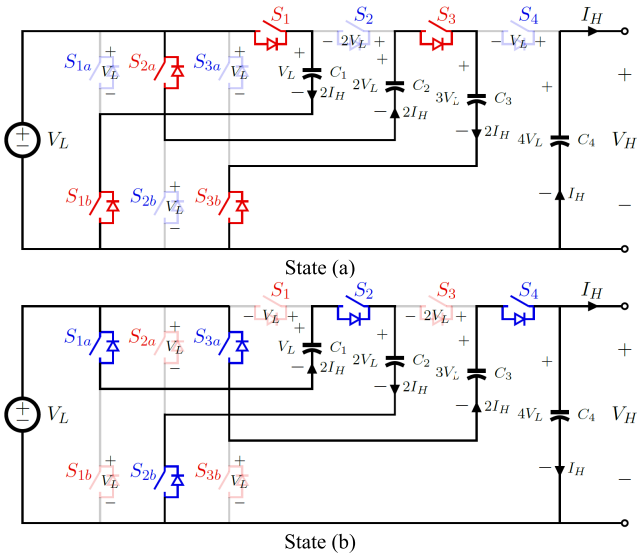


FIGURE 3. Two switching states of Dickson-based SCC.

II. CIRCUIT DERIVATION AND BASIC CONFIGURATION

Figure 2 shows the conventional multilevel modular SCC with indication of voltage stress distribution. And two switching states of multilevel modular SCC is shown in Figure 3. In state a, C_1 is charged by low side voltage source, and C_3 is charged by V_L and C_2 in series. Then in state b, C_2 is charged by V_L and C_1 in series. And C_3 connects with V_L in series to charge the output capacitor C_4 in high voltage side. The low side voltage will be series-connected with capacitor C_{k-1} to charge the capacitor C_k. Therefore, the voltage of capacitors boosts with V_L in each step. Capacitors charge and discharge in turn with adjacent capacitors to keep charge balance and deliver power from input to output. The mechanism of SCC determines the voltage stress of capacitor will increase linearly with voltage gain as (1).

$$V_{C_k} = kV_L \tag{1}$$

As for switching devices, they can be divided into two groups. The switching devices in low voltage side make up a series of half bridges, so their voltage stress is just equal to low side voltage V_L. And the switching devices connected to the positive ends of capacitor together are clamped by capacitors. Except the switching devices directly connect to input and output, voltage stress of other devices in this group is $2V_L$. The current stress is same of all the switching devices. To maintain the charge balance of each capacitor, the average current through each charge or discharge loop should be twice the average output current I_{out} in one switching state. Uniform distribution of current stress and low voltage stress of switching devices contribute to less conduction loss and high efficiency, which is the advantage of Dickson-based SCC, but growing voltage stress of capacitor requires more capacitor volume, especially in high-voltage-gain applications.

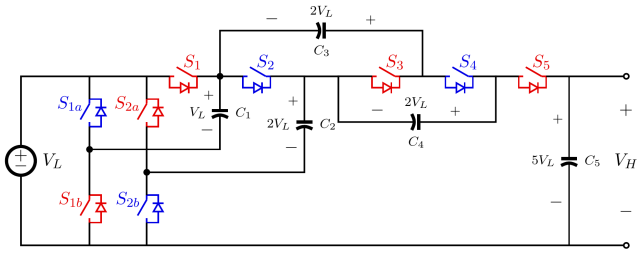


FIGURE 4. Ladder SCC.

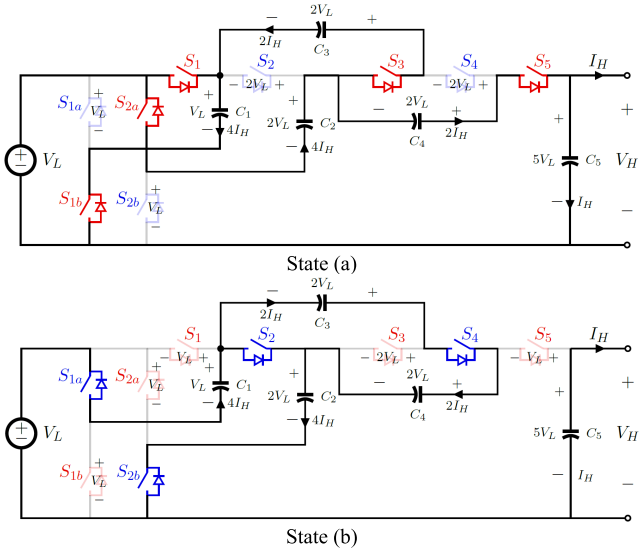


FIGURE 5. Two switching states of ladder SCC.

Figure 4 shows the basic ladder SCC, and corresponding switching states are shown in Figure 5. The charge and discharge modes of ladder SCC in two states is the same as

the Dickson-based SCC. However, the high side voltage is produced by connecting the capacitors with same parity in series (V_L, C_1, C_3, C_{2i-1} and C_2, C_4, C_{2i}). The two groups of capacitors in series are just like the two handrails of a ladder, and the switching devices made up of the "stairs". Therefore, the voltage stress of capacitor in ladder SCC is $2V_L$ (voltage of C_1 is V_L) no matter how much the voltage gain is, which helps high power density design. However, because each group of capacitors is connected in series to the low side voltage source through the switching devices in low voltage side, all the charge or discharge current will flow through the low voltage side switching devices at the same time, which can cause a large current stress as described by (2). G is the voltage gain.

$$I_{sw} = GI_{out} \tag{2}$$

For a high voltage gain, the current stress can be reasonably large. As conduction loss is proportion to the current, the efficiency performance of ladder SCC is poorer than Dickson-based SCC. And another weakness of ladder SCC is that the phase shift modulation method cannot be applied to ladder SCC, so that the ZVS operation and voltage regulation cannot be realized, which is important in some applications.

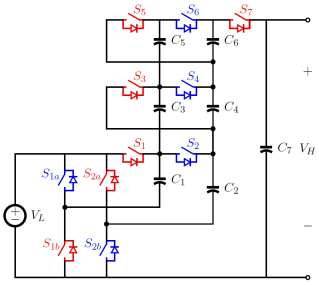


FIGURE 6. Redrawn ladder SCC.

To combine the advantages of these two SCC topologies, a novel topology is proposed. Figure 6 redraws the ladder SCC to present the "ladder" structure more clearly and reveal the common points with Dickson-based SCC. Each two capacitors and the switching devices connected with them consist of one stage of the converter. The output of each stage is connected to the next stage as input. And it is evident that the structure of the low side components and the first stage is similar to Dickson-based SCC. By adding a switching device and output capacitor for each stage as shown in Figure 7, the first stage of ladder SCC is reformed to a Dickson-based SCC, and the stages above can be regard as the extension of the Dickson-based SCC. Figure 7 is an example of the proposed SCC topology. By expanding the switching devices and capacitors in one stage and the number of stages, a general proposed SCC is shown as Figure 8. With N, the number of capacitors in each stage, and M, the number of stages, the nominal voltage gain of the proposed SCC can be calculated by (3).

$$G = (N-1)M + 1 \tag{3}$$

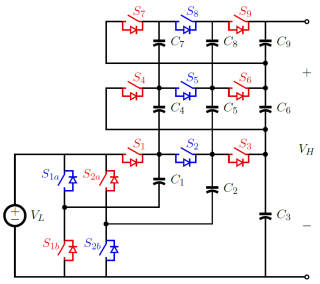


FIGURE 7. Proposed SCC.

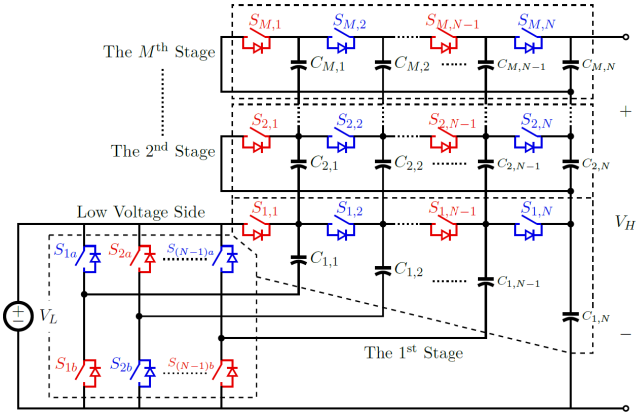


FIGURE 8. M-Stage proposed SCC with $N \times M$ capacitors.

The basic operation with two switching states is shown in Figure 9. The two switching states are just like Dickson-based SCC. The difference is that in state a, the output capacitor of the first stage $C_{1,3}$ will charge the first capacitor $C_{2,1}$ in the second stage in series with V_L, so that the voltage among $C_{2,1}$ is $2V_L$. Then in state b, $C_{2,1}$ charges $C_{2,2}$ to $2V_L$ through two switching devices. By this way, each capacitor in the second stage will be charge to $2V_L$, which is just the difference of the output of the first stage and low side voltage $V_{C_3} - V_L$. Then the output voltages of the first and the second stages connect in series to obtain $5V_L$, which realizes a higher voltage gain. And the maximum voltage stress of capacitor in the circuit is just $3V_L$, which is nearly half of the voltage stress in Dickson-based SCC with the same voltage gain. For more stages, the output voltage of the second stage will be sequentially transmitted to the stages above. The voltage among the first capacitor in the next stage will also be charge to $V_{C_3} - V_L$. Therefore, the voltage stress of each capacitor in the proposed SCC can be described by (4).

$$V_{C_k} = \begin{cases} kV_L & 0 < k \leq N, \text{ in } 1^{st} \text{ layer} \\ (N-1)\,V_L & N < k, \text{ in } m^{th} \text{ layer} \end{cases} \tag{4}$$

And the maximum voltage stress is always born by the output capacitor of the first stage, which can be calculated by voltage gain G and the number of stages M as (5). With larger M, the voltage stress on capacitor can be

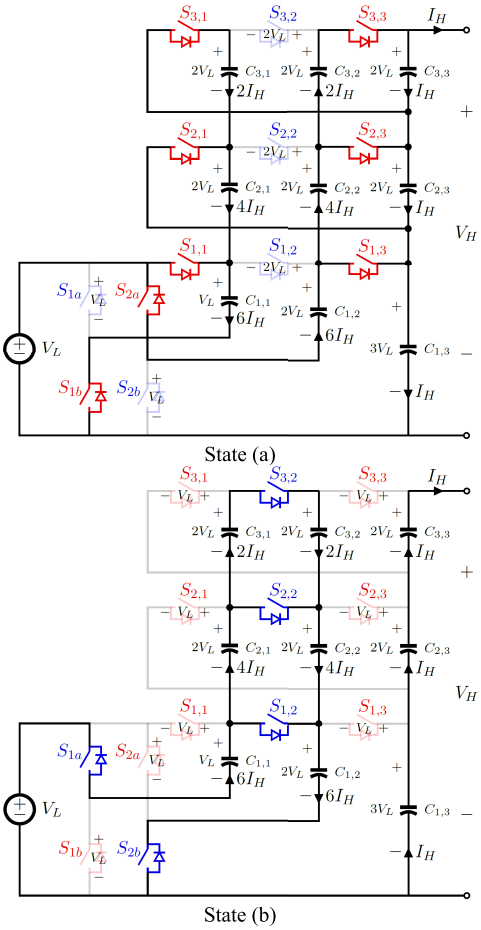


FIGURE 9. Two switching states of proposed SCC.

further reduced.

$$V_{C.max} = NV_L = \left(\frac{G-1}{M} + 1\right) V_L \tag{5}$$

As for switching devices, the voltage stress in proposed SCC is the same as the Dickson-based SCC and ladder SCC, which is just V_L and $2V_L$.

$$V_{sw.max} = 2V_L \tag{6}$$

And the current stress can also be calculated by the charge balance of capacitors. Figure 9 presents the current distribution in two switching states. It can be seen that the switching devices at low voltage side bear the maximum current stress, which involves with the number of stages and can be calculated by (7).

$$I_{sw.max} = 2MI_{out} = \frac{G-1}{(N-1)/2} I_{out} \tag{7}$$

For N larger than 3, the current stress in proposed SCC is less than ladder SCC. For a certain voltage gain, both low voltage stress and current stress can be achieved with elaborately selected N and M, which makes it possible to optimize the efficiency and power density for different design goals.

III. PHASE SHIFT MODULATION AND ZVS OPERATION

A. PHASE SHIFT MODULATION

Figure 10 shows the switching states of phase shift modulation applied on a two-stage 5X proposed SCC as an instance. Several inductors are inserted into the circuit to control the slope of current as the requirement of phase shift modulation. The inductances are small enough to be applied as stray inductance or air-core inductor, which will be proved in the following section, so the magnet-less characteristic of SCC can still be maintained. And the corresponding waveforms are presented in Figure 11. The switching devices are divided into three groups as low voltage side, the first stage and the second stage. Accordingly, the signals of their gate drive are shifted by a certain phase from each other. The time interval between the signals of the low voltage and the first stage is T_1, and the interval between the first stage and the second stage is T_2. Phase shift ratio is defined as (8), where T_s is the switching period.

$$D_1 = 2T_1/T_s \quad D_2 = 2T_2/T_s \tag{8}$$

From t_0 to t_1, the equivalent circuit is similar to the basic state (a) in Figure 9. The voltage in each loop is close to balance and the values of current through inductors change slowly. Then from t_1 to t_2, the states of switching devices in the low voltage side toggle first, which breaks the voltage balance in the first stage. The absence of V_L in the loops of the first stage causes considerable voltage difference on the inductors in the first stage. As a result, the currents in the first stage change fast and even change their direction. However, the operation of switching devices at low voltage side does not affect the equivalent circuit loop in the second stage.

From t_2 to t_3, the states of switching devices in the first stage toggle. As the current direction of the first stage has already changed before t_2, which is now the same as the direction in basic state (b) in Figure 9. The voltage balance sets up again and the change rate of current in first stage slows down. But now the equivalent circuits of the second stage change because of the switching actions in the first stage. The currents in the second stage begin to change fast and turn its direction over in the same way as the first stage. At t_3, the second stage also turn into the basic state b like the first stage.

In another half switching period, the operation is similar. At t_4, the states of switching devices in the low voltage side toggle again and the current values in the first stage enter into fast-change state again. From t_5 to t_6, the equivalent circuits of the first stage turn back to basic state (a) and the current values in the second stage begin to change fast. Finally, at t_6, the second stage turns back to basic state (a) to finish a switching period.

The phase shift operation creates two different switching states for each stage. From t_1 to t_2, t_4 to t_5 for the first stage and from t_2 to t_3, t_5 to t_6 for the second stage, the slope of current becomes significant and change its direction. The change of current directions in these states joins the two basic

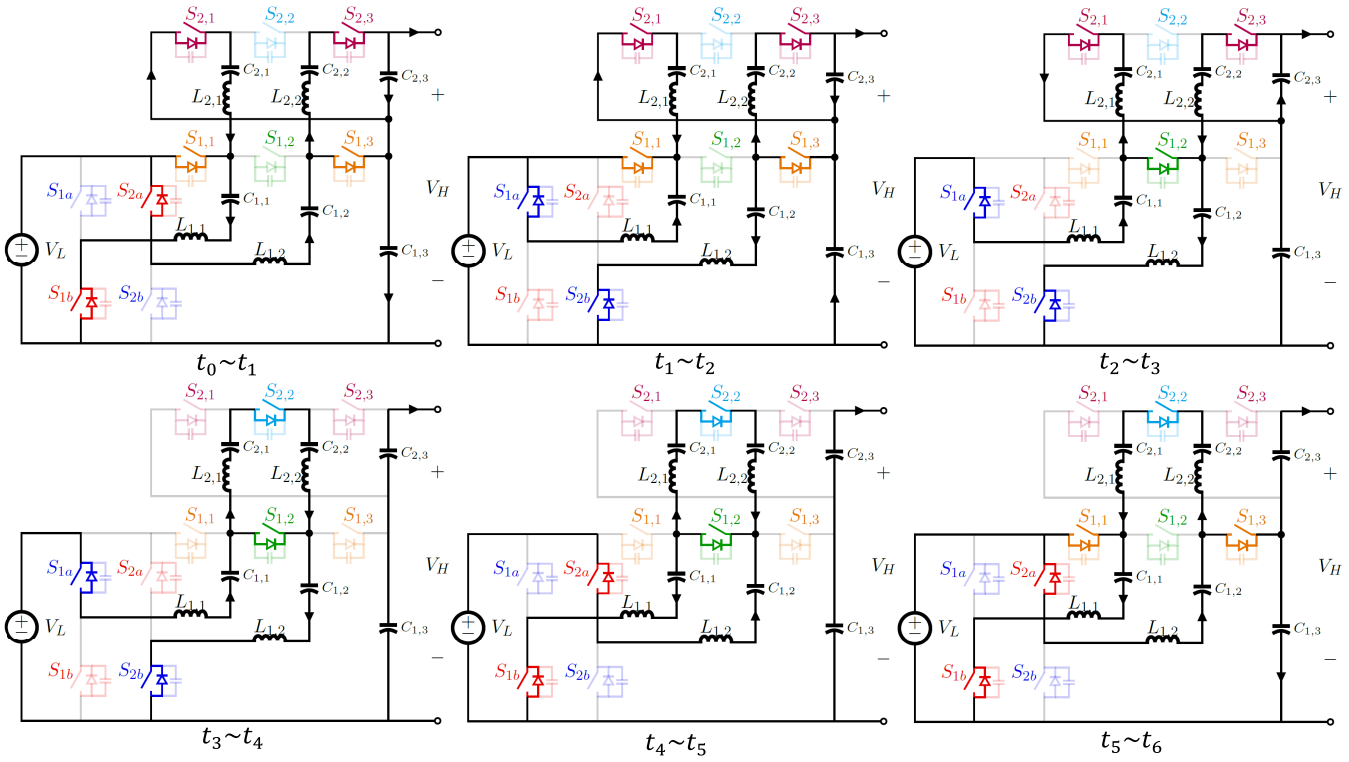


FIGURE 10. Phase shift modulation operation.

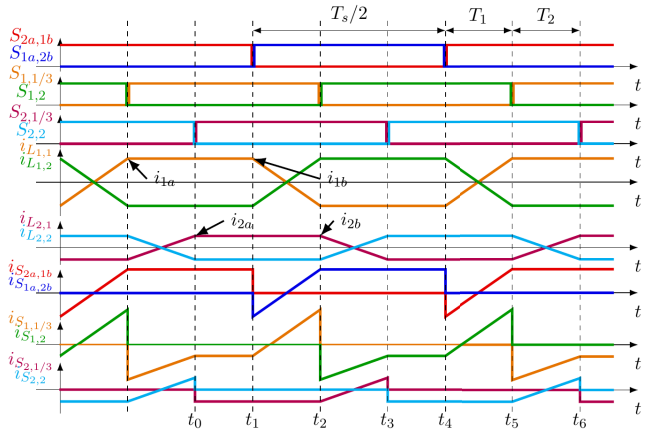


FIGURE 11. Waveforms of phase shift modulation.

states in Figure 9 together and make the transient process more gently. This operation is also the key to achieving ZVS. As shown in Figure 11, when the output voltage is the nominal value calculated by (4), the current waveforms in these states are almost symmetrical about zero, which means there is little charge or energy transferred during these states. Therefore, these time phases are defined as current commutation states for the corresponding circuit stages. The shift time interval T_1 and T_2 labeled in Figure 11 are just the duration time of current commutation states.

From t_6 to t_1 and from t_2 to t_4, current values in the first stage change slowly so that charge and energy are transmitted among capacitors in one circuit stage. These time phases are defined as the power delivery states of the first stage. And from t_0 to t_2, t_3 to t_5 are the power delivery states of the second stage. By adjust D_1 and D_2, the power delivered by the proposed SCC can be controlled. To simplify the modulation strategy, the inductances in the same stage adopt the same value as L_1, L_2 to L_N. And the capacitances are supposed to be large enough to ignore the voltage ripple on capacitors. By listing the volt-second balance equations of inductors and charge balance equations of each output capacitors, the output power can be calculated by (9), where V_N is the voltage of capacitor C_N.

$$P_o = \frac{V_H V_L D_1 (1-D_1)}{8 f_s L_1} \frac{V_{1,N} - V_L}{V_H - V_L} = \frac{V_H V_L D_2 (1-D_2)}{8 f_s L_2} \frac{V_{1,N} - V_L}{N V_L - V_L} \tag{9}$$

According to (8), output voltage can also be adjusted by D_1 and D_2. Therefore, the proposed SCC can realize voltage regulation ability with close-loop control of phase shift ratio, and the voltage gain can also be continuous regulated, which overcomes the inherent shortcomings of SCC.

There are five variables in (9), D_1, D_2, V_H, $V_{1,N}$, P_o and only three of them are free. Define $G = V_H / V_L$ as the voltage gain, $m_1 = V_{1,N} / N V_L$ as the conversion ratio of the first stage. There are also some constraint conditions of these

variables as described in (10).

$$D_1, D_2 \leq 0.5; G > 1; m_1 > \frac{1}{N} \tag{10}$$

In Figure 12, m_1 is set to be 1. The curved surface exhibits the relation between D_1, G and P_o under the constraint conditions. D_2 can be determined by (9) and is not presented in Figure 12. It suggests that the maximum output power is always achieved when $D_1 = 0.5$. And for each value of D_1, the output power first increases linearly with voltage gain and reaches a maximum point. Then P_o begins to drop as G further increases.

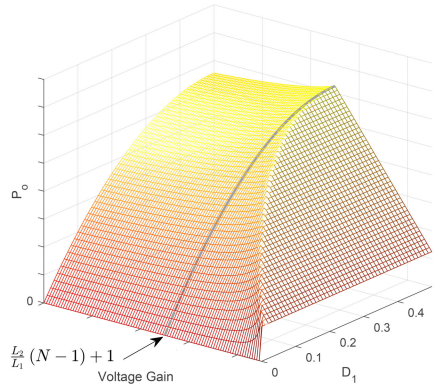


FIGURE 12. The relationship between D_1, G and P_o.

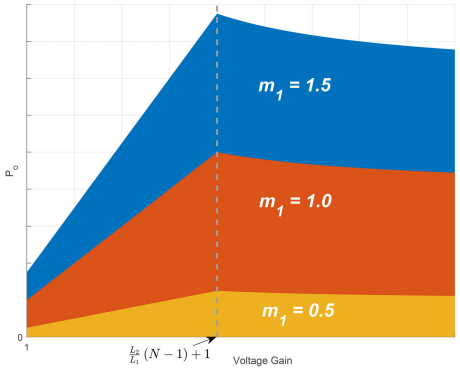


FIGURE 13. The relationship between m_1, G and P_o.

When m_1 is also adjusted, the boundary of output power will change together. Figure 13 presents the output power range with different m_1. The color areas are the projections of Figure 12 to $P_o - G$ plane. It can be seen that the higher m_1 is, the more power can be delivered through converter. And the maximum output power always reaches when $G = L_2\,(N-1)/L_2 + 1$.

For a proposed SCC with M stages, the phase shift modulation can also be applied by shifting the signal of the k^{th} stage from the $(k-1)^{th}$ stage with T_k. There will be $2M + 2$ switching states in one switching period. And the relationship between output power and the shift ratio of the k^{th} stage can be calculated as (11).

$$P_o = \begin{cases} \dfrac{V_H D_1\,(1-D_1)}{8 f_s L_1} \times \dfrac{V_L\left(V_{1,N}-V_L\right)\prod_{i=1}^{M} V_{i-1,N}}{\left(V_{1,N}-V_L+V_{2,N}\right)\prod_{i=1}^{M-1}\left(V_{i,N}+V_{i+1,N}\right)} & k=1 \\ \dfrac{V_H D_2\,(1-D_2)}{8 f_s L_2} \dfrac{\left(V_{1,N}-V_L\right)\prod_{i=2}^{M} V_{i-1,N}}{(N-1)\prod_{i=2}^{M-1}\left(V_{i,N}+V_{i+1,N}\right)} & k=2 \\ \dfrac{V_H D_k\,(1-D_k)}{8 f_s L_k} \dfrac{\prod_{i=k}^{M} V_{i-1,N}}{(N-1)\prod_{i=k}^{M-1}\left(V_{i,N}+V_{i+1,N}\right)} & k>2 \end{cases} \tag{11}$$

B. ZVS OPERATION AND CONSTRAINTS

Phase shift modulation also realizes ZVS operation of the proposed SCC. Figure 14 presents the waveforms of the ZVS commutation process of half switching period from t_1 to t_3. Each time point is spread out to three time t_{x-1}, t_{x-2}, t_{x-3} to display what happens in deadtime.

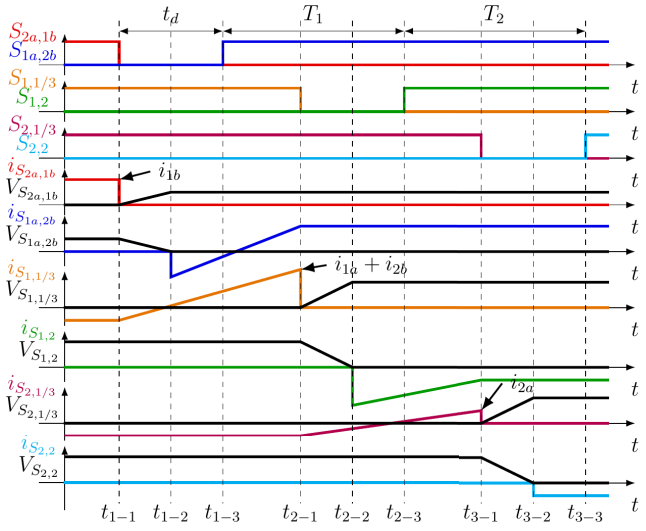


FIGURE 14. Waveforms of ZVS commutation states.

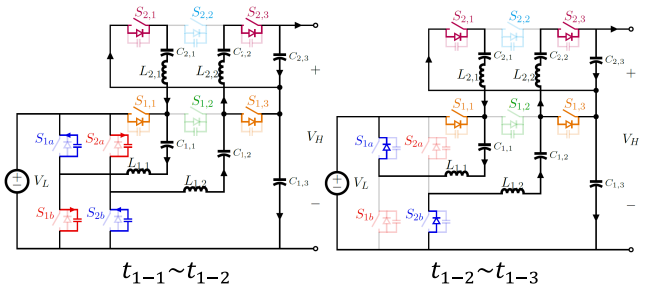


FIGURE 15. ZVS operation of low voltage side devices.

Figure 15 shows the deadtime of switching devices of low voltage side. The switching devices S_{1b} and S_{2a} shut down at t_{1-1}. The current stored in the inductor $L_{1,1}$ and $L_{1,2}$ begins

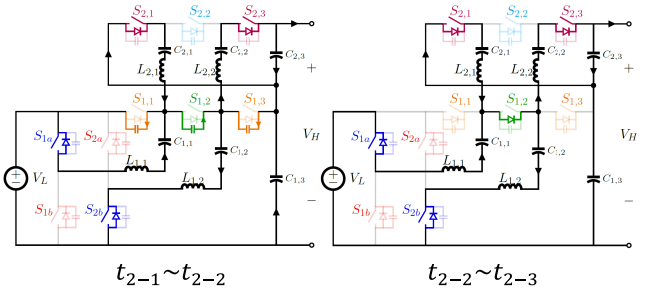


FIGURE 16. ZVS operation of the first stage devices.

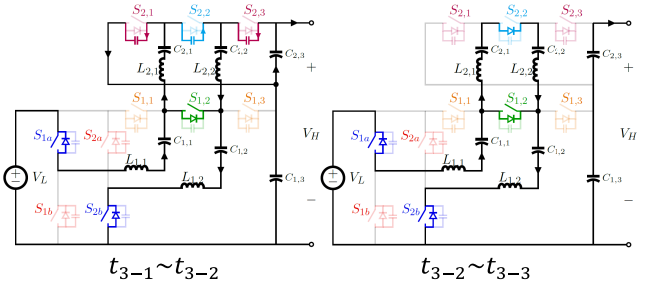


FIGURE 17. ZVS operation of the second stage devices.

to charge and discharge the C_{oss} of the switching devices at low voltage side. At t_{1-2}, the charge or discharge process of C_{oss} completes and the currents make the anti-parallel diodes of S_{1a} and S_{2b} conducted, which clamps the voltage of S_{1a} and S_{2b} to zero. Therefore, when gate drive signals of S_{1a} and S_{2b} rise at t_{1-3}, ZVS of S_{1a} and S_{2b} is realized.

Figure 16 shows the ZVS operation of the switching devices in the first stage. $S_{1,1}$ and $S_{1,3}$ turn off at t_{2-1}. The current of inductors in the first stage charges or discharges C_{oss} of the switching devices $S_{1,1}$, $S_{1,2}$ and $S_{1,3}$. The C_{oss} of $S_{1,1}$ and $S_{1,3}$ are charged to V_L at t_{2-2} and anti-parallel diode of $S_{1,2}$ clamps the voltage of $S_{1,2}$ to zero until it realizes ZVS at t_{2-3} when $S_{1,2}$ turns on.

The ZVS operation of switching devices in the second stage achieves in the same way like the first stage from t_{3-1} to t_{3-3}. At t_{3-1}, $S_{2,1}$ and $S_{2,3}$ turn off and C_{oss} of switching devices in the second stage begins to be charged or discharged by the inductors in L_2 and $L_2^{'}$. Then the anti-parallel diode of $S_{2,2}$ clamps the voltage of $S_{2,2}$ to zero at t_{3-2} and ZVS is realized at t_{3-3}.

With the same mechanism, the ZVS operation of another half switching period can also be realized. As the tail current and diode reverse recovery loss of WBG device are negligible, zero-voltage-turn-on can minimize the switching loss in a WBG-based converter, which is helpful to raise switching frequency, solve EMI problem and increase efficiency.

In order to fully charge or discharge the C_{oss}, the direction of inductor current is supposed to turn over in corresponding current commutation states, and there should be enough energy stored in inductors. Therefore, the current value at the edge of current commutation state and power delivery state decides whether the ZVS operation can be completed. The scope of current in the k^{th} stage can be described by (11) and (12), where $k_{k,a}$ is the current scope of power delivery state and $k_{k,b}$ is the scope of current commutation state.

$$k_{k,a} = \begin{cases} \dfrac{V_N - NV_L}{2(N-1)L_1} & k = 1 \\ \dfrac{V_{2N} - (V_N - V_L)}{2(N-1)L_2} & k = 2 \\ \dfrac{V_{kN} - V_{(k-1)N}}{2(N-1)L_k} & k > 2 \end{cases} \tag{12}$$

$$k_{k,b} = \begin{cases} \dfrac{V_L}{L_1} + k_{1,a} & k = 1 \\ \dfrac{V_N - V_L}{(N-1)L_2} + k_{2,a} & k = 2 \\ \dfrac{V_{(k-1)N}}{(N-1)L_k} + k_{k,a} & k > 2 \end{cases} \tag{13}$$

Then the current expressions of each time state can be listed as following.

The first power delivery state of k^{th} circuit stage:

$$i_{L_k} = \frac{k_{k,a}(1-D_k) + k_{k,b}D_k}{4f_s} - k_{k,a}t \quad 0 \le t < \frac{1-D_k}{2f_s} \tag{14}$$

The first current commutation state of k^{th} circuit stage:

$$i_{L_k} = \frac{-k_{k,a}(1-D_k) + k_{k,b}D_k}{4f_s} - k_{k,b}\left(t - \frac{1-D_k}{2f_s}\right)\frac{1-D_k}{2f_s} \le t < \frac{1}{2f_s} \tag{15}$$

Another power delivery state of k^{th} circuit stage:

$$i_{L_k} = \frac{-k_{k,a}(1-D_k) - k_{k,b}D_k}{4f_s} + k_{k,a}\left(t - \frac{1}{2f_s}\right)\frac{1}{2f_s} \le t < \frac{2-D_k}{2f_s} \tag{16}$$

Another current commutation state of k^{th} circuit stage:

$$i_{L_k} = \frac{k_{k,a}(1-D_k) - k_{k,b}D_k}{4f_s} + k_{k,a}\left(t - \frac{2-D_k}{2f_s}\right)\frac{2-D_k}{2f_s} \le t < \frac{1}{f_s} \tag{17}$$

The current values of states edge which are tagged in Figure 14 as $i_{k,a}$ and $i_{k,b}$ can be calculated by current scopes and phase shift ratios.

$$\begin{aligned} i_{k,a} &= \frac{k_{k,a}(1-D_k) + k_{k,b}D_k}{4f_s} \\ i_{k,b} &= \frac{-k_{k,a}(1-D_k) + k_{k,b}D_k}{4f_s} \end{aligned} \tag{18}$$

As shown in Figure 14, the criteria of ZVS operation can be described by (19).

$$\begin{cases} i_{1,b} > \sqrt{C_{oss}/L_1 V_L} & \text{low voltage side} \\ i_{k,a} + i_{k+1,b} > \sqrt{2C_{oss}/L_k V_L} & k^{th}\text{stage} \\ i_{M,a} > \sqrt{2C_{oss}/L_M V_L} & M^{th}\text{stage} \end{cases} \tag{19}$$

IV. STEADY STATE ANANLYSIS AND COMPARISON

A. SWITCHING DEVICE STRESS

As the V_{DS} of switching device is clamped by nearby capacitors, the voltage stress of switching device will also change when phase shift modulation modifies capacitor voltage. Voltage stress of switching devices in one circuit stage is related to the output capacitor voltage of that stage as described in (11). The voltage stress of device is still around $2V_L$, which ensures the low withstand voltage and low R_{ds} devices to be used for a better conduction loss.

$$V_{S_{k,a/b}} = V_L \quad low\ voltage\ side$$

$$V_{S_{k,j}} = \begin{cases} \dfrac{V_{1,N} - V_L}{N-1} & k = 1, j = 1\ or\ N \\ \dfrac{2\left(V_{1,N} - V_L\right)}{N-1} & k = 1, 1 < j < N \\ \dfrac{V_{k,N}}{N-1} & 1 < k, j = 1\ or\ N \\ \dfrac{2V_{k,N}}{N-1} & 1 < k, 1 < j < N \end{cases} \tag{20}$$

The current stress of switching device can be obtained by expressions of inductor current as (14) ∼ (17). For the switching devices at low voltage side, the current is just the corresponding inductor current in the first circuit stage.

$$\begin{cases} i_{S_{k,a}} = -i_{L_{1,k}} \\ i_{S_{k,b}} = i_{L_{1,k}} \end{cases} \tag{21}$$

For the switching devices from the first circuit stage to the $(M-1)^{th}$ circuit stage, the current stress is the current difference of the two adjacent inductors.

$$i_{S_{k,j}} = \begin{cases} i_{L_{k+1,j}} - i_{L_{k,j}} & 1 \le j < N \\ i_{L_{k,N-1}} - i_{L_{k+1,N-1}} & j = N \end{cases} \tag{22}$$

And for the switching devices in the M^{th} stage, the current stress is just the current of corresponding inductor.

$$i_{S_{M,j}} = \begin{cases} -i_{L_{M,j}} & 1 \le j < N \\ i_{L_{M,N-1}} & j = N \end{cases} \tag{23}$$

Consider for a converter based on WBG devices, the power loss on the device can be breakdown to the conduction loss, gate drive loss and the loss on the C_{oss}. The switch-off loss can be ignored because of the negligible tail current. The gate drive loss can be calculated by the datasheet and the designed switching frequency as (24).

$$P_{gate\_drive} = nV_{GS}Q_G f_s \tag{24}$$

where n is the number of the switching devices. And the loss on the C_{oss} is caused by the hard switch-on, which is related to the voltage stress of the switching device.

$$P_{coss} = C_{oss} f_s \Sigma V_{DS}^2 \tag{25}$$

As ZVS operation has been realized by phase shift method, this part of loss is eliminated from the proposed converter, which helps to increase efficiency and switching frequency.

With the expressions of switching device current as (21) ∼ (23) the current stress of switching devices in k^{th} stage can be described by the inductor current.

And conduction loss can be expressed as the integration of square of the current.

$$P_{con} = R_{ds} \Sigma i_{S_{k,j}}^2 \tag{26}$$

A 600W, 12V low voltage and 60V high voltage converter is taken as a design example. EPC2023 eGaN FET is applied as power devices for a lower conduction resistance in this voltage rating. Table 1 lists main parameters of EPC2023.

TABLE 1. Main parameters of switching devices.

Model#	V_{DS}(V)	V_{GS}(V)	Q_G(nC)	R_{DS}(mΩ)	C_{OSS}(pF)
EPC2023	30	5	19	1.45	1850

B. CAPACITOR STRESS AND REQUIREMENT

As the voltage of output capacitors of each stage can be adjusted with the phase shift ratio as (11), each capacitor in the circuit will change with the adjustment as (27).

$$V_{C_{k,j}} = \begin{cases} \dfrac{(2j-1)V_{1,N} - (2j-N)V_L}{2(N-1)} & k = 1 \\ \dfrac{(2j-1)V_{2,N} + [2(N-j)-1]\left(V_{k,N} - V_L\right)}{2(N-1)} & k = 2 \\ \dfrac{(2j-1)V_{k,N} + [2(N-j)-1]V_{(k-1),N}}{2(N-1)} & k > 2 \end{cases} \tag{27}$$

The ripple voltage on the capacitors is in proportion to the largest variation of the charge in one switching period, which is decided by current stress of capacitor. Except output capacitors of each circuit stage, other capacitors all connect in series with corresponding inductors, so that their charge current is just the current of inductors. As for output capacitors, their charge current can be obtained by KCL theorem.

$$i_{C_{k,j}} = \begin{cases} i_{L_{k,j}} & 1 \le j < N \\ -i_{S_{k,N}} + i_{S_{k+1,1}} + i_{C_{k+1,N}} & j = N, 1 \le k < M \\ -i_{S_{M,N}} - I_H & j = N, K = M \end{cases} \tag{28}$$

The charge current can be described as (28). And Figure 18 shows the charge current waveforms of capacitors in the 5X proposed SCC. Then, for a certain ripple voltage level ΔV_{pp}, the capacitance required can be expressed as (29), where t_{z1} and t_{z2} are two zero-crossing points of the charge current waveforms.

$$C_{k,j} = \frac{1}{\Delta V_{pp}} \int_{t_{z1}}^{t_{z2}} i_{C_{k,j}} \mathrm{d}t \tag{29}$$

The minimum voltage of capacitor bank is limited by the energy stored as $E_C = 1/2CV_C^2$. Therefore, the sum of CV_C^2 for all capacitors in circuit can be a quota to evaluate the

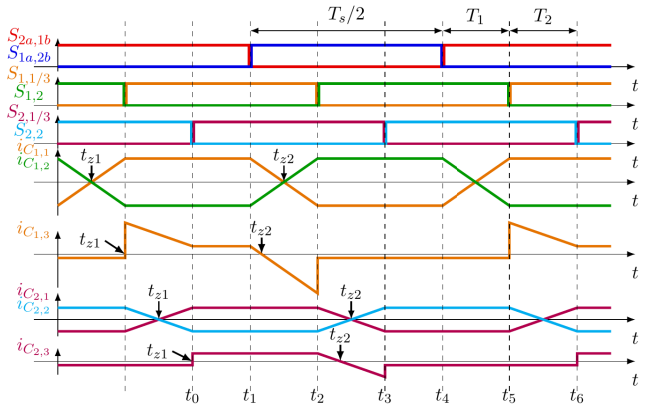


FIGURE 18. Waveforms of capacitors' charge current.

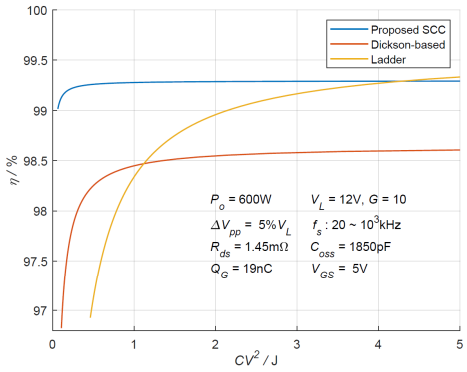


FIGURE 19. Comparison of different SCCs with fixed G.

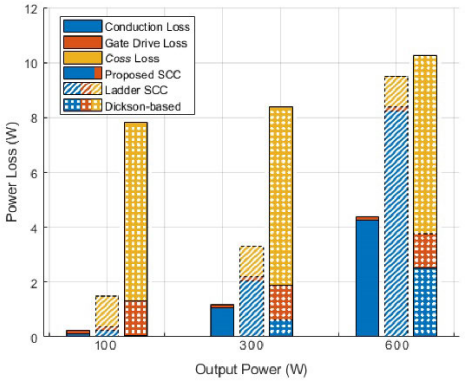


FIGURE 20. Power loss breakdown and comparison.

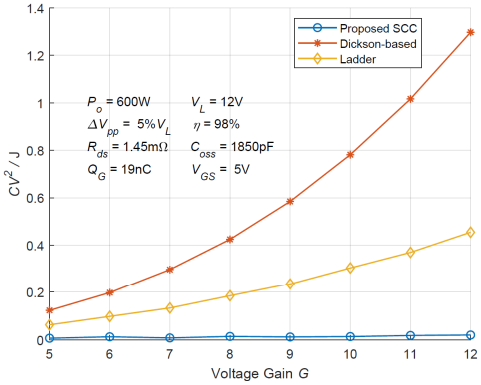


FIGURE 21. Comparison of different SCCs with fixed η.

power density of SCCs as capacitor banks take over most of the volume.

C. COMPARISON WITH OTHER SCCS

To compare the proposed SCC with other conventional SCC, a unified index which combines efficiency and power density performance together should be set up. Figure 19 and Figure 20 show the comparison among proposed SCC, Dickson-based SCC and Ladder SCC. The output power of converter is set as 600W, the low voltage is 12V, and the ripple voltage of capacitor is supposed to be less than 5% of V_L. EPC2023 is still applied as the power device. As presented in Figure 19, the voltage gain of the SCCs is fixed as 10. By trimming the switching frequency, the efficiency and the total energy stored in capacitors, which reveals the volume of converter both change. It suggests that the proposed SCC can realize higher efficiency with the same volume limitation.

Then in Figure 20, situation that $CV^2 = 1$J is further selected and power loss of three kinds of SCC is broken down to three parts to compare power loss feature in different output power. And in Figure 21, the efficiency goal of three kinds of SCC is set to 98%. For different voltage gain situation, the proposed SCC can realize the least capacitor volume and the advantage is more evident in higher voltage gain.

To further illustrate the strengths of proposed SCC with a practical way, the number, cost and size of components are compared comprehensively. The 12V input, 60V output 5X converter with 600W output power and 98.5% efficiency is set as the design goal. Voltage ripple is still set as 5%V_L. Table 2 lists the specifications of the main components.

TABLE 2. Specification of components.

Components	Model #	Company	Cost	Size
25V, 10μF Cap	C2012X5R1E106K125AB	TDK	$0.09	0805/3.6mm^3
50V, 10μF Cap	CGA5L3X5R1H106M160AB	TDK	$0.27	1206/9.7mm^3
100V, 10μF Cap	CGA9N3X7S2A106M230KB	TDK	$1.21	2220/65mm^3
eGaN FET	EPC2023	EPC	$5.08	11.73mm^3
HB Driver	LMG1205YFXR	TI	$1.74	1.94mm^3
Isolated Driver	Si8271GB	Si Lab	$1.54	30mm^3

Then Table 3 shows the capacitor requirement, cost and volume of three kinds of SCCs, under the switching frequency satisfied efficiency goal.

The comparison result reveals the proposed SCC can significantly reduce the capacitor volume and cost by adopting lower voltage capacitors, even the proposed SCC have one more capacitor than conventional topologies. And the proposed SCC also has one more switching device than conventional topologies, but the additional cost and volume of this switching device is much less than the strengths on capacitor, especially in a higher voltage gain converter.

TABLE 3. Comparison of capacitors' cost and volume.

SCC Topology	Dickson-based	Ladder	Proposed
f_s	634kHz	289kHz	867kHz
Capacitance and Voltage	C_1, 26.2μF, 25V	C_1, 115μF, 25V	$C_{1,1}$, 19.5μF, 25V
	C_2, 26.2μF, 50V	C_2, 115μF, 50V	$C_{1,2}$, 19.5μF, 50V
	C_3, 26.2μF, 50V	C_3, 57.7μF, 50V	$C_{1,3}$, 15.2μF, 50V
	C_4, 26.2μF, 100V	C_4, 57.7μF, 50V	$C_{2,1}$, 13.1μF, 50V
	C_5, 26.2μF, 100V	C_5, 57.7μF, 100V	$C_{2,2}$, 13.1μF, 50V
			$C_{2,3}$, 7.69μF, 50V
Total Volume	496.743mm^3	335.34mm^3	94.802mm^3
Total Cost	$9.18	$9.19	$2.61

TABLE 4. Specification of the prototype.

Parameter	Value
Input voltage V_{in}	12V
Output voltage V_o	60V
Output Power P_o	600W
Inductor in 1st layer L_1	110nH
Inductor in 2nd layer L_2	220nH
Capacitor in 1st layer C_1~C_3	300μF
Capacitor in 2nd layer C_4~C_6	150μF
Switching frequency f_s	100kHz
Switching Device	EPC2023

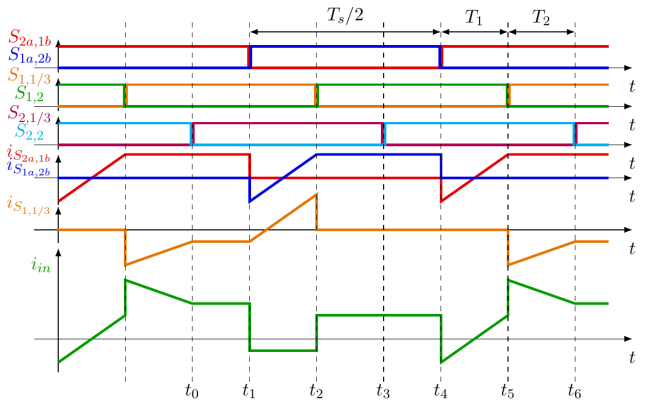


FIGURE 22. Waveforms of input current.

V. PROTOTYPE AND EXPERIMENT

A 600W 12V input and 60V output converter is built to validate the proposed topology and modulation method. The main parameters of the converter are listed in Table 4.

Figure 22 shows the input current waveform of low voltage side. According to the topology configuration, the input current can be calculated by current of three switching devices.

$$i_{in} = i_{S_{1a}} + i_{S_{1b}} - i_{S_{1,1}} \tag{30}$$

The requirement of input electrolytic capacitors depends on the input ripple current. With fourier decomposition of input current waveform, the ripple current at switching frequency is 19.45A. For a less number of input capacitors, high-rated-ripple-current capacitor can be chosen. Conductive polymer aluminum capacitor has much higher rated current than ordinary aluminum electrolytic capacitor, for example, 180 CPS series 330μF capacitor from Vishay can withstand 5A ripple current with $10.4 \times 10.4 \times 12.6\text{mm}^3$ volume, so that only 4 of this kind of capacitors are needed. To further reduce input capacitors and ripple current, two converters can be connected parallel, and the modulation can be interleaved, which can reduce the input ripple current to 5.3A and only one capacitor is needed. For a prototype, ordinary capacitors are selected with much design margin as shown in Figure 23.

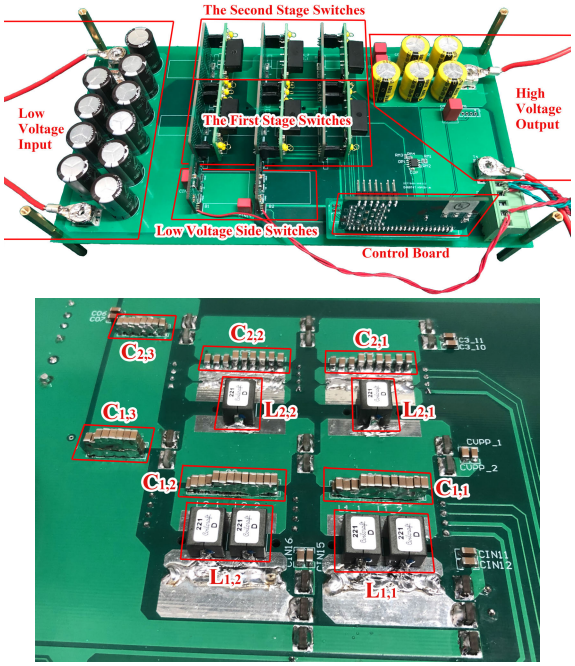


FIGURE 23. Prototype of the proposed SCC.

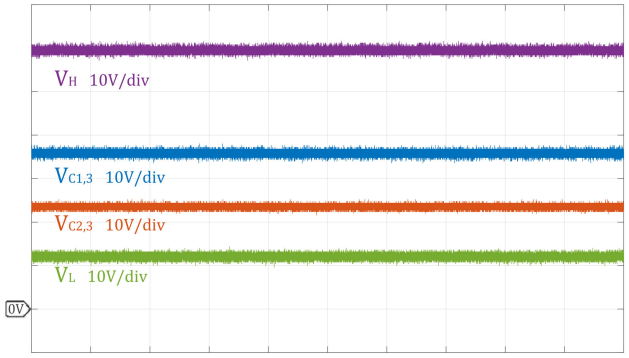


FIGURE 24. Low side voltage V_L, high side voltage V_H, output voltage of 1st stage $V_{C_{1,3}}$ and output voltage of 2st stage $V_{C_{2,3}}$.

The experiment results are presented below. Figure 24 shows the waveforms of low side input voltage V_L and high side output voltage V_H, which reveals the voltage conversion ratio. $V_{C1,3}$ and $V_{C2,3}$ is the output voltage of the first and the second stage on the capacitor $C_{1,3}$ and $C_{2,3}$. And the voltage waveforms of other capacitors are shown in Figure 25, which verifies the capacitor voltage stress distribution.

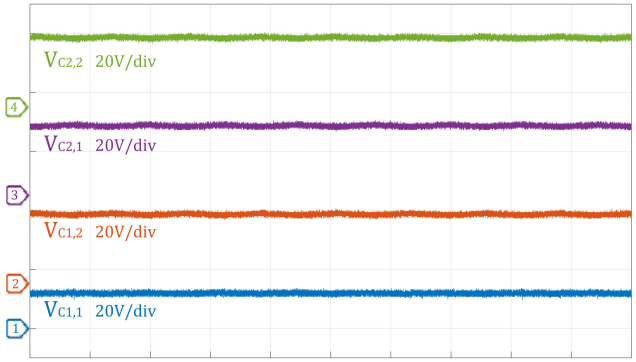


FIGURE 25. Voltage on capacitors $V_{C_{1,1}}$, $V_{C_{1,2}}$, $V_{C_{2,1}}$, $V_{C_{2,2}}$.

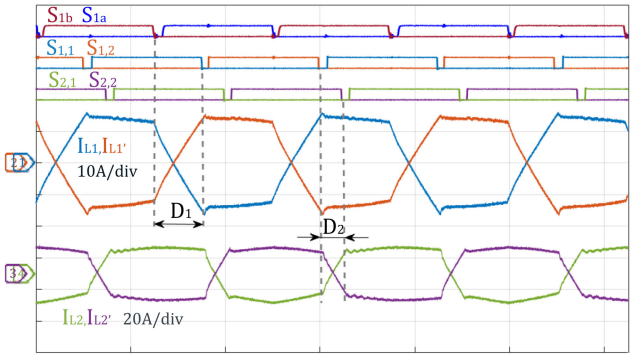


FIGURE 26. Waveform of current through Inductors.

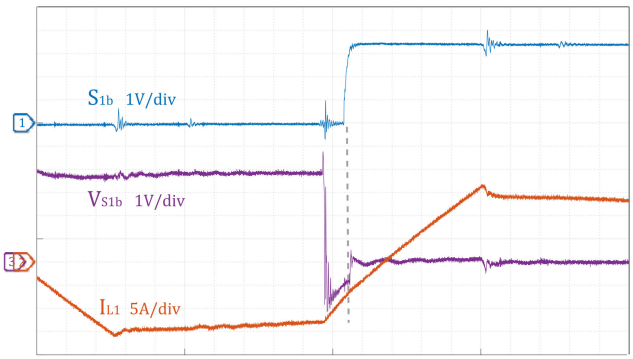


FIGURE 27. The ZVS operation of S_{1b}.

Figure 26 exhibits the phase shift modulation and the current waveforms of inductors. The waveforms tally with the theoretical analysis in Figure 11 and present power delivery states and current commutation states of each circuit stages. The current commutation states of each circuit stages are interlaced and the duration time of current commutation states is just the phase shift time as described in Chapter III.

The ZVS operation of the switching devices is shown in Figure 27, Figure 28 and Figure 29. Figure 27 shows the ZVS operation of device in the low voltage side and switch S_{1b} is chosen as an example. It can be seen that in the deadtime, the current of inductor i_{L1} is negative, which means the inductor can discharge the C_{oss}. Therefore, the V_{DS} of S_{1b}

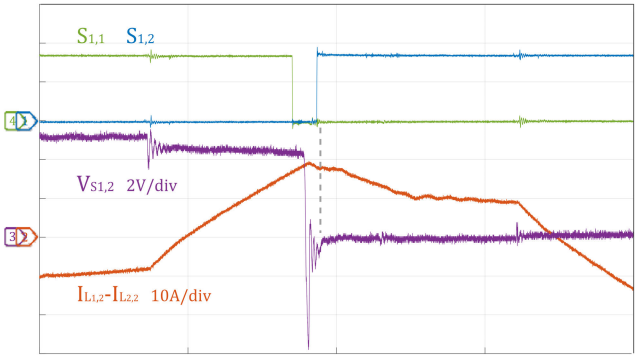


FIGURE 28. The ZVS operation of $S_{1,2}$.

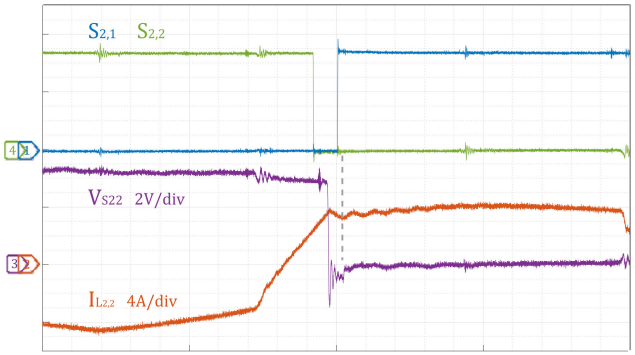


FIGURE 29. The ZVS operation of $S_{2,2}$.

drop to zero fast and the little negative voltage means the anti-parallel diode is conducted. When gate drive signal S_{1b} rises up, the ZVS can be realized.

VI. CONCLUSION

A novel switched-capacitor converter is proposed in this paper. Comparing with existing SCCs, the proposed SCC has following strengths:

1) The maximum capacitor voltage stress can be limited even in high-voltage-gain applications. The voltage stress in a 2-stage proposed SCC is nearly half of the Dickson-based SCC. Low voltage rate capacitors with higher capacitance and less volume can be utilized to achieve high power density.
2) The maximum voltage stress and current stress of switching devices can also be limited instead of increasing with voltage gain. Therefore, switching devices with lower conduction resistance can be applied and the power loss on devices can be reduced.
3) The proposed SCC is capable of phase shift modulation and corresponding phase shift strategy is also proposed in this paper, which realizes voltage regulation ability of SCC.
4) By adopting phase shift modulation, ZVS operation of all the switching devices can be achieved, which is reasonably beneficial to WBG devices as higher switching frequency, zero turn-on loss and lower EMI can be achieved.

The steady state analysis indicates the advantage of the proposed SCC. With the same limitation of energy stored in capacitors, the proposed SCC can improve efficiency by nearly 1%, compared with other conventional SCCs, which is illustrated in Figure 19. And the experiment on the prototype proves the realizability of theoretical design.

REFERENCES

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[2] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% efficiency switched-tank converter for data center application," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6205–6222, Jul. 2018.

[3] W. Qian, H. Cha, F. Z. Peng, and L. M. Tolbert, "55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1668–1678, Apr. 2012.

[4] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid State Circuits*, vol. SSC-11, no. 3, pp. 374–378, Jun. 1976.

[5] D. Cao and F. Z. Peng, "A family of zero current switching switched-capacitor DC-DC converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2010, pp. 1365–1372.

[6] D. Cao and F. Z. Peng, "Zero-current-switching multilevel modular switched-capacitor DC–DC converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, San Jose, CA, USA, Sep. 2009, pp. 3516–3522.

[7] D. Cao and F. Z. Peng, "Multiphase multilevel modular DC–DC converter for high-current high-gain TEG application," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1400–1408, May/Jun. 2011.

[8] D. Cao, S. Jiang, and F. Z. Peng, "Optimal design of multilevel modular switched-capacitor DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Sep. 2011, pp. 537–544.

[9] Y. Li, B. Curuvija, X. Lyu, and D. Cao, "Multilevel modular switched-capacitor resonant converter with voltage regulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2017, pp. 88–93.

[10] D. Cao, X. Yu, X. Lu, W. Qian, and F. Z. Peng, "A double-wing multilevel modular capacitor-clamped DC-DC converter with reduced capacitor voltage stress," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, Sep. 2011, pp. 545–552.

[11] W. Qian, J. G. Cintrón-Rivera, F. Z. Peng, and D. Cao, "A multilevel DC-DC converter with high voltage gain and reduced component rating and count," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Fort Worth, TX, USA, Mar. 2011, pp. 1146–1152.

[12] W. Qian, D. Cao, J. G. Cintron-Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul./Aug. 2012.

[13] D. Cao, X. Lu, X. Yu, and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor DC-DC converter with voltage regulation," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, USA, Mar. 2013, pp. 2029–2036.

[14] D. Cao, W. Qian, and F. Z. Peng, "A high voltage gain multilevel modular switched-capacitor DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Pittsburgh, PA, USA, Sep. 2014, pp. 5749–5756.

[15] D. Gunasekaran, L. Qin, U. Karki, Y. Li, and F. Z. Peng, "A variable (n/m)X switched capacitor DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6219–6235, Aug. 2017.

[16] G. Han, D. Gunasekaran, L. Qin, and F. Z. Peng, "Asymmetrical (n/m)X DC-DC converter for finer voltage regulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Tampa, FL, USA, Mar. 2017, pp. 99–106.

[17] S. Li, W. Xie, and K. M. Smedley, "A family of an automatic interleaved Dickson switched-capacitor converter and its ZVS resonant configuration," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 255–264, Jan. 2019.

[18] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A high efficiency resonant switched-capacitor converter for data center," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 4460–4466.

[19] Y. He, S. Jiang, and C. Nan, "Switched tank converter based partial power architecture for voltage regulation applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 91–97.

[20] S. Jiang, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 81–90.

[21] B. Curuvija, X. Lyu, Y. Li, and D. Cao, "Single-wing ladder resonant multilevel converter," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2016, pp. 328–333.

[22] D. C. S. de Moura, B. Curuvija, and D. Cao, "A wide bandgap device based multilevel switched-capacitor converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Long Beach, CA, USA, Mar. 2016, pp. 3553–3559.

[23] S. Li, K. Xiangli, Y. Zheng, and K. M. Smedley, "Analysis and design of the ladder resonant switched-capacitor converters for regulated output voltage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7769–7779, Oct. 2017.

[24] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high-power high-efficiency switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, Mar. 2008.

[25] Z. Liao, Y. Lei, and R. C. N. Pilawa-Podgurski, "Analysis and design of a high power density flying-capacitor multilevel boost converter for high step-up conversion," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4087–4099, May 2019.

[26] A. Stillwell, M. E. Blackwell, and R. C. N. Pilawa-Podgurski, "Design of a 1 kV bidirectional DC-DC converter with 650 V GaN transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 1155–1162.

[27] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," in *Proc. 26th Annu. IEEE/PESC Power Electron. Spec. Conf.*, vol. 2, Jun. 1995, pp. 1215–1221.

[28] A. Kushnerov and S. S. Ben-Yaakov, "Unified algebraic synthesis of generalized fibonacci switched capacitor converters," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Raleigh, NC, USA, Sep. 2012, pp. 774–778.

[29] Y. Mahnashi and F. Z. Peng, "Generalization of the fundamental limit theory in a switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6673–6676, Sep. 2017.

[30] Y. Li, J. Chen, M. John, R. Liou, and S. R. Sanders, "Resonant switched capacitor stacked topology enabling high DC–DC voltage conversion ratios and efficient wide range regulation," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7.

[31] Y. Li, L. Gu, A. Hariya, Y. Ishizuka, J. Rivas-Davila, and S. Sanders, "A wide input range isolated stacked resonant switched-capacitor DC-DC converter for high conversion ratios," in *Proc. IEEE 19th Workshop Control Modeling Power Electron. (COMPEL)*, Padua, Italy, Jun. 2018, pp. 1–7.

[32] C. Le, M. Kline, D. L. Gerber, S. R. Sanders, and P. R. Kinget, "A stackable switched-capacitor DC/DC converter IC for LED drivers with 90% efficiency," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2013, pp. 1–4.

[33] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[34] M. H. Kiani and J. T. Stauth, "Optimization and comparison of hybrid-resonant switched capacitor DC-DC converter topologies," in *Proc. IEEE 18th Workshop Control Modeling Power Electron. (COMPEL)*, Stanford, CA, USA, Jul. 2017, pp. 1–8.

[35] M. Shoyama and T. Ninomiya, "Output voltage control of resonant boost switched capacitor converter," in *Proc. Power Convers. Conf.-Nagoya*, Nagoya, Japan, Apr. 2007, pp. 899–903.

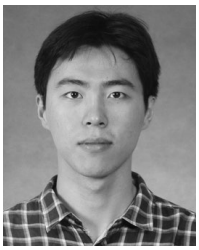
[36] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a Dickson switched-capacitor converter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 770–782, Jan. 2016.

[37] B. B. Macy, Y. Lei, and R. C. N. Pilawa-Podgurski, "A 1.2 MHz, 25 V to 100 V GaN-based resonant Dickson switched-capacitor converter with 1011 W/in3 (61.7 kW/L) power density," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 1472–1478.

[38] Y. Lei, Z. Ye, and R. C. N. Pilawa-Podgurski, "A GaN-based 97% efficient hybrid switched-capacitor converter with lossless regulation capability," *2015 IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 4264–4270.

[39] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011.

[40] J. Zhu and D. Maksimović, "Dynamic modeling of a hybrid switched-capacitor-based converter with phase-shift control," in *Proc. IEEE 19th Workshop Control Modeling Power Electron. (COMPEL)*, Padua, Italy, Jun. 2018, pp. 1–6.
[41] Y. Li, M. John, J. Poon, J. Chen, and S. R. Sanders, "Lossless voltage regulation and control of the resonant switched-capacitor DC-DC converter," in *Proc. IEEE 16th Workshop Control Modeling Power Electron. (COMPEL)*, Vancouver, BC, Canada, Jul. 2015, pp. 1–7.



HONGYANG XIE was born in Zhejiang, China, in 1997. He is currently pursuing the B.S. degree with Shanghai Jiao Tong University, Shanghai, China, in 2019, where he is also a Senior Student majoring in electrical engineering.

His current research interests include dc/dc converter and switched-capacitor converter.

RUI LI (S'10–M'11) received the Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2010.

From 2008 to 2009, he was an Academic Guest with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, ZÜrich, Switzerland. From 2014 to 2015, he was a Postdoctoral Research Scholar with the Center for Advanced Power Systems, Department of Electrical and Computer Engineering, College of Engineering, Florida State University, Tallahassee, FL, USA. Since 2010, he has been with the Department of Electrical Engineering, School of Electronics, Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai, China, where he is currently an Associate Professor. His current research interest includes the application of power electronics in renewable energy conversion. He was a recipient of the IEEE Power Electronics Society Transactions Second Prize Paper Award, in 2015.