IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

SPECIAL SECTION ON MILLIMETER-WAVE AND TERAHERTZ PROPAGATION, CHANNEL MODELING AND APPLICATIONS

Received June 23, 2019, accepted July 19, 2019, date of publication July 29, 2019, date of current version August 26, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2931658

Intra- and Inter-Chip Transmission of Millimeter-Wave Interconnects in NoC-Based Multi-Chip Systems

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This work was supported in part by the U.S. National Science Foundation (NSF) CAREER Grant under Grant CNS-1553264.

ABSTRACT The primary objective of this paper is to investigate the communication capabilities of short-range millimeter-wave (mmWave) communication among network-on-chip (NoC)-based multi-core processors integrated on a substrate board. This paper presents the characterization of transmission between on-chip antennas for both intra- and inter-chip communication in multi-chip computing systems, such as server blades or embedded systems. Through simulation at 30 GHz, we have characterized the inter-chip transmission and studied the electric field distribution to explain the transmission characteristics. It is shown that the antenna radiation efficiency reduces with a decrease in the resistivity of silicon. The simulation results have been validated with fabricated antennas in different orientations on silicon dies that can communicate with inter-chip transmission coefficients ranging from −45 to −60 dB while sustaining bandwidths up to 7 GHz. Using measurements, a large-scale log-normal channel model is derived, which can be used for system-level architecture design. Using the same simulation environment, we perform design and analysis at 60 GHz to provide another non-interfering frequency channel for inter-chip communication in order to increase the physical bandwidth of the interconnection architecture. Furthermore, densely packed multilayer copper wires in NoCs have been modeled in this paper to study their impact on the wireless transmission for both intra- and inter-chip links. The dense orthogonal multilayer wires are shown to be equivalent to copper sheets. In addition, we have shown that the antenna radiation efficiency reduces in the presence of these densely packed wires placed in the close proximity of the antenna elements. Using this model, the reduction of inter-chip transmission is quantified to be about 20 dB compared with a system with no wires. Furthermore, the transmission characteristics of the antennas resonating at 60 GHz in a flip-chip packaging environment are also presented.

INDEX TERMS Channel modeling, inter- and intra- chip transmission, millimeter wave interconnect, multi-chip system, network-on-chip.

I. INTRODUCTION

Various kinds of computing platforms such as server blades or embedded systems are essentially platform-based multi-chip systems that integrate many multicore processor chips, memory banks and other functional units. With the increase in the computational and functional complexity of these platforms, the number of individual System-on-Chips (SoCs) or multicore processing chips in such systems increase manifold. This makes the interconnection in these systems grow in both size and complexity. While intra-chip communication infrastructure is seeing a paradigm shift from bus-based systems to Network- on-Chip (NoC) architectures [1], inter-chip communication also needs to evolve at a rapid pace to cater to increasing bandwidth demands within the strict power and thermal envelopes. Traditionally, inter-chip

The associate editor coordinating the review of this manuscript and approving it for publication was Franco Fuschini.

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interconnections are realized using solder bumps or controlled collapse chip connection (C4) interconnects placing individual chips on a substrate, interposer, Flame Retardant (FR4) board or Printed Circuit Board (PCB). However, recent trends according to the International Roadmap for Devices and Systems (IRDS, formerly ITRS) [2] predict that the pitch of the I/O interconnects in ICs is not scaling as fast as the gate lengths or pitch of on-chip interconnects. This implies a gap in density and performance of traditional I/O systems relative to on-chip interconnections. Moreover, longer and bulkier traces for inter-chip communication due to the wiring complexity, which starts from metal interconnects on chip to copper traces on PCB, further aggravates the crosstalk and the signal integrity issues [3], [4]. Silicon interposers, which are bare dies with abundant wiring resources are used to support inter-chip communication by overcoming the bottlenecks of traditional I/O [5]. However, its benefits are limited due to micro-bump density between the chips and the interposer socket. Often the intra- and inter-chip communication protocols are also different thereby limiting the design flexibility. Due to these factors, the efficiency of the multi-chip system in terms of bandwidth, latency and energy consumption is reduced.

Recent wireless transceiver designs [6]–[8] and system-level simulations [9]–[12] have shown that wireless interconnects in the millimeter-wave (mmWave) bands can reduce energy consumption and increase bandwidth of chip-to-chip communication significantly as compared to the traditional metallic interconnect based systems. Although the computing community has recognized the need for non-traditional solutions to the interconnect problem, most system-level work relies only on simulation of the antenna propagation characteristics in simplified environments [12], [13]. This motivates our work in this paper, where we investigate the capabilities of mmWave communication for short-range links among chips integrated on a typical substrate, especially in the presence of realistic structures like wired interconnects and ground plane. In order to investigate the mmWave communication among such chips, we design and simulate 30GHz on-chip embedded antennas. Simulated results are then validated using fabrication and experimental measurement of these on-chip antennas embedded in chips mounted on a substrate. We analyze the effect of silicon resistivity on radiation efficiency of these antennas. We use these measurements to develop a mmWave path loss model between antennas in such a multi-chip system. Using the validated simulation methodology, we then design and simulate on-chip antennas in the 60GHz band to leverage their smaller footprint as compared to the 30GHz antennas. We analyze the transmission capabilities and radiation efficiencies of these 60GHz embedded antennas in the presence of realistic on-chip structures like metallic interconnects using simulation only since these metallic interconnects require advanced and expensive fabrication processes. We also demonstrate the transmission characteristics of these antennas in flip-chip packaging environment.

The paper is organized as follows. Section II summarizes the relevant related work. Section III explains the rationale for selection of on-chip antenna structures for inter-chip communications. Furthermore, section IV presents the simulation and measurement results. Finally, conclusions are discussed in section V.

II. RELATED WORK

We discuss existing literature in terms of two aspects, namely, novel on-chip antenna design, and, transmission and channel characterization.

A. ON-CHIP ANTENNAS

Several antenna structures have been investigated over the last decade for high frequency communications in both intra- and inter-chip communication [14]–[16]. In [17], [18] authors have looked at metallic antennas such as linear dipole, meander, zigzag and loop antennas and presented most of their transmission characteristics between 10GHz to 18GHz. Also, [17] showed feasibility of inter-chip communication in the 23GHz to 25GHz frequency band, but distances over which transmission is measured ranges from 10cm to 10m which is large for multi-chip systems. Zhang *et al*. in [19], [20] have performed channel modeling in the frequency and time domains using on-chip antennas. They have shown that the dominant propagation for intra-chip communication is surface waves, however, the propagation in case of inter-chip remains unexplored. Sun et al. in [21] designed and evaluated the performance of on-chip meander antennas for intra-chip communications in ultra-wideband (UWB) radios that operate in the 22-29GHz frequency band. In [22], Kikkawa has provided simulated and measured transmission coefficients for on-chip dipole antennas which are designed to operate at 3.5GHz without considering any metal interconnects.

B. TRANSMISSION AND CHANNEL MODELING OF WIRELESS INTERCONNECTS

In [23] a channel model is presented for wireless communication at 60GHz inside an empty metallic cabinet using open waveguide antennas that are not embedded in the silicon dies. In [24] channel model for communication within a computer chassis was presented for the 3GHz to 6GHz UWB frequencies using meander-line monopole antennas which are not integrated on chip. In [25], channel model at 57GHz is presented using V-band patch antennas within a commercial micro-server chassis. However, the channel model could potentially be different for on-chip embedded antennas. In [26], Matolak *et al.* have theoretically discussed the challenges involved in channel modeling for wireless network-on-chip which involves intra-chip communication. In [27], the authors present on-chip antenna analysis and channel characterization at 150GHz. In [28], Wu *et al.* have presented transmission analysis without any parameter modeling in frequency & time domain between 15GHz & 26GHz using zigzag dipole antenna in hybrid engine controller board (HECB). In [29], simulation based transmission

characteristics at 60GHz is shown between on-chip zigzag monopole antennas. In [30], Gade *et al.* have performed simulations for channel modeling using Log-periodic and folded dipole antenna, but they have not taken the effects of on-chip metallic wires. In [31] channel characteristics from a packaging perspective was explored. A ray-tracing based multi-path channel model for intra-chip wireless interconnects is proposed in [32]. In [33], the authors explore metasurfaces for wireless interconnects. In [34], Yordanov *et al.* has demonstrated an on-chip antenna implemented using the CMOS ground plane at the top metal layer on high resistive silicon substrate which operates around 60GHz. Moreover, they have analyzed the effects of small, short metal interconnect just under their antenna, which is not a full chip interconnect network. In this paper, we present transmission characteristics of 30GHz and 60GHz on-chip zigzag antennas for inter-chip communication for three different configurations. The next section explains choice of the on-chip antenna in multi-chip system for inter-chip communication.

III. DESIGN OF ANTENNA CONFIGURATIONS FOR MULTI-CHIP SYSTEMS

The on-chip antenna has to provide the best power gain for the smallest area overhead. Several on-chip antenna designs in the mmWave bands such as, linear dipoles, patch antennas and log-periodic antennas have been investigated. Our choice of the zigzag antenna for this paper, is based on its small footprint and its omnidirectional pattern [35], which allows for easy placement and ability to communicate with other chips at various orientations. Moreover, a sufficiently omnidirectional antenna can also enable broadcast among the wireless nodes in the platform, which is greatly beneficial for handling broadcast or multicast messages to maintain memory or cache coherency protocols and status updates [11]. For this reason, we do not adopt beam-forming antenna arrays, which are the common focus for mmWave systems in other application areas such as 5G communications [36]. In addition, such mmWave antennas, which are fabricated using top layer metals of CMOS processes, are suitable for near-term solutions to the wired interconnect problem compared to other alternatives like Graphene or Carbon Nanotube (CNT) based antennas, although they might operate at higher frequencies [37]. Due to these reasons, we have, in this paper, designed mmWave zigzag on-chip antennas and their co-planar waveguide feed structure to resonate in the mmWave frequencies such as 30GHz and 60GHz. Next, we discuss the characteristics of the antennas in multi-chip systems.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the simulation setup of a multi-chip system is explained for 30GHz followed by the fabrication of on-chip antennas. Measurement of transmission between fabricated antennas is performed along with large-scale channel modeling. Lastly, simulation study of transmission at 60GHz in a multi-chip system in presence of wires is presented. In the following sections, intra-chip refers to the communication between antennas in the same chip and inter-chip refers to the communication between antennas in different chips in the multichip system.

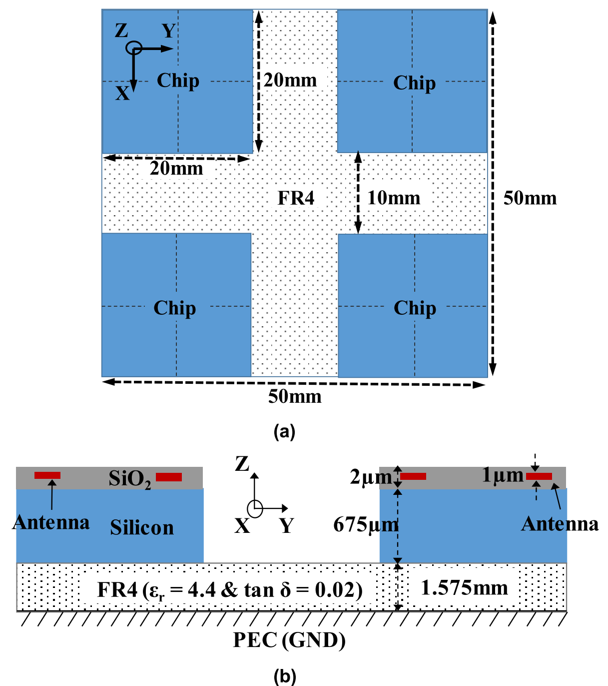


FIGURE 1. (a) Top view of the multi-chip system. (b) Cross section of multi-chip system setup. Note: Figures are not to scale.

A. SIMULATION OF ON-CHIP ANTENNA IN MULTI-CHIP SYSTEMS AT 30GHz

In this section, the design and simulation of on-chip antennas in a multi-chip system are discussed. The on-chip antennas are designed and optimized in ANSYS High Frequency Structure Simulator (HFSS). The simulation of silicon chips with on-chip antennas operating at 30 GHz is performed in a multi-chip system environment. The simulation setup consists of four silicon chips each with typical dimensions of 20mm x 20mm placed on an organic substrate (FR4 - $\varepsilon_r = 4.4$, $\tan(\delta) = 0.02$) of thickness 1.575mm. Each chip is equally divided into four quadrants as seen in the layout shown in Fig. 1(a). A cross-sectional view is also shown in Fig. 1(b). The chips are made of silicon ($\varepsilon_r = 11.7$ & $\rho = 55\Omega$-cm) with thickness 675μm. A 2μm thick silicon-dioxide ($\varepsilon_r = 3.4$) layer is considered above the silicon. A Perfect Electric Conductor (PEC) boundary at the bottom of organic substrate is considered for simulation purpose to emulate the effect of ground plane. Furthermore, the design of on-chip antenna should be small, compact and low-profile for implementing on or inside a silicon-dioxide layer. The design of on-chip antenna is shown in Fig. 2(a). It is a single metal (aluminum) layer zigzag antenna which can be fabricated on a silicon chip using conventional CMOS-based fabrication process.

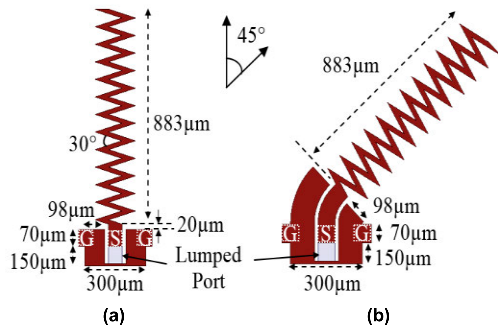


FIGURE 2. On-chip antennas designed at 30 GHz. (a) Orientation 1 (O1), (b) Orientation 2 (O2). The width of the signal trace is 70μm.

The on-chip antenna is 883μm long for operations at 30GHz. The thickness of the aluminum layer is 1μm. In order to use Ground-Signal-Ground (GSG) probes in the fabricated antennas for excitation, the antennas are modified to include probe pads. Cascade ACP40-A is used in the next subsection as the GSG probe. They have a pitch of 150μm and minimum pad size requirement of 50μm. So, three probe pads, each of size 70μm x 70μm with pitch of 150μm, are designed as shown in Fig. 2(a). The width of the signal trace is 70μm. For simulation purpose, a HFSS lumped port is used for exciting the co-planar waveguide (CPW) feed of the on-chip antennas.

Moreover, another on-chip antenna configuration is designed which is rotated 45° as compared to the previous antenna and is shown in Fig. 2(b). The first one is orientation 1 (O1) and the latter is orientation 2 (O2). The reason of the two different orientations is to study the effect of orientation on the transmission between on-chip antennas. For O2, the bend in the feed line shown in Fig. 2(b) is to accommodate the movement of GSG probes in the measurement system which is constrained to only linear three dimensional motion. Next, the on-chip antennas are placed at the center of each quadrant in the silicon chips. Three configurations (Conf) of the silicon chips are designed using the two different orientations of on-chip antennas. The arrangements of on-chip antennas on a chip are shown in Fig. 3, and labeled as Conf 1, Conf 2 and Conf 3. Conf 1, which is shown in Fig. 3(a), has antennas parallel to each other. Conf 2 and Conf 3 are shown in Fig. 3(b) and 3(c), respectively. Conf 2 and Conf 3 have antennas positioned similar to Conf 1 but rotated 45° away from and towards the center of the chip, respectively. We use these three configurations to study the impact of antenna orientations, the ground plane and FR4 substrate on transmission characteristics between the on-chip antennas.

It should be noted that all the on-chip antennas are located in the far field region of each other. The far field boundary is considered to be at a distance of $\lambda/2\pi$ from the antenna [38] which, at 30 GHz corresponds to 1.6mm in free space. In our layout, the minimum distance between antennas in the chip is 10 mm as shown in Fig. 3, therefore, all on-chip antennas are placed in the far field region. For the simulation model, four chips of the same configuration are placed in a multi-chip system on top of the FR4 board as shown in Fig. 1(a). For each

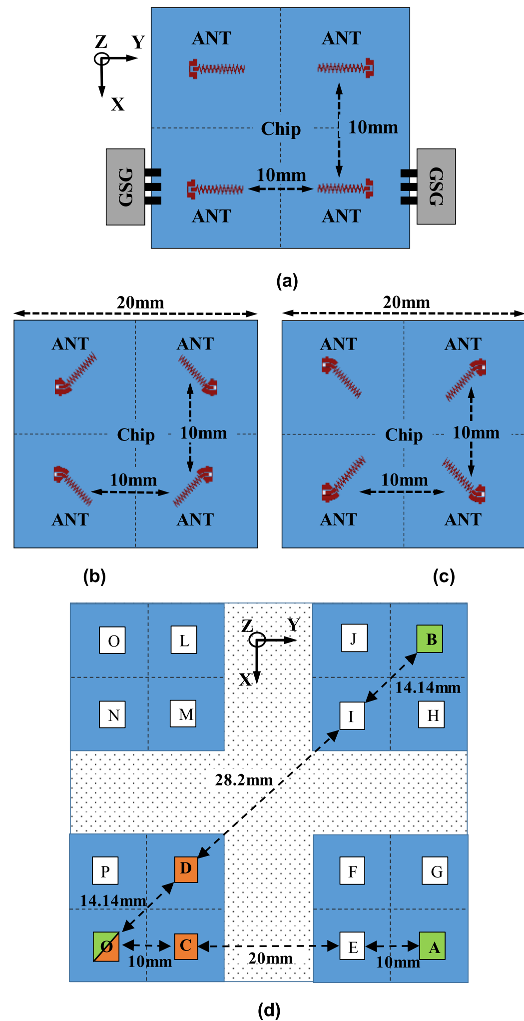


FIGURE 3. Silicon chips with antennas (ANT) in multi-chip system for simulation and fabrication. (a) Configuration (Conf) 1, (b) configuration 2, and (c) configuration 3, (d) top view of multi-chip system showing the placement of antennas under investigation. Note: (i) Figures are not to scale. Antennas are enlarged to show the orientations. (ii) The antennas are placed at the center of the quadrant, (iii) Antenna O is considered as reference for the analysis of transmission coefficients. All distances are from center-to-center of the antennas.

such arrangement corresponding to the three configurations, simulation is performed using ANSYS HFSS.

The on-chip antennas are optimized to have a reflection coefficient (S_{11}) of below −15dB at 30GHz shown in Fig. 4. For each configuration, the reflection coefficient (S_{11}) is shown for only one antenna since all four are identical. The simulated radiation efficiency of zigzag antenna is 15% for all configurations. For transmission coefficients, there are numerous combinations of antenna pairs. So, to make the discussion tractable, only five antennas are considered as shown in Fig. 3(d). These antennas are selected because they include the expected worst cases that is, farthest antenna pairs for intra- and inter-chip pairs (A, B, C and D from O). All transmissions for 30GHz frequency band in this paper are measured relative to the common ANT O. The simulated transmission coefficients for inter-chip communication are

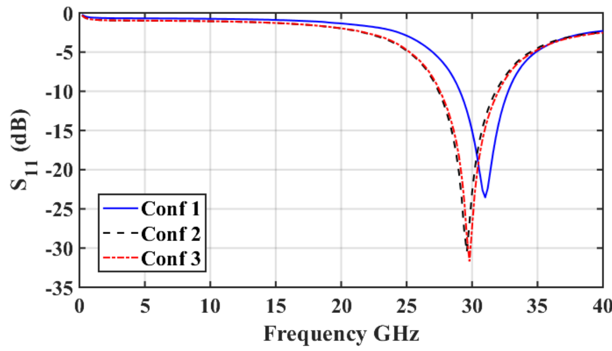


FIGURE 4. S_{11} of antennas in all configurations.

shown in Fig. 5(a), and intra-chip communication are shown in Fig. 5(b).

It is seen that the intra-chip transmission at 30GHz, varies from −31dB to −38dB, and inter-chip transmission varies from −46 to −60dB, which is expected since the distance between the antennas has increased in the latter case. Moreover, in Fig. 5(a) at 30GHz, the transmission between antennas A & O and antennas B & O in Conf 3 is −60.68dB and −46.5dB, despite the fact that the distance between antennas A & O is smaller than that between antennas B & O. This is due to the structure of the multi-chip system and the interference caused by the reflected multi-path propagations from the ground [39]. In addition, Fig. 5(c) shows the simulated magnitude of electric field along the line connecting ANT O & ANT A and ANT O & ANT B. Since, the path between these antenna pairs passes through metal of other antennas such as ANT C (at 9mm on blue trace), ANT E (at 29mm on blue trace) and ANT A (at 38mm on blue trace), the discontinuity effects of electric field are seen in the plot.

We can further observe that the field distribution varies across the structure. To investigate this further, we study the magnitude of the electric field distribution, shown in Fig. 6(a) to Fig. 6(c) for all three configurations in the plane of antenna (surface of silicon-dioxide) and cross section plane containing antennas O and A at 30GHz. The field distribution depends on the structure geometry, material used, and the operating frequency. In Fig. 6(c), low intensity of field distribution can be noticed at the position of antenna A. This is the reason for the fluctuations in the transmissions. The distribution of field in Conf 2 and Conf 3 is different for ANT B, therefore the transmission between ANT B & O is better for Conf 3.

Furthermore, as confirmed by [20], the dominant way of propagation in intra-chip propagation is surface waves. This can be seen in the cross-sectional view of structure in Fig. 6 where high magnitudes of field distribution are on the surface of the chip where the on-chip antenna is excited. Another observation from the electric field plots in Fig. 6 is the diffractions of waves at the edges, which can significantly increase the multi-path effect. If directional on-chip antennas or on-chip phased array for inter-chip communication are used, then these edge diffractions might cause beam to distort which may reduce the gain. Moreover, as the field propagates to other chips, the low intensity regions become significant, which can be observed in Fig. 6. This shows that the expected omnidirectional radiation of zigzag antenna is distorted due to structures, geometry and materials of the setup. Therefore, the analysis of field distribution needs to be considered while placing on-chip antennas for data communication between chips in the multi-chip systems.

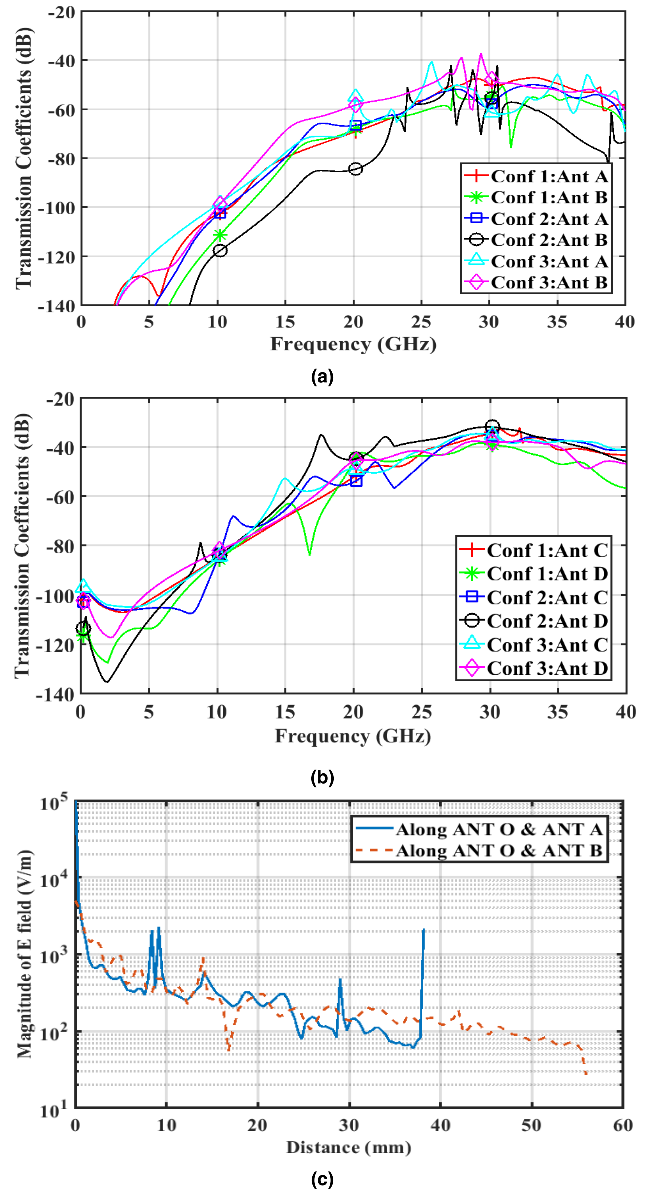
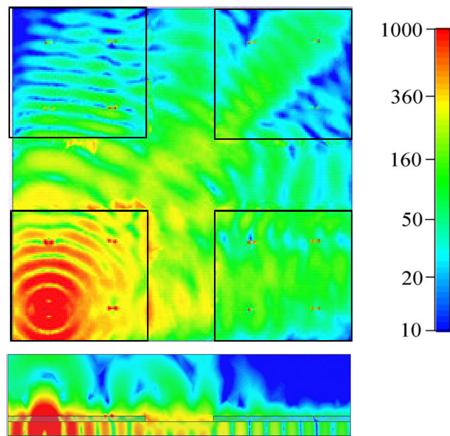


FIGURE 5. Transmission coefficients of antennas under investigation with ANT O as reference. (a) Inter-chip transmission, (b) intra-chip transmission, (c) magnitude of electric field (V/m) along the line connecting ANT O and ANT A & ANT O and ANT B (only ANT O is excited) in Conf 1. Antenna Arrangement is shown in Fig. 3.

Furthermore, analysis of S_{11} is discussed with the variation of resistivity of silicon. The S_{11} of zigzag antenna in Conf 1 is shown in Fig. 7 with different resistivity of silicon. The structure for the simulation is same as previously discussed



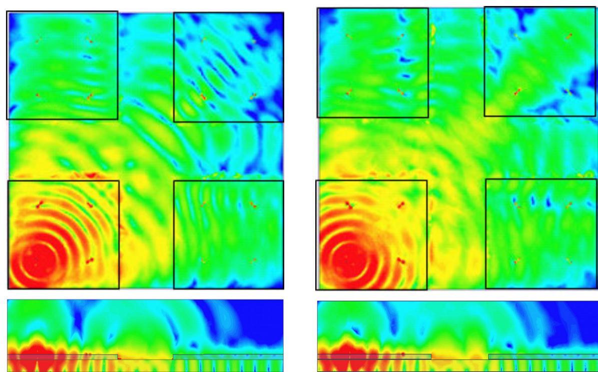


FIGURE 6. Magnitude of electric field (V/m) distribution on the surface of silicon and cross section view across ANT O and ANT A when ANT O is excited at 30GHz. (a) Configuration 1, (b) configuration 2 and (c) configuration 3 as shown in Fig. 3.

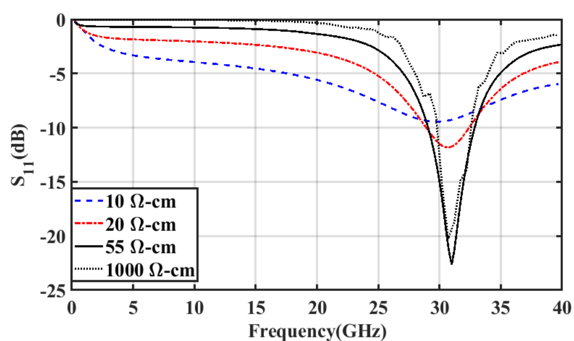


FIGURE 7. Magnitude of S_{11} of on-chip antenna for Conf 1 for different resistivity of silicon.

here, while only the resistivity of silicon is varied. It can be noted that the resonant frequency of the antenna is similar, however, the S_{11} is reduced. Table 1 shows the radiation efficiency of the antenna with variation in resistivity of silicon. The radiation efficiency decreases because of the decreasing resistivity. This can be attributed to increase in loss due to the silicon. This shows that higher resistive silicon is more desirable for on-chip antennas. Next, we present the measurement results from fabricated on-chip antennas corresponding to the designs discussed in this section.

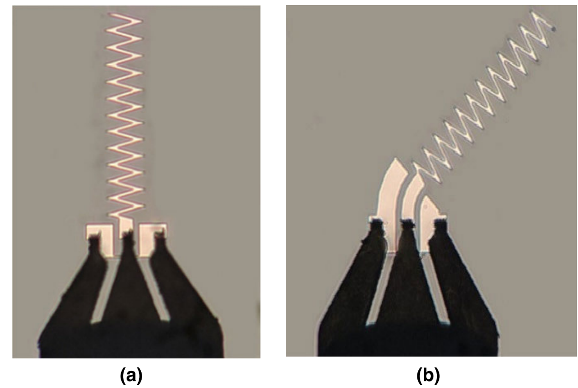


FIGURE 8. Micrograph of fabricated antennas on silicon, (a) an antenna from a Conf 1 die, (b) an antenna from a Conf 2 die.

TABLE 1. Radiation efficiency of on-chip antenna for Conf 1 for different resistivity of silicon.

Silicon Bulk Resistivity (Ω-cm)	10	20	55	1000
Simulated Radiation Efficiency at 30GHz (in %)	0.2	1	15	30

B. FABRICATION & MEASUREMENTS OF ON-CHIP ANTENNAS

In order to validate the simulation results, the designed antennas are fabricated on a 6-inch p-type (100) silicon wafer of thickness 675μm and resistivity of 55 Ω-cm, measured by a 4-point probe method. The first step in the fabrication process involves wafer cleaning using the RCA cleaning method. Next, a 2μm layer of oxide is grown using a wet oxidation method in a Bruce Thermal Furnace. After growing the silicon-dioxide, the thickness of oxide is confirmed using a Prometrix SM200 SpectraMap reflectometer. The aluminum is then deposited via a sputter deposition process in a CVC 601 Sputter. After aluminum deposition, a layer of photoresist is applied on the wafer using an automated SSI Track and the shape of the antenna is defined through a 1x contact-lithography process with a Karl-Suss MA150 Aligner. After the photoresist development process, aluminum is etched using a chlorine-based dry etch process, in a Lam 490 Plasma Etch, to ensure the needed resolution and sharpness of the antenna features before removing the photoresist. This step completes the fabrication of antennas. Lastly, the wafer is cut into 20mm x 20mm dies using a KS780 Dicing Saw. These silicon dies are used to make a multi-chip arrangement. Microscopic pictures of the fabricated antennas are shown in Fig. 8.

Furthermore, Cascade Summit 9000 probe station along with Agilent 8363B vector network analyzer (VNA) is used for testing of the fabricated antennas. The measurement setup is shown in Fig. 9(a). The VNA is calibrated from 1GHz to 40GHz using Short-Open-Load-Thru (SOLT) method with Cascade impedance standard substrate (P/N: 106-682).

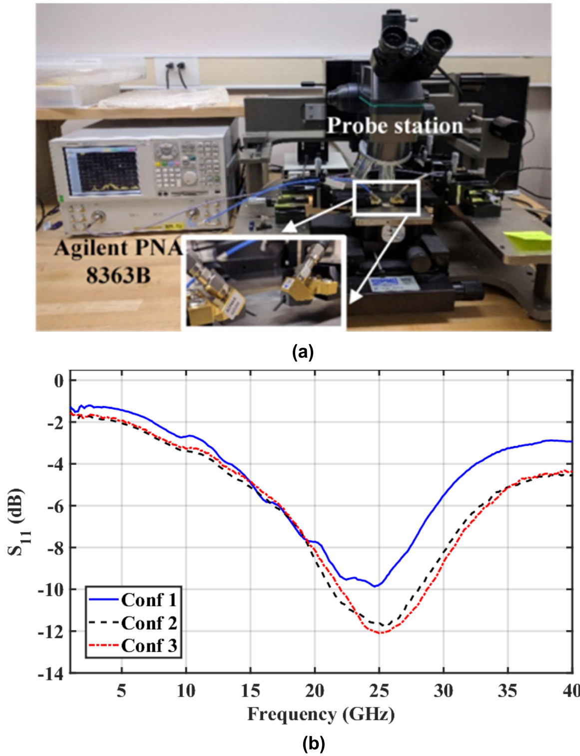


FIGURE 9. (a) Measurement setup. (b) S_{11} of one fabricated antenna from each configuration.

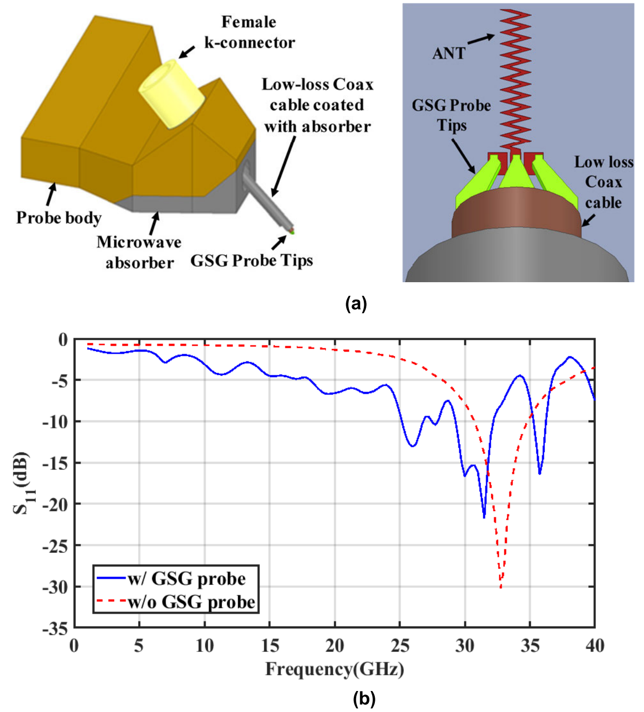


FIGURE 10. (a) Cascade GSG probe modeled in HFSS and close-up top-view of one of the zigzag antennas of Conf 1 with GSG probe on its contact pads simulated in HFSS, (b) simulated S_{11} of on-chip antenna with and without probe.

The IF bandwidth is set to 5kHz to increase the dynamic range of VNA, and reduce the noise in measurements. Also, each measurement is further repeated 10 times to average out the noise. As mentioned in section IV.A Cascade ACP40-A are used as GSG contact probes. They have a pitch of 150μm and minimum pad size requirement of 50μm. Also, the simulation design shown in Fig. 1 has a ground plane. This ground plane is not fabricated on silicon wafer, rather the metal chuck of the probe station emulates the effect of the ground plane.

Using the measurement setup, first the reflection coefficient (S_{11}) of fabricated antennas in different configurations is measured. It should be noted that the reflection coefficient (S_{11}) of all on-chip antennas in a configuration is same due to same design, therefore, only one trace of reflection coefficient (S_{11}) from each of the three configurations is shown in Fig. 9(b). The reflection coefficient (S_{11}) shows that the fabricated antennas resonate at 25GHz with a S_{11} magnitude of −10dB to −12dB. However, the simulated reflection coefficient (S_{11}) of antennas in all configuration show the resonant frequency to be around 30GHz as indicated in Fig. 4. In order to investigate the reasons for this shift in resonant frequency between the simulated and fabricated antennas we modeled the probe structure to study its impact on the resonant frequency. The 3-dimensional probe model, shown in Fig. 10(a), has been created from US Patent no. 5506515 by Cascade [40] in conjunction with many dimensional measurements and microscopic pictures of the probe from various perspectives. The probe is excited by a HFSS lumped port at the k-connector. The S_{11} of the antenna when simulated in presence of the probe is seen in Fig. 10(b) to reduce by about 1.5GHz. The SOLT calibration that we adopted in our measurements, is also seen to introduce additional measurement discrepancies between the probe tip and the antenna feed structure [41]. These discrepancies vary between specific probes and Device-Under Test (DUT). Some other challenges related to measurement of mmWave antennas are reviewed in [42]. Therefore, typically at mmWave frequencies a few fabrication iterations are necessary to match simulation with measured results. Furthermore, it can be also noticed that the slightly longer feed in Conf 2 and Conf 3 provides a better match as can be inferred from the simulated reflection coefficient in Fig.4, where it is about 2dB lower than Conf 1.

Also, the −10dB bandwidth of the fabricated antennas in Conf 2 and Conf 3 are about 6.5GHz. Here, fabricated antennas in Conf 1 have a reflection coefficient higher than −10dB, so in this case 7dB bandwidth is considered which comes out to be about 10GHz.

Furthermore, transmission coefficients (S_{21}) between ANT O and other antennas ANT A, B, C & D in all configurations in multi-chip system are measured between 20GHz to 30GHz and plotted in Fig. 11 when the chip boundaries are 10mm apart. Transmission between ANT B and ANT O in Conf 1 cannot be measured due to constraint in the movement of probe arms. All the measurements show that there is sufficient transmission between antenna pairs which varies from −35dB to −60dB at resonant frequency 25GHz.

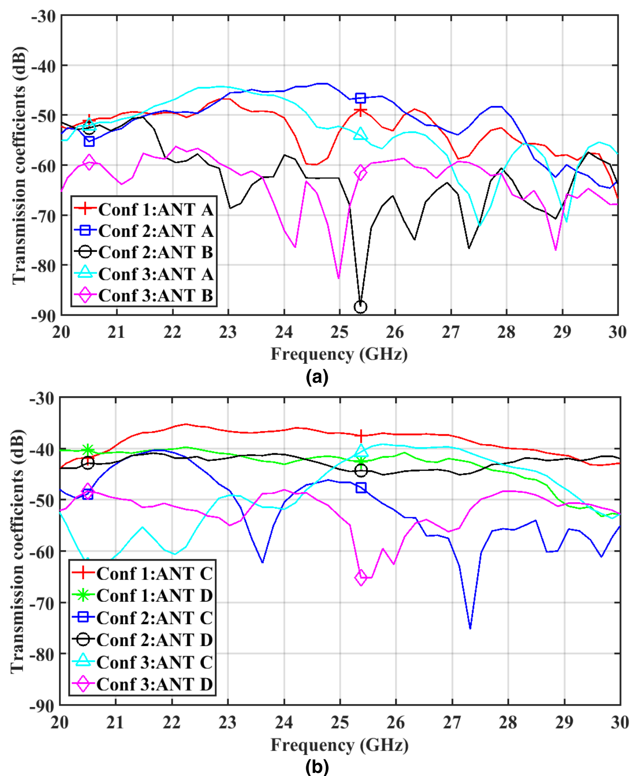


FIGURE 11. Transmission coefficients (S_{21}) for ANT A & B (a), and ANT C & D (b) relative to ANT O in all configuration when the distance between chip is 10 mm. Note: ANT B in configuration 1 is not measured due to constraint in movement of probe arms.

For intra-chip transmission, ANT C & ANT O in Conf 1 as shown in Fig. 11(b) has maximum transmission. As expected, the intra-chip transmissions are more than the inter-chip transmission by about 10dB. Similar to the simulations, the antenna B in Conf 2 and 3 shows dips in transmissions from 20 to 30GHz frequency interval due to low field distribution.

The transmission measurements with respect to ANT O also show that some antennas like Conf 3:ANT D, Conf 2:ANT B and Conf 3:ANT B have dips around the resonant frequency of 25GHz. These dips in transmissions are the result of multi-paths involved in propagation. This shows that the reflection from ground plane and structure of chip change the transmission due to reflections.

C. LARGE-SCALE CHANNEL MODEL FOR INTER-CHIP COMMUNICATION IN MULTI-CHIP SYSTEMS

In this section, we derive parameters of large-scale channel modeling for inter-chip wireless communication links, which can be used to evaluate path losses for inter-chip communication systems. Large-scale channel model is required to predict the required transmit power for specific SNR of received signal in a communication system. This will enable the development of design rules for transceiver circuits and overall interconnection architecture regarding antenna placement and orientation. Generally, the large-scale channel according to the log-normal model [43] is given by:

$$PL\,(d)|_{dB} = PL(d_0)|_{dB} + n \times 10\log_{10}\left(\frac{d}{d_0}\right) + X_\sigma \quad (1)$$

where $PL(d)|_{dB}$ is the average path loss at a distance d relative to path loss $PL(d_0)|_{dB}$ at a close-in reference distance d_0, n represents the path-loss exponent, and X_σ is a zero-mean Gaussian random variable with standard deviation σ denoting the attenuation (in dB) caused by shadowing. For channel modeling, we have chosen frequency range from 20GHz to 30GHz based on the operating range of the antennas. The VNA is calibrated in this frequency range. This range is ultra-wideband (UWB), so the channel characteristics are a function of frequency and distance between antennas. Therefore, the average transmission across the frequency range is used to find channel characteristics as a function of distance [44]. Furthermore, the reflection coefficients (S_{11} and S_{22}) of antennas is about −10dB. So, to remove the losses due to the reflection from antenna, the measured transmission coefficients, S_{21}, are processed using the transmission coefficient, G_a:

$$G_a = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad (2)$$

In our model, G_a is used as path loss between the antennas. Moreover, the channel under investigation for multi-chip system is considered as a time-invariant due to absence of relative motion between the chips in a multi-chip system.

Generally, for indoor and outdoor environments large-scale channel models indicate the path loss in the channel only, so, it should not depend on the antenna or the transmitted power level. Unlike in free space, where the simplicity of Friis' equation to evaluate a reference path loss can be used, inter-chip channel modeling depends on the on-chip antennas. The fabricated on-chip antennas are not in a free-space environment and the rigid structure of fabricated on-chip antenna adds constraints to performing measurements. In this way, the channel model becomes dependent on antenna design and the structure of chip. Therefore, for inter-chip channel modeling we measure the transmission between antennas at a specific distance (or shortest distance possible) and use that as a reference in (1). In this paper, the reference distance (d_0) between fabricated antennas ANT A and ANT O is considered to be 40mm by placing the chips 10mm apart. For ANT B and ANT O, the reference distance is 42.42mm by placing chips adjacent to each other that is zero millimeter apart.

As discussed in previous section, the multi-chip systems use a substrate which, in our case, is an organic substrate, namely FR4. The fabricated silicon chips are mounted on top of the FR4 substrate. Here, FR4 substrate has no ground plane of its own so the metal chuck of probe station would work as the ground plane. The arrangement of chips on FR4 along with probes is shown in Fig. 12. A pair of antennas is identified on two different chips. Keeping the distance between the two antennas constant, the chip pair is moved to

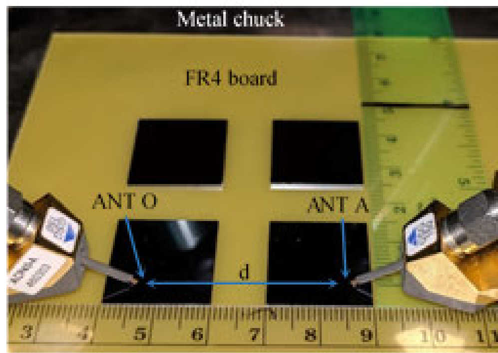


FIGURE 12. Measurement setup for path loss measurement. The silicon chips are placed on FR4 board at different distances. *d* is the distance between antennas.

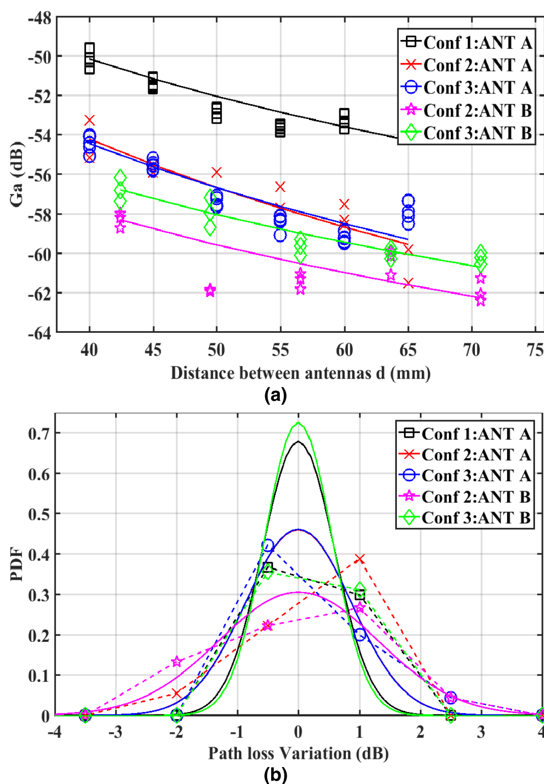


FIGURE 13. (a) Measured path-loss for fabricated dies with ANT O as reference fitted to a Log-Normal distribution. (b) Probability density function (PDF) of path loss variation.

different locations on the FR4 board and corresponding inter-chip transmission measurements are made. A sequence of such measurements are made for different distances between the chips and hence the antennas. After these measurements are post-processed with (2), the measured average path loss as a function of distance between the antennas is plotted and shown in Fig. 13(a). Inter-chip transmission measurements are restricted to a distance of 75mm between the antennas due to the size of metal chuck of the probe station. Curve-fitting is performed on the measured average path loss to extract parameters required for modeling by (1). The derived model parameters are shown in Table 2. The measured path loss

TABLE 2. Modeled parameters for different configurations and orientations.

PL with respect to ANT O	d_0 (mm)	$PL(d_0)$ (dB)	n	σ (dB)
Conf 1: ANT A	40	-50.13	1.95	0.587
Conf 2: ANT A	40	-54.19	2.53	0.866
Conf 3: ANT A	40	-54.42	2.30	0.863
Conf 2: ANT B	42.42	-58.29	1.78	1.304
Conf 3: ANT B	42.42	-56.76	1.77	0.550

model shows that the path loss exponent in case of inter-chip transmissions is close to 2, which is the path loss exponent for free space. This suggests that dominant propagation path is free space in inter-chip communication.

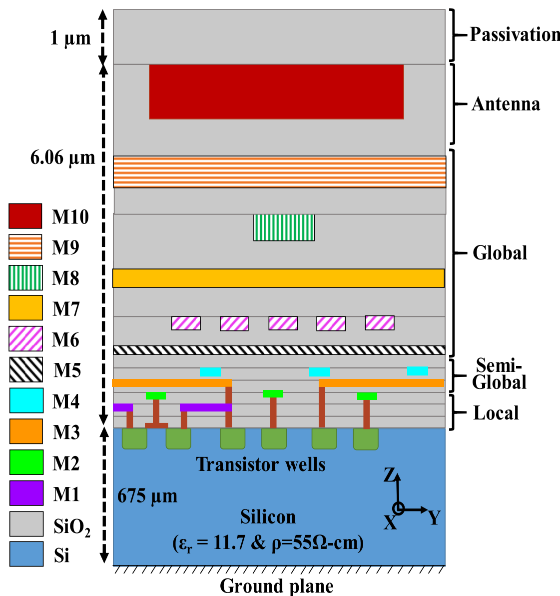
Moreover, the variation in path loss as the pair of chips are placed in different locations on the FR4 substrate is modeled by X_σ. The probability density function (PDF) for modeling X_σ based on experimental measurements is shown in Fig. 13(b). As can be seen, the path loss variation is restricted to -2dB to $+2$dB around the model estimate. However, the standard deviation is a maximum of 1.3dB while in most cases it is less than 1dB signifying low shadowing effects at the antenna locations. The case of maximum standard deviation is for ANT B and ANT O in Conf 2. With the parameters provided in Table 2, the path loss model from (1) can be used to measure the path loss at other distances between similar antennas in similar multi-chip systems. A similar methodology can be adopted for channel modeling at other mmWave frequencies such as 60GHz. This analysis will be useful in estimating path loss and establishing link budget for specific architectures depending on antenna orientations and placement.

D. ON-CHIP ANTENNAS IN THE 60GHz BAND WITH METALLIC WIRES

Following our studies with 30GHz antennas, we investigate 60GHz antennas as they will occupy smaller footprints in dense processor chips. However, in real chips, particularly in large multi-core processors, millions of copper interconnects are present in the silicon dioxide layers. We know that the metal objects influence the propagation of electromagnetic waves and if the metal objects are placed near the antenna, the objects influence the antenna's properties like resonant frequency, bandwidth and radiation pattern. In this section, we first model numerous metallic wires into structures that can be used for practical simulations and then evaluate and analyze 60GHz on-chip antennas in their presence.

1) MODELING OF ON-CHIP METALLIC WIRES

General process of fabricating the transistors, resistances and other devices except metal interconnects on silicon is referred to as front end of line (FEOL). The other part of fabrication which is depositing metal interconnect with insulating layers and bonding contacts is referred to as back end of line (BEOL). As an example of metal



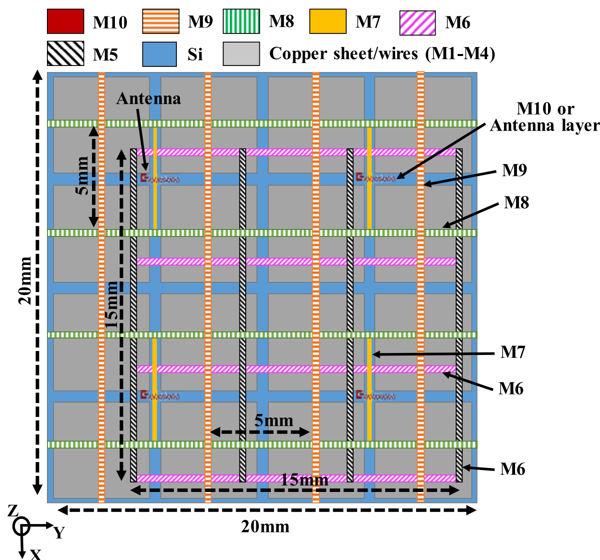


FIGURE 14. (a) Side view of the chip showing the copper interconnects in SiO_2 layer, (b) top view of the multi-core chip.

interconnects fabricated using BEOL, the side-view of a die with ten layers of metal interconnects (M1-M10) including the top layer used for the antenna is shown in Fig. 14(a). The dimensions of interconnects of different layers along with its use are shown in Table 3. Each layer is separated by an interlayer dielectric (ILD) such as silicon dioxide (SiO_2) which acts as an insulating layer. Generally, the thickness of ILD of a layer is equal to its corresponding thickness of metal layer. Modern processes use copper as the choice for fabricating wires due to its better conductivity compared to previously used aluminum. In this section and later, copper wires/interconnects and metal wires/interconnects are used interchangeably. Moreover, the copper interconnects are laid down according to Manhattan architecture [45] that is, wires

TABLE 3. Dimensions for wires in different metal layers. East, West, North and South are abbreviated as E, W, N, and S, respectively.

Layer	Width (µm)	Thickness (µm)	Layer Description
M10	-	1	ANT
M9	2	0.5	VCC/GND
M8	2	0.5	VCC/GND
M7	1	0.35	CLK
M6	0.1	0.3	NoC (E-W)
M5	0.1	0.3	NoC (N-S)
M4	0.05	0.02	E-W
M3	0.05	0.02	N-S
M2	0.05	0.02	E-W
M1	0.05	0.02	N-S

in each consecutive layer are laid in an orthogonal manner with respect to each other.

In modern BEOL, the interconnects are divided into three tiers: local, semi-global and global as shown in Fig. 14(a) depending on the length of interconnect and devices it connects. Global interconnects are used for power supply, clock signals or long-range communication. Due to their relatively long lengths, their cross section is wider than the other tiers to reduce resistance. In this work, we have considered metal layers (M5-M10) belonging to the global tier. The NoC metal interconnects which connect the processing cores in a multicore chip are designed using M5 and M6. In our work, we model the NoC architecture as a 2-D Mesh topology [46] as it is relatively easy to design, verify and fabricate due to its repetitive nature and is hence, chosen in hybrid wired and wireless NoC based systems [12]. Usually, NoC wires will be multi-bit (or wire) bus which are fabricated side by side, so to reduce the mesh size in HFSS the bus is considered as a single thick copper wire. We consider each multi-core chip to have 4 x 4 equal-sized cores (4.5mm x 4.5mm each) in a 20mm x 20mm die with the mesh links connecting each core to its cardinal neighbors. M7 is used for an H-Tree based clock network as it is known to reduce clock skew [47]. M8 and M9 are used for the power and ground supply straps [48]. Second, the semi-global tier is used for inter-block communications within a processing core spanning shorter distances compared to the global wires. M3 and M4 are considered to belong to the semi-global tier and are used to connect adjacent circuitry within a block or core. Lastly, local tier of interconnects which connect the transistors within a unit or cell. Local interconnects are very short and narrow. Usually M1 and M2 layers, which are in the local tier, are employed for connecting neighboring transistors. The various wired interconnects in the metal layers are shown in Fig. 14(b). The M1-M4 layers are so dense that they are shown as a grey box in the figure. Further, we will show that the wires in the M3 and M4 layers which are of the form an unbounded grid like structure, can be replaced by a copper sheet at M4 layer for simulation purposes as we explain next.

Typically, the wire interconnects in the M3 layer are orthogonal to the wires in M4 layer in order to reduce crosstalk among wires in adjacent layers by following what is known as Manhattan architecture [45]. In order to model these multiple layers of metallic interconnects, we can consider that they form a very large unbounded grid-like structure of the size of a processor core. This large grid-like structure is impossible to simulate in ANSYS HFSS due to colossal mesh size and computational cost especially, at carrier frequencies of 60GHz. Therefore, to simulate the effect of semi-global interconnects on the transmission between wireless interconnects in a multi-chip system, a simplified model is required which can emulate its effects. The aim of the following simulations is to show that the loading effects of a copper grid and of a copper sheet, on the antenna are equivalent. Using this equivalent model, for simulation, the effects of copper wires in a multichip multicore system can be analyzed. Before using the model, we prove that the effect of a copper grid of interconnects on the antenna is equivalent to that of a copper sheet through the following simulation.

A small square area partially including the wire grid area inside each of the four cores around an antenna is simulated with a zigzag antenna. It is a small 1.4mm x 1.4mm area around one of the antennas shown in Fig 14(b) along with the small portions of surrounding copper sheet. The copper sheet represents the copper grid formed by M3 and M4 layers. Generally, the pitch of these wires vary from about 0.15μm in modern technology nodes (smaller than 65nm technology) to about 0.5μm or more in older technology nodes (larger than 65nm nodes). However, such dense and fine-grained structures are beyond the simulation capabilities of our tools. Hence, the minimum pitch of the grid considered here is 70μm.

In Fig. 15 (a), a zigzag antenna with a length of 405μm is placed in antenna layer which is the M10 layer (as shown in Fig. 14(a)) and on top of a grid of interconnects with spacing of 70μm corresponding to the M3 and M4 layers of thickness 0.02μm. The wires in M4 layer are orthogonal to the wires in M3 layer. The thickness of silicon and silicon dioxide is 675μm and 7μm, respectively. The size of the simulated area is 1.4mm x 1.4mm. Structures such as ground plane at the bottom of silicon and other interconnects are removed for this analysis to model the effect of the wires only. In another simulation, the grid of wires is replaced with a copper sheet at M4 layer with same thickness of 0.02μm (figure not shown). Also, a simulation is performed with just the antenna on silicon and without the grid or sheet. The results from the third simulation are used as reference to compare the previous two simulation (of grid and sheet). The simulated S_{11} of the three cases are shown in Fig. 15(b). It can be seen that the shift in resonance of antenna with grid and the sheet is the same, though there is a 3dB difference in magnitude of S_{11}. It can be concluded that the grid and sheet have the similar loading effect in terms of resonant frequency.

In Fig. 16(a), the zigzag antenna is surrounded by four copper grids. Each of these grids is identical to the one in Fig. 15(a) where it was placed directly below the antenna. This arrangement is representative of the structure described in Fig. 14(b) with spacing between the cores, except the

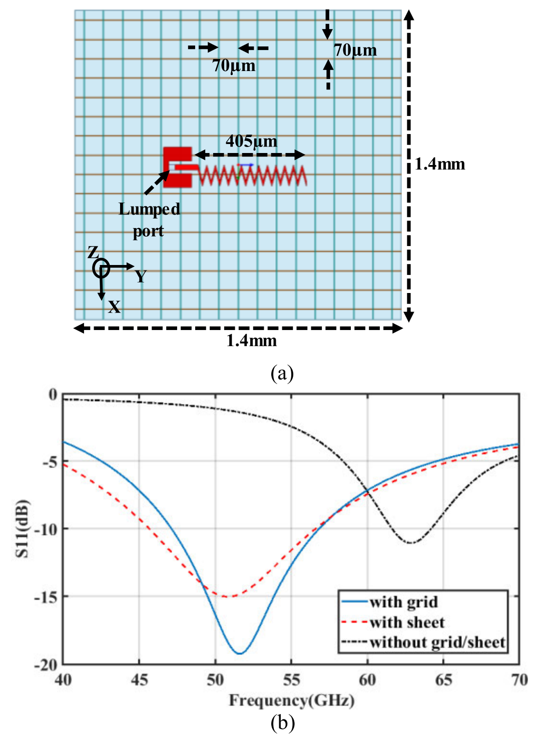


FIGURE 15. (a) Top view of copper grid (M3-M4) under an on-chip antenna, (b) plot of S_{11} with grid, with sheet, and without grid & sheet.

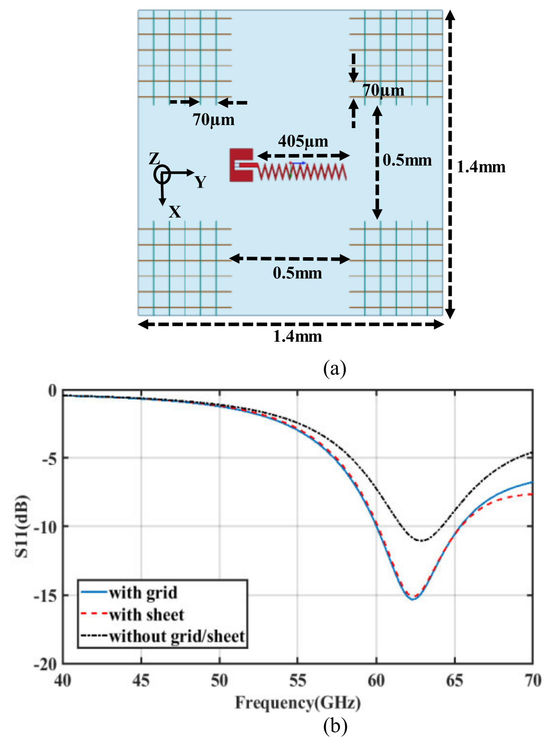


FIGURE 16. (a) Top view of copper grids (M3-M4) beside the on-chip antenna, (b) plot of S_{11} with grid, with sheet, and without grid & sheet.

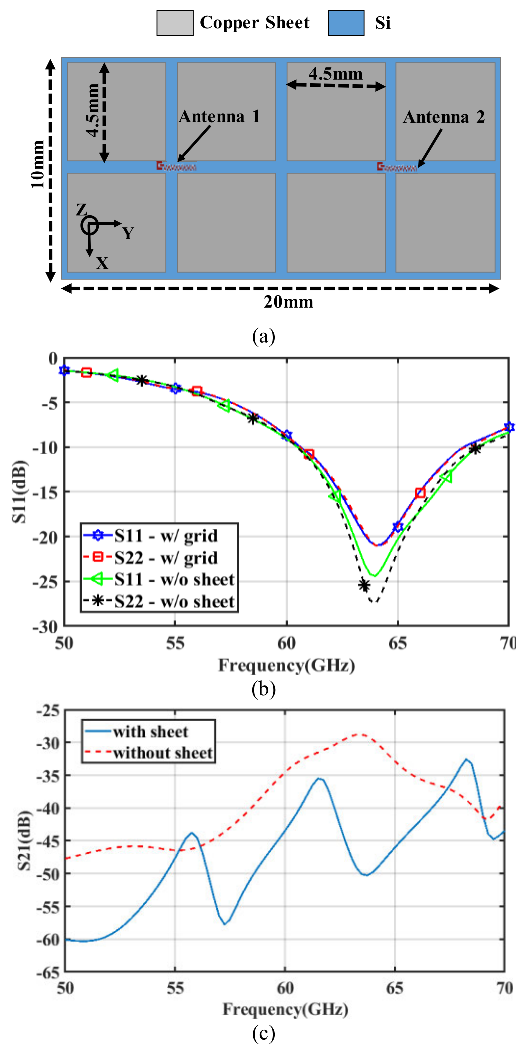
ground plane at the bottom of the chip. In Fig 16(b), the S_{11} is shown which indicates that there is very little to no effect on the resonant frequency of the antenna. The difference of about 4dB in the magnitude of S_{11} can be noticed from Fig. 16(b). Similarly another simulation is performed by replacing the grid structure with a sheet of copper, and the results are shown in Fig. 16(b). The S_{11} plot with copper sheet overlaps with the S_{11} plot with copper grid. This shows that the effects of both the grid and sheet are equivalent for the case where antenna is surrounded by the grid with spacing between the individual sheets. As the pitch of the wires here are considered to be 70μm in this model, it can be concluded that a finer pitch resembling those in modern fabrication technologies will also behave similarly and can be modeled as a copper sheet.

Having established the equivalence of copper grid with a copper sheet in terms of S_{11}, the effect of the sheet in the M4 layer on the transmission characteristics in terms of S_{21} is analyzed. In Fig. 17(a), a small chip with 2x4 cores is shown where the copper grids are replaced by copper sheets, and the ground plane at the bottom and other interconnects are removed. The antenna is the same as used in above cases. The magnitude of S_{11} and S_{22} are shown in Fig. 17(b). The S_{11} for all cases is below -20dB with the antenna resonating at 64GHz. In Fig. 17(c), the S_{21} plot is shown in a system with and without the interconnect model (as copper sheet). Unlike in the system without interconnect models, the transmission between the antennas with interconnect models have dips even as the antenna is resonating at 64GHz. This shows that the transmission between antennas is dependent on the existence of the metallic interconnect model. In Fig. 17(d) and (e), magnitude of electric field is plotted at 65GHz in HFSS. As shown in Fig. 17(b) the S_{11} and S_{22} at 64GHz have worsened by 3.5dB and 6.5dB in the presence of the metallic plane. In addition, as can be seen in Fig. 17 (c), S_{21} reduces by about 15dB at 64GHz. Further, radiation efficiency of the antenna with grid and without grid (Figs 17(d) and (e)) is 8% and 19% respectively due to destructive interference with the antenna radiation.

The electric field plots show significant effects of the copper sheet on electric field propagation supporting our inference above. Based on the results in Fig. 17, we can infer that the S_{21} differs significantly in presence of metallic interconnect model compared to a scenario where they are not present. Moreover, orthogonal wires in adjacent metal layers on a chip, which require advanced and expensive fabrication processes, can be modeled as a continuous sheet due to similar impact on antenna characteristics. Therefore, in the next section, similar strategy is implemented for simulating an MCMC system.

2) 60GHZ TRANSMISSION ANALYSIS IN PRESENCE OF METAL INTERCONNECTS

The interconnect model (as copper sheet) described above is used in the simulation performed here. In addition to the copper sheet modeling M1-M4 layers, other metal layers (M5-M10) are also considered here. The dimensions of the length, width and thickness of copper wires is shown in Fig. 14 and Table 3. As discussed earlier that NoC bus is usually multi-wire bus, but for simulation purposes to reduce the computational demand, the NoC bus is considered as a single thick wire. The chip along with copper interconnects is replicated into four chips and placed on FR4 board ($\varepsilon_r = 4.4$ and $\tan(\delta) = 0.02$) of thickness 1.575mm. Fig. 18(a)



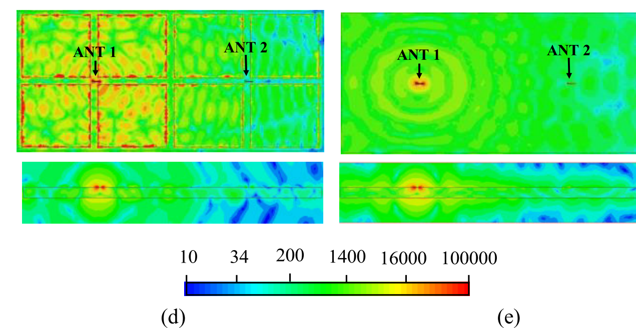


FIGURE 17. (a) Top view of the2x4 multicore chip with 8 copper sheets and two antennas, (b) plot of S_{11} and S_{22} of antennas, (c) plot of S_{21} between antennas, (d) and (e) magnitude of electric field (V/m) at the plane of antennas in two scenarios that is with copper sheets and without copper sheets.

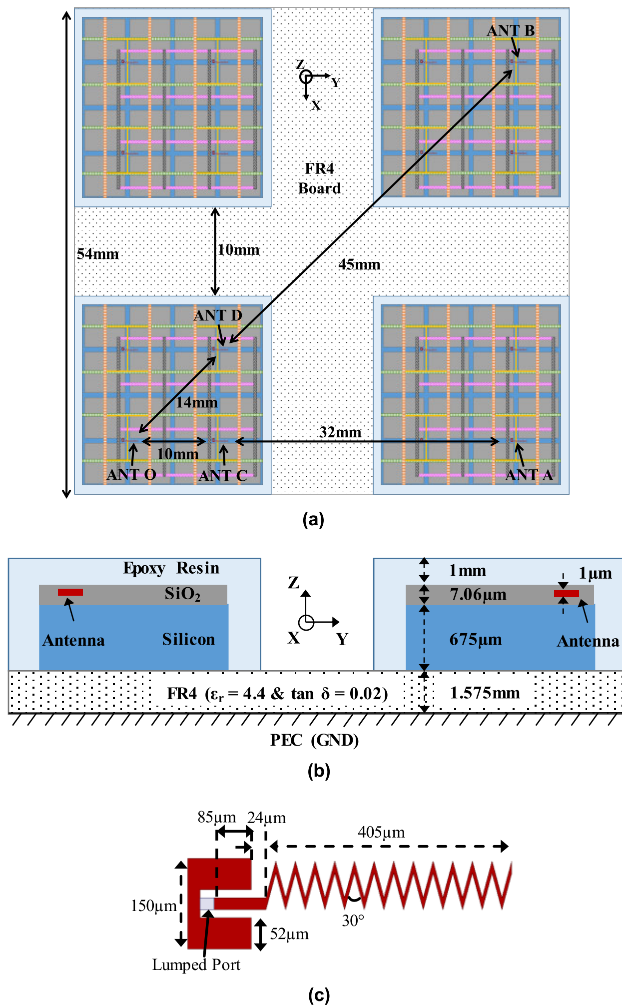


FIGURE 18. (a) Top view of the multichip system (Note: Distances are measured from the center of the antenna), (b) cross-sectional view of the multichip system, (c) zigzag antenna used at 60GHz.

shows the arrangement of the multichip system. The spacing between the chips is 10mm. Moreover, the chips are coated with an epoxy resin layer of 1mm. Epoxy resin ($\varepsilon_r = 2.9$) is commonly used to cover the silicon chip for protection and robustness. The side view of the chip is shown in Fig. 18(b). The antenna used for transmission analysis is shown in Fig. 18(c) which is a zigzag antenna modeled at the M10 layer shown in Fig. 14. Now, there are four antennas on each chip that is a total of 16 antennas in a four-chip system.

To analyze the transmission between these many antennas will be complicated. Therefore, only five representative antennas are selected for analysis. The antennas under analysis are shown in Fig. 18(a). These antennas are selected because they include the expected worst cases that is farthest antenna pairs for intra- and inter-chip pairs. A common antenna ANT O is chosen as a reference. Two antennas ANT A and ANT B are selected to form inter-chip pairs with ANT O. Here, ANT B and ANT O are the farthest apart. The Two other antennas ANT C and ANT D are selected to form intra-chip pairs with ANT O as they are on same chip. The distance between antennas are shown in the Fig. 18(a).

Simulations of the multichip system with interconnects (WI) and without interconnects (WOI) are performed in ANSYS HFSS. It should be noted that the WOI case still has FR4 board, bottom ground plane and epoxy resin. The reflection coefficient and transmission coefficients are plotted from frequency 50GHz to 70GHz. Fig. 19(a) shows reflection coefficient (S_{11}) in both cases. It should be noted that though the same antenna is used in previous analysis while showing equivalence between grid and sheet, the antenna in Figs. 15 and 16 has different S_{11} characteristic with no grid or sheet from the S_{11} - WOI case in Fig. 19(a) due to the absence of FR4 board, bottom ground plane and epoxy resin. In presence of copper interconnects the antennas resonate at 60GHz as shown in Fig. 19(a). However, when all copper interconnects and copper sheets are removed, the resonant frequency of antennas shifts to about 61GHz. Moreover, the magnitude of reflection coefficient drops showing an impedance mismatch. This shows that the design of mmWave on-chip antennas requires the knowledge of the layout of the copper interconnects.

Transmission between antennas are analyzed for inter-chip and intra-chip pairs and shown in Fig. 19(b). For the inter-chip antenna pairs the transmission coefficient can be seen to vary between −60 to −85dB with copper wires. This is lower than the transmission coefficient without copper wires by 20dB for antenna pair ANT A & O. Moreover, for intra-chip pairs, the transmission coefficients with copper wires varies from −40dB to −50dB. Significant difference can be seen for antenna pair ANT D & O in presence and absence of metal interconnects. The transmission between ANT D & O is about −50dB with copper wires and about −40dB without copper wires. This shows that the copper wires can significantly change the transmission between on-chip antennas.

Furthermore, the radiation pattern of the antenna is shown in Fig. 19(c). The electric field distribution is also provided with and without the presence of copper wires in Figs. 19(d) and 19(e), respectively. It shows that the distribution is affected by the M3 and M4 layers, which are modeled as copper sheets, when compared with the field distribution without the copper wires. Overall, generally neglected copper interconnects are seen to affect the resonant frequency and transmission coefficients between on-chip antennas. Therefore, appropriate consideration must be given to the metal interconnects when designing on-chip antennas.

E. ON-CHIP ANTENNAS IN THE 60GHZ BAND ON A TWO-CHIP MULTIPLE CORE FLIP-CHIP PACKAGE

Modern processors use Flip-chip Ball Grid Array (FCBGA) and Flip-chip Land Grid Array (FCLGA) [49]. In Flip-chip technology, the chip is flipped on top of a substrate which can be an organic, ceramic and Polytetrafluoroethylene (PTFE). In such processors the heat sink is separated from the chip by a heat spreader which provides a larger surface area for heat extraction [49]. In this section, we present the transmission characteristics of the antennas discussed in this paper in processor environments with flip-chip packaging and

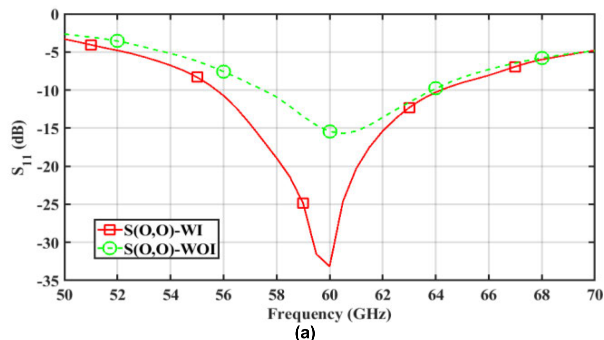
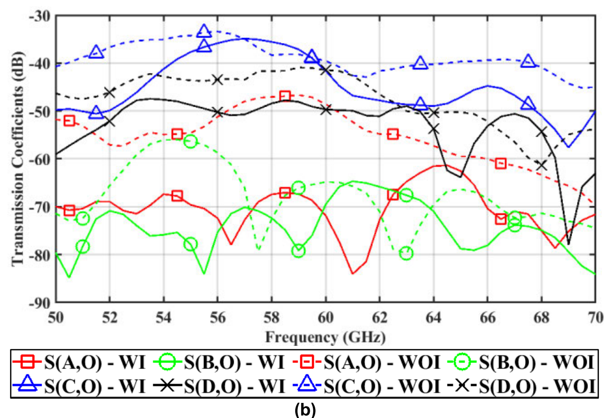
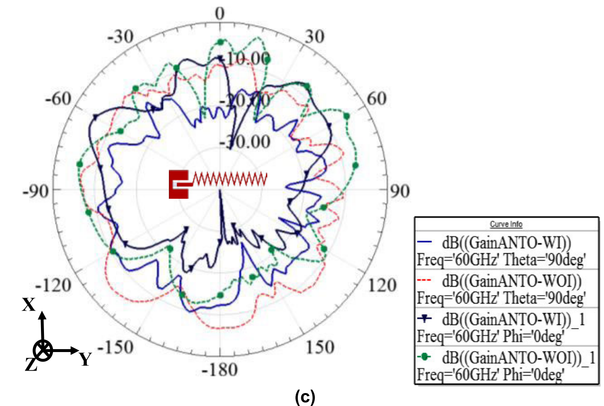
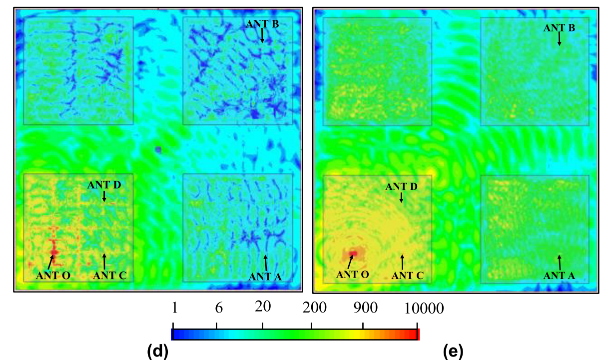





FIGURE 19. (a) Reflection coefficient (S_{11}): WI = with interconnects, WOI = without interconnects, (b) transmission coefficients, (c) radiation pattern of ANT O in XY plane. Magnitude of E-field (V/m) at M10 layer height when ANT O is excited at 60GHz (d) with and (e) without interconnects.

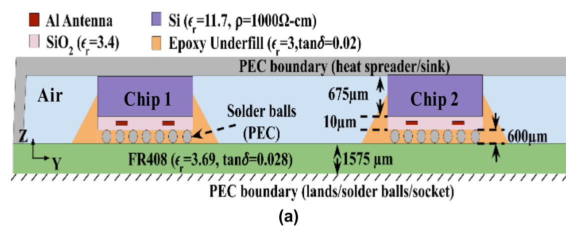
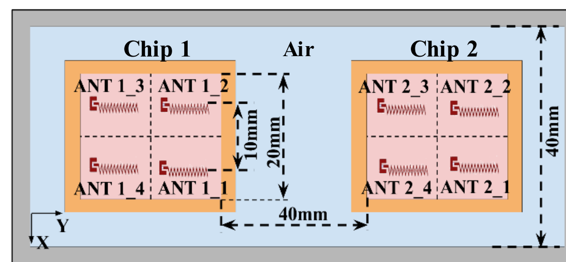
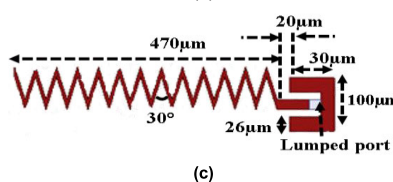
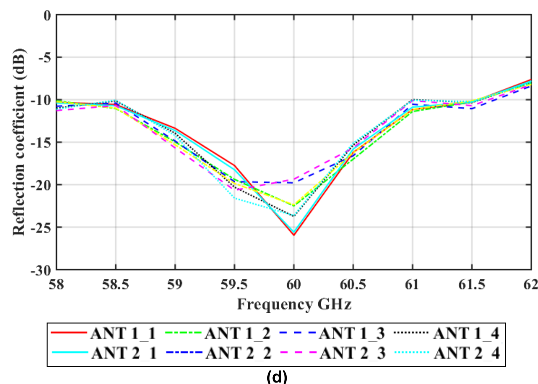
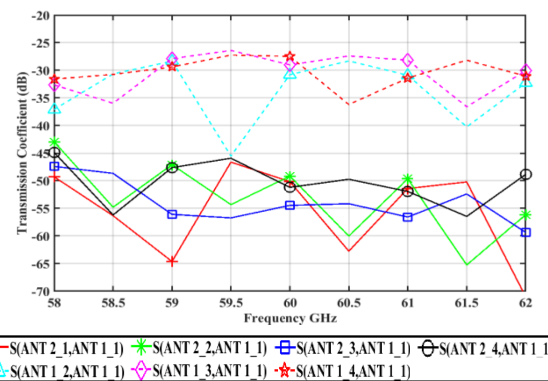






FIGURE 20. (a) Cross-sectional view of the multichip system (not to scale) [50], (b) top view of the multichip system, (c) zigzag antenna used at 60GHz, (d) S_{11} responses for all antennas, (e) intra- and inter-chip transmission coefficients between antenna pairs in the system.

heat spreader. The four antennas are placed in the center of four equally divided quadrants on a 20mm x 20mm silicon chip [50]. The cross section of package adopted from Intel Xeon [49] is shown in Fig. 20(a). The top-view is presented in Fig. 20(b). The optimized antenna is shown in Fig. 20(c). Two PEC boundaries are considered here – one for heat spreader cover and another is for lands/solder balls/metallic

processor loading mechanism as shown in [49]. Dielectric constant and loss tangent for the structure has been acquired from [51]. The diameter and pitch of solder balls is 0.6mm and 1mm, respectively. The number of solder balls in grid array is 364.

Due to the complexity of the system discrete frequency sweep at intervals of 0.5GHz is simulated. The S_{11} for all eight antennas in the system are shown in Fig. 20(d). The transmissions between ANT1_1 in chip 1 and all other antennas covering intra-chip and inter-chip pairs are shown in Fig. 20(e). It can be observed from Fig. 20(e) that at 60GHz the intra-chip transmission coefficients between the antenna pairs are around −30dB. On the other hand, the inter-chip transmission at 60GHz between the different pairs of antennas ranges from −50dB to −55dB. This trend is similar to the packaging configuration studied in the previous subsection where the transmission (between ANT A and ANT O) without considering the wires (WOI case in previous subsection) in Fig 19(b) is also around −50dB at the resonant frequency.

V. CONCLUSION

The paper presents transmission characteristics of on-chip antennas for inter-chip communication in multi-chip systems. Through simulation at 30GHz, we have characterized the inter-chip transmission, and studied the electric field distribution to explain the transmission characteristics. The simulation results have been validated with fabricated antennas in different orientations on silicon dies, that can communicate with inter-chip transmission coefficients ranging from −45dB to −60dB while sustaining bandwidths up to 7GHz. Our fabricated antennas show a shift in resonance to 25GHz. In order to investigate the reasons for this shift we modeled the probe structure to study its impact. On including the probe in our simulation model the resonant frequency was found to shift by 1.5GHz. The SOLT calibration that we adopted in our measurements, is also seen to introduce additional measurement discrepancies between the probe tip and the antenna feed structure. It is shown that the antenna radiation efficiency reduces with decrease in the resistivity of silicon that results in increased losses. Using the experimental measurements, a large-scale, log-normal channel model is derived, which can be used for system level architecture design. In most cases, the shadowing effect remains below 1dB. We have designed on-chip antennas and studied them at 60GHz in the presence of densely packed multilayer copper wires typical of NoC based multicore processors. Dense wires have been shown to be equivalent to copper sheets and modeled as such, to reduce the complexity of simulations. Using this interconnect model, reduction in inter-chip transmission is obtained as much as 20dB. In presence of densely packed metallic wires in close proximity to the antenna is shown to reduce its radiation efficiency by about 11%. Furthermore, we found the intra- and inter-chip transmission characteristics of these antennas to be similar in a flip-chip packaging environment, indicating their suitability for such a technology as well.

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