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An Algorithmic Framework to Construct Optical Switch via Scaling From N-to-2N Ports for Optical Network on Chip

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ABSTRACT Optical network-on-chip (ONoC), designed with non-blocking optical switches, is gaining a significant research attention to meet the upcoming requirements of higher throughput, larger bandwidth, lower latency, and reduced power consumption for manycore processors. In this paper, we propose an algorithmic framework to construct non-blocking optical switches with multiple interconnection possibilities. The design is accomplished by scaling the optical switch from N-to-2N ports using two intermediate mapping matrices each of size $2N \times 2N$. These mapping matrices are the row and column permutations of identity matrices, where 1's represent passive interconnections among the optical switching units (OSUs). The proposed framework provides validation to the design by identifying all the non-blocking permutations of the mapping matrices, thereby, providing a flexibility to adopt any permutation as an interconnection scheme. Furthermore, it has the ability to quantify the redundancy in switching combinations which exists for any input-to-output routing, authenticates the non-blocking feature of the optical switch and to reduce the number of optical switching units while preserving the non-blocking characteristic. For the scaled 4×4 and 6×6 optical switches, we respectively identified 16 and 192 different interconnections to build multiple non-blocking switches. Moreover, a 20% reduction in OSUs is achieved by optimizing a 6×6 switch. The influence of the insertion loss, power consumption, and crosstalk noise on various scaled optical switch networks are also analyzed and compared with several existing optical switch topologies.

INDEX TERMS Optical network-on-chip (ONoC), optical switch, optimization, scalability, silicon nanophotonics.

I. INTRODUCTION

In the past decade, demand for computationally intensive applications has increased which leads to the evolution of manycore era. Requirements of the on-chip parallel processing can be fulfilled with network on chips (NoC) in manycore processors [1], [2]. Optical network on chip (ONoC) has progressed as a feasible replacement of electrical NoC which can provide superior network performance [3], [4]. Design of optical switch (OS) is an important aspect for ONoC, where optical switching units (OSUs) provide routing of data from the input to the output (I/O) ports. As the radix of network increases, OSU count also increases which leads to higher latency, poor power consumption and insertion loss [5]. Scalability of high radix optical switch, designed for high performance applications, requires special design considerations to alleviate the intrinsic characteristics of insertion loss, crosstalk noise and power consumption in optical on-chip interconnects.

Increase in switching units also affects the complexity and footprint of optical switch [6]. Optimal number of OSUs and their configuration can reduce overall crosstalk noise, insertion loss and power consumption for the optical switch [7]. Several non-blocking architectures based on different network topologies have been proposed in literature

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i.e. Spanke-Benes (SB) [8], Benes [9], double layer network (DLN) [10], clos [11], switch and select (S&S), cross-point switch matrix (CSM) [12] and path independent loss (PILOSS) [13]. Spanke-Benes is a N-stage non-blocking switch architecture based on $N(N\text{-}1)/2$ number of switching units to construct $N \times N$ port switch [8]. Benes network is a rearrangeable non-blocking architecture with $((2\log_2 N)\text{-}1)N/2$ OSUs for $N \times N$ port switch [9] (details of different topologies are provided in Section V). Design of an optical switch based on aforementioned non-blocking architectures, with minimal number of switching units, needs optimization of OSUs. Several schemes are adopted to construct optical switch with optimal number of switching units and different methods are proposed to optimize the number of OSUs [14]–[20].

Optimization of optical switch topology by substituting OSUs with waveguide crossings while maintaining non-blocking feature intact with reduced optical switching units is proposed in [14]. A universal scheme for construction of Microring (MR) based N-port non-blocking optical switch is proposed for different sizes in [15]. Another methodology for constructing a universal non-blocking N-port optical router for photonic NoC is proposed in [16] where MRs or Mach-Zehnder (MZ) based switch, works as a 2×2 optical switching element. A reconfigurable 5-port optical router based on eight OSUs that uses thermo optical tuning effect is proposed in [17]. Transfer matrix based simulation framework with modeling of a 4×4 non-blocking MZ optical switch which allows to calculate transmission spectra of any multistage switch is proposed in [18]. A mathematical theorem is presented in [19] to find the routing path in MR based Benes network which can reduce power consumption of switch network. Another approach to minimize computational time for optimal optical switch network using heuristics is proposed in [20]. However, optimization of optical switch along with scalability to meet future requirements of ONoCs requires a comprehensive framework which is lacking in previously proposed methodologies. Aforesaid methodologies does not provide a generic algorithmic scheme to construct an OS.

Higher port count of optical switches for high end application in future on-chip optical interconnects and large bandwidth communication applications are greatly anticipated [21]–[24]. For instance, high performance computers (HPC) require optical switching fabrics that can evade the limitations of power consumption and port count caused due to conventional interconnects [25]. From the perspective of ONoCs, cluster based Mesh ONoC needs 8 ports optical switch and Clos based ONoC requires 9 / 12 ports optical router at terminal and middle nodes respectively [16]. From that viewpoint, higher scale network are extremely desirable for future on chip interconnections [26]. The number of OSUs, per path OSU count and number of waveguide crossings are key factors that play critical role in insertion loss, crosstalk and power consumption of OS topology. For instance, Benes network requires fewer number of OSUs which consume lower power, however, first order crosstalk is unavoidable in this type of switch network [27]. Spanke-Benes network utilizes lesser OSUs with reduced first order crosstalk as compared to Benes network, however, requirement of per path OSUs is higher. DLN employs higher number of OSUs to achieve non-blocking feature with suppressed first order crosstalk. Therefore, it's a tradeoff between number of OSUs, per path OSU count and waveguide crossings that needs to be addressed during the design of optical switch network.

Motivated with the aforementioned requirements and demands, in this manuscript, we propose a comprehensive framework which not only constructs optical switch using scaling from any multistage $N \times N$ optical switch to $2N \times 2N$ optical switch network but also provides an algorithmic methodology to check the non-blocking feature and optimize the OSU count in optical switch with different interconnection possibilities. Switch topology designed using proposed framework provides a combination of reduced OSU count, number of OSU per path used and number of crossings. To the best of our knowledge, the proposed framework is most up-to-date approach that can scale any multistage network as well as provides optimization and verification of non-blocking property of optical switch. Before proceeding further, we list our major contributions in this paper as follows:

- An algorithmic framework is proposed that maps $N \times N$ non-blocking optical switch to a $2N \times 2N$ non-blocking optical switch to construct a higher order switch.
- We present, a set of algorithms for validation of switch topology construction with optimization to: identify the redundant switching combinations for a desired I/O mapping; verify the non-blocking feature of proposed switch network and utilized optimization procedure to substitute the OSUs with waveguide crossings while maintaining the non-blocking property of optical switch.
- In addition, an algorithm to find all non-blocking inter-connection possibilities that can provide multiple options to connect intermediate stages is also proposed. Hence, it allows flexibility for designers to select and choose between different parameters depending upon actual requirements e.g. reduced power consumption, insertion loss or crosstalk noise. Different permutations yield multiple non-blocking switch designs e.g. 16 and 192 different designs for $N = 4$ and 6 port optical switches respectively.

This paper proceeds as follows; Section II provides the details of mapping model and transfer matrix for 2×2 optical switch. Section III focuses on proposed framework for scaling methodology from $N \times N$ to $2N \times 2N$ optical switch and emphasizes on generalized scheme illustrated with the help of an example. Section IV furnishes with the details of proposed algorithms for intended optical switch networks. Simulations, experimental results and their detailed assessment are discussed in Section V. Finally, our conclusion along with future work is added in Section VI of this article. In later part of this article, we will use term optical switch, alternatively network

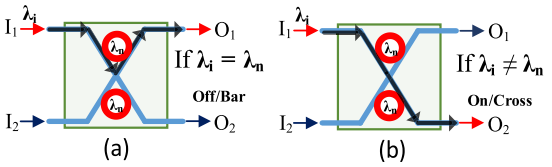


FIGURE 1. 2 × 2 OSU (a) 2-MRs based OSU Off / Bar state; (b) 2-MRs based OSU On / Cross state.

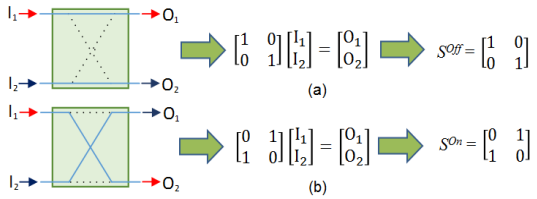


FIGURE 2. OSU matrix representation (a) Off / Bar state; (b) On / Cross state.

or topology for a whole or complete optical switch while term optical switching element or unit (OSU) for a basic 2 × 2 switching element.

II. OPTICAL SWITCHING UNIT AND MATRIX TRANSFORMATION

In this Section, we review the analytical model using matrices to define transfer matrix for a multistage optical switch architecture provided in [14]. Most common element used for optical switching consists of a 2 × 2 I/O pair. A 2 × 2 switch has two switching states; bar (off) and cross (on) states. Different types of OSU architectures are available, one of the type is based on MR optical switch, in which switching of MR depends upon the resonating wavelength. If the resonance of wavelength matches with the MR's respective wavelength, it means that signal propagates to respective output port, otherwise the signal is transmitted via other output port. Fig. 1 (a) and Fig. 1(b) show the MR based optical switch in "off" and "on" states respectively [7].

Non-blocking multistage network architectures consist of a basic 2 × 2 OSU. An OSU in either state can be analytically expressed in the form of 2 × 2 matrices as S_{Off} or S_{On} [14] as expressed in (1). Step wise pictorial transformation of 2 × 2 OSU to corresponding transfer matrices is shown in Fig. 2 [14].

$$S^{Off} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} S^{On} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{1}$$

Any $N \times N$ non-blocking optical switch network is composed of number of OSUs, straight or cross interconnects and waveguides that can be divided into K stages / columns [28] as shown in Fig. 3 [14]. Any particular stage of switch can be modeled by an $N \times N$ block diagonal matrix, which we will call as the permutation matrix for that stage. Each diagonal entry in matrix represents an OSU (S_{On} for on and S_{Off} for off), a straight interconnect or a waveguide crossing.

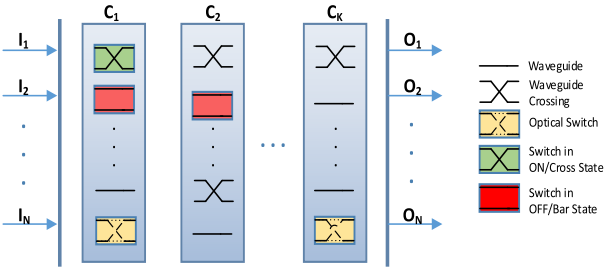


FIGURE 3. $N \times N$ Non-blocking stage wise division of optical switch network, C_1, C_2 ...C_K represents K stages of networks.

If we consider the k-th stage, then its permutation matrix is denoted by G_k [14] and is given by the following relation (2);

$$G_k = blk\_diag[\, S^{On/Off} \quad S^{On/Off} \quad \cdots \quad S^{On/Off} \,] \tag{2}$$

We call this as a permutation matrix because every permutation of input ports yields a different switching combination and hence a different matrix. To elaborate, we write down the permutation matrix for the stage C_1 in Fig. 3 as in (3)

$$\begin{aligned} G_1 &= blk\_diag\left[\, S^{On} \quad S^{Off} \quad \cdots \quad 1 \quad S^{On/Off} \,\right] \\ &= \begin{bmatrix} S^{On} & 0 & 0 & 0 & 0 \\ 0 & S^{Off} & 0 & 0 & 0 \\ 0 & 0 & \ddots & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & S^{On/Off} \end{bmatrix} \end{aligned} \tag{3}$$

where the straight interconnect has given a unity gain. Since the whole switch is divided into K cascaded stages [14], the permutation matrix of the complete switch, which we will call as transfer matrix and denote by T expressed in (4), can be obtained as the product of permutation matrices of individual stages i.e.

$$T = G_K G_{K-1} \cdots G_2 G_1 = \prod_{k=K}^{1} G_k \tag{4}$$

The over-all I/O relation is then given by the following expression (5);

$$O = TI \tag{5}$$

where $O = [O_1, O_2 \ldots O_N]^T$ and $I = [I_1, I_2 \ldots I_N]^T$ are length N vectors of I/O ports and $[.]^T$ represents the matrix transpose operation [14]. Depending upon the state of OSUs (on or off), the permutation matrix of each stage will have different values. This means that there exist more than one switching combinations that can yield the desired I/O mapping. In Section IV an algorithm, to identify all the switching combinations that are derived by the same transfer matrix, is proposed. This also manifests that there exists a redundancy in the switching states for multistage network architectures. For complete I/O mapping, an N-port non-blocking optical network with n number of OSUs requires $N!$ switching states where each switching state is mapped via unique permutation matrix [14]. Since there are 2^n, possible switching states, this implies that there exist 2^n - $N!$ redundant switching states.

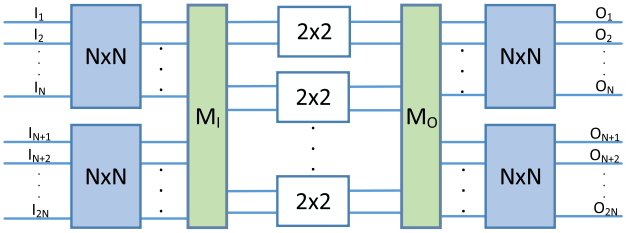
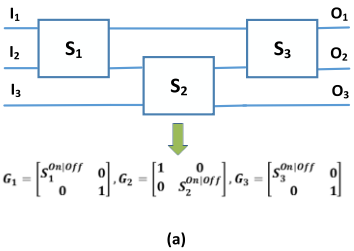


FIGURE 4. Block level architecture of proposed $2N \times 2N$ non-blocking optical switch.



I/O Mapping			Switching States		
O_1	O_2	O_3	S_1	S_2	S_3
I_1	I_2	I_3	0	0	0
I_2	I_1	I_3	0	0	1
I_1	I_3	I_2	0	1	0
I_3	I_1	I_2	0	1	1
I_2	I_1	I_3	1	0	0
I_1	I_2	I_3	1	0	1
I_2	I_3	I_1	1	1	0
I_3	I_2	I_1	1	1	1

FIGURE 5. (a) 3 × 3 Non-blocking optical switch with stage wise matrices G_1, G_2 and G_3; (b) Possible switching states and I/O mapping.

Hence, for the $N \times N$ optical network to be non-blocking there exists $N!$ different permutation matrices. Based on this concept we present another algorithm that verifies the non-blocking property of an optical switch. Since $2^n > N!$ for all $N > 2$, this redundancy in the network is intrinsic and cannot be completely eliminated. However, it can be minimized by reducing the OSU count. In Section IV we present an optimization algorithm to reduce the number of OSUs which results in reduced redundancy [14].

III. MAPPING FROM N × N TO 2N × 2N NON-BLOCKING OPTICAL SWITCH

In this Section, we present a mapping model to construct N port optical switch fabric using scaling from $N \times N$ to $2N \times 2N$ non-blocking optical switch. The block level architecture of the proposed mapping network is shown in Fig. 4, where the intermediate passive interconnects are connected based on interconnection matrices that provides non-blocking property for proposed switch. Multiple non-blocking permutation matrices are available that can be identified using our proposed Algorithm-4 in Section IV. The Fig. 4 shows that the proposed switch topology comprises of an input-stage (with two $N \times N$ switch networks), an intermediate stage with N 2×2 OSU and an output-stage same as input-stage. The middle stage connects input-stage OSUs to the output-stage elements in non-blocking fashion to construct an over-all non-blocking switch topology. For illustration, we have chosen one of the possible permutations that connect the top (bottom) inputs of each intermediate stage elements to outputs of the top (bottom) network of input-stage, thereby, making sure that each output from the input-stage gets routed in either cross or bar mode depending upon the switching state. A similar argument holds for routing the intermediate stage outputs to the output-stage inputs. Our proposed design consists of $N(N-1)/2$ OSUs with $K = N + 1$ number of stages for a $2N \times 2N$ optical switch.

To construct optical switch via proposed framework, we introduce two passive intermediate stages M_I and M_O, which provide mapping between the input side and output side as shown in Fig. 4. The matrices M_I and M_O are respectively the column and row wise permutations of the identity matrix and can be effectively computed by employing Algorithm-4 provided in Section IV. This algorithm is capable of identifying all the non-blocking interconnection possibilities for the OS constructed via proposed framework.

The algorithm works by first listing down all the $N!$ permutations of $N \times N$ identity matrix and then subsequently verifying the non-blocking property of the OS by inserting each permutation as M_I (column wise) and M_O(row wise).

As an example, we transform a 3×3 optical switch to a $2N = 6$ i.e. for instance, a 6×6 OS network via proposed mapping. For that purpose, as an example, we employ a 3×3 optical switch using basic 2×2 OSUs as shown in Fig. 5 (a) and then apply the mapping to scale the network up to 6×6. It can be seen that the 3×3 switch has three stages, each having one switch and a straight interconnect which implies a simple structure for the permutation matrices G_1, G_2 and G_3. The transfer matrix T for 3×3 switch is given by the following relation (6);

$$T = G_3 G_2 G_1 = \begin{bmatrix} S_3^{On/Off} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & S_2^{On/Off} \end{bmatrix} \begin{bmatrix} S_1^{On/Off} & 0 \\ 0 & 1 \end{bmatrix} \tag{6}$$

In order to design a scaled 6×6 non-blocking network, we first need to verify the non-blocking feature of 3×3 optical switch. This can be done by exhausting all possible switching combinations (states) and then calculating the over-all transfer matrix T for each state via above relation. For a 3×3 switch, there exists eight possible switching states which are shown in Fig. 5 (b) and each state generates a transfer matrix. Since $3! = 6$, there exist six possible input permutations, which implies that two out of the eight transfer matrices are redundant and only six are required for complete I/O mapping. This shows that the 3×3 switch is a non-blocking switch and can be used to build larger networks. This scheme forms the basis of our generalized non-blocking test algorithm that will be discussed in detail in Section IV. A schematic output of that algorithm is shown in Fig. 6. Once it is established that the designed 3×3 switch is non-blocking, we are in a position to map it to a 6×6 network. Transfer matrices of 3×3 switch are shown in Fig. 5 (a).

Detailed design of 6×6 optical switch is shown in Fig. 7. It can be observed that the 6×6 switch has seven active stages each consists of certain number of OSUs and two passive intermediate stages M_I and M_O that provide the I/O mapping. These mapping matrices are the column and row permutations of the identity matrices, where '1' represent passive interconnection among OSUs. The transfer matrix for

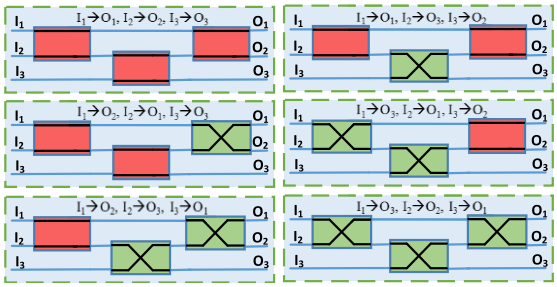


FIGURE 6. Schematic view of all I/O mapping with OSUs in "On" or "Off" states.

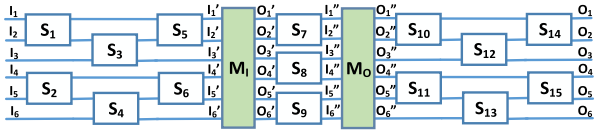


FIGURE 7. Detailed architecture of proposed 6 × 6 non-blocking optical switch.

6 × 6 can be expressed as (7);

$$T = G_1 G_2 G_3 M_I G_4 M_O G_5 G_6 G_7 \tag{7}$$

where G_1, G_2,G_3, G_4, G_5, G_3 and G_7 are permutation matrices of each stage of the network and are radially identified from Fig. 7 as shown in relations (8), (9), (10) and (11)

$$G_1 = \begin{bmatrix} S_1^{On|Off} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & S_2^{On|Off} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

$$G_2 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & S_3^{On|Off} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & S_4^{On|Off} \end{bmatrix} \tag{8}$$

$$G_3 = \begin{bmatrix} S_5^{On|Off} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & S_6^{On|Off} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

$$G_4 = \begin{bmatrix} S_7^{On|Off} & 0 & 0 \\ 0 & S_8^{On|Off} & 0 \\ 0 & 0 & S_9^{On|Off} \end{bmatrix} \tag{9}$$

$$G_5 = \begin{bmatrix} S_{10}^{On|Off} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & S_{11}^{On|Off} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

$$G_6 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & S_{12}^{On|Off} & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & S_{13}^{On|Off} \end{bmatrix} \tag{10}$$

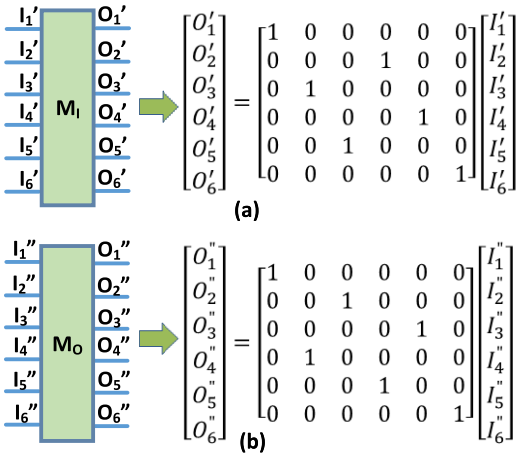


FIGURE 8. (a) Matrix representation of M_I for 6 × 6 OS; (b) Matrix representation of M_O for 6 × 6 OS.

$$G_7 = \begin{bmatrix} S_{14}^{On|Off} & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & S_{15}^{On|Off} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{11}$$

From Fig. 7, it can be seen that scaled 6 × 6 switch architecture consists of 15, 2 × 2 OSUs. I_1 to I_6 are the inputs of the OS, I_1' to I_6' are the inputs of the mapping M_I, O_1' to O_6' are outputs of M_I and joined to inputs of intermediate stage OSUs S_7, S_8 and S_9. Similarly, the outputs of S_7, S_8 and S_9 OSUs are denoted by $I_1''$to I_6'', act as inputs to M_O stage producing O_1'' to O_6'', which are finally routed to the actual outputs O_1 to O_6 of the optical switch architecture. Thus, for each intermediate interconnecting stage, there exists an analytical mapping matrix as shown in Fig. 4, where M_I and M_O takes the outputs from one stage and maps to the inputs of other stage.

To further illustrate, pictorial representation of M_I and M_O to construct 6 × 6 OS is shown in the Fig. 8. From Fig. 8 (a), it can be observed that M_I is the column wise permutation of identity matrix and maps inputs of M_I from $I_1' \sim I_6'$ to outputs $O_1' \sim O_6'$ via permutation matrix M_I. Similarly, M_O is also shown in Fig. 8 (b). Once the interconnection scheme is finalized for a particular scale, we can generalize it for N port OS. We have used [1 3 5 2 4 6] permutation as interconnection in 6 × 6 OS, which consumes least number of waveguide crossings and given a generalized form using brute force method to compute M_I. The generalized expressions to compute M_I and M_O to build higher scale OS with least number of waveguide crossings achieving the mapping expressed in (12) are provided in (15) and (16) respectively.

$$\begin{cases} [I_1', I_2', I_3' \ldots I_N'] \rightarrow [O_1', O_3' \ldots O_{2N-1}', O_2', O_4' \ldots O_{2N}'] \\ [I_1'', I_2'', I_3'' \ldots I_N''] \rightarrow [O_1'', O_3'' \ldots O_{2N-1}'', O_2'', O_4'' \ldots O_{2N}''] \end{cases} \tag{12}$$

Detailed method to find non-blocking intermediate mappings with minimum crossings is elaborated via Algorithm-4 in

Section IV. Permutation interconnection examples of different scales are expressed as follows;

4×4: $[I_1, I_2, I_3, I_4] \rightarrow [O_1, O_3, O_2, O_4]$

6×6: $[I_1, I_2, I_3, I_4, I_5, I_6] \rightarrow [O_1, O_3, O_5, O_2, O_4, O_6]$

8×8: $[I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8] \rightarrow [O_1, O_3, O_5, O_7, O_2, O_4, O_6, O_8]$

Similarly for the higher scales, interconnection for intermediate permutation matrices can be calculated and used. For a 6×6 network, mappings M_I and M_O are the column and row wise permutations of a 6×6 identity matrix given by the following relations expressed as (13).

$$M_I = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \quad M_O = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{13}$$

The inputs and outputs are related to these mappings via following relations (14);

$$O' = M_I I' \text{ and } O'' = M_O I'' \tag{14}$$

where I'/O' are the 6×1 input / output of the map M_I and I''/O'' serve the similar purpose for the map M_O. A detailed architecture of the proposed 6×6 switch along with the intermediate mappings is shown in Fig. 7. The architecture shown in Fig. 7 is taken for the sake of illustration, however, any other $N \times N$ non-blocking OS can be used to construct $2N \times 2N$ using proposed scaling scheme.

An important observation is that the proposed mappings partition the whole network into symmetric architectures for input-output stages. This feature results in significant reduction in matrix computations thereby allowing fast implementation of algorithms proposed in Section IV. For instance G_1, G_3, G_5, and G_7 hold the same structure while G_2 andG_6 are similar in construction. Thus for same switching states, one can obtain the transfer matrix T for the 6×6 network only by computing G_1, G_2, and G_4 with respective OSU index. Since there exist 2^{15} possible switching states, only 6! transfer matrices are needed to compute for complete I/O mapping which can also be verified by the proposed algorithm. The key idea upon which the proposed mapping relies is to identify the column and row permutations of identity matrix. Based on above mentioned architecture and mathematical model, we propose a generalized mapping scheme that can scale any $N \times N$ to $2N \times 2N$ optical switch architecture for which the column and row permutations are given by the following vectors (15) and (16) respectively;

$$P_I = \begin{bmatrix} 1 & 3 & \ldots & 2N-1 & 2 & 4 & \ldots & 2N \end{bmatrix}^T \tag{15}$$

$$P_O = \begin{bmatrix} 1 & 3 & \ldots & 2N-1 & 2 & 4 & \ldots & 2N \end{bmatrix} \tag{16}$$

where P_I permutes the column of $2N \times 2N$ identity matrix for the input side and P_O permutes the rows of $2N \times 2N$ identity matrix for the output. Table 1 summarizes the required steps to transform an $N \times N$ network to a $2N \times 2N$ network.

TABLE 1. Procedure to construct optical switch using scaling from an N × N network to a 2N × 2N network.

Summary of required steps

1. Design an $N \times N$ optical network and establish its non-blocking characteristics.
2. Lay out the architecture according to Fig. 4, where intermediate stage consists of N 2×2 switching element.
3. Obtain the input side column permutation of $2N \times 2N$ identity matrix via
   $P_I = \begin{bmatrix} 1 & 3 & \ldots & 2N-1 & 2 & 4 & \ldots & 2N \end{bmatrix}^T$ and
   determine M_I by permuting the columns according to the entries of P_I.
4. Repeat above step and obtain M_O by permuting the rows using
   $P_O = \begin{bmatrix} 1 & 3 & \ldots & 2N-1 & 2 & 4 & \ldots & 2N \end{bmatrix}$
5. Connect the inputs / outputs according to the entries of M_I and M_O.
6. Insert the mapping matrices as shown in Fig. 7.
7. Calculate the over-all transfer matrix including the mapping matrices and verify desired I/O routing.

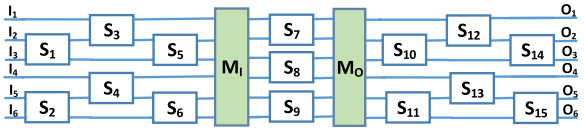


FIGURE 9. 2nd configuration of 6 × 6 non-blocking optical switch.

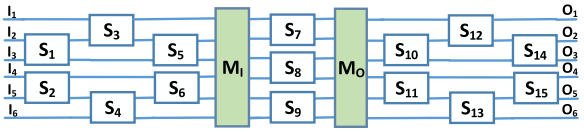


FIGURE 10. 3rd configuration of 6 × 6 non-blocking optical switch.

The permutation vectors shown in (15) and (16) are one of the non-blocking permutations written in generalized form, however, multiple switching permutations are available for the presented optical switch topology which can be identified using proposed framework and can be used to construct OS. To further extend our idea, we have shown several switch designs / configurations of 6×6 non-blocking optical switches in Figs. 9, 10 and 11 using different combinations of 3×3 switch. We present only 4 non-blocking configurations in this article, however proposed framework allows several possible non-blocking switch configurations that can be used as alternatives depending upon requirement of different applications. The mapping matrices M_I and M_O used in Figs. 9, 10 and 11 are same as expressed in (13). For different scales, number of OS configurations would be different.

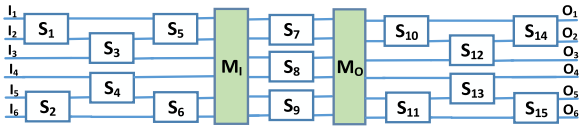


FIGURE 11. 4th configuration of 6 × 6 non-blocking optical switch.

TABLE 2. Algorithm-1 to identify switching combination for a particular I/O mapping.

Inputs: Number of I/O ports (N), Number of stages (K) and OSUs in each stage (n_k), Desired I/O mapping
Outputs: Total number of switching combination (N_c) routing the desired I/O mapping. Set I_c of identified combinations

Procedure:

1. Calculate the total number of switches using $N_s = \sum_{k=1}^{K} n_k$ and all the possible switching states by means of $L = 2^{N_s}$
2. Define S^{Off} and S^{On} using (1) and transfer matrix T_d according to desired I/O mapping
3. Generate switching combinations for all the N_s switches and set N_c to zero
4. for i = 1 to L
5. Pick the i-th combination C_i
6. for j = 1 to N_s
7. if($C_i(j) = 0$) $S(j) = S^{Off}$
8. else $S(j) = S^{On}$
9. end
10. Obtain stage wise matrices $G_1, G_2 \ldots G_{K-1}, G_K$ via $S(n)$ and calculate $T(i) = G_1 G_2 \ldots G_{K-1} G_K$
11. if($T = T_d$) Increment N_c and store the combination C_i
12. else Discard the combination.
13. end

IV. ALGORITHMS

In this Section, we proposed a set of algorithms i.e. first algorithm is used to identify the switching combinations for particular I/O mapping. Second algorithm verifies the non-blocking property of optical switch. Third algorithm adapted from [14] is tailored for the proposed design to optimize the number of OSUs by replacing them with the waveguide crossing. Finally, an algorithm to determine all possible interconnection possibilities that can be used to construct multiple non-blocking optical switches.

A. ALGORITHM FOR IDENTIFICATION OF SWITCHING COMBINATIONS FOR A PARTICULAR I/O MAPPING

As mentioned in Section 2 that multistage optical networks suffer from an inherent redundancy in switching states, which is mainly caused by more than one state of the OSU that yield different permutation matrices for each stage of the switch. In other words, by redundancy, we mean that there exist more than one switching combinations that can achieve a desired I/O mapping. In Table 2 we present an algorithm to identify such switching combinations.

Using Algorithm-1, for straight I/O mapping we identify total 16 and 144 non-blocking switching combinations for 4 × 4 and 6 × 6 optical switches respectively. For 4 × 4, best case combination with minimum OSU in off states utilized 2 OSUs in off state and 4 OSUs in on state, while for 6 × 6, only 3 OSUs found in off state and 12 OSUs in on state. By using best case, minimum power consumption and insertion loss can be achieved.

TABLE 3. Algorithm-2 to check non-blocking characteristics of optical switch.

Inputs: Number of I/O ports (N), Number of stages (K) and OSUs in each stage (n_k)
Outputs: Decision showing whether the network is non-blocking

Procedure:

1. Calculate the total number of switches using $N_s = \sum_{k=1}^{K} n_k$ and all the possible switching states by means of $L = 2^{N_s}$
2. Define S^{Off} and S^{On} using (1)
3. Calculate required switching states via $R_s = N!$
4. Generate switching combinations for all the N_s switches
5. for i = 1 to L
6. Pick the i-th combination C_i
7. for j = 1 to N_s
8. if($C_i(j) = 0$) $S(j) = S^{Off}$
9. else $S(j) = S^{On}$
10. end
11. Obtain stage wise matrices $G_1, G_2 \ldots G_{K-1}, G_K$ via $S(n)$ and calculate $T(i) = G_1 G_2 \ldots G_{K-1} G_K$
12. end
13. Find number of unique matrices U_T from $T = \{T(1), T(2) \ldots T(L)\}$
14. if($U_T = R_s$) The input network is a non-blocking network
15. else The input network is blocking network

B. ALGORITHM TO VERIFY NON-BLOCKING PROPERTY OF OPTICAL SWITCH

To verify the non-blocking property of proposed framework, an algorithm to check non-blocking feature of proposed OS is adapted from [14] which is modified according to design scheme of the proposed OS. For an $N \times N$ optical switch to be non-blocking, $N!$ switching states are required to provide complete I/O mapping. Since there exist 2^n permutation matrices from which if repeated (redundant) matrices are counted only once, then remaining matrices are unique and equal to $N!$. If this is not true, then the network is unable to route all input permutations, hence, the network is

TABLE 4. Algorithm-3 to optimize switching elements.

Inputs: Number of I/O ports (N), Number of stages (K) and OSUs in each stage (n_k), Desired I/O mapping
Outputs: Optimized network in which switches are replaced by waveguide crossings

Procedure:
1. Execute Algorithm–1 to determine N_c and the set I_c
2. Chose a combination C_d from I_c according to design ease and requirement
3. Layout the network and enumerate the OSUs as S_i where $i = 1, 2 \ldots n$
4. Denote by S_O the set of OSUs that needs to be optimized
5. Replace the first switch of S_O with the waveguide crossing
6. Execute Algorithm–2 to verify the non-blocking property of the resulting network.
7. if(non-blocking) Go the step – 9
8. else Insert back the switch for wave-guide crossing and go the step – 9
9. Replace the next switch of S_O with waveguide crossing and go the step – 6
10. Repeat steps 6 ~ 9 for all OSUs of the set S_O

TABLE 5. Algorithm-4 to identify all possible non-blocking permutations.

Inputs: Number of I/O ports (N), Number of stages (K) and OSUs in each stage (n_k), Desired I/O mapping
Outputs: Total number of all possible non-blocking permutations

Procedure:
1. Execute Algorithm –1 to determine N_c and the set I_c
2. Chose a combination C_d from I_c accordingly
3. Calculate all the permutation Q_i of 2N-port switch
4. for i = 1 to P (where **P** is the total number of perms)
5. Set $Q_i(i) = P(i)$
6. Layout the network and enumerate the OSUs as S_i where $i = 1, 2 \ldots n$
7. Execute Algorithm–2 to verify the non-blocking property of the resulting network.
8. if(non-blocking) Save the permutation $Q_i(i)$
9. else Discard and go the step – 11
10. end
11. Repeat steps 4 ~ 9 for all P and find all non-blocking permutations for interconnection matrices

blocking [14]. Steps for the proposed algorithm are detailed in Table 3.

For 4 × 4 optical switch to be non-blocking, it should find 24 total unique matrices and similarly for 6 × 6 it should have 720 unique matrices. Optical switches constructed using proposed framework allows non-blocking feature, hence for 4 × 4 and 6 × 6, simulation results match the unique matrices count of 24 and 720 for 4 × 4 and 6 × 6 switches respectively.

C. OPTIMIZATION ALGORITHM

We utilize optimization algorithm proposed in [14] in combination with algorithms, presented in Table 2 and Table 3 for proposed framework to minimize the number of OSUs. To accomplish this, first we have to choose a desired I/O mapping for which the network is to be optimized. The algorithm in Table 2 effectively performs this task from which a suitable layout can be adopted according to the design requirements. In order to quantify the feasibility of optimization, the algorithm in Table 3 can be adopted. We tailored the complete optimization algorithm in accordance with proposed framework. Algorithm is summarized in Table 4 that substitutes some OSUs with waveguide crossings to minimize the OSU count keeping the non-blocking property intact e.g. for $N = 4$, total 24 switching combinations and for $N = 6$, total 720 switching combinations are intact. This reduction in number of OSUs aid to minimize power consumption and gain compact footprint. Detailed results of optimizations in different configurations are discussed in Section V.

D. IDENTIFICATION OF ALL POSSIBLE NON-BLOCKING PERMUTATIONS

We present another algorithm which identifies all possible non-blocking permutations that can be employed as intermediate matrices to provide interconnection between stages in proposed switch topology. This feature provides the flexibility and multiple choices to construct optical switch topology. For instance, using Algorithm-4 for 4 × 4 we get 16 non-blocking permutations and for 6 × 6 we found 192 non-blocking permutations, where optical switches are established as non-blocking. In other words, 16 and 192 different type of switches can be constructed using proposed framework according to design requirements. Complete algorithm is described in Table 5. Using Algorithm-4, we compute all possible permutations for interconnection matrices that can be used in intermediate stages as M_I and M_O in column and row wise permutations.

Starting from descending order, each permutation is verified for non-blocking property, if the particular M_I and M_O interconnection scheme holds the non-blocking feature, it is stored in permutation table else discarded. Once, the table is filled with all non-blocking interconnection permutations, the non-blocking permutation listed at the bottom possesses least number of waveguide crossings, which leads to most optimum design of OS with minimum number of waveguide crossings as shown in Table 6. The design of 4 × 4 switch topology using proposed framework is shown in Fig. 12. Six OSUs are used to construct non-blocking 4-port optical switch. We have chosen 1st and 16th permutations from

TABLE 6. Possible non-blocking permutations.

	Non-Blocking Permutations Count	Non-Blocking Permutations					
4×4	1	4	2	3	1		
	2	4	2	1	3		
	3	4	1	3	2		
	4	4	1	2	3		
	5	3	2	4	1		
	6	3	2	1	4		
	7	3	1	4	2		
	8	3	1	2	4		
	9	2	4	3	1		
	10	2	4	1	3		
	11	2	3	4	1		
	12	2	3	1	4		
	13	1	4	3	2		
	14	1	4	2	3		
	15	1	3	4	2		
	16	1	3	2	4		
6×6	1	6	4	2	5	3	1
	2	6	4	2	3	5	1
	3	6	4	2	3	1	5
	⋮			⋮			
	190	1	3	5	4	6	2
	191	1	3	5	4	2	6
	192	1	3	5	2	4	6

Table 6 to construct two non-blocking 4 × 4 switch shown in Figs.13 (a) and (b) respectively. From figure, it can be observed that Fig. 13 (a) has maximum number of crossings which is constructed using permutation [4 2 3 1] presented as non-blocking permutation count "1" in Table 6. However, Fig. 13 (b) is constructed using non-blocking permutation count "16" i.e. [1 3 2 4] with minimum number of waveguide crossings. Similarly, for 6 × 6 we have chosen permutation [1 3 5 2 4 6] as interconnection matrix with minimum number of crossings presented in Table 6 at non-blocking permutation count "192" for 6 × 6. For 4 × 4 OS there exits 4! = 24 possible interconnection permutations, but all are not non-blocking, only 16 out of 24 interconnection permutations are identified in which 4 × 4 OS holds the property of non-blocking OS. Similarly for 6 × 6 there exists total of 6! = 720 possible interconnection permutations, but only 192 are identified as non-blocking. Our proposed framework provides 16 different possibilities to construct 4×4 non-blocking switch topologies. These 4 × 4 switch designs can be further utilized to construct 8 × 8 scale switch topology exploiting presented framework. We can observe that Fig. 13 (b) is similar to 4 × 4 Benes architecture. Using Table 6, we can select any non-blocking permutation from 16 different permutations to connect intermediate stages for 4 × 4 and any from 192 for 6 × 6 optical switch topologies. We list all the 16 possible non-blocking permutations of 4 × 4 and few possible out of 192 for 6 × 6 optical switches in Table 6.

An important aspect in the proposed framework is the computational cost associated with the computations of the stage (e.g. G_i) and the permutation (M) matrices. The proposed set of algorithms may lead to enhance the

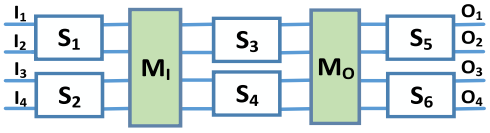


FIGURE 12. 4 × 4 optical switch topology.

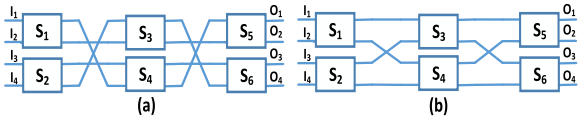


FIGURE 13. 4 × 4 optical switch topology with possible permutations.

TABLE 7. Calculation of execution time for $N = 4, 6$.

Scale	Total OSUs	Single Permutation (Sec)	$N!$ Permutation (Sec)
4×4	Un-Optimized	0.053	1.1725
	Optimized	0.039	0.9632
6×6	Un-Optimized	391.3	281735.3
	Optimized	6.34	4565.4

complexity in terms of execution time as the scale of network grows. However, because of the symmetry with respect to the central stage, the matrix computation actually gets halved. Once the input side matrices are computed, the output side matrices can be determined using the symmetry of the architecture. To estimate the computational time, we use Matlab 2016a to implement the algorithms and run on Intel core i5-4590 CPU desktop computer with 8GB memory and acquired the following execution time for 4×4 and 6×6 scales. Elapsed time for single and total permutation in case of 4 × 4 and 6 × 6 OS architectures are listed in Table 7.

The reason for higher execution time in case of 6-port un-optimized optical switch is because of the $2^{15} = 32768$ possible switching combinations, where 15 is the number of OSUs in 6 × 6 OS. After optimization, we observed a significant reduction in execution time i.e. 6.34 seconds for one iteration. In case of optimized 6 × 6 OS with 12 OSUs, there exists only $2^{12} = 4096$ which is 87.5% lower than 32768 switching combinations. Small reduction in the number of OSUs lead to significant decrease in number of switching combinations which yield lower computational time. The execution time provided includes the time to compute set of all the transfer matrices $T's$ expressed as (7), as well as the time to determine the set of unique matrices U_T required in Steps 13 and 14 of non-blocking Algorithm-2 for validation of non-blocking property of optical switch. So higher number of OSUs not only affects the performance and area of overall switch but also leads to higher execution time which may increase the design complexity of OS.

To identify the non-blocking interconnections for M_I and M_O without any intelligent / algorithmic approach is a difficult task. Therefore, proposed Agorithm-4 allows the feature to identify all possible non-blocking interconnection

permutations and select whichever is most suitable according design requirements. In some cases, the complexity of M_I and M_O is higher where number of crossing waveguides is higher. In this article, we have chosen the best interconnection scheme in which least number of waveguide crossings are identified i.e. 06 (three on left side and three on right side) for 6×6 OS. In addition, the proposed framework also allows the design of optical switches based on asymmetric non-blocking permutations and is the subject of our future work. The passive interconnection scheme provides more flexibility for input-output routing paths, where least number of optical switching units (OSUs) are identified in off / bar states which lead to minimize power consumption and insertion loss of optical switch architecture. Detailed performance analysis is provided in Section V of this article.

V. SIMULATION RESULTS, ANALYSIS AND COMPARISONS

In this Section, we compare proposed switch topology with different switch designs and then analyze the performance of proposed framework from view point of OSU count, waveguide crossings, per path OSU count, network optimization and performance parameters like power consumption, insertion loss and cross talk for 4×4 and 6×6 scale switch fabrics. We use MATLAB to implement above algorithms and perform simulations with different arrangements and OS scales to verify the authenticity of proposed framework. For simplicity, we chose straight I/O mapping i.e. $I_1 \rightarrow O_1$, $I_2 \rightarrow O_2$ and $I_N \rightarrow O_N$ for proposed switch (any I/O mapping can be chosen). For proposed 6×6 switch, employing algorithm-1, one can verify that for straight transfer matrix, there exit 144 switching states that provide the desired I/O mapping, whereas 237 switching states exist for the Spanke-Benes architecture yielding a higher index of redundancy than the proposed. This reduction in redundancy is gained because of the I/O mappings introduced in the intermediate stage of the network.

A. HARDWARE COST OF NON-BLOCKING SWITCH TOPOLOGIES

We have compared proposed switch network with different topologies in terms of OSU count, waveguide crossings and per path OSU count discussed in [25]. Table 8 lists comparisons of different switch topologies in terms of N I/O ports. Waveguide crossings of proposed switch are shown as arbitrary because, for different permutations and configurations crossing count is different, so it cannot be given in a generalized form. However, for a particular scale, we have shown numerical value of waveguide crossings that can be easily calculated once optical switch construction using scaling framework is accomplished.

Performance comparisons of different architectures taking aforementioned parameters for different scales e.g. $N = 4, 6$ is listed in Table 9. Here we can observe that proposed switch for $N = 4$, consumes 6 OSUs which is same as Benes and Spanke-Benes switch networks and in case of optimized form only 5 OSUs are consumed. While in case of $N = 6$, optimized switch utilizes only 12 OSUs that is lowest as compared to other switch topologies of the same radix. We have also noticed, that per path OSU count has also reduced in case of optimized form which leads to reduce crosstalk noise in overall switch network. Waveguide crossing count varies, depending upon optimization structure that is discussed in later part of this Section.

Comparisons for state of the art optical switches/routers for 4×4 and 6×6 in terms of OSU count, number of waveguide crossings and per path maximum number of OSUs are also provided. From Table 10, it can be observed that optical switches (OS) constructed using proposed framework has advantage of reduced number of OSUs and per path maximum number of OSUs. For the scale of 4×4, proposed optimized OS utilizes only 5 OSUs which is lesser than [15], [24] and [29] and similar to proposed in [14]. In addition, proposed optimized 4×4 OS uses lesser number of per path OSUs i.e. only 3 OSUs. Similarly, for the scale of 6×6, in comparison to [15] and [24], 50% reduction in OSU is observed and up to 20% decrease in number of OSU as

TABLE 8. Comparison of non-blocking switch topologies.

Switch Topology	OSU Count	Per Path Waveguide Crossings	Max. Per Path OSUs
Benes	$((2log_2(N))-1)N/2$	$2(N-log_2(N)-1)$	$2log_2(N)-1$
SB	$N(N-1)/2$	0	N
DLN	$5/4N^2-2N$	$3N-2log_2(N)-4$	$2log_2(N)-1$
S&S	$2N(N-1)$	$(N-1)^2$	$2log_2(N)$
CSM	N^2	0	$2N-1$
PILOSS	N^2	$N-1$	N
Proposed	$N(N-1)/2$	-	$N+1$

TABLE 9. Comparison for different scales.

Scale	Switch Topology	OSU Count	Per Path Waveguide Crossings	Max. Per Path OSUs
4×4	Benes	6	2	3
	SB	6	0	4
	DLN	12	4	3
	S&S	24	9	4
	CSM	16	0	7
	PILOSS	16	3	4
	Proposed Un-Opt.	6	2	3
	Proposed Opt.	5	2/3	2/3
6×6	Benes	-	-	-
	SB	15	0	6
	DLN	33	-	-
	S&S	60	25	-
	CSM	36	0	11
	PILOSS	36	5	6
	Proposed Un-Opt.	15	4	7
	Proposed Opt.	12	4/5	6

TABLE 10. Comparisons of 6-port optical switches/routers.

Scale	Switch Topology	OSU Count	Waveguide Crossings	Max.Per Path OSUs
4×4	[14]	5	0	3
	[15]	8	8	4
	[24]	8	0	5
	[29]	6	0	5
	Proposed Un-Opt.	6	2	3
	Proposed Opt.	5	3	3
6×6	[14]	12	3	4
	[15]	24	24	4
	[24]	24	0	9
	[29]	15	0	9
	[30]	12	11	4
	[31]	12	3	4
	Proposed Un-Opt.	15	6	5
	Proposed Opt.	12	7/9	5

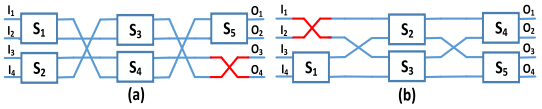


FIGURE 14. 4 × 4 port optical switch optimization.

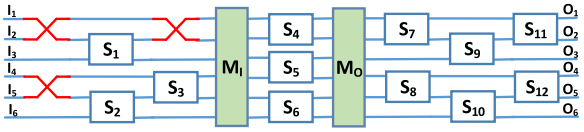


FIGURE 15. Optimized 6 × 6 optical switch in 1st configuration.

compared to [29]. The OSU count of [14], [30] and [31] are same as proposed 6 × 6 OS i.e. 12 OSUs. However, the architecture presented in [30] consumes more number of crossings and doesn't support $N!$ routing combinations as well as doesn't allow one-to-one I/O mappings.

B. OPTIMIZATION OF PROPOSED OPTICAL SWITCH TOPOLOGIES

For network optimization we consider one-to-one I/O mapping and apply the optimization algorithm. In order to ensure that no switching states are lost, we verify the non-blocking property before and after optimization of switch network. First, we consider $N = 4$ in two different configurations shown in Figs. 14(a) and 14(b) and optimize those switches to reduce the OSU count. We observe that S_6 and S_1 are replaced with waveguide crossings in respective OS networks, corresponding optimized switches are shown in Figs. 14(a) and 14(b) respectively, where almost 17% reduction in OSU count is noticed.

For 6 × 6 using the same optimization algorithm, we observed that 3 OSU are substituted with waveguide crossings. It can be seen in Fig. 15 that S_1, S_2 and S_5 are replaced by waveguide crossings providing almost 20% reduction in OSUs as compared to the un-optimized network. Using the optimization algorithm Spanke-Benes switch also

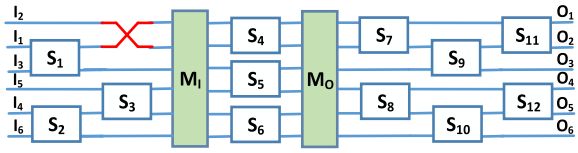


FIGURE 16. Optimized 6 × 6 optical switch with swapped inputs.

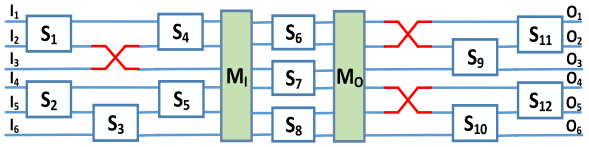


FIGURE 17. Different OSU optimization results in 1st configuration.

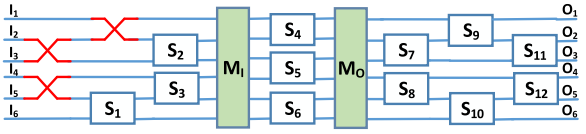


FIGURE 18. OSU Optimization in 3rd Configuration.

achieved 20% reduction in OSU count as reported in [14]. Although the optimization gain is similar for proposed and Spanke-Benes networks in terms of OSUs optimization, still proposed framework provides another opportunity with multiple design configurations for designers to choose switch topology according to varying application demands.

Further optimization of optical switch shown in Fig. 16 by replacing waveguide crossing with straight waveguides and swap inputs I_1 with I_2 and I_4 with I_5, we can reduce the number of crossings and stage count for optical switch topology. Optimized topology is shown in Fig. 16, it we can be observed that further optimization eliminates one more stage with crossings that can reduce insertion loss and crosstalk noise in optical switch topology. Optimization of different OSUs can be achieved for particular OS using optimization algorithm. We have shown another optimized structure in Fig. 17 for initial design configuration where S_3, S_{10} and S_{11} are also replaced with waveguide crossings to reduce OSU count.

Multiple switch configurations are shown in Figs. 9, 10 and 11 respectively, which can achieve different optimization results with non-blocking characteristics. For instance, we have shown the optimization of third configuration where S_1, S_2 and S_3 are replaced with waveguide crossings as shown in Fig. 18. In a similar fashion, several configurations and permutations can be employed and variety of optical switch topologies can be constructed using proposed framework. Table 11 lists possible optimization in number of OSUs for different scales for proposed switch topologies.

C. IMPACT OF OSU COUNT OF PERFORMANCE METRICS

In this Section, we analyze the impact of OSU count on power consumption, insertion loss and crosstalk noise for 4 × 4 and 6×6 scale topologies. In order to calculate, we assume 2-MRs based switch as basic OSU shown in Fig. 1 with following

TABLE 11. OSU count after optimization for different scales.

Switch Topology	Total OSUs	Remaining OSUs After Optimization
4×4	6	5
6×6	15	12
8×8	28	23
10×10	45	38
12×12	66	57

TABLE 12. Performance analysis.

Scale	Switch Topology	Max. PWR (mW)	Max. IL (dB)	Min. IL (dB)
4×4	Benes	1.2	8.4	1.2
	SB	1.2	8.4	1.2
	DLN	2.4	16.8	2.4
	S&S	4.8	33.6	4.8
	CSM	3.2	22.4	3.2
	PILOSS	3.2	22.4	3.2
	Proposed Un-Opt.	1.2	8.4	1.2
	Proposed Opt.	1	7	1
6×6	Benes	-	-	-
	SB	3	21	3
	DLN	6.6	46.2	6.6
	S&S	12	84	12
	CSM	7.2	50.4	7.2
	PILOSS	7.2	50.4	7.2
	Proposed Un-Opt.	3	21	3
	Proposed Opt.	2.4	16.8	2.4

performance parameters i.e. power consumption (PWR) at off / bar state is 200μW, on / cross state is 0 μW, insertion loss (IL) at off / bar state is 1.4dB, On / cross state is 0.2dB, crosstalk noise (CN) at off / bar state is -44.6dB and on / cross state is -17.8 dB respectively [20].

From Table 12, it can be seen that OSU count has significant influence on PWR and IL of the optical switch topologies. For maximum PWR and IL, we assume all OSUs in off / bar states and minimum PWR and IL are calculated considering all OSUs in on / cross states. It can be observed that optimized switch for both scales i.e. for $N = 4, 6$ has minimum PWR and IL. For $N = 4$, up to 17% in PWR and IL is achieved in comparison to Benes and Spanke-Benes switch networks. While for $N = 6$, in comparison to Spanke-Benes up to 20 % reduction in PWR and IL is achieved. We have also provided maximum crosstalk noise for 4×4 and 6×6 optical switches. The OSU is characterized by insertion loss (IL), extinction ratio (ER) and crosstalk noise (CN) in "off" and "on" states [32]. Crosstalk noise is determined by insertion loss and extinction ratios and expressed as (17) and (18) [32]:

$$CT^{Cross} = IL^{Bar}/(IL^{Cross} \cdot ER^{Bar}) \quad (17)$$

$$CT^{Bar} = IL^{Cross}/(IL^{Bar} \cdot ER^{Cross}) \quad (18)$$

Total crosstalk of optical switch is sum of CT of all OSUs in on / cross and off / bar states. Extinction ratio of 2-MRR based switching element in off / bar state is 11.5dB, whereas 7.8dB in on / cross state [33] while insertion loss in off / bar state is 1.4dB and 0.2dB in on / cross state [20]. Using the above expressions, we have calculated the crosstalk noise of 4×4 and 6×6 for one-to-one mapping and observed maximum crosstalk noise of 2.47dB for un-optimized 4×4 OS and 1.86dB for optimized 4×4 OS. Similarly, maximum of 7.35dB of crosstalk for un-optimized 6×6 OS while 5.53dB for optimized 6×6 OS is observed.

TABLE 13. Best and worst case switching combinations.

Scale	Switch Topology	Best ($S_1S_2 \ldots S_{15}$)	Worst ($S_1S_2 \ldots S_{15}$)
4×4	Proposed Un-Optimized	110011	000000
	Proposed Optimized	10011	00010
6×6	Proposed Un-Optimized	111111000111111	000000000000000
	Proposed Optimized	111000111111	000000000001

Finally, Table 13 presents the best and worst case switching combinations of OSUs for straight I/O mappings for $N = 4, 6$. We present best and worst cases for one-to-one I/O mapping. Best case is defined as minimum number of OSUs in off / bar state, whereas worst case is the switching combinations of OSUs with maximum OSUs in off / bar state. Switching combinations of S_1, $S_2 \ldots S_{15}$ are shown in Table 13, where, '0' represents off / bar state and '1' represents on / cross state. It can be observed that for the worst case maximum number of OSUs are found in off / bar state for one-to-one I/O mapping which leads to maximum power consumption. However, the best case for same I/O mapping has minimum number of OSUs in the off / bar state which lead to minimized power consumption.

Lastly, we have analyzed the feasibility of fabrication and implementation of proposed OS depending upon available technology and fabrication options. Several examples for fabrication / realization of optical switches of different scales are available where implementation options are available to realize optical switches. During past few years, diverse manufacturing technologies, fabrics and packaging methods using various switching schemes are proposed and discussed for on-chip optical switch architectures. A comprehensive most up to date review about current methodologies used by researchers to construct OS fabric and survey of state of the art architectures from view point of technological as well as architectural level is presented and discussed in [25].

Different fabrication options for OSU to construct OS i.e. Mach-Zehnder interferometer (MZS), microring resonator (MRR) and directional coupler based optical switches are recently proposed and demonstrated. Some latest and recently proposed OS with physical demonstration of MRR and MZS based OS includes; 5-port router constructed on MRR based OSU [17], a rearrangeable non-blocking 5×5 optical switch for optical Mesh topology is fabricated using MZS is demonstrated in [5], an optimized 6-port optical

switch constructed for cluster Mesh NoC topology is realized in [31] using MZS. Another example of polymer/silica hybrid OSU based OS is proposed and realized in [29]. Several other examples of fabrication and demonstration of optical switches are available in literature [33]–[36]. Similarly, proposed architecture can be realized and demonstrated in similar fashion with any of the available technologies as discussed, which may be considered as future work once the design validation via simulation method is accomplished.

VI. CONCLUSION

We proposed an algorithmic framework to construct optical switch topologies using scaling from $N \times N$ to $2N \times 2N$ non-blocking optical switch that can easily scale the switch fabric to higher order switch networks. In addition, we presented a set of algorithms, first, to identify the non-blocking switching combination; second, algorithm to check the non-blocking feature of proposed optical switch; third, optimization algorithm in combination with first two algorithms to optimize the number of OSU count and last algorithm to identify all possible non-blocking permutations that can connect intermediate stages of proposed switch network constructing multiple switches of same radix. We have discussed and analyzed different configurations with different permutations and evaluated results in un-optimized and optimized form and compared to other optical switch networks in terms of power consumption, insertion loss and crosstalk noise.

Our simulation results show reduced OSU count that lead to compact optical switch architecture keeping the non-blocking property intact. Up to 20% reduction in total as compared to original 6×6 scale network and Spanke-Benes architecture in OSUs has been achieved. In addition, reduction in insertion loss and power consumption are also reported in this article for proposed network architecture. Lastly, we presented best and worst case switching combinations for different switch scales that would help to minimize the power consumption and insertion loss to gain overall better performance of ONoC. This scalable and optimized framework is highly suitable for high radix optical switch port requirements in high bandwidth ONoC architectures as well as upcoming high performance computing systems. Detailed performance evaluation, analysis and design consideration for higher order switch networks are aimed as future work. In future, we also aim to extend this work for construction of OS using asymmetrical non-blocking permutations as well as to build analytical model for latency, bit error rate, crosstalk noise and insertion loss parameters for multistage networks with higher scale.

REFERENCES

[1] D. Bertozzi, G. Dimitrakopoulos, J. Flich, and S. Sonntag, "The fast evolving landscape of on-chip communication: Selected future challenges and research avenues," *Des. Automat. Embedded Syst.*, vol. 19, nos. 1–2, pp. 59–76, 2015.

[2] A. B. Achballah, S. B. Othman, and S. B. Saoud, "Problems and challenges of emerging technology networks-on-chip: A review," *Microprocess. Microsyst.*, vol. 53, pp. 1–20, Aug. 2017.

[3] S. Werner, J. Navaridas, and M. Luján, "A survey on optical network-on-chip architectures," *ACM Comput. Surv.*, vol. 50, no. 6, 2017, Art. no. 89.

[4] M. R. Yahya, N. Wu, G. Yan, and Y. Yasir, "Review of photonic and hybrid on chip interconnects for MPSoCs in IoT paradigm," in *Proc. 21st Saudi Comput. Soc. Nat. Comput. Conf. (NCC)*, Apr. 2018, pp. 1–6.

[5] T. Zhou, H. Jia, J. Dai, S. Yang, L. Zhang, X. Fu, and L. Yang, "Rearrangeable-nonblocking five-port silicon optical switch for 2-D-mesh network on chip," *IEEE Photon. J.*, vol. 10, no. 3, Jun. 2018, Art. no. 6601208.

[6] L. Lu, S. Zhao, L. Zhou, D. Li, Z. Li, M. Wang, X. Li, and J. Chen, "16×16 non-blocking silicon optical switch based on electro-optic Mach-Zehnder interferometers," *Opt. Express*, vol. 24, no. 9, pp. 9295–9307, 2016.

[7] X. Tan, M. Yang, L. Zhang, Y. Jiang, and J. Yang, "A generic optical router design for photonic network-on-chips," *J. Lightw. Technol.*, vol. 30, no. 3, pp. 368–376, Feb. 1, 2012.

[8] R. A. Spanke and V. E. Benes, "N-stage planar optical permutation network," *Appl. Opt.*, vol. 26, no. 7, pp. 1226–1229, 1987.

[9] V. E. Beneš, "Algebraic and topological properties of connecting networks," *Bell Syst. Tech. J.*, vol. 41, no. 4, pp. 1249–1274, 1962.

[10] C.-C. Lu and R. A. Thompson, "The double-layer network architecture for photonic switching," *J. Lightw. Technol.*, vol. 12, no. 8, pp. 1482–1489, Aug. 1994.

[11] A. Joshi, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanovic, and V. Stojanovic, "Silicon-photonic clos networks for global on-chip communication," in *Proc. 3rd ACM/IEEE Int. Symp. Netw.-Chip (NoCS)*, May 2009, pp. 124–133.

[12] P. DasMahapatra, R. Stabile, A. Rohit, and K. A. Williams, "Optical crosspoint matrix using broadband resonant switches," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 4, pp. 1–10, 2014.

[13] T. Shimoe, K. Hajikano, and K. Murakami, "Path-independent insertion loss optical space switch," in *Proc. Opt. Fiber Commun. Conf.*, vol. 4, 1987, pp. 999–1003.

[14] T. Zhou and H. Jia, "Method to optimize optical switch topology for photonic network-on-chip," *Opt. Commun.*, vol. 413, pp. 230–235, Apr. 2018.

[15] R. Min, R. Ji, Q. Chen, L. Zhang, and L. Yang, "A universal method for constructing n-port nonblocking optical router for photonic networks-on-chip," *J. Lightw. Technol.*, vol. 30, no. 23, pp. 3736–3741, Dec. 1, 2012.

[16] Q. Chen, F. Zhang, R. Ji, L. Zhang, and L. Yang, "Universal method for constructing N-port non-blocking optical router based on 2×2 optical switch for photonic networks-on-chip," *Opt. Express*, vol. 22, no. 10, pp. 12614–12627, 2014.

[17] H. Jia, Y. Zhao, L. Zhang, Q. Chen, J. Ding, X. Fu, and L. Yang, "Five-port optical router based on silicon microring optical switches for photonic networks-on-chip," *IEEE Photon. Technol. Lett.*, vol. 28, no. 9, pp. 947–950, May 1, 2016.

[18] N. Dupuis, B. G. Lee, A. V. Rylyakov, D. M. Kuchta, C. W. Baks, J. S. Orcutt, D. M. Gill, W. M. J. Green, and C. L. Schow, "Modeling and characterization of a nonblocking 4×4 Mach–Zehnder silicon photonic switch fabric," *J. Lightw. Technol.*, vol. 33, no. 20, pp. 4329–4337, Oct. 15, 2015.

[19] B.-C. Lin, S. Chen, Y. Huang, and C.-T. Lea, "Power minimization in microring-based benes networks," *IEEE Trans. Commun.*, vol. 66, no. 8, pp. 3517–3525, Aug. 2018.

[20] P.-H. Yuen and L.-K. Chen, "Optimization of microring-based interconnection by leveraging the asymmetric behaviors of switching elements," *J. Lightw. Technol.*, vol. 31, no. 10, pp. 1585–1592, May 15, 2013.

[21] A. Biberman and K. Bergman, "Optical interconnection networks for high-performance computing systems," *Rep. Prog. Phys.*, vol. 75, no. 4, 2012, Art. no. 046402.

[22] S. Rumley, M. Bahadori, R. Polster, S. D. Hammond, D. M. Calhoun, K. Wen, A. Rodrigues, and K. Bergman, "Optical interconnects for extreme scale computing systems," *Parallel Comput.*, vol. 64, pp. 65–80, May 2017.

[23] B. G. Lee, N. Dupuis, P. Pepeljugoski, L. Schares, R. Budd, J. R. Bickford, and C. L. Schow, "Silicon photonic switch fabrics in computer communications systems," *J. Lightw. Technol.*, vol. 33, no. 4, pp. 768–777, Feb. 15, 2015.

[24] M. Geng, Z. Tang, K. Chang, X. Huang, and J. Zheng, "N-port strictly non-blocking optical router based on Mach–Zehnder optical switch for photonic networks-on-chip," *Opt. Commun.*, vol. 383, pp. 472–477, Jan. 2017.

[25] B. G. Lee and N. Dupuis, "Silicon photonic switch fabrics: Technology and architecture," *J. Lightw. Technol.*, vol. 37, no. 1, pp. 6–20, Jan. 1, 2019.

[26] Z. Wang, J. Xu, P. Yang, Z. Wang, L. H. K. Duong, and X. Chen, "High-radix nonblocking integrated optical switching fabric for data center," *J. Lightw. Technol.*, vol. 35, no. 19, pp. 4268–4281, Oct. 1, 2017.
[27] W. J. Dally and B. Towles, *Principles and Practices of Interconnection Networks*. San Francisco, CA, USA: Morgan Kaufmann, 2003.
[28] N. Dupuis and B. G. Lee, "Impact of topology on the scalability of Mach–Zehnder-based multistage silicon photonic switch networks," *J. Lightw. Technol.*, vol. 36, no. 3, pp. 763–772, Feb. 1, 2018.
[29] L. Liang, K. Zhang, C. T. Zheng, X. Zhang, L. Qin, Y. Q. Ning, D. M. Zhang, and L. J. Wang, "N × N reconfigurable nonblocking polymer/silica hybrid planar optical switch matrix based on total-internal-reflection effect," *IEEE Photon. J.*, vol. 9, no. 4, Aug. 2017, Art. no. 7904611.
[30] E. Yaghoubi, M. Reshadi, and M. Hosseinzadeh, "Mach–Zehnder-based optical router design for photonic networks on chip," *Proc. SPIE*, vol. 54, no. 3, 2015, Art. no. 035102.
[31] H. Jia, T. Zhou, Y. Zhao, Y. Xia, J. Dai, L. Zhang, J. Ding, X. Fu, and L. Yang, "Six-port optical switch for cluster-mesh photonic," *Nanophotonics*, vol. 7, no. 5, pp. 827–835, 2018.
[32] R. Ji, L. Yang, L. Zhang, Y. Tian, J. Ding, H. Chen, Y. Lu, P. Zhou, and W. Zhu, "Five-port optical router for photonic networks-on-chip," *Opt. Express*, vol. 19, no. 21, pp. 20258–20268, 2011.
[33] B. G. Lee, A. Biberman, N. Sherwood-Droz, C. B. Poitras, M. Lipson, and K. Bergman, "High-speed 2 × 2 switch for multiwavelength silicon-photonic networks–on-chip," *J. Lightw. Technol.*, vol. 27, no. 14, pp. 2900–2907, Jul. 15, 2009.
[34] X. Li, X. Xiao, H. Xu, Z. Li, T. Chu, J. Yu, and Y. Yu, "Mach–Zehnder-based five-port silicon router for optical interconnects," *Opt. Lett.*, vol. 38, no. 10, pp. 1703–1705, 2013.
[35] Y.-T. Han, J.-U. Shin, S.-H. Park, H.-J. Lee, W.-Y. Hwang, H.-H. Park, and Y. Baek, "N × N polymer matrix switches using thermo-optic total-internal-reflection switch," *Opt. Express*, vol. 20, no. 12, pp. 13284–13295, 2012.
[36] Q. Cheng, M. Bahadori, Y.-H. Hung, Y. Huang, N. Abrams, and K. Bergman, "Scalable microring-based silicon Clos switch fabric with switch-and-select stages," *IEEE J. Sel. Topics Quantum Electron.*, vol. 25, no. 5, Sep./Oct. 2019, Art. no. 3600111.

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