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Analog Statistical Design for Manufacturability Using Linear and Nonlinear Response

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ABSTRACT Manufacturing yield, overkill, and defect level can limit the feasibility of analog circuits in SoCs. The conventional method of handling process and environmental variation is to assign the design margin such that the design meets specifications at several processes and environmental corners. However, checking only a few extreme corners limits performance more than the more rigorous statistical approach of computing manufacturing and quality figure of merit. On the other hand, the statistical approach requires transistor level simulation of hundreds or thousands of samples, not just a few corners, and hence is very time-consuming. This paper gives a way to sidestep the problem by characterizing each of many samples of building blocks once at the transistor level. The building blocks are scalable so that statistics are preserved when a building block is adjusted to the requirement of a higher level design. Many design scenarios may be rapidly explored by assembling and scaling the building block samples without SPICE simulation. A continuous-time low-pass filter design example is used to extract the requirements of the building block approach. The requirements include a method to assemble building blocks (biquad element for the example) into a filter design while preserving the statistics that would have been extracted by simulation of the entire filter at the transistor level. The assembly method for both linear and nonlinear response is proposed.

INDEX TERMS Continuous-time filter, Gm-C, design for manufacturing, analog standard-cell.

I. INTRODUCTION

Mixed-signal Application Specific IC (ASIC) and System-on-Chip (SoC) integrate analog components such as PLLs, IOs, filters, analog-to-digital and digital-to-analog converters, thermal sensors, etc. within larger digital systems with component counts and areas considerably less than the digital system. Several analog design solutions exist that meet the required specifications. However, each design alternative, i.e. different topology, transistor implementation, responds differently to manufacturing variations and may require different testing strategies [1] resulting in different sensitivities to the final SoC product manufacturing and quality Figures-of-Merit (FoM), viz. yield, test-escape, overkill and defect level.

Although analog design methods are well established, a persistent problem is characterization in the presence of process variation. It is difficult to include manufacturing and quality figures-of-merit affected by process variation in the design methodology since statistical data for all performance metric are needed. In principle, the statistics can be obtained from Monte Carlo SPICE simulation of many samples of the circuit in transistor level. Conventional Monte Carlo approach is compute-intensive and limits the circuit complexity that can be explored, to find an optimal design alternative for given Test and Use scenarios. Efficient Monte Carlo sampling methods such as quasi-Monte Carlo [2], latin hypercube sampling [3], Bayesian inteference [4], etc. have been proposed. However, these approaches still require transistor simulation on each analog design alternative to estimate their corresponding yields. Fast estimation of performance metrics of analog systems using analytical performance models are proposed in [5], [6] that can be used to quantify manufacturing and quality FoMs. These approaches require finding the sensitivity of various parameters of interest of the analog systems to different process and environmental conditions which is non trivial for complex systems in nanoscale technologies, since bias dependent short-channel effects (such as V_T roll-off, velocity saturation and drain-induced barrier lowering or DIBL) [7] and layout dependent effects

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(such as well-proximity and shallow trench isolation or STI stress) [8], [9] increase the dimensionality of analytical models. Not having a highly efficient methodology to obtain manufacturing FoMs for analog design alternatives limits the ability to analyze trade-offs that can be made for different designs, component counts, areas, manufacturing yield, and quality early in the product life cycle. When a final design does not meet manufacturing specifications, difficult choices must be made to either tolerate low SoC yield or integrate a different analog design into the SoC and invest more expensive design time.

An alternate approach to analog system design is to synthesize analog circuits, inlcuding topology selection, transistor sizing, hardening synthesized circuits for process variation and layout generation. Reasoning-based topology synthesis method to design a low power opamp is shown in [10]. Higher level circuits, such as filters, are synthesized using the concept of building blocks (op-amps, resistors and capacitors) in [11] using tabu search heuristic that sizes transistors for optimal area and performance. Synthesis of more complex analog circuits such as ADC, PLL and filters by leveraging digital design tools for accelerating circuit layout have been proposed in [12]–[14]. These approaches still require SPICE simulations to obtain quantitative statistical measures for the performance of analog circuits and estimate the manufacturing and quality FoMs. Parametric variations aware circuit synthesis is described in [15]–[17] where the synthesys algorithm generates transistor sizing taking into account process and supply variations to generate OTAs. Variation aware VCO design synthesis using DoE assisted Monte Carlo simulations is shown in [18]. However, the yield aware analog circuit synthesis is still limited to small building blocks such as op-amps and VCOs.

This paper proposes an analog system design methodology that enables evaluation of manufacturing and quality FoMs in order to evaluate different design alternatives in early product life cycle. The analog systems are built using building blocks [11]. Instead of using analytical models [5], [6], the linear and non-linear responses of the building blocks are pre-characterized for process and environmental variations using SPICE simulations. Using the pre-characterized library of building blocks, circuit performance, parametric manufacturing yield and defect level of different toplogies are evaluated without additional SPICE simulations for 200kHz antiasling or reconstruction filter that can be used for GSM/DECT receiver [19].

This paper is organized as follows: The motivation and main contribution of this work are described in Section-II. The proposed building block approach for design for manufacturing is described with filter as example in Section-III. The characterization of the building block library is shown in Section-IV. Sections-V and VI describe the methodology used to estimate linear and non-linear performance of filters. Section-VII shows the results of evaluation for different filter design alternatives to maximize yield and minimize defect level.

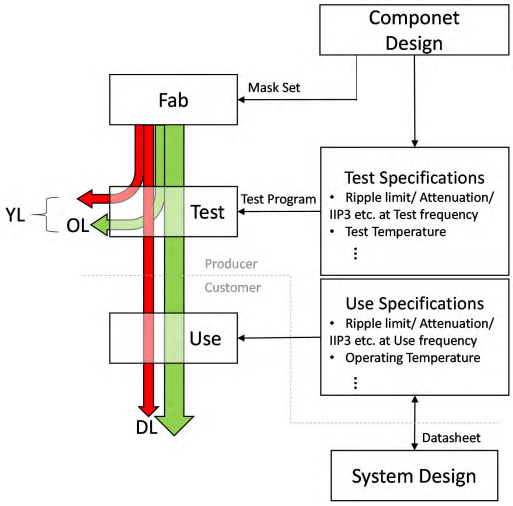


FIGURE 1. Relationship of Figure-of-Merit to population category probabilities in the context of an analog filter. Without Test phase, a fraction (red) of the population of components would fail in Use. Test reduces the customer-perceived defect level (DL) by trimming and screening components. Reducing DL increases yield loss (YL) and overkill (OL).

II. MOTIVATION AND CONTRIBUTIONS

Fig. 1 shows the flow of circuit components from the silicon fabrication factory (Fab) through the Test factory and finally to the customer (Use). Because of process variation in the Fab, a fraction of devices produced by the Fab, shown in red in the figure, will not satisfy the performance requirements in the published datasheet, called the Use Specification. The Use Specification gives the performance limits assumed by the customer's system designer when designing a system using the components. The Use Specification is also the component producer's definition of a *good* component. For high-performance components, the fraction of components produced by the Fab not meeting the Use Specification is usually unacceptably high and must be controlled by screening the population of components produced by the Fab using the manufacturing Test operation in the producer's factory.

Producer and OEM - i.e. the party using the design component, manufacturing cost models require quantitative statistical Figure-of-Merit (FoMs). However the usual method of simulating analog circuits at process and environmental coners does not quantify parametric variation reflected in manufacturing FoMs such as yield loss at the producer and shipped defect levels (quality) received by the OEM.

Manufacturing and quality FoM, yield loss (YL), overkill (OL) and defect level (DL), are computed as follows:

$$\begin{aligned} YL &= \frac{FF + FP}{FF + FP + PF + PP} \\ OL &= \frac{FP}{FF + FP + PF + PP} \\ DL &= \frac{PF}{PF + PP} \end{aligned} \tag{1}$$

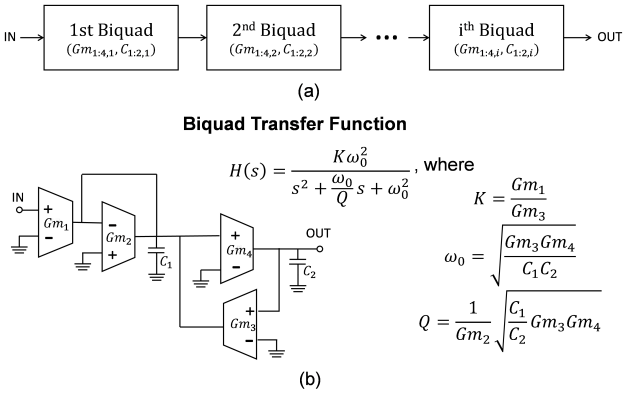


FIGURE 2. (a) A 2N-order low pass cascaded biquad Gm-C filter using N biquads. (b) Each biquad is constructed with transconductor (Gm) and capacitors (C).

where FF is the number of samples that fail in both test and use conditions, FP is the number of samples that fail in test condition, but passes in use condition, PF is the number of samples passing in test condition, but failing at use condition and PP is the number of samples that pass in both test and use conditions [20].

The proposed methodology implements analog systems by employing scalable building blocks of circuits which preserve correct process statistics when used in a larger system. The library of building blocks is built with transistor level simulation of many process samples (Section-IV) avoiding the need for complex analytical multidimensional modeling, especially for non-linear responses in highly scaled processes. The methodology

1) minimizes SPICE simulation to predict linear and non-linear response of design alternatives by reusing small and large-signal SPICE simulations from an analog building block library.
2) estimates - early in the design cycle - manufacturing variation effects on a filter design's linear and non-linear response and verifies test specification setting for improved correlation between test and use.
3) provides a quantitative comparison of manufacturing and quality FoMs for filter design alternatives and without transistor level SPICE simulation.

The methodology is demonstrated by evaluating two different design alternatives for a continuous-time low pass filter with a pass-band gain of 0dB, bandwidth of 200kHz and stop-band rejection of >30dB at 435kHz in a 45nm CMOS technology to maximize the manufacturing and quality FoMs. Cascaded biquads (Fig. 2) are used to realize the low-pass filter transfer function, $H_F(s)$, in (2) since it is a more general topology that can be used to implement a transfer function that is a quotient of two polynomials. Additionally, a biquad allows for a scalable design since different transfer functions can be obtained by minor changes to the component values without changing the circuit topology [21]. The biquads can be implemented either using Opamp-RC or Gm-C topologies depending on

TABLE 1. Filter use requirements and test specifications.

Passband		**Use**	**Test**
Cut-off	f_p	200kHz	
Ripple	A_r	±3.5 dB	±3dB @ 140kHz
Gain	K_p	0dB	Trim
Stopband			
Cut-off	f_s	435kHz	
Gain	A_s	<-30dB	< -12 dB @ 300kHz
Linearity			
IIP_3	IIP_3	> -16dB @ 100kHz	> -16dB @ 140kHz

the power, noise and linearity requirements of the filter and for this demonstration, a Gm-C topology was chosen since it can be implemented with a lower power to achieve a given bandwidth as well as being more compact compared to OpampRC filters [22]. The gain (K), pole frequency (ω_0) and quality factor (Q) of the individual biquads, $H_i(s)$, are chosen to achieve the desired frequecny response.

$$H_F(s) = \prod_{i=1}^{N} H_i(s) \tag{2}$$

$$H_i(s) = \frac{K\omega_0^2}{s^2 + s\,(\omega_0/Q) + \omega_0^2} \tag{3}$$

III. BUILDING BLOCK METHODOLOGY FOR MANUFACTURING AND QUALITY FOM PREDICTION

As described in the previous section, a cascaded biquad filter design is used to demonstrate the design methodology for manufacturing. Filter *use requirement* such as DC gain, cut-off frequency, in-band-ripple, stop-band attenuation and linearity are listed in Table-1. These design specifications can be achieved with continuous time filter architectures such as cascaded biquads or ladder filters. Either of these architectures can be realized using active circuit topologies such as OPAMP-RC or Gm-C. Furthermore, the filter specification can be met by a plethora of filter order and types (e.g. Butterworth, Chebyshev, elliptical, etc.). Since the specifications can be met using different filter types, order, topology or architecture, it is important to evaluate which design alternative will perform best considering all aspects of the product. Table-1 also lists the *test conditions* for the filter. This is required because during the test phase, it is impractical (and often not needed) to characterize the filter AC and non-linear response across entire use condition due to the large test times involved. In order to reduce the test time and cost, the filter is often only tested at few frequencies. The manufacturing FoMs are evaluated at these test specifications.

Fig. 3 shows the building block methodology for cascaded filter design where the biquad is used as the building block. To realize a given transfer function, a cascade of these biquads with slight variation in the component values can be used [21]. The basic building block (in this case the biquad) can be designed using tradition analog design flow or

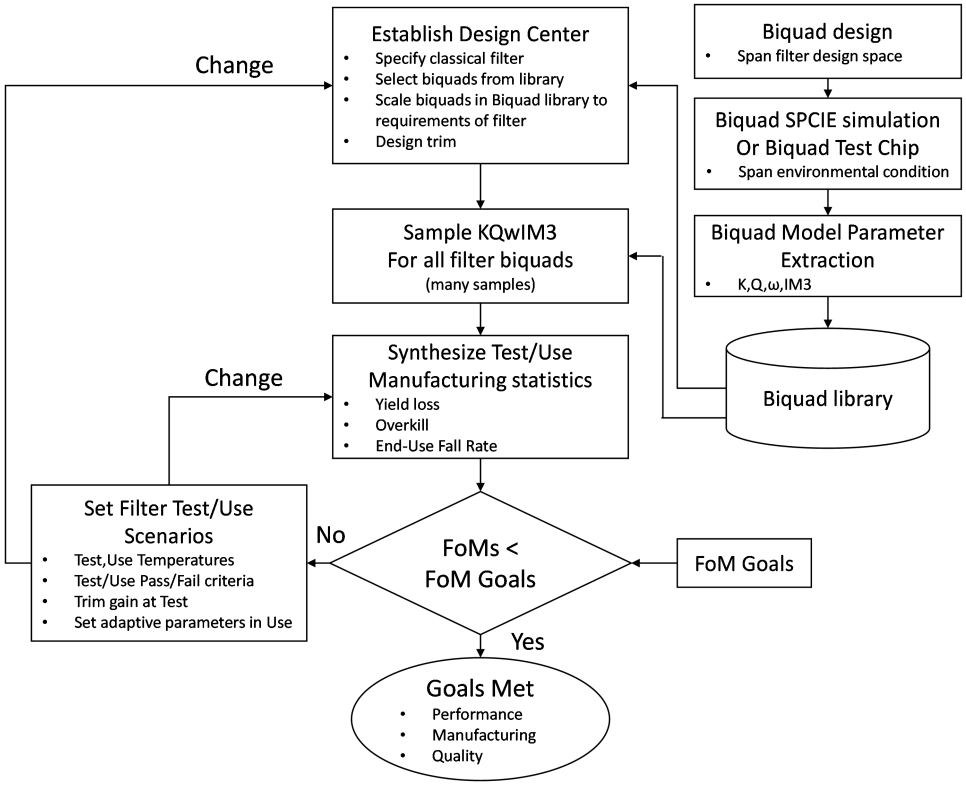


FIGURE 3. Building Block methodology: Biquad as building block replaces the compute intensive SPICE simulation of the filter in Test/Use and building block level design optimization by much less compute intensive sampling and scaling of the KQw IM3 statistical model. SPCIE simulations to establish the KQw IM3 biquad model need be done only once.

using synthesis methodologies described in [10]–[18]. Each biquad circuit is Monte Carlo simulated for many samples to capture the effect of process variation. Optionally, advanced simulation methodologies [2]–[4] can also be used.

The specifications in Table-1 can be broadly classified into small-signal (or linear) characeristics or large-signal (or non-linear) characteristics. Transfer-function (DC gain, cut-off frequency, inband ripple, stop band rejection, etc.) are dictated by the small signal responses and can be evaluated using transfer functions of cascaded blocks as shown in (2). Characteristics such as gain compression, harmonic distortion and intermodulation can be determined by the non-linear response of the system as described in (4)

$$v_{out} = \Sigma_{i=0}^{n} \alpha_i v_{in}^i \tag{4}$$

where v_{out} is the output voltage, v_{in} is the input and α_i are the coefficient of the Taylor series describing the large signal behavior of the system. The third order intermodulation (IM_3) is a useful metric to quantify non-linearity [23] when the third order distortion (or α_3) is the dominant source as is the case with most circuits.

Transfer function parameters, K, Q and ω_0 and large signal parameter IM_3 are extracted for each sample and stored in the Biquad library. Filter design has two parts: First the *design center* is established, and second, variation around the center is characterized. Mean values of biquad K, Q and ω_0 parameters from the Biquad Library are used to establish the design center. Then, to characterize variation, K, Q and ω_0 parameters of a sample of filter instances is created by *scaling* from biquad K, Q, ω_0 and IM_3 parameters sampled from the Biquad Library. Scaling transforms samples of Biquad Library parameters to samples of biquads that match filter requirements while preserving the proper statistics of the parameters. Bootstrap sampling or generation from the parametric statistical model is used to create K, Q, ω_0 and IM_3 samples from the Biquad Library.

Filter design requires exploration of many hypothetical design, test, and use scenarios as shown in Fig. 3. Construction of the filter transfer function and nonlinear response from samples of biquad K, Q, ω_0 and IM_3 parameters , rather than circuit simulations requires much less computation. In fact the what-if design/test/use scenarios for the filter design examples given in this paper were coded in Python and were executed in real time on a PC.

IV. BIQUAD LIBRARY AND CHARACTERIZATION

The generation and characterization of the analog library is key to the entire design flow. For cascaded biquad filter, the building-block is a biquad shown in Fig. 2. The frequency response of the biquad can be represented using a closed

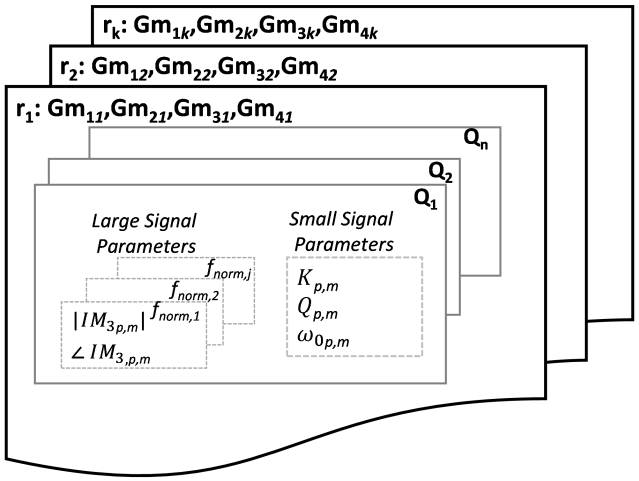


FIGURE 4. Biquad library: Building-block library for the Gm-C biquads comprising of small-signal and large signal characterization as well as process and mismatch data.

form equation as a function of Gms and the capacitors. The library contains practical values for the ratio of Gm_1 to Gm_4. This is analogous to digital standard-cell library which typically contains a subset of all possible sizing for digital gates. The analog library used in this paper (Fig. 4) consists of three biquad designs (r_k where $k \in [1, 2, 3]$) which has unique values of biquad Gm ratios (Gm_{1-4}) for demonstration. Each biquad is characterized for four different Qs (Q_n, where $n \in [1, 2, 3, 4]$). The Q of the biquad is tuned by the capacitor ratios of the biquad. The biquad is characterized for its frequency response using small-signal simulations. Non-linear response at different frequencies ($f_{norm,j}$, where $j \in [1, 2, \ldots 8]$) normalized to the pole frequency (ω_0) are characterized using two test tones separated by 5% around f_{norm} for large-signal simulations [23]. As we will see in Section-VI, both magnitude and phase of the IM_3 are required to estimate the overall filter IM3 from the building blocks. In order to capture process variation and mismatch, Monte Carlo SPICE simulations are run on each biquad $B_{r,Q}$. The effect of process ($p \in [1, 2, \ldots 250]$) and mismatch ($m \in [1, 2, \ldots 5]$) on $K_{p,m}$, $Q_{p,m}$,$\omega_{0p,m}$ and IM_3 are stored and each biquad sample in this library can be indexed by its four vectors, viz. Gm ratio, Q, process and mismatch identifiers ($B_{r,Q,p,m}$). Note that the biquad filter transfer function parameters ($K_{p,m}$, $Q_{p,m}$ and $\omega_{0p,m}$) for each Monte Carlo sample are extracted from the simulated AC transfer function by least square fitting to the ideal transfer function (3). Performing Monte Carlo SPICE simulations on a small building-block is very efficient and eliminates the need for doing these simulations for higher level circuits. The fully characterized building-block now contains all the information necessary for the subsequent steps and is shown in Fig. 4.

The analog building block characterization must identify and retain non-ideal effects as well as include the effects of component variation from processing and the effects of component mismatch. The characterization could also include the variation of biquad capacitor (C1 and C2) as well as parasitic interconnect components in the SPICE simulations. Interconnect parasitics can be estimated [24] and be absorbed into the filter design capacitor scaling step. Integrated Gm-C biquad circuits are dominated by two non-ideal Gm effects; 1) frequency dependent Gm due to internal parasitic poles and; 2) finite input (G_i) and output (G_o) admittances [22]. Parasitic poles alter an Gm-C biquad transfer function and a finite Gm output admittance limits an Gm-C biquad operating Q. In this work, the effects of a parasitic pole changed biquad parameterization by less than 1 part in 10^5 and were ignored in filter design. The non-ideal Gm output admittance was significant, $G_o \approx 0.05 G_m$ and was included during filter design.

The database organization and storage of its design characterization can be visualized as shown in (5). Each row retains the characterization data for one Monte-Carlo sample of a specific library biquad design $\boldsymbol{r_k}$ of quality factor $\boldsymbol{Q_n}$ and normalized frequency $\boldsymbol{f_{norm,j}}$ used for IM_3 simulations.

$$\begin{bmatrix} 1 & K_1 & Q_1 & \omega_{0,1} & |IM_{3,1}| & \angle IM_{3,1} \\ 2 & K_2 & Q_2 & \omega_{0,2} & |IM_{3,2}| & \angle IM_{3,2} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ pm & K_{pm} & Q_{pm} & \omega_{0,pm} & |IM_{3,pm}| & \angle IM_{3,pm} \end{bmatrix} \quad (5)$$

The biquad sample index unique to a specific biquad design and specific Monte Carlo sample ranges from 1 *to* $p \times m$ (1250 in this demonstration). The data in each row is one example of the non-ideal effects and transistor variation on a biquad design. Simulation data for each biquad design are randomly selected during bootstrap generation of a sample of a filter and will be described in Section-V.

V. ESTIMATION OF FILTER FREQUENCY RESPONSE USING BIQUAD LIBRARY

The quality factor, Q_i, and the pole-frequency, ω_{0i} for the i^{th} biquad in the filter that needs to be generated could be different from that in the analog library. The biquads in the library can be mapped to the required Q and ω_0 for i^{th} stage biquad by scaling the capacitors C_1 and C_2 from a biquad design r using the following equations

$$\begin{aligned} S_{1i}(Q_i,\ \omega_{0i}|\ Q_r,\ \omega_{0r}) &= \frac{\omega_{0r}}{\omega_{0i}}\frac{Q_i}{Q_r} \quad C_{1i} = S_1 \cdot C_{1r} \\ S_{2i}(Q_i,\ \omega_{0i}|\ Q_r,\ \omega_{0r}) &= \frac{\omega_{0r}}{\omega_{0i}}\frac{Q_r}{Q_i} \quad C_{2i} = S_2 \cdot C_{2r} \end{aligned} \quad (6)$$

The flow chart explaining the filter generation is shown in Fig. 5(a).

Multiple filter samples can be generated by bootstrapping. Fig. 6 shows an example to generate multiple filter samples for a 4^{th}-order filter. In order to generate a filter sample, biquads from the same process index, p, are selected from the library. If biquad design r_k is used more than once, the filter sample is generated by selecting biquads from the same process p, but with different mismatch indexes m. For example, if all biquads used in the filter are from the same biquad

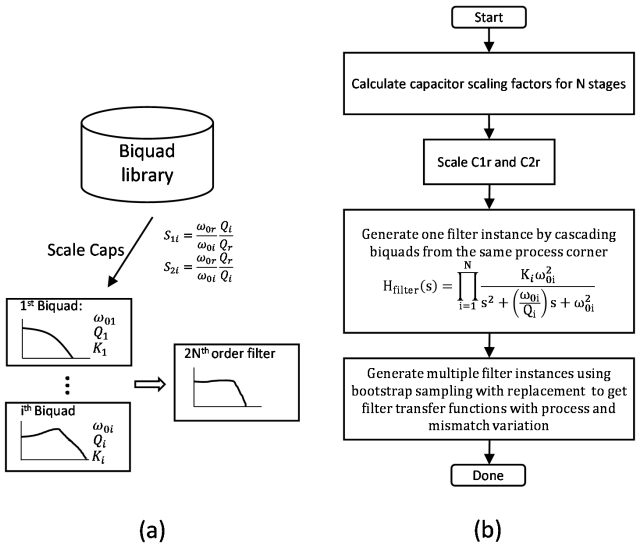


FIGURE 5. (a) Filter synthesis flow and (b) flow chart to estimate filter transfer function using analog library.

design, there are P(M,N) filter samples can be generated for each process p where M is the total number of mismatch simulations for each process index in the biquad library and 2N is the order of the synthesized filter. Repeating this for each process index, a total of P × P(M, N) filter samples can be created. If the filter uses different biquad designs for each stage, then it is possible to generate even higher number of samples. All permutations of biquads from r_i yields P × $P(M, 1)^N$ filter samples. The small-signal filter performance (filter transfer function) for the generated filter samples is calculated using (2).

VI. ESTIMATION OF LINEARITY (IIP_3) USING BIQUAD LIBRARY

There are well known equations to calculate linearity of cascaded systems, taking into account the gain and non-linearity of individual stages [23]. For example, the magnitude of third-order intermodulation distortion product (IM_3), A_{IP3}, of a cascaded system with three or more stages is given by

$$\frac{1}{A_{IP3}^2} = \frac{1}{A_{IP3,1}^2} + \frac{G_1^2}{A_{IP3,2}^2} + \frac{G_1^2 G_2^2}{A_{IP3,3}^2} + \cdots \tag{7}$$

where $A_{IP3,1-3}$ are input IP3 of stages 1−3, and G_1 and G_2 are the voltage gains for stage-1 and stage-2 respectively. However (7) assumes that the intermodulation products from different stages add in power and does not take into account the phase of the IM_3 products from different stages. As a result, the calculation does not yield accurate results. Fig. 7 shows the mechanism by which the intermodulation products generated in different stages interact with each other. Two fundamental frequency tones at f_1 and f_2, applied to the input goes through $\mathbf{H_1(f)}$ and $\mathbf{H_2(f)}$ to the output of the second stage. IM_3 products are generated by the first stage at frequencies f_3 and f_4. Similarly, IM_3 products are generated in stage-2 from the fundamental tones at its input. The total IM_3 at the output of the second stage is given by the vector sum of IM_3 propagated from stage-1 and the IM_3 generated in stage-2. At the output of stage-i, the IM_3 can be derived

$$\begin{aligned} |IM_3|_i = {} & |IM_3|_{i-1} \times G_i(f_3) \times \angle IM_{3,i-1} \\ & + |IM_3|_i \times G_{i-1}^2(f_1) \times G_{i-1}(f_2) \times \angle IM_{3,i} \\ & + 2 \times \theta_{i-1}(f_1) - \theta_{i-1}(f_2) \end{aligned} \tag{8}$$

where G_i is the voltage gain, $\theta_i(f_t)$ is the linear phase shift at (f_t), $|IM_3|_i$ is the magnitude and $\angle IM_{3,i}$ is the phase of IM_3 at stage-i. As shown in Fig. 7, the final non-linearity at the output of two stages can be expressed in terms of the non-linearity of individual stages and the appropriate frequency response of the different stages. By storing this information in the biquad library and extending this concept to N-stages, it is possible to accurately estimate the IIP_3 of a $2N^{th}$ biquad filter.

Filter synthesis described in Section-V scales the capacitors using (6) of the biquad library elements to realize the required filter. The final biquads in the synthesized filter will have different IM_3 characteristics compared to the elements in the biquad library since the cap scaling changes the Q and ω_0. Additionally, the frequencies at which the IM_3 in biquad library are characterized could be different from where the test-tones are applied for the filter use condition. Both these challenges can be addressed by performing a bilinear interpolation of the IM_3 magnitude and phase ($|IM_3|$ and $\angle IM_3$) from a grid of Q and normalized test-tone frequency, f_{norm}, of the selected filter biquad sample as shown in Fig. 8. Since the IM_3 magnitude and phase varies with process and mismatch, it is important to note that the bilinear interpolation has to be performed on each process and mismatch indexed biquad.

Multiple filter samples around the design average can be generated by bootstrapping as described in section-V and the synthesis of multiple filter IIP_3 response is shown in Fig. 9.

This section outlined the use of bootstrap sampling of the biquad standard-cells in a filter design. Scaling and interpolation of biquad characterization data reflects the cell's use in specific filter designs. In the next section, efficient bootstrap filter sampling is used to permit sufficient sample sizes to obtain statistically meaningful manufacturing FoMs such as AC and IIP_3 yield loss or customer defect level.

VII. RESULTS: COMPARISON OF DESIGN ALTERNATIVES

Two filter design alternatives are used throughout the paper. The two design alternatives —a *4th*-order 1dB ripple Chebyshev filter and an *8th*-order Butterworth filter— meet the same requirements in use and are tested to the same specification. Test and use specifications are summarized in Table-1. The use requirement low-pass are shown with the dashed lines in figure 10(a-b). The ideal filter transfer functions are shown as the bold trace. The *4th*-order Chebyshev and *8th*-order Butterworth are designed based on a

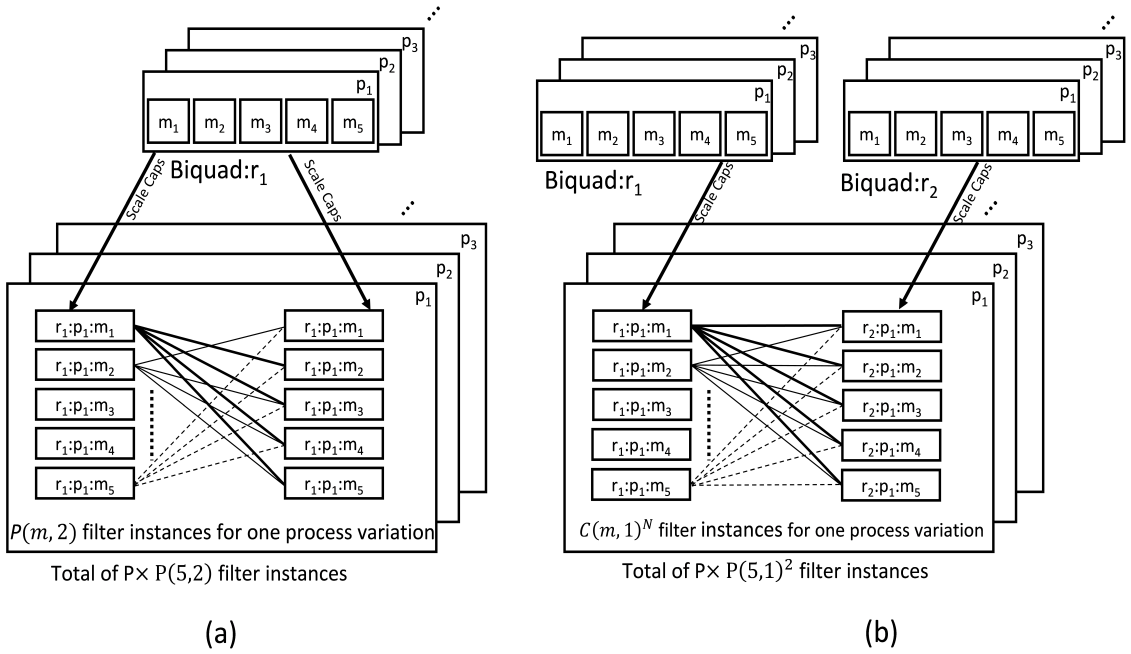
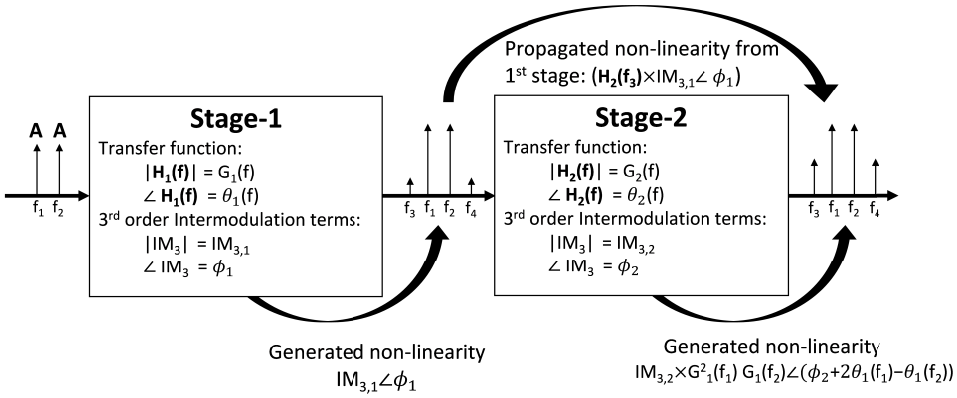


FIGURE 6. Generating multiple filter samples using bootstrap sampling for 4th-order filter (a) using biquads from the same biquad design r_1 and (b) using biquads scaled from different biquad designs, r_1 and r_2.



Frequency	Input	Stage-1 Output	Stage-2 Output
f_1	A∠0	$A\times G_1(f_1)\angle\theta_1(f_1)$	$A\times G_1(f_1)G_2(f_1)\angle(\theta_1(f_1)+\theta_2(f_1))$
f_2	A∠0	$A\times G_2(f_2)\angle\theta_2(f_2)$	$A\times G_1(f_2)G_2(f_2)\angle(\theta_1(f_2)+\theta_2(f_2))$
$f_3 (=2f_1 - f_2)$	0∠0	$IM_{3,1}\angle\phi_1$	$IM_{3,1}\times G_2(f_3)\angle(\phi_1+\theta_2(f_3))$ + $IM_{3,2}\times G^2_1(f_1)\, G_1(f_2)\angle(\phi_2+2\theta_1(f_1)-\theta_1(f_2))$

FIGURE 7. Modeling of IM_3 for cascaded stages using magnitude and phase of the generated and propagated IM_3 terms from different stages.

common library of pre-characterized biquad building block. The component biquad ideal transfer functions are included in figure 10.

Each filter's biquad library usage and biquad parameters are summarized in Table-2. In general, many library biquad building block could be selected to complete a given filter's design. In this paper, specific biquad choices (and biquad ordering) were made to highlight important features of design scaling, performance estimation and the computation of manufacturing statistical Figures-of-Merit (FoM). The biquad ordering determines the AC signal flow from input to output. The filter's input is accepted by biquad #1 and continues, in sequence, to biquad #N which delivers the filter's output. The maximum value of N is set by the filter order. The filter biquad ordering is from minimum to maximum Q.

Section-V explains the flexibility to set biquad Q, and ω_0 is achieved by scaling two biquad design capacitors, C_1 and C_2. In Table-2 each component biquad $S_{1\#c}$ and $S_{2\#c}$ scaling

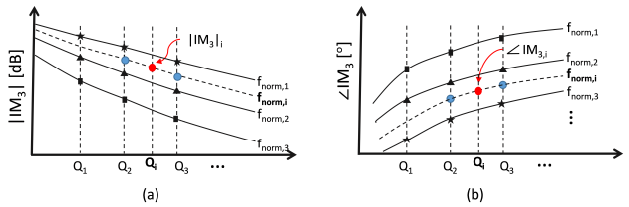


FIGURE 8. Bilinear interpolation for (a) IM_3 magnitude and (b) IM_3 phase at arbitrary (Q_i, f_i) for a single process and mismatch indexed biquad sample.

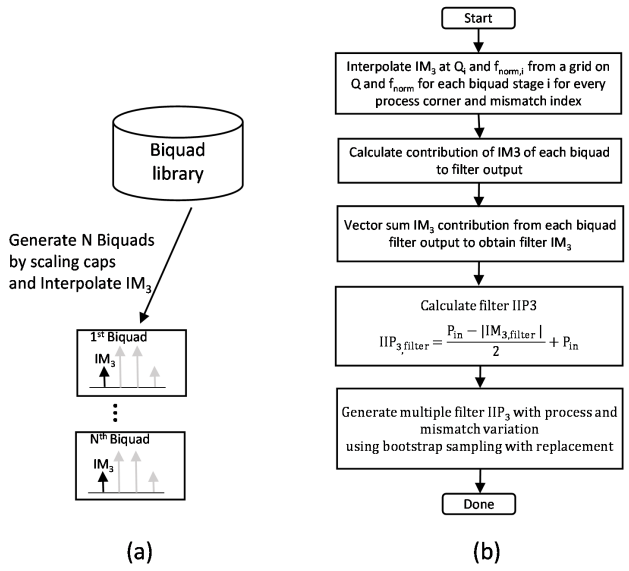


FIGURE 9. Flow chart for (a) generating biquad IM_3 in synthesized filter and (b) calculating filter IIP_3.

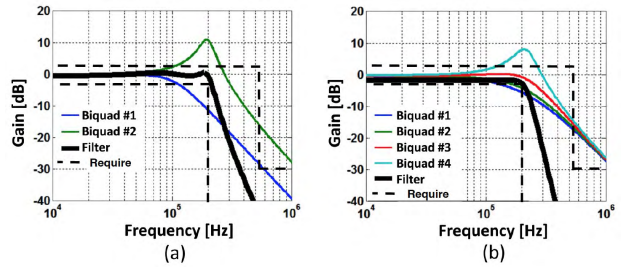


FIGURE 10. Ideal filter transfer functions (a) *4th*-order Chebyshev and (b) *8th*-order Butterworth. Additional plots are library biquad component transfer functions after scaling to filter design specifications. Use requirement upper and lower magnitude brick-walls are shown as dashed lines.

parameter values (and each biquad's capacitor values) are given.

The filter generation methodology described in Section-V is used to create 250 filter samples each for the *4th*-order Chebyshev filter and *8th*-order Butterworth filter and estimate each sample's AC and IM_3 (and related IIP_3) response. Sample size is an important consideration when deciding which of design alternative meets manufacturing yield and quality requirements. Roughly speaking larger sample sizes increase decision confidence. For a given sample

TABLE 2. Filter design specifications and Biquad library usage.

	Filter Design Alternative					
Filter	4th-Cheb		8th-Butter			
Biquad (#c)	#1	#2	#1	#2	#3	#4
$K_{\#c}$[V/V]	0.944	0.944	1.000	1.000	1.000	1.000
$Q_{\#c}$	0.785	3.559	0.510	0.601	0.900	2.563
$f_{p\#c}$ [kHz]	106	199	218	218	218	218
$S_1 \cdot C_1$ [pF]	237	1057	78	87	134	550
$S_2 \cdot C_2$ [pF]	287	72	219	185	120	58
Library	**#1**	**#2**	**#1**	**#2**	**#3**	**#4**
Gm	1:1:1:1	4:1:4:1	1:1:1:1	1:1:1:1	1:1:1:1	2:1:2:1
C_1 [pF]	140	540	140	135	135	270
C_2 [pF]	67	270	270	270	135	135
S_1	1.691	1.953	0.541	0.642	0.989	2.032
S_2	4.247	0.266	0.810	0.683	0.887	0.427
OTA transconductance base value, g_m=170uS						

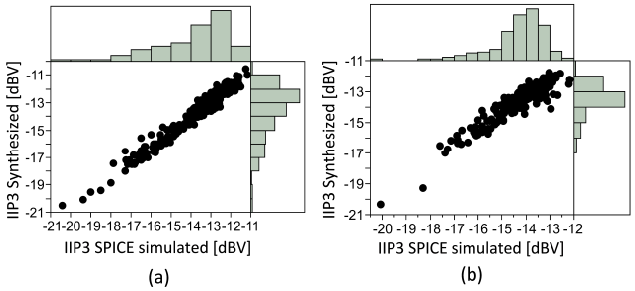


FIGURE 11. (a) *4th*-order Chebyshev and (b) *8th*-order Butterworth. Filter design alternatives IIP_3 values are compared by scatter-plot and by marginal histograms. Each simulation and estimate use 250 filter samples. SPICE IIP_3 evaluation is from transient analysis. IIP_3 estimates are from interpolation. IIP_3 center frequency is 140kHz for both filters.

size the design alternative with fewer test fails is the design alternative with higher manufacturing yield. Similarly, customer quality level increases with the design alternative that has fewer test escapes. For a sample size of 250, a greater than 90% confidence level for yield and quality FoMs is possible when test fails or test escapes counts are less than ten.

To select a filter design without direct SPICE simulation requires validation of the alternative bootstrap estimates to the traditional SPICE simulation. Building block characterization data for AC and inter-modulation were used to compute bootstrap estimates which were compared to results obtained from SPICE simulation. Sets of sample filters were assembled by scaling a bootstrap selected samples of biquad standard-cells. To permit direct comparison, the generation of each filter sample netlist was carefully controlled and bootstrap and SPICE netlists were manually confirmed to be identical. AC validation was established by matching the bootstrap transfer function to corresponding SPICE simulated transfer function. The AC SPICE simulated $H_F(s)$ and estimated by the cascade scaled biquads (2) matched with an absolute error of less than 1 part in 10^7 across all frequencies in the passband and in the stopband.

Bootstrap estimation of filter inter-modulation based on pre-characterized biquad introduces two potential

TABLE 3. IIP_3 correlation between SPICE and semi-custom.

		Filter Design Alternative			
		4th-Cheb		8th-Butter	
Center Frequency [kHz]		100	140	100	140
IIP3 Median [dB]	SPICE	-13.5	-13.3	-14.2	14.1
	Synthesis	-13.5	-13.4	-13.8	13.3
Std. Dev. IIP3 [dB]	SPICE	1.1	1.7	1.1	0.9
	Synthesis	1.1	1.9	1.2	0.9
Synthesis vs. SPICE Correlation		0.98	0.97	0.80	0.93

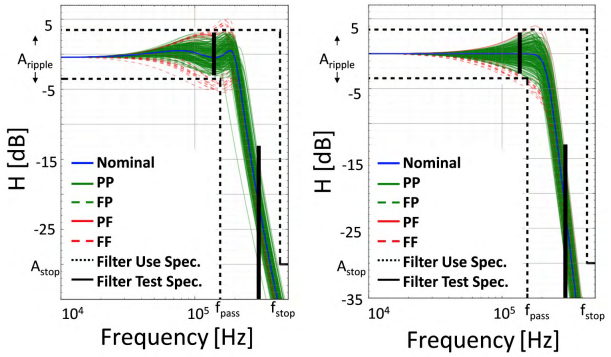


FIGURE 12. AC transfer functions of 1200 samples of two filter design alternatives (a) *4th*-order Chebyshev (b) *8th*-order Butterworth. Each filter is DC trimmed to 0dB at test. Black vertical bars locate test frequency and magnitude specifications. Passband test guard-band is 0.5dB @ 190kHz. Nominal trace denotes ideal AC response. Legend denotes results of test and use, see Table 1. For example, PF denotes pass at test and fail in use. Use specifications are the dashed lines.

sources of miscorrelation to direct SPICE filter simulation. 1) Pre-characterization set equal test-tone power levels whereas within the filter the power levels may be different. The power difference is greatest when the test-tone center-frequency is near the filter's low-pass pass-band edge. 2) Pre-characterization IM_3 data is collected for a limited number of specific test-tone frequencies and offsets and biquad Q and cut-off frequencies.

Validation of filter bootstrap estimates of IM_3 used the correlation of IIP_3 at a center-frequency of 140kHz. Fig.11 (a) and (b) plots the bootstrap synthesized IIP_3 estimate versus SPICE for 250 samples each of the *4th*-order Chebyshev filter and the *8th*-order Butterworth. The plots emphasize the IIP_3 correlation (i.e. no significant outliers) and the four marginal histograms long-tailed structures. Table-3 summarizes statistics and correlation of the two different method's for computing IIP_3 for each filter design. The agreement of AC transfer functions and IIP_3 marginal distribution shapes and correlations ≥ 0.8 allows the computationally less demanding bootstrap estimates to replace exhaustive SPICE simulation as a means to estimate statistical FoMs for different filter designs.

The combination of test limits and use limits divides the manufactured filters into four bins (see Table-4 and Table-5). Test frequency selection and guard-band test limit settings are a trade-off between test-time and test-cost. Manufacturing yield loss (YL) from true fails and overkill (OK) and user observed defect level (DL) are FoM statistics that quantify the

TABLE 4. Filter comparison from AC manufacturing results.

		Filter Design Alternative	
	Bin	4th-Cheb	8th-Butter
Test/Use	F/F	23	13
	F/P	4	2
	P/F	4	3
	P/P	219	232
Yield Loss (YL)		**10.8%**	**6.0%**
Overkill (OK)		**1.6%**	**1.0%**
Defect Level (DL)		**1.8%**	**1.3%**

AC test frequencies 140kHz and 300kHz

trade-off between test and use. For the test and use settings, the four classification bin counts are used to compute YL (and the yield loss overkill component) and DL FoMs. (Eq. 1).

Bootstrap estimation and final design selection considered first AC response assessment of manufacturing yield and quality. Fig.12 (a) and (b) plots transfer function magnitudes for a bootstrap generated semi-custom *4th*-order Chebyshev filter and a *8th*-order Butterworth filter, respectively. The traces are coded by line style and color for PASS and FAIL at test (manufacturing yield FoM) and at use (quality FoM). For reference, the blue overlay trace is each filter's ideal (i.e. ideal OTAs and no manufacturing variation) transfer function. All green and red traces are filter transfer functions in the presence of non-ideal OTAs and process variation and transistor mismatch. Green traces denote filters which PASS all AC use specifications. Red traces denote test escape filters which FAIL one or more AC use specifications. Solid line traces denote filters which PASS test (PP or PF) and dashed line traces denote filters which FAIL one or more AC test specifications (FP or FF).

For the AC magnitude test, bootstrap estimated the *4th*-order Chebyshev filter yield loss is 1.5× greater than the *8th*-order Butterworth filter yield loss, Table-4. For the sample size, the filter defect levels are statistically insignificant. The computed bootstrap estimates of filter yield loss etc. are the result of non-ideal OTAs and manufacturing variation and not from random point defects. For example, the *4th*-order Chebyshev yield loss is largely explained by the one high-Q biquad stage increased sensitivity to device variation.

Estimatation of IIP_3 yield loss and defect level FoMs for the bootstrapped *4th*-order Chebyshev filter and the *8th*-order Butterworth show design selection may result in different trade-offs than the AC results. In Fig.13, filter IIP_3 estimates are plotted with test and use bin limits as lines. Each sample filter is a single dot. Fig.13 adopts the AC binning color scheme. The green shaded area surrounds the filters that PASS IIP_3 in use. The red area surrounds the filters that FAIL IIP_3 in test. The x-axis is a filter test IIP_3 estimate at guard-banded center-frequency = 140kHz. The test limit is plotted as a vertical (red) dashed line. The y-axis is the use IIP_3 estimate at center-frequency = 100kHz. The use limit is plotted as a horizontal solid (red) line. The limits divide

TABLE 5. IIP_3 manufacturing results.

	Bin	Filter Design Alternative 4th-Cheb	8th-Butter
Test/Use	F/F	6	3
	F/P	34	8
	P/F	2	9
	P/P	208	230
Yield Loss (YL)		**16%**	4.4%
Overkill (OK)		**13.6%**	3.2%
Defect Level (DL)		1.0%	**3.8%**

Test center frequency = 140kHz
Use center frequency = 100kHz

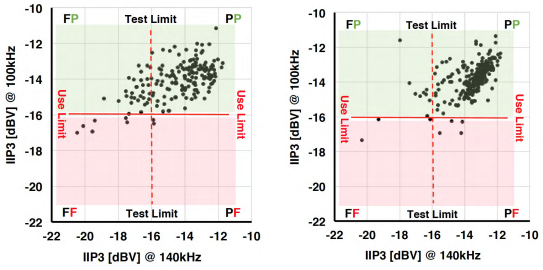


FIGURE 13. Bootstrap IIP_3 estimates for 250 (a) 4th-order Chebyshev filters and (b) 8th-order Butterworth filters. Use IIP_3 set the center-frequency test-tone =100kHz and at test guard-banded the center-frequency =140kHz. Frequency offset =∓ 2.5% of the center-frequency. Vertical and horizontal lines mark the IIP_3 test and use limits. Each dot 'ů' in FP and PF quadrants is a test escape or test overkill, respectively. Counts in FP and PF quadrants assess manufacturing risks from the miscorrelation of test and use.

sample filter responses into four distinct groups shown in the plots four corners.

The IIP_3 comparison for the test and use limits is summarized in Table-5. Yield loss for *4th*-order Chebyshev is 4× the Butterworth filter. Based on IIP_3 yield loss the preferred design alternative is the *8th*-order Butterworth. While the overall IIP_3 yield loss is consistent with the AC, the source of the loss is different. For both design alternatives the yield loss is the result of test overkill, that is the component of yield loss from the miscorrelation between test and use. Of particular concern is when test overkill is a large multiple of filters FAIL the IIP_3 limit at the guard-banded test center-frequency but meet IIP_3 at the use center-frequency. For example, in Table-5 *the 4th*-order Chebyshev has a 'kill ratio' of FP/FF=34/6 meaning 5 or 6 filters are removed as FAILs (and not shipped to the customer) for each true FAIL at use. Test escapes are assessed by customers as a defect level. The bootstrap estimates suggest in the customer view (that is for an SOC the performance in use) the *8th*-order Butterworth alternative has nearly 4× as many faulty units delivered downstream. The trade-off is balancing the choice of the guard-band center-frequency, different test limits or some combination to reduce the kill-ratio by the risk of increasing the number of test escapes (PF = 2 and = 9 for the two filters,

TABLE 6. Run time comparison SPICE and building block method.

250 Sample Statistics	Filter Design Alternative		
SPICE Run Time	**4th-Cheb**	**8th-Butter**	**Total**
AC	26s	77s	113s
IIP_3	3.2 hrs	6.3 hrs	9.5 hrs
Building Block Method Run Time	**4th-Cheb**	**8th-Butter**	**Total**
AC	2.6s	5.2s	7.8s
IIP_3	166s	332s	498s

respectively). The bootstrap reuse of Monte Carlo data of building blocks provides a consistency of estimation that can prove difficult to reproduce when each filter response estimate is modeled separately and correlation functions between responses parameterized.

The filter design using the biquad building blocks offers other benefits for design comparison. In the design description Table-2 the *4th*-order Chebyshev filter input biquad section was of type 1:1:1:1 and output section of type 4:1:4:1. The wider transistors in the latter biquad means the biquad requires about 4× more power. The *8th*-order Butterworth filter used three biquad sections of type 1:1:1:1 and one of type 2:1:2:1. By using more of the lower power 1:1:1:1 biquads, the *8th*-order Butterworth filter power consumption is SPICE estimated to be 137% of the *4th*-order Chebyshev and by comparing their biquad standard-cell counts 122%. Using capacitor area as the dominate layout component, the *8th*-order Butterworth filter area is ∼14% smaller than the *4th*-order Chebyshev filter.

The computation time for SPICE simulation and bootstrapped estimate of the FoMs is summarized in Table-6. To obtain the manufacturing statistics requires sufficient sample size and at the modest sizes used in this study, the difference in computational time is substantial. Using SPICE to compute one 250 sample is entire engineering work day, 9.5hrs. Using the building block method roughly 10mins.

Summarizing the entire FoM analysis for the two design alternatives leads one to select the *8th*-order Butterworth filter as the final design. This conclusion should not be confused with a recommendation that maximally-flat filters are in general the preferred design. Rather this conclusion demonstrates the potential of a coordinated semi-custom, biquad building block approach which includes sufficient characterization of the biquads to compare 5, 10 or 100 different filter design alternatives that meet the original use requirements and select the design which has the best chance of simultaneously meeting manufacturing, test and use requirements.

VIII. CONCLUSION

The paper demonstrated a computationally efficient methodology to give analog filter designers performance of different filter designs at test and at use condition and provide statistically significant manufacutring Figures-of-Merit. The foundation of the efficiency is the reuse of the

linear and non-linear response data from pre-characterized biquad building block library to manufacturing variation. Bootstrapped filter generation and reuse of building block SPICE simulations provides important manufacturing FoM statistics early in the design phase without SPICE simulation of each design alternative. Trends in multiple manufacturing FoMs provides as complete a picture as possible to all the stakeholders; system engineers, circuit engineers, manufacturing engineers and test engineers and reduces the risk of selecting an alternative which is more sensitive to advanced technology manufacturing variation. Yield loss and defect level FoMs allow design and test engineers to adjust limits to improve manufacturing test and product use correlation and gain the feel for a design alternative's sensitivity to manufacturing variation. Analyzing the trade-offs between different filter designs, specification settings, manufacturing yield and quality are essential when small analog filters are integrated into (a more expensive to produce) SoC or ASIC. The estimation of every possible filter design's yield and filter defect level requires accounting for non-idealities and for process variation and mismatch variation effects. Replacing intensive Monte Carlo SPICE simulations of each design alternative with bootstrap synthesis using the pre-characterized biquads from the library efficiently and quickly estimates the power, area and manufacturing and quality FoMs of any filter design alternative.

The biquad building block design is set by a small number of independent design degrees-of-freedom which can varied systematically for pre-characterization and Monte-Carlo samples of each set stored in a library. The low-cost of data storage allows linear and non-linear response of each Monte-Carlo sample of the building block to be stored and simple models developed to estimate both linear and non-linear responses of a random sample of each filter design alternative and preserve the inherent correlation between different responses without the use of ad-hoc and difficult to parametrize statistical models.

This paper describes design selection for manufacturability of analog circuits, specifically continuous-time filters. The methodology adapts to analog design the common practice of a standard-cell library in digital circuit design. The results demonstrate linear and non-linear response predictions for different design alternatives can select a preferred final design early in the design flow and reduce the risk of expensive design iterations. Future work is to establish the building block library and model to synthesize manufacturing FoM for other type of analog circuits. There are three rules suggested when exploring potential building blocks for any analog circuit under test (CUT): (i) repetitive common circuits found in CUT (ii) circuits that have similar architecture as the CUT (iii) combination of sub-circuits which can represent the CUT performance. The selection of building blocks is designed based on characterizing the building block's responses such as gain, bandwidth, linearity, noise and possibly others at different environmental conditions. The building block is identified that can best describe the CUT behavior. Potential analog circuits that could benefit from the methodology proposed are cascaded transimpedance amplifier, ring oscillators, ADCs and DACs, etc.

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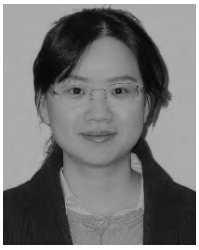

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