IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 20, 2019, accepted July 12, 2019, date of publication July 23, 2019, date of current version August 1, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2929088

A Frequency Multiplication Method Based on Extracting Harmonic From Narrow Pulse

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This work was supported in part by the Natural Science Basic Research Plan in Shaanxi Province of China under Grant 2018JM1025, in part by the National Natural Science Foundation of China under Grant 11403018, and in part by the Innovation and Entrepreneurship Training Program for College Students of China under Grant 2019271.

ABSTRACT Frequency multiplier is a nonlinear circuit that can realize frequency multiplication of input signal with wide application in communication, navigation, radar, and other fields. This paper proposes a frequency multiplication method based on extracting harmonic from a narrow pulse. Then, in accordance with this means, it develops a ten times frequency multiplier, finally achieving frequency multiplication taking the rubidium atomic frequency standard as a reference. The frequency multiplier possesses some features of high-efficient multiplication, low noise floor, simple structure, easy implementation, and cheaper cost. Based on the experimental results, if PRS10, the rubidium atomic frequency standard, is regarded as a reference, the noise floor of frequency multiplier is superior to $1.60E^{-}12$/s. Additionally, the relative frequency error of the output ten times the frequency multiplication signal (100 MHz) is less than $8.00E^{-}12$.

INDEX TERMS Frequency multiplication, narrow pulse, filter, stability, accuracy.

I. INTRODUCTION

Time is a basic physical quantity that characterizes the motion of matter. *Frequency*, which is a basic quantity closely related to time, denotes the number of periodic movements per unit time. Normally, time is generated and maintained by frequency standards. A frequency standard is a device used to provide a stable frequency signal at a particular frequency point. It should be noted that the accuracy of time is determined by that of frequency. Nowadays, the generation and maintenance of time or frequency play a significant role in supporting the development of information technology. It is also crucial in the field of national defense science and technology, national economic construction and social life. For example, navigation and positioning in satellite navigation systems are inseparable from high-precision time and frequency [1]–[4]. The basic working system is to adopt a multi-star ranging and distance rate of change measurement system, which realizes the user navigation and positioning based on the strict time synchronization of the on-board clock and the ground clock. Therefore, the precise time and frequency are a basic parameter necessary for the normal operation of the satellite navigation and positioning system, and have a very important status and role. It can be said that the time error of only 1 nanosecond will lead to the ground ranging error of 30 centimeter, so that the precision measurement of time determines the accuracy of navigation and positioning [5]–[8]. In addition, in the high-speed operation of logistics and information flow, the precision of time-frequency systems used in important fields such as communication, electric power, high-speed transportation, and Internet of things has reached the microsecond level, and the demand in individual fields has reached the nanosecond level [1], [9]–[11].

The high-stability crystal oscillator or atomic clock is the common frequency standard. Typically, these frequency standards have single and low output frequency, such as 5MHz or 10MHz. However, the stable and accurate reference frequency is required in many existing electronic systems. For example, Gao et al. present a multi-channel stripmap Synthetic Aperture Radar imaging system implemented on the platform of FPGA, in which the operating frequency is 100MHz [12]. Vishal et al. present an area-efficient frequency synthesizer for parallel wideband RF spectrum sensing in cognitive radios by using an Injection Locked Oscillator Cascade (ILOC). It happens that the ILOC uses an external

The associate editor coordinating the review of this manuscript and approving it for publication was Gian Domenico Licciardo.

FIGURE 1. The application fields of the frequency multiplier.

signal of 500MHz for its reference paper [13]. A novel Radio-Frequency Frequency-Modulated (RF-FM) signal generation method is proposed by the authors of [14]. In that prototype circuit, a 10MHz clock signal is multiplied by 20 using a phase locked loop within a DDS chip in order to achieve clock speeds suitable for RF generation. In [15], a partially integrated optical frequency synthesizer is reported, where a stable and low-noise frequency comb is used as the optical reference. In their design architecture, a heterodyne integrated Electro Optical Phase Locked Loop (EOPLL) phase-locks the tunable laser (TL) to the selected comb tooth. Under the phase lock condition, fine frequency tuning is performed by adjusting the frequency of an RF Local Oscillator (LO), and it is suggested that this LO be tuned more than 100MHz.

Therefore, it is of great practical significance to design circuit components with atomic clocks or crystal devices as the core to synthesize, transform, filter and amplify the frequency signals and generate and output stable higher frequency reference signal required by electronic system equipment, namely frequency multiplication, as shown in Fig.1.

The methods that achieve frequency multiplication can be roughly divided into two categories: 1, One is to lock the higher output frequency of voltage-controlled oscillator in the lower reference input frequency by using PLL, thereby achieving frequency multiplication; 2, The other is to use a nonlinear device to nonlinearly transform the waveform of the input signal, and then use the bandpass filter to select the desired harmonics to achieve frequency multiplication.

Different from the above methods, this paper proposes a frequency multiplication method based on extracting harmonic from narrow pulse. The low-frequency standard signal is divided into two channels, in which the phase of one signal is fine-tuned. The pulse synthesis circuit is designed to process the sinusoidal signal with a certain phase difference into a narrow pulse with a specific pulse width. A band pass filter is further designed to select the high harmonics of the narrow pulses. Finally, we design a low-noise drive amplifier circuit to achieve high gain output of frequency multiplication signal. The frequency multiplier developed based on this method has the characteristics of high frequency multiplication efficiency, low noise floor, simple structure, easy implementation and low cost, which is expected to provide technical reference for the field of time-frequency generation and maintenance engineering.

The rest of the paper is organized as follows. In Section 2, the traditional frequency multiplication methods are summarized and their advantages and disadvantages are analyzed. In Section 3, the basic principle of the new frequency multiplication methods are described. Section 4 gives the development of the frequency multiplier. The results of test experiments are given in Section 5. Section 6 concludes the paper.

II. TRADITIONAL FREQUENCY MULTIPLICATION METHODS

The traditional frequency multiplication methods can be roughly divided into two types, namely, a method based on phase locked loop and a method based on nonlinear components.

Phase-locked loop (PLL) is a basic component of a wide range of applications in modern electronic systems. It has the basic function of generating an oscillating signal in the loop, and the frequency of this signal is affected by the control voltage. When the loop is locked, the output frequency of the oscillating signal is exactly equal to the frequency of the input signal, and the phase difference between the two signals is maintained. Thus, signal tracking without frequency error is achieved. If the frequency divider is connected in the basic phase-locked loop, the frequency can be multiplied. The PLL multiplier has good narrow-band characteristics and low output noise. The disadvantage is that the circuit structure is complex and the debugging is difficult [16], [17].

The typical frequency multiplier using nonlinear devices has transistor monopole multiplier, step recovery diode frequency multiplier and varactor diode multiplier.

Transistor frequency multiplication is a common frequency multiplication method. The basic principle is to use the inherent nonlinearity of the voltage between the base and emitter of the transistor and the current transfer characteristic of the collector. The bias of the transistor and the excitation intensity of the input signal are appropriately selected. The current waveform of the collector contains the fundamental

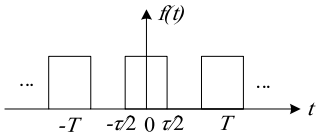


FIGURE 2. Waveform of a periodic rectangular pulse signal.

and every harmonic component of the wave of the input signal. Tuning the tuning loop of the frequency multiplier to the N-th harmonic frequency of the fundamental of the input signal, and the output of the transistor is obtained with the Nth harmonic frequency. Transistor frequency multipliers have good unidirectional, isolation and gain. The power of the frequency multiplier is inversely proportional to the square of octave frequency, and the octave frequency cannot be too high, generally 2-3 times [18], [19].

The typical step recovery diode frequency multiplier is generally composed of an input-output matching network, a pulse generator, a resonant frequency selection circuit and a bandpass filter. The signal of frequency fin is sent to the step recovery diode pulse generating circuit. The pulse generating circuit converts the energy of each input cycle into a large voltage narrow pulse, and the narrow pulse contains rich harmonics, which in turn excites the resonant circuit to convert the pulse into a N∗fin damped oscillating signal, and finally through the filter. The filter filters out unwanted harmonics and thus an equal amplitude frequency signal with an output frequency of N∗fin is obtained on the load. Step recovery diode frequency multipliers are frequently used in high-order and high-efficiency microwave frequency doubling [20], [21].

Varactor diode is a kind of nonlinear capacitive element. The varactor frequency multiplication uses the nonlinearity of the junction capacitance as a function of voltage to generate harmonics, thereby achieving frequency multiplication. The varactor diode multiplier generally consists of an input-output matching circuit, a filter circuit, an idle circuit and a bias circuit. Although power and efficiency of the varactor frequency multiplier are relatively large, the circuit structure of frequency multiplier is relatively complex and difficult to debug [22]– [24].

III. FREQUENCY MULTIPLICATION METHOD BASED ON EXTRACTING HARMONICS FROM NARROW PULSE

Different from the traditional frequency multiplication method, the method based on extracting harmonic from narrow pulse proposed in this paper is a new frequency multiplication method. The key technology is the generation of narrow pulse and the extraction of harmonics. In general, the method needs to generate appropriate narrow pulses and extract the desired harmonic signal with corresponding filters.

As shown in Fig.2, suppose f(t) is a periodic rectangular pulse signal with amplitude 1, pulse width τ, repetition period T, and angular frequency $\omega = 2\pi/\mathrm{T}$.

With the Fourier transform for the rectangular pulse, and the Fourier coefficient can be obtained as:

$$A = \int_{-T/2}^{T/2} f(t)e^{-k\omega\tau}dt = \frac{2\tau}{T}\left(\frac{\sin\frac{k\omega\tau}{2}}{\frac{k\omega\tau}{2}}\right) \tag{1}$$

Therefore, the kth harmonic amplitude of the rectangular pulse is:

$$A_k = \frac{2\tau}{T}\left(\frac{\sin\frac{k\omega\tau}{2}}{\frac{k\omega\tau}{2}}\right) = \frac{2\tau}{T}\left(\frac{\sin\frac{k\pi\tau}{T}}{\frac{k\pi\tau}{T}}\right) \tag{2}$$

According to the knowledge in the signal and system, in order to facilitate the selection of the required harmonic signals, it is necessary to select a suitable width of the rectangular pulse signal, and thus the amplitude of the harmonic signal to be selected is maximized for easy extraction.

Obviously, only when (2) takes the maximum value, the desired harmonic signals can be extracted according to the circuit. That is:

$$\sin\frac{k\omega\tau}{T} = 1 \tag{3}$$

Assuming that a 10MHz standard frequency signal is multiplied by 10 to obtain a 100MHz signal. It is first necessary to generate a narrow pulse of 10MHz and a 100MHz harmonic signal is extracted from the narrow pulse, that is, T = 100ns, K = 10. At this point, the correct pulse width can be calculated by the frequency multiplication principle:

$$\tau = \frac{T}{2k} = \frac{100ns}{2\times 10} = 5ns \tag{4}$$

Therefore, it is necessary to generate a narrow pulse with a pulse width of 5ns, and then extract a 100MHz harmonic signal with an appropriate filter and filter out other useless signals.

IV. DEVELOPMENT OF FREQUENCY MULTIPLIER

To verify the effectiveness of the frequency multiplication method based on extracting harmonic from narrow pulse proposed in this paper, a frequency multiplier is developed. The main points of the development are as follows.

A. STRUCTURAL DESIGN

Just as shown in Fig.3, the example of the frequency multiplier takes the rubidium oscillator PRS10 as a reference to achieve a 10-fold frequency multiplier, and output an accurate and stable sinusoidal signal of 100MHz. The PRS10 is an ultra-low phase noise, 10MHz rubidium-disciplined crystal oscillator. The system specifically includes four circuit modules of the distribution amplifier, the narrow-pulse generator, the filter and the low-noise driver amplifier.

B. CIRCUIT DESIGN

1) DISTRIBUTION AMPLIFIER CIRCUIT

The present study applies the frequency allocation amplification technology to provide two accurate and stable signals for

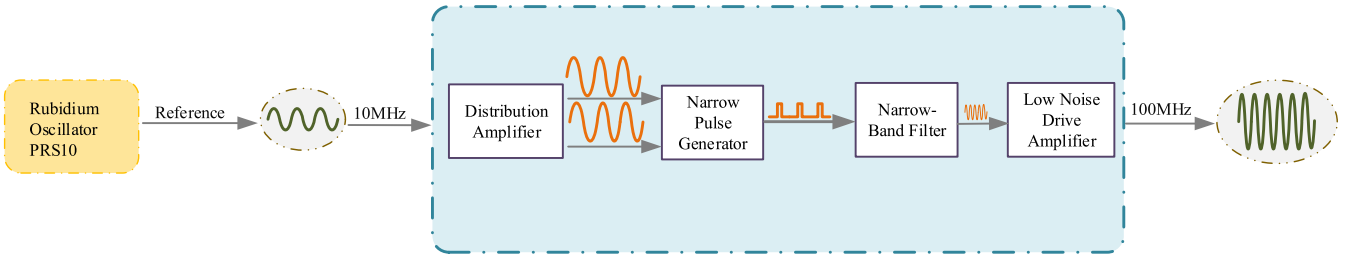


FIGURE 3. Circuit design block diagram.

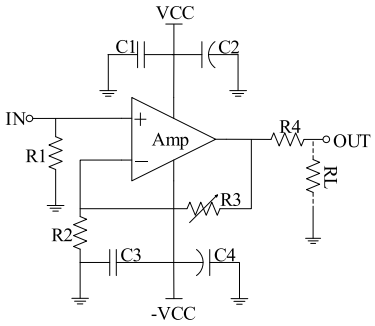


FIGURE 4. Core circuit of the frequency distribution amplifier.

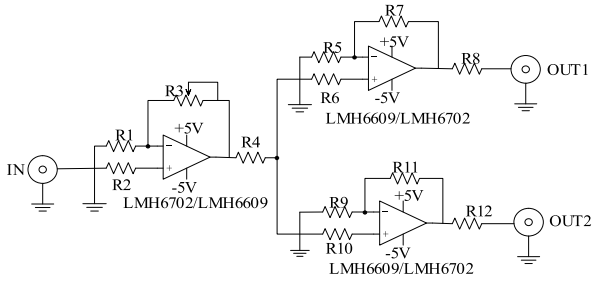


FIGURE 5. Schematic diagram of the distribution amplifier.

the latter stage of circuit. The frequency distribution amplifier circuit consists of one input and two output ports to amplify and distribute the 10MHz signal provided by rubidium oscillator PRS10 with low phase noise, thus providing two identical 10MHz standard signals for the latter stage. Besides, a negative feedback link is added to the amplifier circuit to stabilize the static operating point. Due to the existence of the GBW of the integrated operational amplifier, a part of the gain is sacrificed while the passband is widened. In addition, the effects of amplifier nonlinearities and internal noise can also be reduced. The schematic diagram of the basic circuit is shown in Fig.4, where the Amp is operational amplifier.

The calculation formula of the voltage amplification factor can be obtained from Fig. 4:

$$\frac{u_o}{u_i} = \frac{R_L(R_2 + R_3)}{R_2(R_4 + R_L)} \tag{5}$$

According to the core circuit, a distribution amplifier circuit that complies with the frequency multiplier is designed. Due to LMH6609 and LMH6702 have good waveform output and low noise. Meanwhile, the amplification capacity and parameters of the two chips are similar, so both of LMH6609 and

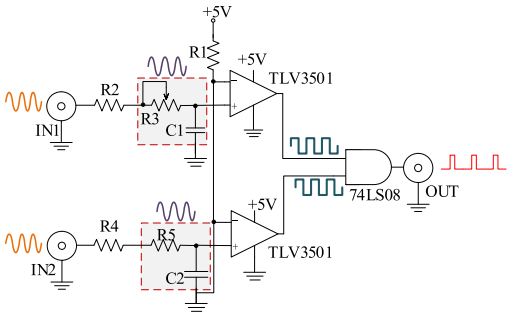


FIGURE 6. Narrow pulse generation circuit.

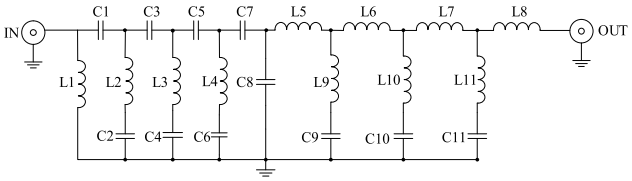


FIGURE 7. Schematic diagram of band pass filter.

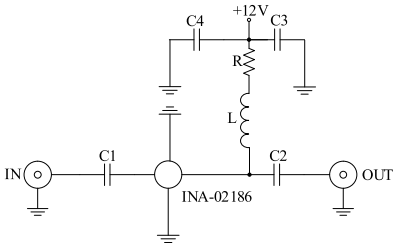
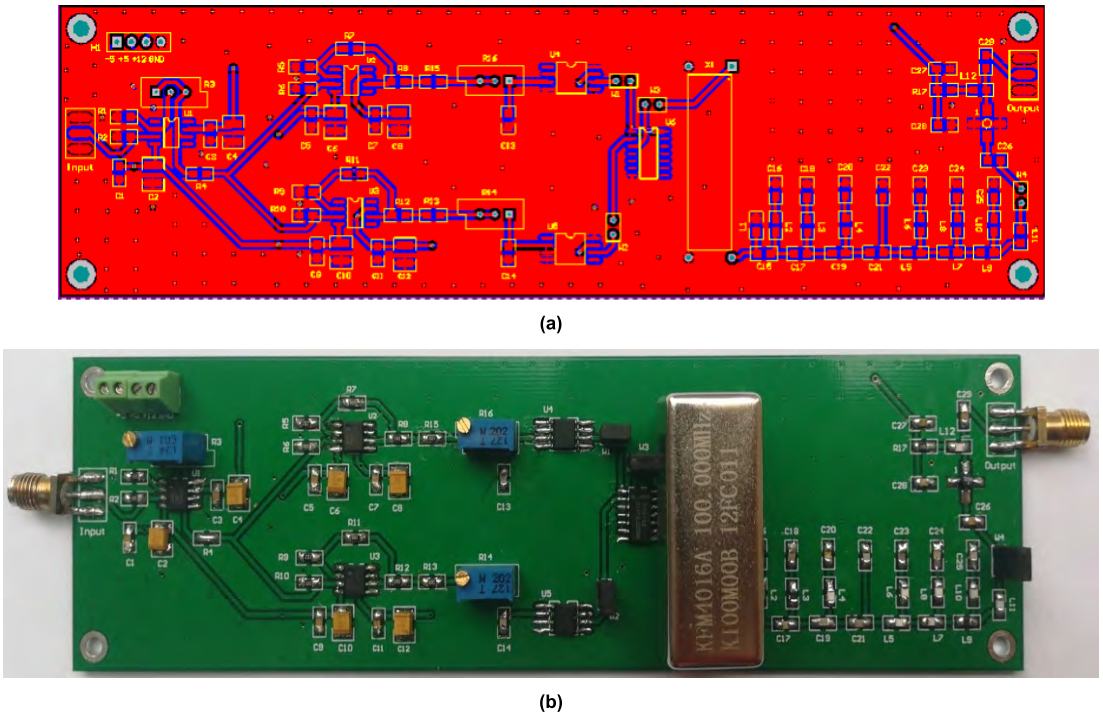


FIGURE 8. Schematic diagram of low-noise driving amplifier circuit.

LMH6702 are good choices in our design. The voltage series of negative feedback method is adopted to amplify and distribute the10MHz reference signal. Fig.5presents the schematic diagram of the circuit.

2) NARROW PULSE GENERATOR CIRCUIT

An appropriate pulse width can be conductive to extracting the corresponding harmonic signal. The shorter the duration of the pulse, the wider the bandwidth expanded by the pulse. In the current work, a 5ns narrow pulse generation circuit is designed. The schematic diagram of the circuit is shown in Fig.6, in which R3, C1 and R5, C2 are phase-shifting networks, and they can shift the phase. The two identical 10MHz sine wave signals from the distribution amplifier are input into the voltage comparator to generate a square



(a)

(b)

FIGURE 9. Photograph of the frequency multiplier: (a) PCB photograph and (b) Physical photograph.

wave with phase difference, which is sent to the high-speed AND gate to generate extremely narrow pulses. In addition, TLV3501 chip is used in the circuit as the voltage comparator and the 74LS08 is used as the high-speed AND gate chip. These two chips have a short delay time and a relatively fast speed, which is quite advantageous for the generation of extremely narrow pulses as well as facilitates the extraction of subsequent harmonics.

3) FILTER CIRCUIT

Extracting harmonic is the key technology in the current study and thus the filter circuit is the core of the circuit system. In this paper, a filter circuit composed of a crystal filter and a band-pass filter is employed to extract the harmonics. In this circuit, the crystal filter KFM4016A exerts a major role in extracting harmonic. However, it is observed by the spectrum analyzer that some near-end spurious harmonics exist in the extracted signal through the crystal filter. Therefore, a 90-100MHz band pass filter circuit is connected in series behind the crystal filter so as to extract the 100MHz harmonics with very stable and accurate frequency. Fig.7 shows the schematic diagram of the band-pass filter circuit.

4) LOW NOISE DIVER AMPLIFIER CIRCUIT

High frequency reference signals usually have strict requirements for the frequency and amplitude of signals. Due to the attenuation effect of the filter circuit, the amplitude of the harmonic signal extracted by the narrow-band filter is relatively low, only over 30 millivolts, and the driving ability is low, so the signal must be amplified. However, on the premise of low noise, noise coefficient and gain of the amplifier must be considered in the amplification of the signal. Meanwhile, due to the volatility of the RF circuit, the stability and standing wave ratio of the amplifier should also be taken into account. Therefore, more stringent requirements are put forward for the design of the high-frequency driving amplifier.

In this paper, a low-noise driving amplifier circuit is designed, and its schematic diagram is presented in Fig.8. Since the INA02186 is a low cost, low noise, large bandwidth and high gain amplifier with a typical noise figure of 2dB and bandwidth of 0.8GHz, the gain curve is extremely flat. It is designed for applications requiring high gain and low noise RF amplification. Consequently, microwave integrated circuit amplifier INA02186 is adopted to amplify the gain.

C. CIRCUIT MANUFACTURE

In order to improve the overall performance of the developed frequency multiplier, this paper combines the four module circuits designed in the previous section, draws the PCB board, and solders the circuit according to the circuit requirements, thus producing a multiplier with the frequency ranging from 10MHz to 100MHz. Fig.9shows the system PCB diagram and the hardware circuit diagram.

V. TEST EXPERIMENTS

According to the new frequency multiplication method proposed in this study, a frequency multiplier with the frequency ranging from 10MHz to 100MHz is developed. In this section, the feasibility of the proposed method is verified through the verification of the frequency

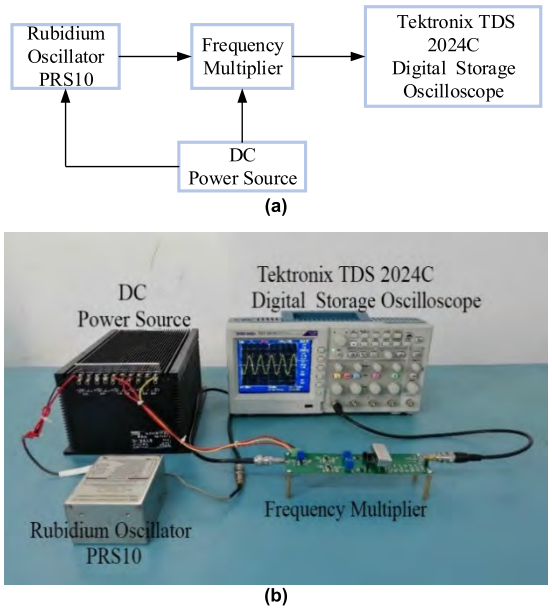


FIGURE 10. Experimental platform tested with oscilloscope: (a) Block diagram of experimental platform and (b) Photograph of the experimental platform.

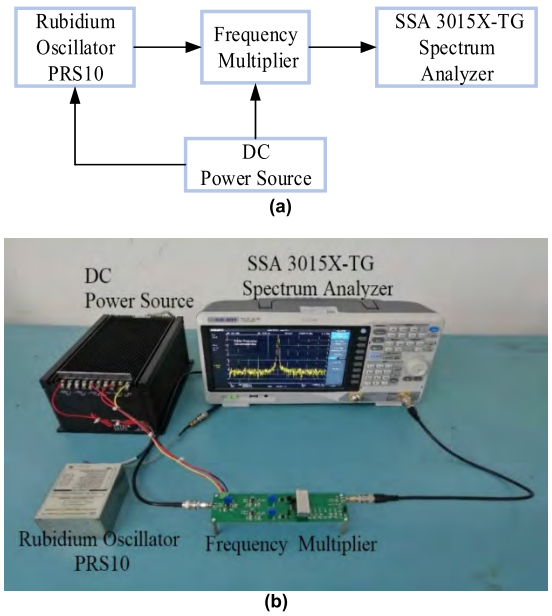


FIGURE 11. Experimental platform tested with spectrum analyzer: (a) Block diagram of experimental platform and (b) Photograph of the experimental platform.

multiplier's performance. Specifically, under the condition of indoor temperature, the performance of the frequency multiplier is evaluated through the construction of different experimental platforms and the measurement of three indicators: including signal waveform, frequency accuracy and noise floor.

A. WAVEFORM AND SPECTRAL PURITY

The waveform, amplitude and frequency of signal can reflect intuitively the feasibility of frequency multiplier. In the present study, the oscilloscope and spectrum analyzer are respectively used to build an experimental test platform to test the output signal of the frequency multiplier. Fig.10 shows the block diagram of the specific test device, and Fig.11 presents the experimental test platform diagram.

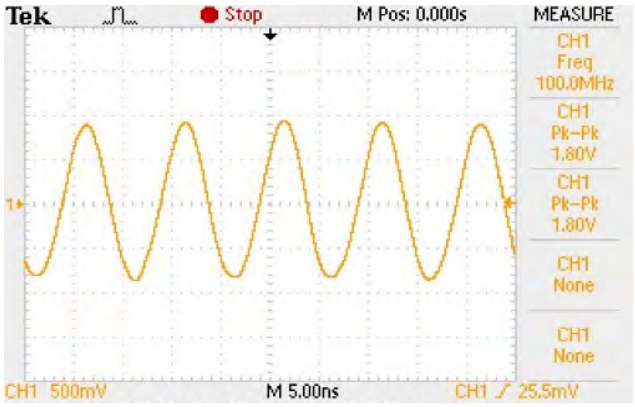


FIGURE 12. Output signal waveform diagram.

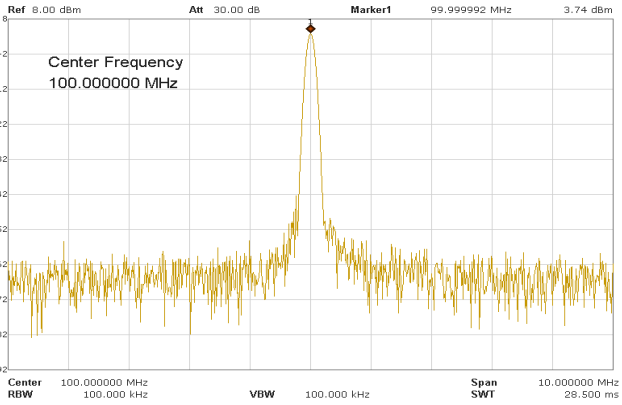


FIGURE 13. Output signal spectrum diagram.

The 10MHz signal output from the rubidium oscillator PRS10 provides an input reference for the experiment. The test results can be found in Fig.12 and Fig.13.

The output is the standard sine wave signal with the amplitude of 1.8V and the frequency of 100MHz. The noise floor is constant, and the waveform is pure while there is no other interference distortion. The experimental results demonstrate that the frequency multiplier can have10 times of the frequency. While the output is RC parallel load, the output amplitude has been reduced, and the nonlinear load affects the frequency of the output current.

B. ACCURACY

Accuracy is an important indicator to measure the performance of the frequency multiplier, and frequency accuracy is the maximum amplitude of the frequency offset. The higher the accuracy, the smaller the frequency deviation and the higher the precision of the frequency multiplier. In this paper, an experimental test platform is built. The block dia-

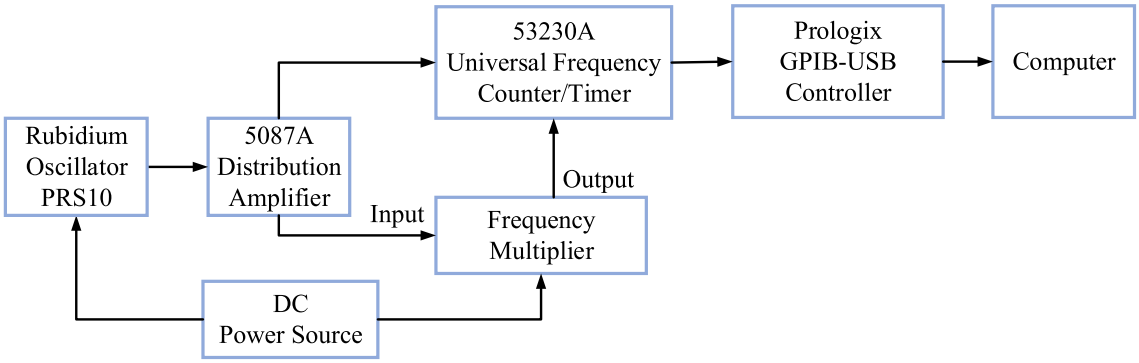


FIGURE 14. Experimental test block diagram.

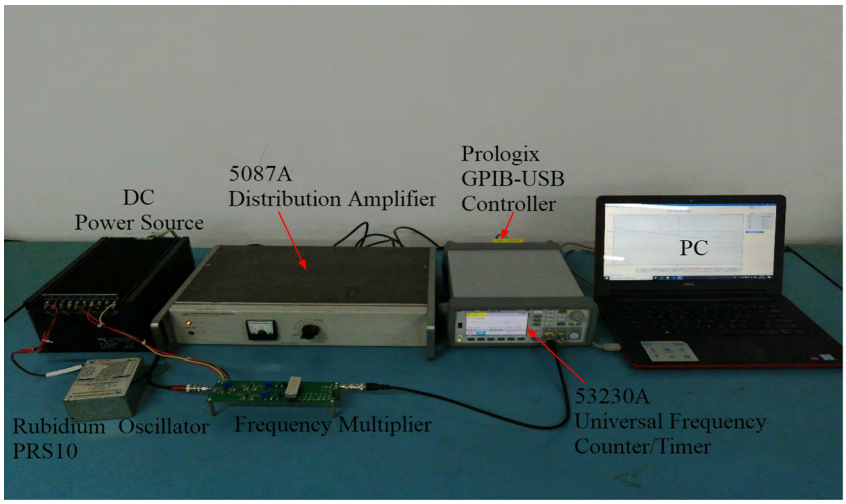


FIGURE 15. Experimental test platform.

gram of the experimental device is shown in Fig.14, and Fig.15 presents the experimental platform to measure the accuracy.

Since the Rubidium Oscillator PRS10 does not provide a perfectly accurate 10MHz signal, there are certain errors in the output of the frequency multiplier. Table 1 and Fig.16 show the accuracy measurement results by employing the homologous method. Agilent 53230A is used as the measuring instrument. Obviously, the frequency relative error of the output signal of the frequency multiplier is less than 8.00E-12. Therefore, the error is small, the accuracy is high, and the expected index is reached, satisfying the design requirements of the frequency multiplier. In engineering applications, if cesium atomic clock provides a better 10MHz reference signal, frequency multiplication signal with higher accuracy can be obtained.

TABLE 1. Frequency difference data.

Avg Time (s)	Frequency (Hz)	Relative Error
1	99 999 999.999 216 497	-7.84E-12
3	99 999 999.999 201 596	-7.98E-12
10	99 999 999.999 280 304	-7.20E-12
30	99 999 999.999 234 021	-7.66E-12
100	99 999 999.999 260 828	-7.39E-12
300	99 999 999.999 277 130	-7.23E-12
1000	99 999 999.999 277 934	-7.22E-12
3000	99 999 999.999 273 375	-7.27E-12
10000	99 999 999.999 280 691	-7.19E-12

C. NOISE FLOOR

Another important performance indicator of the frequency multiplier is the noise floor, which usually refers to any interference in the electronic system that has nothing to do with the presence or absence of a signal. In the field of time-frequency measurement and control, it is usually characterized by the short-term stability of the output signal of the measured object. Frequency stability is the degree of random fluctuation of frequency in unit time interval, indicating the ability to maintain frequency. Due to the influence of flicker noise on the frequency source, the classical variance has serious defects in characterizing the frequency stability. Consequently, Allan variance is adopted as the mathematical representation of frequency stability and noise floor the current work. The specific device block diagram and experimen-

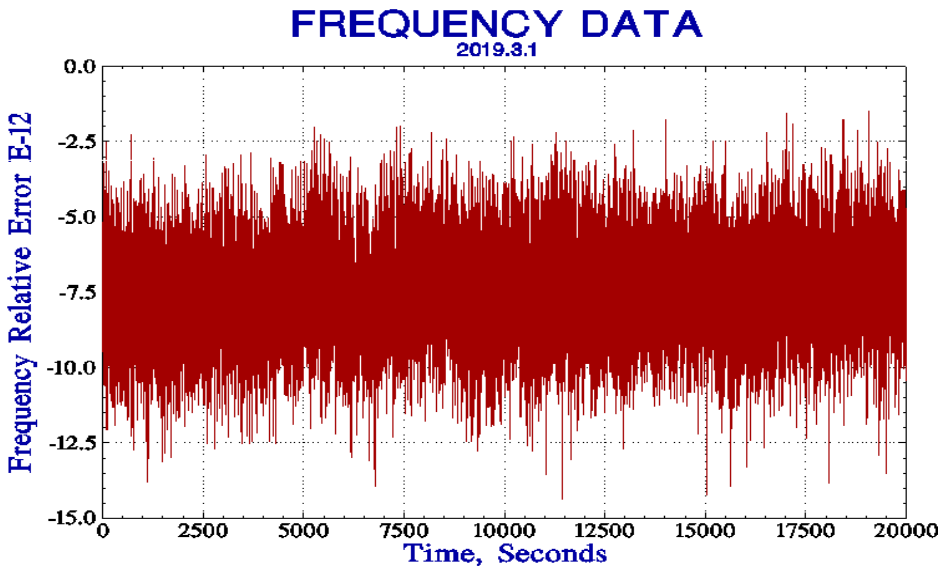


FIGURE 16. Frequency accuracy.

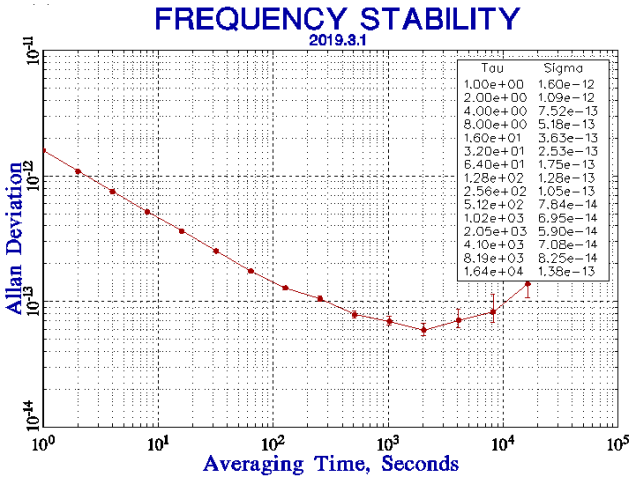


FIGURE 17. Frequency Stability.

TABLE 2. Test results of frequency doubler.

Name	Unit	Specification
frequency	MHz	100.00
Amplitude	V	1.80
Noise Floor	s^{-1}	1.60E-12
Relative Frequency Error	–	8.00E-12

tal test platform are shown in Fig.14 and Fig.15, respectively. The noise floor of the frequency multiplier obtained through the homologous method measurement is shown in Fig.17 and is approximately 1.60E-12/s.

D. TEST RESULTS

According to the test scheme, the performance indicators of the frequency multiplier are tested. All the results are tested under the condition of 50Ω linear load, and the test results are shown in the following table:

As can be seen from the test results in Table II, the frequency multiplier developed in this paper achieves high efficiency multiplication from 10MHz to 100MHz, with low noise floor and high output frequency accuracy, proving that the frequency multiplication method based on extracting harmonic from narrow pulse proposed in this paper is effective and feasible.

VI. CONCLUSION

As the frequency reference of electronic system, the frequency reference source is a vital part consisting of the modern electronic system. Therefore, it is of great practical significance to study the frequency multiplication method where the reference frequency of high-frequency points is obtained. In this paper, there is a frequency multiplication method on basis of extracting harmonic from narrow pulse. To verify how effective this method is, this paper designs a distribution amplification circuit, a narrow pulse generation circuit, a filter circuit and a low-noise drive amplifier circuit, and develops a 10 times frequency multiplier. The frequency multiplier takes the 10MHz signal provided by Rubidium Oscillator PRS10 as reference to output the signal of 100MHz under high-efficient multiplication. The experimental results show that the noise floor of frequency multiplier is about 1.60E-12/s, the waveform is pure without distortion when 100MHz signal is output, and the relative error is less than 8.00E-12. Thus, the design theory of frequency multiplication method is proved to be correct and technically feasible. At the same time, it is featured by high-efficient doubling efficiency, low noise floor, simple structure, easy implementation and cheaper cost. Therefore, it is expected to provide technical reference for time-frequency generation and maintenance engineering.

Simultaneously, there exists huge room for the improvement of this design at technical level, as follows:

(1) The filter design with smaller attenuation coefficient and better bandpass selectivity is conductive to choosing higher harmonics and further improving the frequency multiplication efficiency. In the future, we are willing to research on active filters for extracting harmonic.

(2) The design of the distribution amplifier circuit with lower noise: The distributive amplifier circuit is located at the front of the whole circuit, and its optimization design of noise index plays a particularly significant role in improving the noise floor of frequency multiplier.

(3) Electromagnetic compatibility design: With increasing frequency of output signal of frequency multiplier, the EMC design during circuit implementation becomes more and more important. It is essential to consider the selection of active components, the reasonable layout of PCB circuit, transient disturbance suppression and necessary shielding to further improve the performance of frequency multiplier.

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