IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received July 2, 2019, accepted July 9, 2019, date of publication July 23, 2019, date of current version August 8, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2930595

Systematic Design of Bandgap Voltage Reference Using Precomputed Lookup Tables

HESHAM OMRAN, MOHAMED H. AMER, AND AHMED M. MANSOUR
Integrated Circuits Laboratory (ICL), Faculty of Engineering, Ain Shams University, Cairo 11517, Egypt

Corresponding author: Hesham Omran (hesham.omran@eng.asu.edu.eg)

This work was supported by the Information Technology Industry Development Agency (ITIDA) under Grant PRP2018.R24.7.

ABSTRACT Bandgap voltage references are indispensable in any analog/mixed-signal system. In this paper, we introduce a systematic gm/ID-based procedure to design a CMOS bandgap reference. The proposed iterative methodology relies on one-time-generated precomputed lookup tables (LUTs); thus, it does not require invoking a simulator in the loop. Despite the inherent finite accuracy of the LUT-based design approach, we demonstrate that a precision bandgap circuit can be designed with less than 1-ppm error. We verified the proposed procedure against the Spectre simulations and probed the design space using a symbolic circuit solver. Moreover, we demonstrated how variations and mismatch can be taken into account in the context of the proposed methodology. The results demonstrate that the proposed procedure can provide very accurate results in a short execution time, enabling the designer to explore the design space of key performance metrics, such as power-supply rejection (PSR) and noise.

INDEX TERMS Systematic analog design, gm/ID methodology, bandgap voltage reference, PSR, noise, corners, mismatch.

I. INTRODUCTION

Although the exponential expansion of electronics is dominated by digital circuits, analog circuitry is usually the bottleneck in design cost and time. Commonly, the analog designer employs his intuition and expertise to reach a rough starting point, then lots of tweaking follows using a circuit simulator (e.g., SPICE) until specifications are hopefully met. This tedious process must be repeated every time the specs or the technology changes. In addition, this ad-hoc methodology usually includes uninformed design decisions and leads to suboptimal solutions. The everlasting increase in demand, however, has been laying more aggressive requirements on product time-to-market, leading designers into a deadlock of increasing model and design complexities and tightening delivery intervals.

The advances in computer-aided analog design partially ameliorated both issues. Commercial CAD tools are capable of performing local and global optimization given proper user constraints. However, they rely on invoking the simulator at every iteration, resulting in long runtimes, in addition to expensive software licenses. Fast-SPICE simulators and Verilog-A behavioral models can provide significant savings in runtime for large circuits; however, they come at the expense of accuracy and precision. Moreover, simulation-based optimization manifests a situation in which the designer is totally detached from the circuit he is trying to design in the first place. On the other hand, equation-based approaches can offer short execution time; however, with the increase in circuit and modeling complexities, expressions run out of hands, making the design procedure intractable, and obscuring any useful insight into the circuit's operation [1]–[3].

A worthy placeholder connecting the link between both extremes is the g_m/I_D methodology, introduced by Silveira *et al.* [4]. The g_m/I_D methodology is based on the notion of a set of reference devices and normalized quantities. It circumvents the complexity of the model equations by emphasizing that a device is just a geometry operated at specific width-independent design quantities. From that perspective, data extraction from a set of reference devices suffices to construct lookup tables (LUTs) that fully capture all possible realizations of such a device. Hence, the designer does not have to get troubled by the intricacies of post-design iterations and can devote his effort to develop a systematic and portable design procedure. Moreover, the methodology avoids multiple simulator calls which grants it a major speed edge over SPICE-in-the-loop techniques. Ever since, the methodology has been gaining an increasing popularity among designers, and has been extrapolated and studied in ways emphasizing

The associate editor coordinating the review of this manuscript and approving it for publication was Cihun-Siyong Gong.

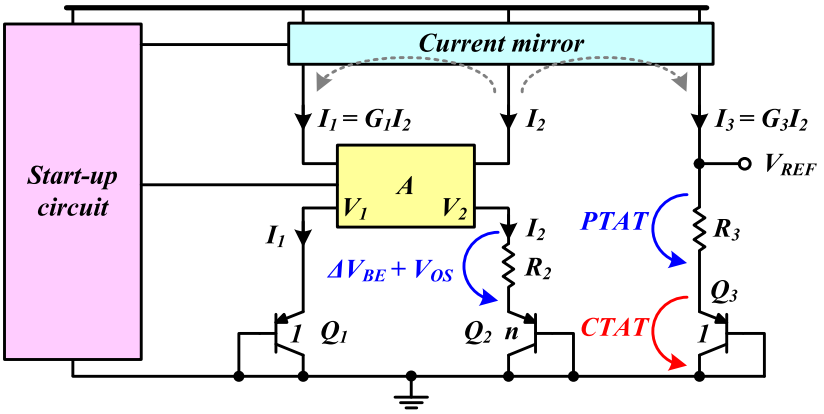

FIGURE 1. Generic bandgap voltage reference circuit.

the relation between its figures and various important circuit performance metrics [5]–[9]. For readers not familiar with the g_m/I_D methodology and design using precomputed LUTs, the tutorial introduction in [8] is recommended.

Voltage reference circuits are an integral part in any analog/mixed-signal system. Equation-based approaches for voltage reference design were reported in [10] and [11]. The authors used a simplified all-region analytical MOSFET models to perform the optimization. However, the process of model parameter extraction is cumbersome and error prone, especially noting that industry-standard MOSFET models used by semiconductor foundries are much more complicated than the simple analytical models. In addition, the performance of reference circuits is very sensitive to modeling errors; thus, parameter extraction errors are intolerable. A hybrid approach where equations and design-specific simulation charts are used to generate a design point was proposed in [12], but it considered the design of a current reference circuit. In addition, simulation-based optimization was still required to fine-tune the circuit parameters.

Although the use of the g_m/I_D methodology and precomputed LUTs can, in general, alleviate the drawbacks of the previous equation-based and simulation-based approaches, the systematic design of bandgap voltage references using precomputed LUTs is particularly difficult. First, the bandgap reference is a precision circuit; thus, any computation error due to the limited accuracy of the LUTs will render the design procedure useless. Second, the key requirement in a bandgap circuit is to cancel the temperature dependence, which may misleadingly indicate that the LUTs must be extracted at every temperature, resulting in an impractically inflated dataset. In this work, we propose a robust and efficient g_m/I_D-based systematic design procedure for bandgap voltage references that addresses the aforementioned problems. We demonstrate that extracting the LUTs at the temperature extremes in addition to the nominal point is totally sufficient. We also show that circuit effects that are not accounted for in simple textbook models can be efficiently incorporated into the design flow with ease due to the agnosticism of the methodology. We manifest the true power of the methodology represented in its ability to expose the whole design space of the circuit and place it into the hands of the designer in a very short time. Furthermore, we show how the effect of process corners and mismatch can be analyzed in the context of the proposed design methodology.

The rest of the paper is organized as follows: Sec. II demonstrates a systematic procedure to design the core of a bandgap circuit regardless of the implementation details. Sec. III details the design procedure of a complete CMOS bandgap circuit. Sec. IV discusses the effect of variations and mismatch. Sec. V presents detailed results and comparisons to validate the proposed procedure and illustrate its merits. Finally, conclusions are presented in Sec. VI.

II. SYSTEMATIC DESIGN OF GENERIC BANDGAP CORE

Consider the circuit shown in Fig. 1, which represents a generic realization of a basic bandgap voltage reference. The circuit has three branches numbered (1 to 3) from left to right. Q_{1-3} are substrate PNP BJTs available in any standard CMOS process. Q_2 is composed of n instances in parallel (typically 8 or 24 for layout considerations); thus, $V_{BE1} \neq V_{BE2}$. The A-block serves to equate the voltages at nodes V_1 and V_2, hence it imposes a voltage drop equal to ΔV_{BE} across R_2. The reference current $I_2 = \Delta V_{BE}/R_2$ is copied to the other two branches by a current mirror, forcing equal currents in all branches. Since the zero-current state (zero current in all branches) is another possible operating point for the circuit, a start-up circuit is necessary to drive the bandgap circuit out of this undesired state.

Using the simple BJT exponential model, it can be easily shown that ΔV_{BE} is proportional-to-absolute-temperature (PTAT). Consequently, the currents flowing in all branches are PTAT. As a result, a PTAT voltage is developed across R_3. On the other hand, $|V_{BE}|$ itself has a complementary-to-absolute-temperature (CTAT) behavior. The bandgap circuit output V_{REF} is the sum of the PTAT and CTAT voltages

$$V_{REF} = \frac{\Delta V_{BE}}{R_2} \cdot R_3 + |V_{BE3}| . \quad (1)$$

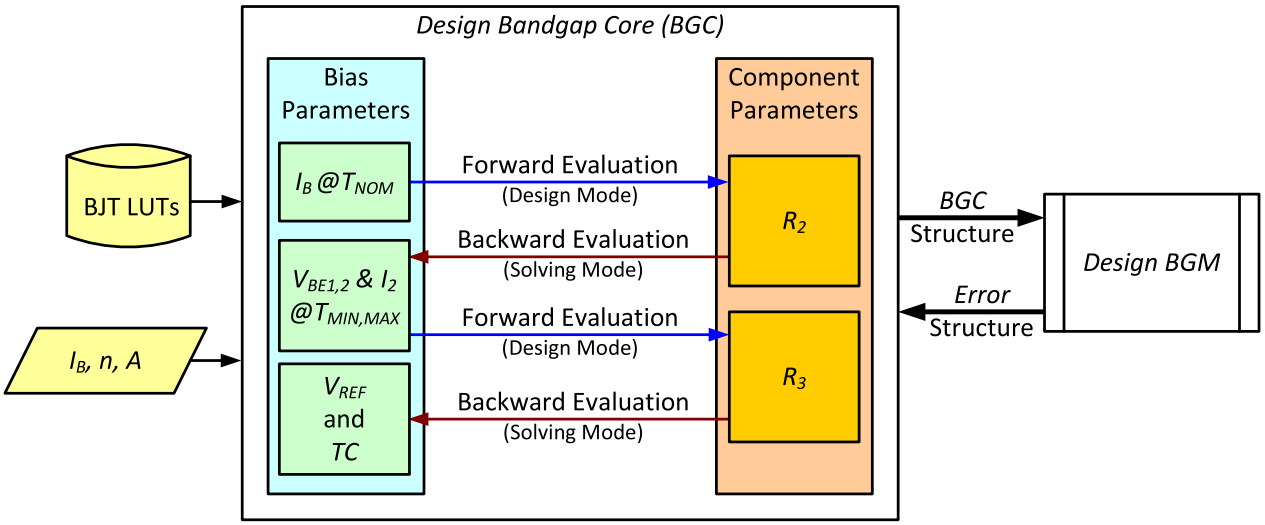

FIGURE 2. Simplified illustration for the *"Design bandgap core (BGC)"* function.

Therefore, V_{REF} can be made temperature independent by properly selecting R_3 to satisfy

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_3}{R_2}\frac{\partial \Delta V_{BE}}{\partial T} + \frac{\partial |V_{BE3}|}{\partial T} = 0. \tag{2}$$

Since the temperature coefficient (TC) of the PTAT and CTAT voltages is itself temperature dependent, perfect cancellation (i.e., satisfying (2)) can only be achieved at a single temperature (e.g., T_{NOM}). The overall bandgap TC in ppm over a temperature range from T_{MIN} to T_{MAX} is defined as

$$TC\ (ppm) = \frac{10^6}{V_{REF,T_{NOM}}} \cdot \frac{V_{REF,MAX} - V_{REF,MIN}}{T_{MAX} - T_{MIN}}. \tag{3}$$

The deviation of the circuit behavior from the aforementioned ideal behavior can be described by the following three imperfections: 1) The mirroring error in branch #1 ($G_1 = I_1/I_2$), 2) the mirroring error in branch #3 ($G_3 = I_3/I_2$), and 3) the offset voltage between V_1 and V_2 ($V_{OS} = V_2 - V_1$). These three errors depend on the actual implementation of the A-block and the current mirror, and they are temperature dependent in general. The dissection of the circuit non-ideal behavior into these three types of errors enables considering them in the design flow regardless of the actual transistor level implementation of the circuit. In addition to these errors, the actual TC of the PTAT and CTAT voltages deviates from the simple predictions of textbook models. However, such variation can be accounted for by relying on precomputed BJT LUTs. Taking these imperfections into account, (1) and (2) can be rewritten as

$$V_{REF} = \frac{\Delta V_{BE,EFF}}{R_2} \cdot G_3 \cdot R_3 + |V_{BE3}|, \tag{4}$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_3}{R_2}\frac{\partial}{\partial T}\left(\Delta V_{BE,EFF} \cdot G_3\right) + \frac{\partial |V_{BE3}|}{\partial T} = 0, \tag{5}$$

where $\Delta V_{BE,EFF} = \Delta V_{BE} + V_{OS}$ and ΔV_{BE} is a function of G_1.

The proposed systematic design procedure dissects the design process into two functions: bandgap core (*BGC*), which will be explained shortly in this section, and bandgap MOS (*BGM*), which will be presented in the next section (Sec. III). The *BGC* procedure assumes that the imperfections G_1, G_3, and V_{OS} are precisely known at T_{NOM} and temperature extremes. The *BGM* procedure is concerned with calculating these errors and sizing the MOS transistors that are used in the actual implementation of the A-block and the current mirror.

A simplified illustration of the function that designs the bandgap core *(BGC)* is shown in Fig. 2. The function accepts three types of input parameters: 1) the BJT LUTs, 2) the designer's degrees of freedom, namely, the total nominal bandgap bias current (I_B), Q_2 multiplier (n), and BJT emitter area (A), and 3) an error structure that contains circuit imperfections, namely, G_1, G_3, and V_{OS}. The output of the function is a *BGC* structure that contains the bias and component parameters of the circuit.

Two distinct directions of evaluation can be noticed in Fig. 2. First, in the forward evaluation direction (the design mode), the component parameters are calculated given the bias parameters. Second, in the backward evaluation direction (the solving mode), the circuit is solved to calculate unknown bias parameters (e.g., bias parameters at temperature extremes) given known component parameters (which have well-defined temperature dependence). The evaluation of R_2 is performed given the bias current at nominal temperature as shown in Algorithm 1. The notation $\mathcal{L}[Y](X)$ is used to indicate a lookup operation in the precomputed LUTs for the parameter Y given the set of parameters in X.

The evaluation of R_3 is a bit more complicated because the temperature dependency of different parameters must be taken into account as dictated by (5). In the case of a very sensitive circuit like the bandgap in hand, calculating the subtle change of a variable over a small temperature step will

Algorithm 1 Forward Evaluation of R_2

$I_{2,T_{NOM}} = I_B/3$
$I_{1,T_{NOM}} = G_{1,T_{NOM}} I_{2,T_{NOM}}$
$V_{BE2,T_{NOM}} = \mathcal{L}[V_{BE}](I_{2,T_{NOM}}/N)$
$V_{BE1,T_{NOM}} = \mathcal{L}[V_{BE}](I_{1,T_{NOM}})$
$\Delta V_{BE,T_{NOM}} = \left|V_{BE1,T_{NOM}}\right| - \left|V_{BE2,T_{NOM}}\right|$
$\Delta V_{BE,EFF,T_{NOM}} = \Delta V_{BE,T_{NOM}} + V_{OS,T_{NOM}}$
$R_2 = \Delta V_{BE,EFF,T_{NOM}}/I_{2,T_{NOM}}$

be sensitive to the LUTs finite accuracy. Consequently, we resorted to a more pragmatic and robust approach that makes use of the fact that the temperature behavior of the PTAT and CTAT parameters is dominantly linear. Thus, a good estimate of the TC of a variable X at T_{NOM} can be obtained from

$$\left.\frac{\partial X}{\partial T}\right|_{T_{NOM}} \approx mean\left(\frac{X_{T_{NOM}} - X_{T_{MIN}}}{T_{NOM} - T_{MIN}}, \frac{X_{T_{MAX}} - X_{T_{NOM}}}{T_{MAX} - T_{NOM}}\right). \quad (6)$$

Besides being a more robust evaluation approach, Eq. (6) implies that in addition to the nominal temperature, the LUTs need to store the device data at the temperature extremes only.

Evaluating (6) requires solving the circuit at T_{MIN} and T_{MAX} (backward evaluation). Since the linear PTAT behavior of I_2 is not perfect, an iterative procedure is used till the relative error (*relerr*) is smaller than a predefined relative tolerance (*reltol*):

$$relerr\,(X) = \frac{\left|X^{(i)} - X^{(i-1)}\right|}{X^{(i-1)}} < reltol, \quad (7)$$

where i corresponds to the i^{th} iteration of the variable X. The iterative procedure to calculate circuit parameters at temperature extremes is shown in Algorithm 2.

Algorithm 2 Backward Evaluation of *BGC* Bias Parameters at Temperature Extremes

for $T_x = [T_{MIN}, T_{MAX}]$ **do**
  Initially assume I_2 is perfectly PTAT: $I_{2,T_x} = I_{2,T_{NOM}} \cdot (T_x + 273.15) / (T_{NOM} + 273.15)$
  for $i = 1 : max\_num\_iter$ **do**
    $I_{1,T_x} = G_{1,T_x} I_{2,T_x}$
    $V_{BE2,T_x} = \mathcal{L}[V_{BE}](I_{2,T_x}/N)$
    $V_{BE1,T_x} = \mathcal{L}[V_{BE}](I_{1,T_x})$
    $\Delta V_{BE,T_x} = \left|V_{BE1,T_x}\right| - \left|V_{BE2,T_x}\right|$
    $\Delta V_{BE,EFF,T_x} = \Delta V_{BE,T_x} + V_{OS,T_x}$
    $I_{2,T_x} = \Delta V_{BE,EFF,T_x}/R_2$
    if $relerr\left(I_{2,T_x}\right) < reltol$ **then**
      break
    end if
  end for
end for

Following this procedure, forward evaluation of R_3 can be performed. The backward evaluation of V_{REF} and its TC follows, all without invoking the simulator. These steps are summarized in Algorithm 3.

Algorithm 3 Forward Evaluation of R_3 and Backward Evaluation of V_{REF} and TC. Circuit parameters Are evaluated at T_{NOM}, T_{MIN}, and T_{MAX} (Element-Wise Vector Operations)

$I_3 = G_3 \cdot I_2$
$V_{BE3} = \mathcal{L}[V_{BE}](I_3)$
Evaluate R_3 using (6) in (5)
Evaluate V_{REF} using (4)
Evaluate TC using (3)

It is worth noting that the systematic *BGC* procedure is valid regardless of the implementation details of the *A*-block and the current mirror.

III. SYSTEMATIC DESIGN OF CMOS BANDGAP CIRCUIT

Consider the actual realization of a CMOS bandgap circuit shown in Fig. 3. This circuit is a simple implementation of the generic bandgap circuit given in Fig. 1. The *A*-block is implemented using the pair $M_{N1,2}$, where the two NMOS transistors serve to equate the voltages at their source terminals. The current mirror is implemented using M_{P1-3}. The errors G_1 and G_3 arise because each device in M_{P1-3} has a different V_{DS} and a finite output resistance. The V_{OS} error is due to the different V_{DS} across $M_{N1,2}$, in addition to the G_1 error. The start-up circuit guarantees that the bandgap circuit does not operate in the zero-current state, while it consumes negligible current during normal operation [13].

A simplified illustration of the function that designs the bandgap MOS circuit *(BGM)* is shown in Fig. 4. The function accepts three types of input parameters: 1) the MOS LUTs, 2) the designer's degrees of freedom, namely, the supply voltage V_{DD}, the nominal bias point of the PMOS and NMOS transistors ($\rho_{P,N} = (g_m/I_D)_{P,N}$ at T_{NOM}), and their channel length $L_{P,N}$, and 3) the *BGC* structure.

The dissection of the design procedure into *BGC* and *BGM* functions defines the major iterative loop, where the output of *BGC* (the *BGC* structure) is passed as input to *BGM* and the output of *BGM* (the *Error* structure) is fed-back to *BGC* to generate a refined set of inputs to *BGM* once more. Inside either of *BGC* or *BGM*, minor iterative loops refine the variables of the scope of the section, e.g., I_2 correction loop presented in Algorithm 2. A variable of the scope is a variable that can only be updated or assigned inside its respective section (for example, I_2 is a variable of the scope of *BGC*, while V_{OS} is a variable of the scope of *BGM*). In doing so, a section treats the variables of the scope of the other section as stationary variables of iteration, i.e., they are constants as far as the section is concerned. The major loop convergence test uses R_3, as it is the key parameter that controls PTAT and CTAT cancellation as given by (5). A simplified outline for the proposed synthesis procedure is summarized in Algorithm 4.

Similar to *BGC*, the operation of *BGM* occurs in two directions as shown in Fig. 4. First, in the forward evaluation direction (the design mode), the component parameters (W_P and W_N) are calculated given the bias parameters

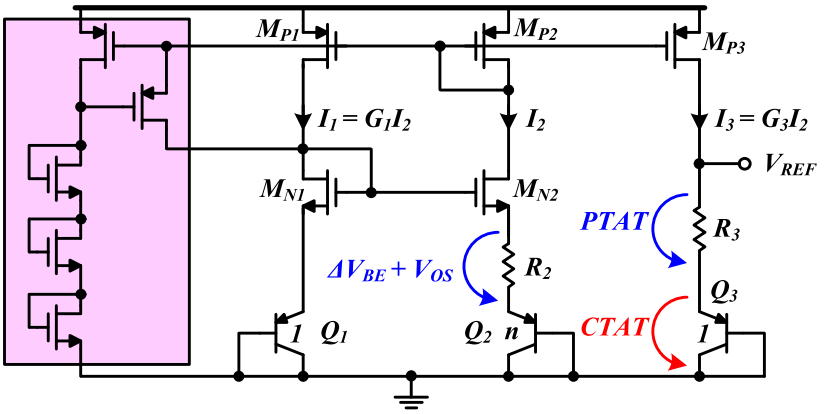

FIGURE 3. CMOS implementation of the generic bandgap voltage reference circuit in Fig. 1.

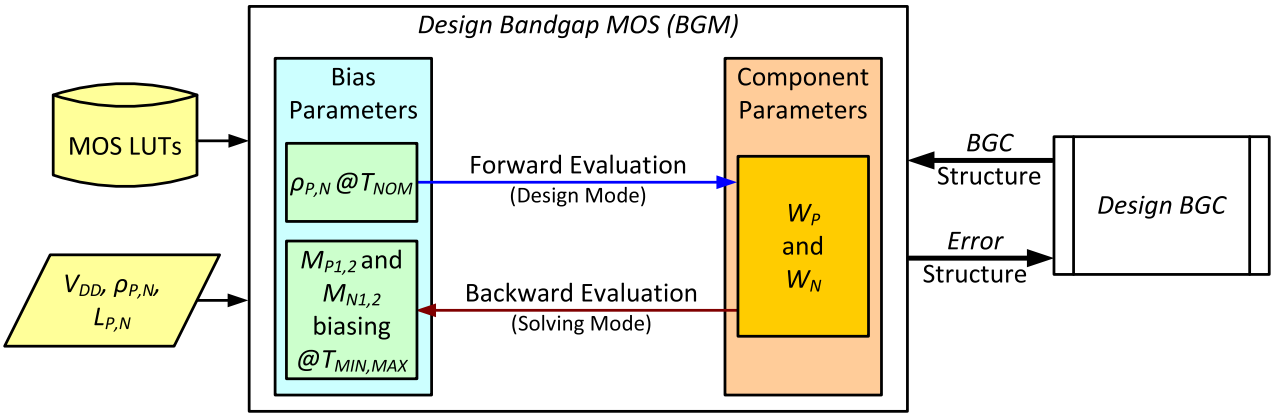

FIGURE 4. Simplified illustration for the *"Design bandgap MOS (BGM)"* function. The symbol ρ denotes g_m/I_D. The top-level pseudo code is given in Algorithm 4.

Algorithm 4 Simplified Outline for the Overall Operation of the Bandgap Synthesis Procedure

Initial seed for the *Error* structure: $G_1 = 1$, $G_3 = 1$, $V_{OS} = 0$
Invoke *BGC* to get initial estimate for the *BGC* structure (R_2, R_3, I_2, V_{BE1-3}, V_{REF})
for $i = 1 : max\_num\_iter$ **do**
  Invoke *BGM* to perform transistor sizing and calculate improved estimate for the *Error* structure (G_1, G_3, and V_{OS})
  Invoke *BGC* to get improved estimate for the *BGC* structure
  if *relerr* (R_3) $<$ *reltol* **then**
    break
  end if
end for
Calculate performance metrics of the synthesized bandgap circuit

Algorithm 5 Forward Evaluation of W_P Given ρ_P at T_{NOM}. The Notation $\mathcal{L}[Y](X)$ Is Used to Indicate a Lookup Operation in the Precomputed LUTs for the Parameter Y Given the Set of Parameters in X

Initial seed: $V_{DS,P2,T_{NOM}} = V_{DD}/3$
for $j = 1 : max\_num\_iter$ **do**
  $J_{P2,T_{NOM}} = \mathcal{L}[J](L_P, \rho_{P,T_{NOM}}, V_{DS,P2,T_{NOM}})$
  $V_{GSP,T_{NOM}} = \mathcal{L}[V_{GS}](L_P, J_{P2,T_{NOM}}, V_{DS,P2,T_{NOM}})$
  $V_{DS,P2,T_{NOM}} = V_{GSP,T_{NOM}}$
  if *relerr* $(V_{DS,P2,T_{NOM}}) <$ *reltol* **then**
    break
  end if
end for
$W_P = W_{P1-3} = I_{2,T_{NOM}}/J_{P2,T_{NOM}}$

at T_{NOM}. Second, in the backward evaluation direction (the solving mode), the circuit is solved to calculate the bias parameters at temperature extremes given known component parameters (which have no temperature dependence).

The width of the PMOS transistors ($W_P = W_{P1-3}$) is determined using the bias point information of M_{P2} at nominal conditions (ρ_P) as shown in Algorithm 5, where a minor iterative loop is used to correct $V_{DS,P2}$.

The synthesis procedure also checks the computed device width and breaks the device into multiple fingers if the width is very large. Similarly, the forward evaluation of ($W_N = W_{N1,2}$) is performed using the bias point

Algorithm 6 Forward Evaluation of W_N Given ρ_N at T_{NOM}

$V_{DS,N2,T_{NOM}} = V_{DD} - \left|V_{DS,P2,T_{NOM}}\right| - \Delta V_{BE,EFF,T_{NOM}} - \left|V_{BE2,T_{NOM}}\right|$
$V_{SB,N2,T_{NOM}} = \Delta V_{BE,EFF,T_{NOM}} + \left|V_{BE2,T_{NOM}}\right|$
$J_{N2,T_{NOM}} = \mathcal{L}[J](L_N, \rho_{N,T_{NOM}}, V_{DS,N2,T_{NOM}}, V_{SB,N2,T_{NOM}})$
$V_{GS,N2,T_{NOM}} = \mathcal{L}[V_{GS}](L_N, J_{N2,T_{NOM}}, V_{DS,N2,T_{NOM}})$
$W_{N1,2} = W_N = I_{2,T_{NOM}}/J_{N2,T_{NOM}}$

information of M_{N2} at nominal conditions (ρ_N) as shown in Algorithm 6.

On other hand, the biasing parameters at T_{MIN} and T_{MAX} are calculated using backward evaluation. The biasing parameters of M_{P2} are calculated as in Algorithm 7, which is similar to Algorithm 5; however, J_{P2} is calculated using W_P rather than ρ_P because W_P is fixed, while ρ_P and J_{P2} are temperature dependent.

Algorithm 7 Backward Evaluation of M_{P2} Bias Parameters at Temperature Extremes

for $T_x = [T_{MIN}, T_{MAX}]$ **do**
  Initial seed: $V_{DS,P2,T_x} = V_{DD}/3$
  for $j = 1 : max\_num\_iter$ **do**
    $J_{P2,T_x} = I_{2,T_x}/W_P$
    $V_{GSP,T_x} = \mathcal{L}[V_{GS}](L_P, J_{P2,T_x}, V_{DS,P2,T_x})$
    $V_{DS,P2,T_x} = V_{GSP,T_x}$.
    if $relerr\left(V_{DS,P2,T_x}\right) < reltol$ **then**
      break
    end if
  end for
end for

Turning to M_{N2}, the biasing at temperature extremes is solved using Algorithm 8, which is similar to Algorithm 6 but J_{N2} is calculated using the forward evaluated fixed parameter W_N rather than the temperature dependent parameter ρ_N.

Algorithm 8 Backward Evaluation of M_{N2} Bias Parameters at Temperature Extremes

for $T_x = [T_{MIN}, T_{MAX}]$ **do**
  $V_{DS,N2,T_x} = V_{DD} - \left|V_{DS,P2,T_x}\right| - \Delta V_{BE,EFF,T_x} - \left|V_{BE2,T_x}\right|$
  $V_{SB,N2,T_x} = \Delta V_{BE,EFF,T_x} + \left|V_{BE2,T_x}\right|$
  $J_{N2,T_x} = I_{2,T_x}/W_N$
  $V_{GS,N2,T_x} = \mathcal{L}[V_{GS}](L_N, J_{N2,T_x}, V_{DS,N2,T_x})$
end for

Although the sizing of M_{P1} and M_{N1} is already resolved, their biasing parameters are interlinked; thus, they are jointly solved at $T_{NOM,MIN,MAX}$ using a nested loop, which also yields V_{OS} behavior vs temperature as shown in Algorithm 9. The first iteration of $M_{P1,N1}$ sizing starts with the value of V_{OS} from the previous major iteration, rather than starting from zero. This helps to achieve convergence quickly. The corrected value of V_{OS} can be used to correct

Algorithm 9 Backward Evaluation of M_{P1} and M_{N1} Biasing Using Nested Iterations. The Procedure Is Repeated at T_{NOM}, T_{MIN}, and T_{MAX}

$V_{SB,N1} = |V_{BE1}|$
for $j = 1 : max\_num\_iter$ **do**
  $V_{GS,N1} = V_{GS,N2} + V_{OS}$
  $V_{DS,N1} = V_{GS,N1}$
  $\left|V_{DS,P1}\right| = V_{DD} - V_{DS,N1} - |V_{BE1}|$
  $J_{P1} = \mathcal{L}[J](L_P, V_{GSP}, V_{DS,P1})$
  $I_1 = W_P \cdot J_{P1}$
  $J_{N1} = I_1/W_N$
  for $k = 1 : max\_num\_iter$ **do**
    $V_{GS,N1} = \mathcal{L}[V_{GS}](L_N, J_{N1}, V_{DS,N1}, V_{SB,N1})$
    $V_{DS,N1} = V_{GS,N1}$
    if $relerr\left(V_{DS,N1}\right) < reltol$ **then**
      break
    end if
  end for
  $V_{OS} = V_{GS,N1} - V_{GS,N2}$
  if $relerr\,(V_{OS}) < reltol$ **then**
    break
  end if
end for

$V_{DS,N2}$ and $V_{SB,N2}$ and repeat the M_{N2} iterations; however, this is not necessary as the overall error is negligible and the new V_{OS} value will be used in the next major iteration. Lastly, we turn to M_{P3} and calculate $G_{1,3}$ at T_{NOM}, T_{MIN}, and T_{MAX} as shown in Algorithm 10.

Algorithm 10 Evaluation of G_1 and G_3. All Parameters Are Evaluated at T_{NOM}, T_{MIN}, and T_{MAX} (Element-Wise Vector Operations)

$V_{DS,P3} = V_{DD} - V_{REF}$
$J_{P3} = \mathcal{L}[J](L_P, V_{GSP}, V_{DS,P3})$
$I_3 = W_P \cdot J_{P3}$
$G_1 = I_1/I_2$
$G_3 = I_3/I_2$

At this point in the procedure, *BGM* becomes ready to output its major iteration cycle output. Notice that at both T_{NOM} and the temperature extremes, the same sequence of steps is employed but while noting that the sizing is readily settled according to the nominal conditions. In other words, the behavior at temperature extremes is not actively involved in the transistor sizing process, but it is important for the estimation of the errors G_1, G_3, and V_{OS}.

It is worth noting that the proposed design methodology enables the designer to sweep the circuit's degrees of freedom (for both the *BGC* and *BGM* functions) to explore the design space as will be shown in Sec. V.

IV. VARIATIONS AND MISMATCH

Bandgap reference circuits are strongly influenced by variations and mismatch. Regarding variations, the effect of

process, voltage, and temperature (PVT) variations must be considered. Ideally, the output reference voltage should not change with PVT variations. The effect of temperature variations was already included in the design flow presented in Sec. II and III. The effect of process and voltage variations can be seamlessly considered in the design flow similar to the way the temperature extremes were handled, i.e., backward evaluation (solving mode) of biasing parameters given the component parameters. For example, to study the effect of voltage variations, we simply modify *BGM* input parameters to include the newly required supply voltage level (V_{DD}). Next, the forward evaluation (design mode) is skipped and only the backward evaluation steps are performed to solve the circuit at the new value of V_{DD}. However, since the value of R_3 does not change in the iterative backward evaluations (solving mode), another variable must be used to check for the convergence of the major loop (see Algorithm 4). The variable we chose for this convergence check is V_{REF} itself, since it is the most important bandgap parameter that is affected by variations.

Similarly, the effect of process corners can be considered by changing the device LUTs used with *BGC* and *BGM*. In the design mode, LUTs extracted at the typical conditions are used. However, to study the effect of process corners, we supply *BGC* and *BGM* with LUTs extracted at the slow and fast corners of every device. Note that these precomputed LUTs are generic and normalized LUTs that are extracted for a set of reference devices, i.e., the set of LUTs are design-independent and they can be used with any circuit type and any topology without the need to repeat the precomputation. As in the case of voltage variations, solving the circuit involves backward evaluations only, and V_{REF} is used to check convergence.

The effect of mismatch on the behavior of the bandgap circuit is usually quantified using Monte Carlo simulations. In this type of analysis, some of the device model parameters are randomly modified according to a normal (Gaussian) distribution, e.g., the threshold voltage of MOS devices. The standard deviation of the Gaussian distribution is extracted from measurements and included in the model file supplied by the semiconductor foundry in a normalized form (Pelgrom's coefficients [14]). The standard deviations are then appropriately scaled depending on the device geometry according to Pelgrom's Model [15]. At every random set of model parameters, the circuit is re-solved by the circuit simulator using the complete large-signal non-linear models of the devices. This is then repeated hundreds of times to yield the output statistical distribution. In the context of the proposed LUT-based design procedure, the effect of mismatch can be calculated using a faster and simpler approach. Since the mismatch error is actually a small perturbation superimposed on the nominal conditions, the linearized small-signal models of the devices can be used. The transfer function from each mismatch source to the bandgap output can be calculated using linear circuit analysis. Next, the mean-square values of the mismatch contributions at the output are summed together to yield the output statistical distribution, which is fully characterized by its mean and standard deviation. A comparison between conventional corners and Monte Carlo simulations using Cadence Spectre and the results of the proposed systematic procedure will be provided in Sec. V.

V. RESULTS AND DISCUSSION

The proposed systematic design procedure was implemented in MATLAB. The lookup function that is used to access the LUTs and interpolate off-grid points ($\mathcal{L}[Y](X)$ operations) is an enhanced version of the function provided in [16]. The main introduced enhancements are: 1) Implementing new functions to generate and look up BJT parameters, 2) including the temperature as a search parameter for both BJT and MOSFET, and 3) using two-step interpolation, where a multidimensional linear interpolation is followed by a one-dimensional pchip interpolation for V_{GS}.

The top-level script of the proposed methodology invokes the bandgap synthesis function, then it automatically generates a netlist and invokes Cadence Spectre to compare synthesis and simulation results. Fig. 5 shows the results of a bandgap circuit synthesized in a 180 *nm* CMOS technology using the following set of parameters: $V_{DD} = 1.8\,V$, $I_B = 10\,\mu A$, $L_N = L_P = 4\,\mu$, and $\rho_N = \rho_P = 15\,V^{-1}$. The bandgap output ($V_{REF}$) shows the typical second-order curvature, which indicates that the first-order dependence on temperature is canceled (i.e., (5) is satisfied). As evident in Fig. 5, synthesis and simulation results show excellent agreement, and the proposed iterative synthesis procedure can precisely calculate the subtle changes in G_1, G_3, and V_{OS} vs temperature. Moreover, Fig. 6 shows that the required specifications at the nominal point ($I_B = 10\,\mu A$ and $\rho_N = \rho_P = 15\,V^{-1}$) are perfectly achieved. Remarkably, the whole synthesis procedure completes in $5.95\,s$ on a quad-core machine with 4 *GB* RAM.

TABLE 1. Comparison of results for LUTs with different V_{GS} step.

V_{GS} step	V_{REF} (V)			TC (ppm)			Time (s)
	Syn	Sim	|Err|	Syn	Sim	|Err|	
5 mV	1.2327	1.2327	0	13.68	13.65	0.03	5.95
10 mV	1.2326	1.2327	0.1m	13.50	13.71	0.21	3.55
20 mV	1.2320	1.2319	0.1m	16.31	15.09	1.22	1.87

The previous results were achieved using MOSFET LUTs with a V_{GS} step of $5\,mV$ and synthesis $reltol = 1e-5$. Since the primary variable that controls the MOS drain current is V_{GS}, the step of the V_{GS} sweep is the dominant factor affecting the LUTs accuracy. We experimented using LUTs with different V_{GS} steps. Initially, using linear interpolation as in [16], the error in the synthesis output grew considerably; however, when we modified V_{GS} interpolation to be two-step, as previously explained, the results improved substantially. Table 1 summarizes the results for V_{GS} steps of 5, 10, and $20\,mV$. As V_{GS} step increases, the error slightly increases, but the execution time becomes significantly faster.

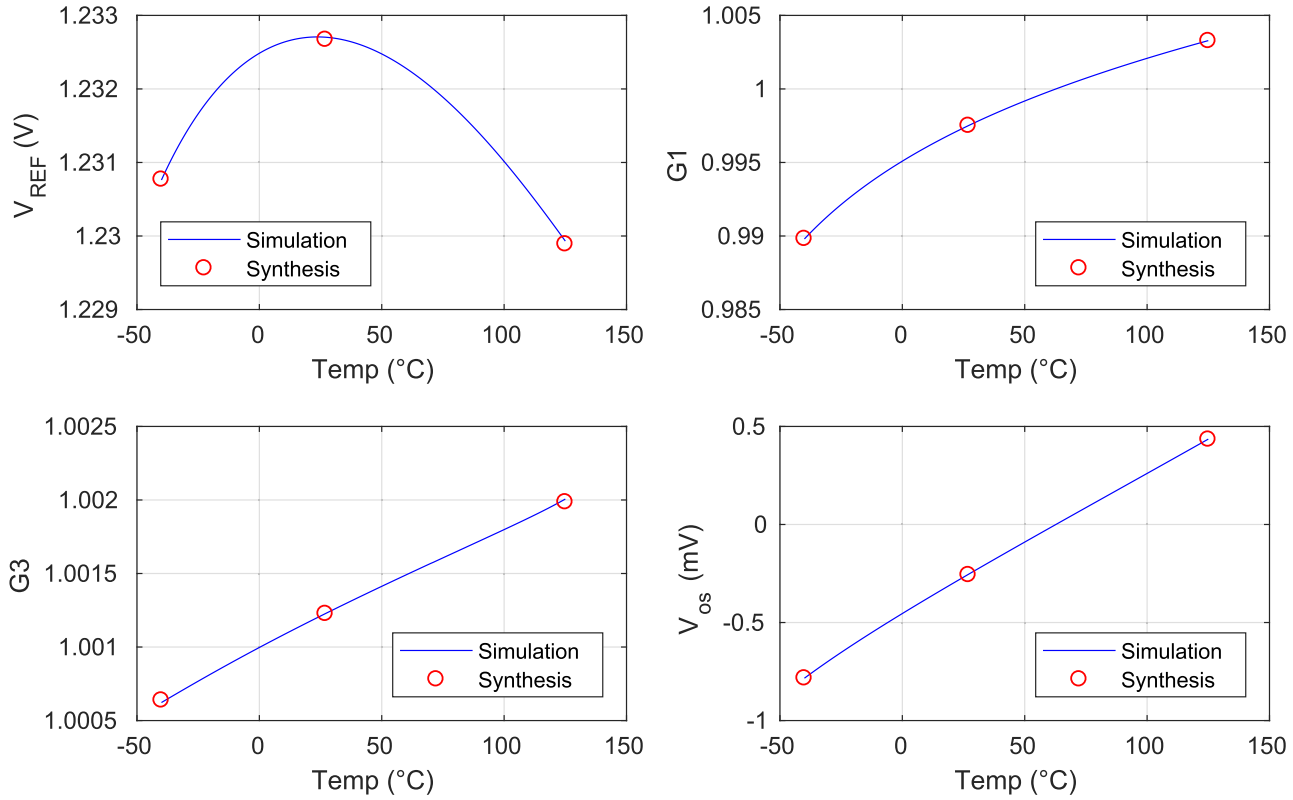

FIGURE 5. Comparison of synthesis and simulation results showing V_{REF}, G_1, G_3, and V_{OS} vs temperature.

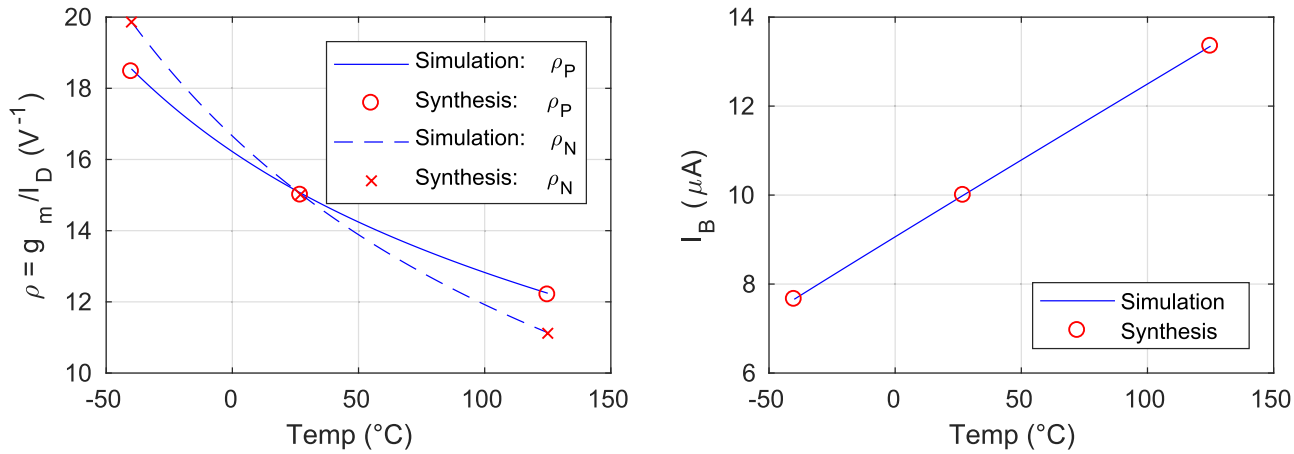

FIGURE 6. Comparison of synthesis and simulation results showing ρ_P, ρ_N, and I_B vs temperature.

It should be noted that the step size in BJT LUTs sweeps has negligible impact on the LUTs size because the substrate PNP is essentially a two-terminal device with few choices for the emitter area parameter (A). Another important factor that controls the accuracy and the synthesis time is the *reltol* used in the iterative procedure. Table 2 shows that even if *reltol* is relaxed by two orders of magnitude, the error is still tolerable, while the execution time becomes faster.

In order to illustrate the merit of the proposed design procedure, the same set of parameters used in the previous design example was used in Cadence optimization to automatically design the circuit (simulation-based optimization). As shown in Table 3, the proposed procedure can achieve better and more accurate results. More importantly, although DC

TABLE 2. Comparison of results for different values of *reltol*.

reltol	V_{REF} (V)			TC (ppm)			Time
	Syn	Sim	|Err|	Syn	Sim	|Err|	(s)
1e-5	1.2327	1.2327	0	13.68	13.65	0.03	5.95
1e-4	1.2327	1.2327	0	13.68	13.64	0.04	4.53
1e-3	1.2327	1.2328	0.1m	13.70	13.55	0.15	2.64

TABLE 3. Comparison of the proposed design procedure with Cadence optimization.

	Requirement	Cadence optimization	Proposed procedure
I_B (μA)	10	11.16	10
ρ_P (V^{-1})	15	15	15
ρ_N (V^{-1})	15	14.8	15
TC (ppm)	Minimum	20.25	13.68
Execution Time (s)	Minimum	**2,460**	**< 6**

simulations are generally fast, the time required by Cadence optimization is orders of magnitude longer than the time required by the proposed procedure because it is difficult for the optimizer to tune several circuit parameters simultaneously. Using the proposed methodology, the designer can quickly sweep the circuit's degrees of freedom and explore the design space as will be shown shortly. On the other hand, using simulation-based optimization this is impractical because the search for each design point requires considerable execution time.

The previous synthesis example verifies the proposed systematic design procedure; however, it only considers a single design point. Consequently, we used nested sweeps for the circuit's degrees of freedom ($L_{P,N}$, $\rho_{P,N}$, I_B, and A) to verify the proposed procedure in three design spaces: L_P *vs* L_N $= 1\mu m \rightarrow 8\mu m$ (Fig. 7), ρ_P *vs* ρ_N $= 10 \rightarrow 20$ (Fig. 8), and I_B *vs* A: $I_B = 1\mu A \rightarrow 100\mu A$ and $A = 5\mu m \times 5\mu m$, $10\mu m \times 10\mu m$ (Fig. 9). The comparison of V_{REF} and TC obtained from the synthesis procedure and simulations delivers two important messages: 1) the synthesis results match the simulations very well across this wide range of values which validates the robustness of the proposed methodology and 2) the TC is quite low, which means that the synthesis procedure properly designs the bandgap to cancel the first order temperature dependence. It is worth noting that TC starts to increase at low $\rho_{P,N}$ as the transistors are driven to the edge of saturation.

The accuracy and speed of the proposed systematic design procedure enables the designer to explore the degrees of freedom available in the circuit. As the designer sweeps one design variable, the whole design is readjusted to restore the zero-TC point at T_{NOM} and properly size the transistors, which is a key merit of the proposed procedure. Once the synthesis procedure generates the readjusted design, the simulation engine can be invoked to compute any important

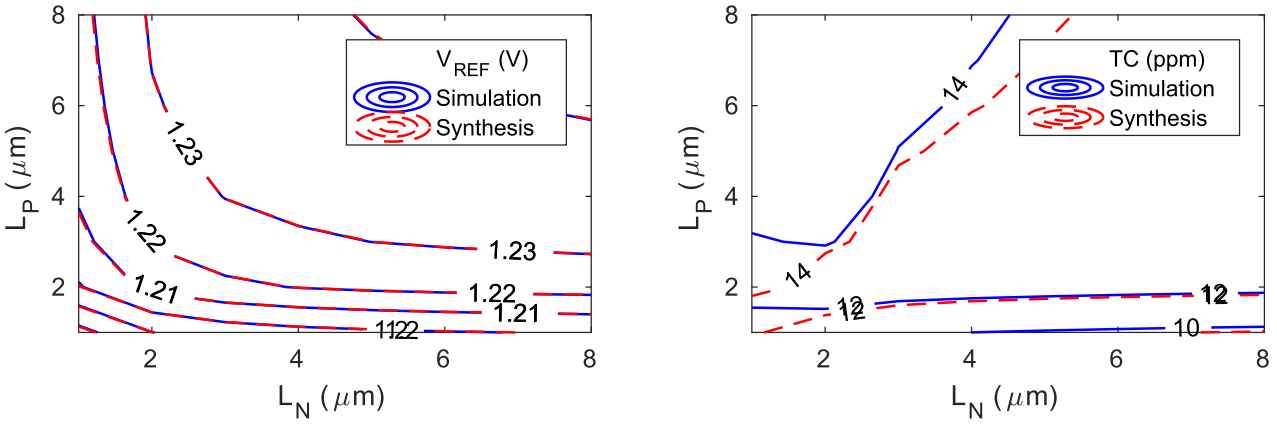

FIGURE 7. V_{REF} and TC in the design space of L_N vs L_P.

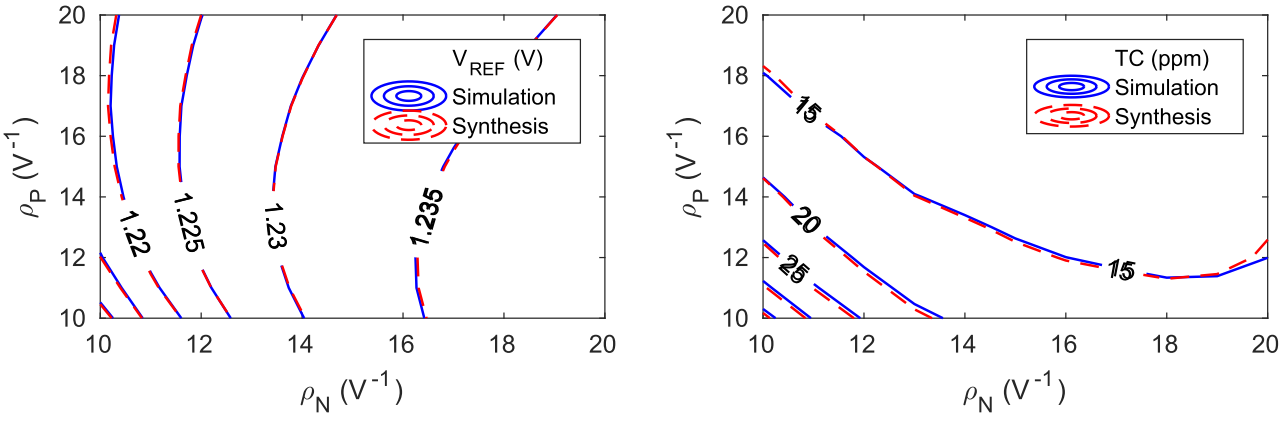

FIGURE 8. V_{REF} and TC in the design space of ρ_N vs ρ_P.

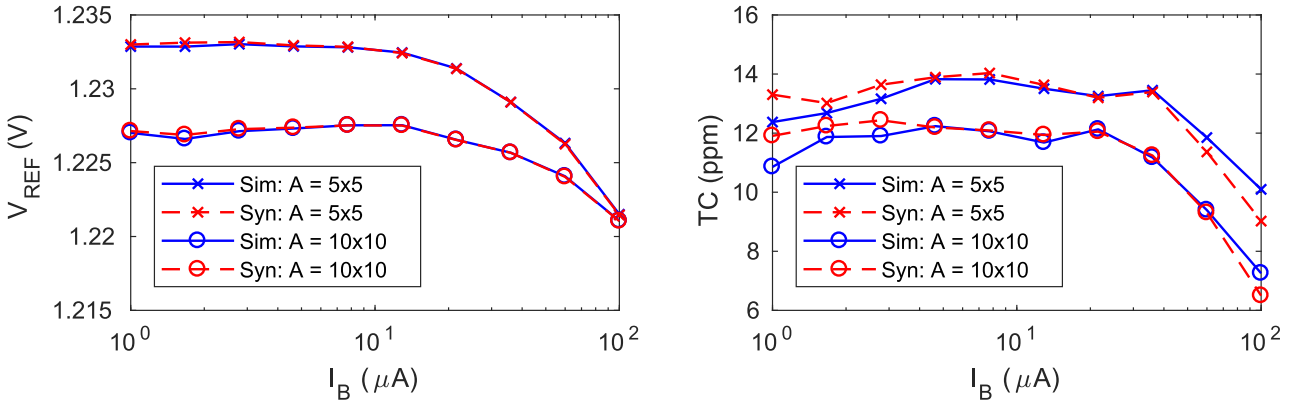

FIGURE 9. V_{REF} and TC in the design space of I_B and emitter area (A).

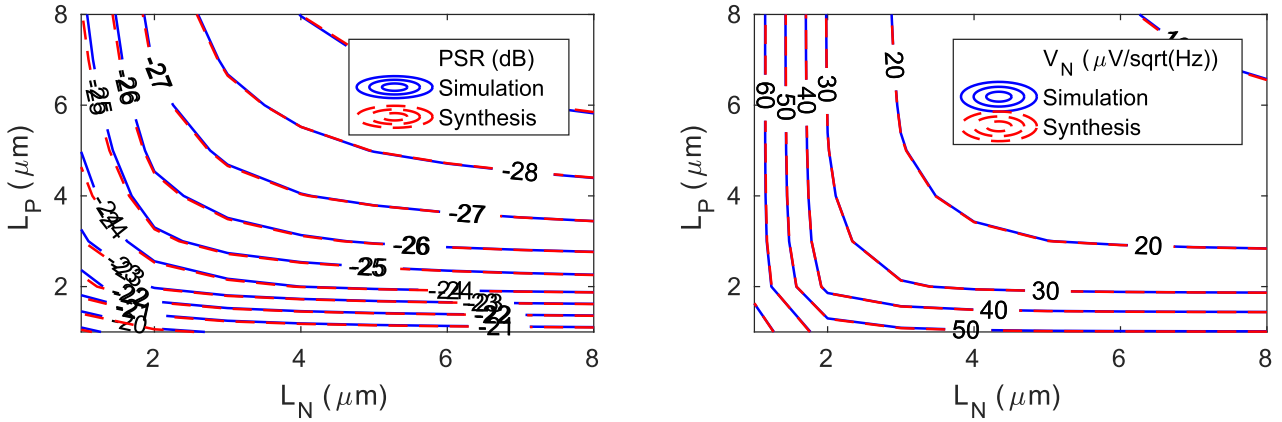

FIGURE 10. PSR and voltage noise density at 1 *Hz* in the design space of L_N vs L_P.

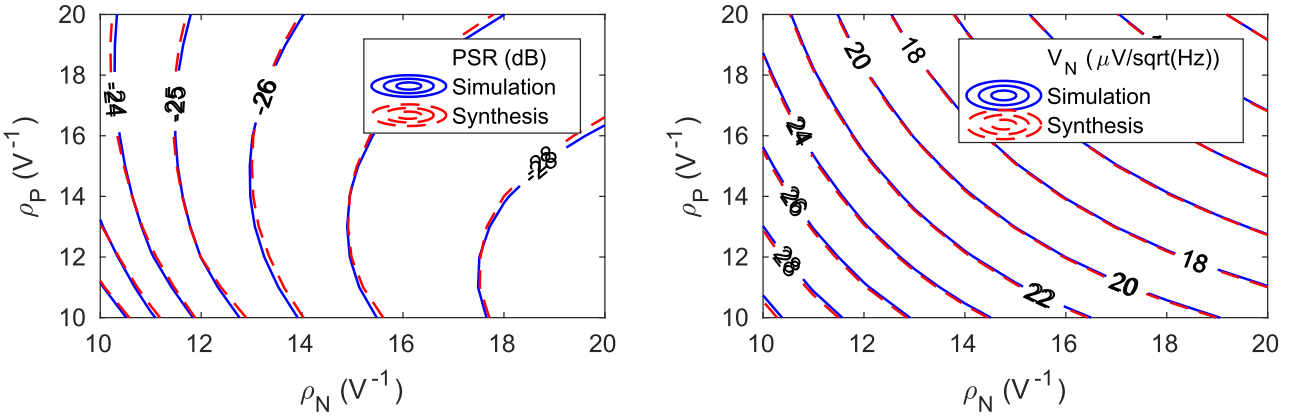

FIGURE 11. PSR and voltage noise density at 1 *Hz* in the design space of ρ_N vs ρ_P.

design metric, e.g., power supply rejection (PSR) and noise. Consequently, contours of key specifications can be generated to aid in the design process and provide insights into circuit trade-offs. In an even better and more powerful approach, a symbolic circuit solver (e.g., SLiCAP [17]) can be used to generate an accurate expression for the required design metric. Although the analytical expression may span several lines, computing the result out of it just requires looking up some parameters in the LUTs and direct substitution, which consumes only few milli-seconds. As a result, the design space can be explored without invoking the simulator in the loop. We applied this approach to explore the PSR and noise in the aforementioned design spaces: L_P *vs* L_N (Fig. 10), ρ_P *vs* ρ_N (Fig. 11), and I_B *vs* A (Fig. 12). The PSR and noise results computed by the synthesis procedure are in excellent agreement with the simulation results. This design

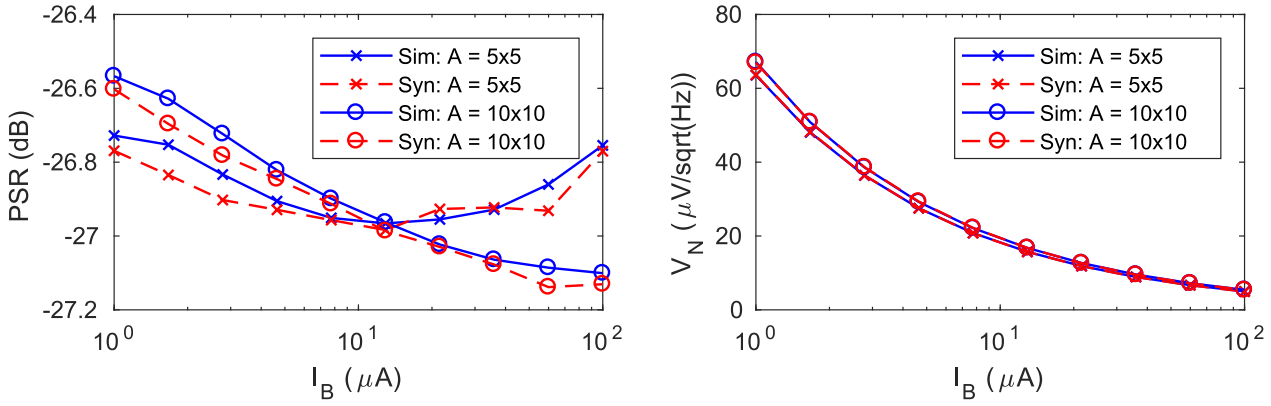

FIGURE 12. PSR and voltage noise density at 1 *Hz* in the design space of I_B and emitter area (A).

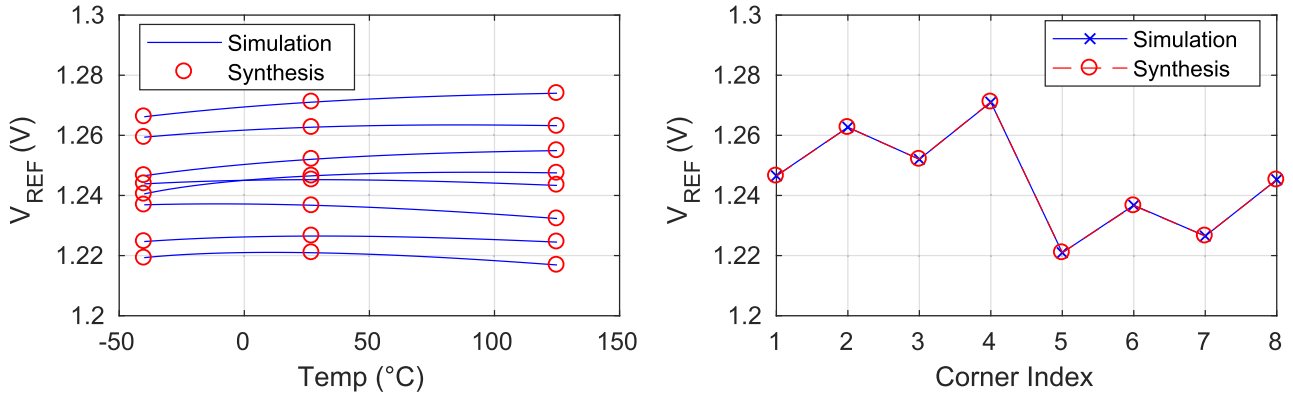

FIGURE 13. Comparison of synthesis and simulation results showing V_{REF} vs temperature at eight different corners and the nominal value of V_{REF} vs corner index.

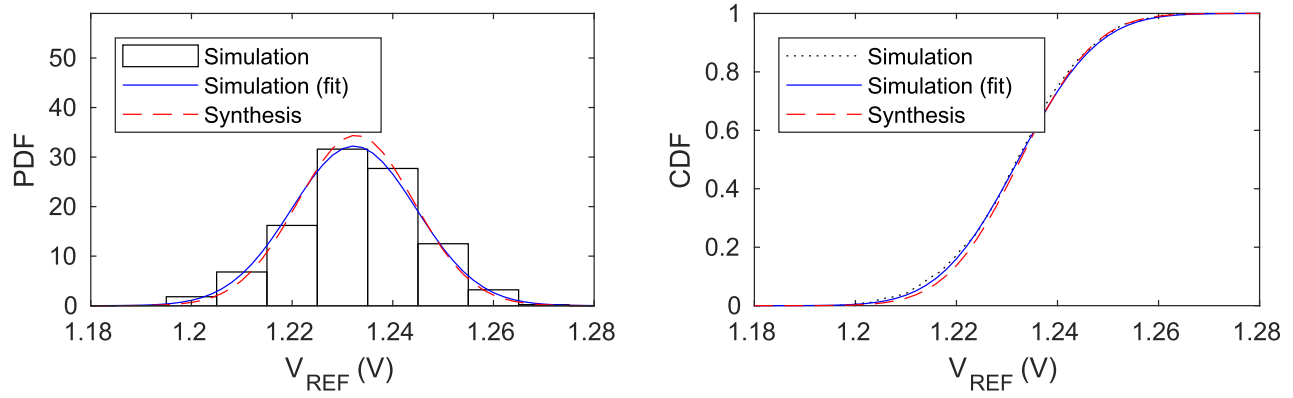

FIGURE 14. Probability density function (PDF) and cumulative distribution function (CDF) of V_{REF} due to random mismatch.

space exploration provides the designer with design insights, e.g., Fig. 11 indicates that to achieve higher PSR the NMOS transistors need to be biased in weak inversion (WI). A design in this realm boils down to the creation of a circuit-specific lookup function that can simply look up the design according to a set of required specifications without the need to restart the design process all over again.

As discussed in Sec. IV, the effect of process corners can be considered by changing the input parameters of the synthesis procedure and applying back*ward evaluation (solving mode). Fig. 13 compares the synthesis and simulation results of eight different corners, where excellent agreement is achieved. The effect of random mismatch is calculated using the linear transfer functions generated by the symbolic solver similar to noise analysis. To verify the output of the proposed procedure, Monte Carlo simulations were performed on Cadence Spectre using 1,000 runs. Fig. 14 shows the normalized histogram (probability density function, PDF) and the empirical cumulative distribution function (CDF) using the data generated from the simula-

tions. The estimated mean and standard deviation of the simulation data are used to fit a normal distribution to the simulation results. Similarly, another normal distribution is plotted in the figure using the mean and standard deviation computed by the proposed synthesis procedure. As shown in Fig. 14, the PDF and CDF generated by the synthesis procedure are in close agreement with those generated using actual simulation data. In conclusion, the bandgap output variation due to PVT corners and random mismatch can be accurately estimated using the proposed procedure without invoking the simulator in the loop.

VI. CONCLUSION

We proposed a g_m/I_D-based systematic approach to the design of bandgap voltage references. We devised an algorithm that iterates on precomputed LUTs without the need to invoke a simulator in the loop. The results of the proposed synthesis procedure were verified against simulation results over a wide design space. With the aid of a symbolic circuit solver, we explored the circuit's key performance metrics in a short time with no simulator required. The proposed procedure is totally agnostic towards the adopted technology and hence, is extrapolatory to various technology nodes. The proposed methodology can effectively take into consideration the effect of PVT corners and random mismatch, and can be similarly applied to other bandgap reference topologies.

REFERENCES

[1] M. Barros, J. Guilherme, and N. Horta, *Analog Circuits and Systems Optimization Based on Evolutionary Computation Techniques*. Berlin, Germany: Springer, 2010.
[2] A. Dastgheib and B. Murmann, "Calculation of total integrated noise in analog circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 2988–2993, Nov. 2008.
[3] R. Iskander, M.-M. Louerat, and A. Kaiser, "Hierarchical sizing and biasing of analog firm intellectual properties," *Integration*, vol. 46, no. 2, pp. 172–188, 2013.
[4] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996.
[5] S. Seth and B. Murmann, "Settling time and noise optimization of a three-stage operational transconductance amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1168–1174, May 2013.
[6] J. Ou and P. M. Ferreira, "A g_m/I_D-based noise optimization for CMOS folded-cascode operational amplifier," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 61, no. 10, pp. 783–787, Oct. 2014.
[7] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge, U.K.: Cambridge Univ. Press, 2017.
[8] M. N. Sabry, H. Omran, and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelectron. J.*, vol. 75, pp. 87–96, May 2018.
[9] J. Ou and P. M. Ferreira, "Implications of small geometry effects on g_m/I_D based design methodology for analog circuits," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 66, no. 1, pp. 81–85, Jan. 2019.
[10] F. Olivera and A. Petraglia, "A computer-aided approach for voltage reference circuit design," *Analog Integr. Circuits Signal Process.*, vol. 89, pp. 511–520, Dec. 2016.
[11] D. M. Colombo, G. I. Wirth, and C. Fayomi, "Design methodology using inversion coefficient for low-voltage low-power CMOS voltage reference," in *Proc. 23rd Symp. Integr. Circuits Syst. Design (SBCCI)*, New York, NY, USA, 2010, pp. 43–48.
[12] D. Osipov and S. Paul, "Compact extended industrial range CMOS current references," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 6, pp. 1998–2006, Jun. 2019.
[13] R. J. Baker, *CMOS: Circuit Design, Layout and Simulation*. Hoboken, NJ, USA: Wiley, 2011.
[14] H. Omran, H. Alahmadi, and K. N. Salama, "Matching properties of femtofarad and sub-femtofarad MOM capacitors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 6, pp. 763–772, Jun. 2016.
[15] M. Pelgrom, H. Tuinhout, and M. Vertregt, "A designer's view on mismatch," in *Nyquist AD Converters, Sensor Interfaces, and Robustness*. New York, NY, USA: Springer, 2013, pp. 245–267.
[16] B. Murmann. *Gm/ID Starter Kit*. Accessed: Mar. 30, 2019. [Online]. Available: https://web.stanford.edu/~murmann/gmid
[17] A. Montagne. *SLiCAP: Symbolic Linear Circuit Analysis Program*. Accessed: Nov. 15, 2018. [Online]. Available: https://www.analog-electronics.eu/slicap

HESHAM OMRAN received the B.Sc. (Hons.) and M.Sc. degrees from Ain Shams University, Cairo, Egypt, in 2007 and 2010, respectively, and the Ph.D. degree from the King Abdullah University of Science and Technology (KAUST), Saudi Arabia, in 2015, all in electrical engineering. From 2008 to 2011, he was a Research and Teaching Assistant with the Integrated Circuits Laboratory (ICL), Ain Shams University, and a Design Engineer with Si-Ware Systems (SWS), Cairo, where he worked on the circuit and system design of the first miniaturized FT-IR MEMS spectrometer (NeoSpectra). From 2011 to 2016, he was a Researcher with the Sensors Lab, KAUST. He held internships at Bosch Research and Technology Center, CA, USA, and Mentor Graphics, Cairo. In 2016, he rejoined ICL, Ain Shams University, as an Assistant Professor. He has published more than 30 papers in international journals and conferences. His research interests include the design of analog and mixed-signal integrated circuits, especially in analog and mixed-signal CAD tools and design automation.

MOHAMED H. AMER received the B.Sc. degree (Hons.) in electrical engineering from Ain Shams University, Cairo, Egypt, in 2018, where he is currently pursuing the M.Sc. degree in electrical engineering. He is also a Research Assistant with the Integrated Circuits Laboratory (ICL), Ain Shams University. His research interests include the design of analog and mixed-signal integrated circuits and design automation.

AHMED M. MANSOUR received the B.Sc. degree in electronics and communications engineering from the Faculty of Engineering, Alexandria University, Egypt, in 2017. He is currently pursuing the M.Sc. degree in electronics and communications engineering with the Faculty of Engineering, Ain Shams University, Egypt. Since 2018, he has been a Research Assistant with the Integrated Circuits Laboratory (ICL), Ain-Shams University. His research interests include design of analog/mixed-signal integrated circuits, systematic design of analog integrated circuits, and fast analytical techniques in linear networks.