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Comparison of Synchronization Techniques Under Distorted Grid Conditions

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ABSTRACT In grid-connected power converter applications, the phase-locked loop (PLL) is probably the most widely used grid synchronization technique, owing to its simple implementation. However, in power grids some very common problems, such as voltage distortion, voltage unbalance, and frequency instability make synchronization a challenging task. The performance of the conventional synchronous reference frame PLL (SRF-PLL) is greatly reduced in the presence of distorted grid conditions. For a polluted grid some advance PLL techniques have been proposed, such as moving average filter PLL (MAF-PLL) and cascaded delayed signal cancellation PLL (CDSC-PLL). These techniques have been mostly evaluated in the presence of odd and even harmonics but the effects of interharmonics on these synchronization techniques still needs to be investigated. In this paper, a detailed performance comparison has been made between SRF-PLL, MAF-PLL, and CDSC-PLL for grid voltages contaminated with interharmonics in the presence of different grid disturbances, such as frequency jump, phase angle jump, and dc offset. The techniques are simulated using Matlab/Simulink. The CDSC-PLL shows excellent performance as compared with other techniques in terms of dynamic response as it settles to frequency step change in a half cycle but the presence of interharmonics greatly reduces its filtering capability. On the other hand, MAF-PLL gives a ripple free behavior in frequency estimation but with a much slower dynamic response as it settles to a frequency step change in more than three cycles. SRF-PLL only performs well under harmonics free grid voltages.

INDEX TERMS Grid synchronization, phase locked loop, interharmonics and power quality improvement.

I. INTRODUCTION

Synchronization of grid connected power converters is one of the important issues to be solved in industrial and power applications [1]–[3]. Synchronization is the process of extracting the information about the frequency and phase angle of the fundamental frequency positive sequence component of the grid voltage. The phase information of the grid voltage is needed to obtain the reference of the current delivered by the power electronics converter [4]–[6]. This infers that the quality of the injected power highly depends on the accuracy of phase information.

Phase locked loop (PLL) is commonly used for grid synchronization [7], [8]. Between several types of PLL, the synchronous reference frame PLL (SRF-PLL) established on PI controller is perhaps the most frequently used because of its easy implementation and simple structure [9]–[13]. Many researchers have worked on SRF-PLL for the estimation of grid phase and proved its accuracy if the electric grid does not contain harmonics and is balanced [14], [15]. On the other hand, if the grid voltage contains harmonics components, the PI-based SRF-PLL shows inaccurate estimation of phase [16], [17]. The harmonics filtering capability of the SRF-PLL can be improved by carefully selecting the tuning parameters of the PI controller [18]. However, this approach results in a slower dynamic response. In [19], a feed forward action is used to improve the response speed. Likewise, in [20] and [21], a number of techniques are presented to remove unwanted ripples in the estimated phase, but a drift in the grid frequency is not taken into account in testing the proposed technique. In [14] an improved small signal SRF-PLL model is proposed to analyze the variations of input voltage magnitude in addition to effects of grid frequency and phase angle changes.

In [22]–[24] using a MAF in the PLL control loop is suggested. The MAF technique is proved to be effective under adverse grid, however, the open-loop bandwidth of a PLL is drastically reduced after incorporating a MAF into its structure giving rise to slower dynamic response. In [25] a detailed analysis and design guideline of a MAF-PLL and its

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frequency adaptive implementation are presented, in which a performance comparison of the well-tuned MAF-based PLL with a PI controller and the PID controller is presented. The PID-type MAF-PLL is shown to have a higher bandwidth giving a faster dynamic response while decreasing the noise immunity and disturbance rejection capability. A novel MAF-based PLL consisting of a frequency detector and an initial phase is presented in [26], in which the effect of discrete sampling on the MAF is analyzed and a linear interpolation is employed to enhance the performance of the MAF. In [27], a novel design of a low-gain PLL introducing an adaptive MAF before the loop-filter (LF) and its discrete domain model are presented. Compared with the conventional high gain SRF-PLL, the phase and voltage frequency errors are reduced and the phase angle tracking is faster and more accurate. In [28], a quasi-type-1 PLL (QT1-PLL) is presented. In this structure, the proportional integral (PI) controller is replaced by a simple gain. Thus, a larger open-loop bandwidth can be realized. However, the QT1-PLL cannot filter out the dc offset or even order harmonics. In [29] a differential MAF-PLL is proposed. This PLL can rapidly eliminate the low order harmonics by narrowing the window width of the MAF. In [30] several types of PLL techniques including MAF-PLL are compared to perform the synchronization of active power filter. According to the results, the author has demonstrated that the MAF-PLL provides good filtering capability, which is attained at the cost of slower dynamic response.

In order to improve the dynamic response, many techniques have been proposed by the researchers. Delayed signal cancellation PLL (DSC-PLL) is proposed recently in [31] that shows good capability in filtering only certain orders of harmonics. In [32] a sag detection algorithm based on DSC is proposed for a dynamic voltage restorer. A digital filter based phase lead compensator is cascaded into CDSC-PLL to improve the transient response [33]. In [34] a new open loop synchronization technique based on compensating the phase deviation is proposed. For eliminating a quantified set of harmonics multiple DSC blocks can be cascaded with different time delays [35]–[39]. Nevertheless, in order to eliminate all orders of harmonics five DSC blocks are necessary to be cascaded. In [40] an improved DSC-PLL including a phase lead compensator is proposed with good filtering capability and fast dynamic response. An adaptive DSC-PLL is proposed in [41] that provides more flexibility to configure the undesired order of harmonics. In [18] harmonic extraction based on generalized trigonometric function delayed signal cancellation (GTFDSC) is proposed to extract either the fundamental component or the desired harmonic component.

The PLL techniques discussed above have been evaluated in the presence of harmonics, but effect of interharmonics on the performance of these PLL techniques has not been considered. Interharmonics are any signal of a frequency that is not an integer multiple of the fundamental frequency. Interharmonics are not periodic at the fundamental frequency, so any waveform that is non-periodic on the power system frequency will include interharmonics distortion. Power system interharmonics are most often created by two general phenomena. The first is rapid non-periodic changes in current and voltage caused by loads operating in a transient state (temporarily or permanently) or when voltage or current amplitude modulation is implemented for control purposes. The second source of interharmonics is static converter switching not synchronized to the power system frequency (asynchronous switching). Some specific sources of interharmonics include arcing loads, induction motors (under some conditions), electronic frequency converters, variable load drives, voltage source converters and power line communications.

Interharmonics, like harmonics, add additional signals to the power system. These additional signals can cause a number of effects, particularly if they are magnified by resonance. The wider the range of frequencies present, the greater the risk of resonance. Many of the effects of interharmonics are similar to those of harmonics, but some are unique as a result of their non-periodic nature.

In this paper the performance of three PLL techniques including SRF-PLL, MAF-PLL and CDSC-PLL is analyzed in the presence of Interharmonics. The effects of interharmonics on dynamic response and filtering capability of PLL techniques are studied. This study will be helpful in exploring the advantages and shortcomings of these PLL techniques under such distorted grid conditions. In section II a brief overview of the PLL techniques is presented. Section III gives detailed simulation results and section IV concludes the paper.

II. OVERVIEW OF PLL TECHNIQUES

In this section a brief overview of three PLL techniques including SRF-PLL, MAF-PLL and CDSC-PLL is outlined.

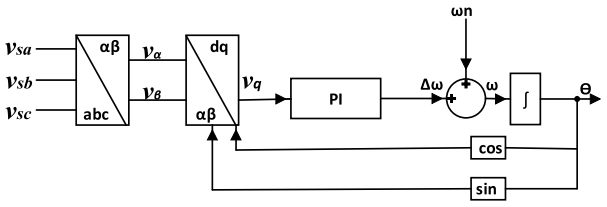

FIGURE 1. Structure of SRF-PLL.

A. SRF_PLL

Synchronous reference frame PLL (SRF-PLL) is the standard PLL used in three phase applications. The SRF-PLL is simple to implement and has fast dynamic response in addition to accurate phase detection in case of normal grid conditions [42]. The basic block diagram of the SRF-PLL is shown in Fig.1. The proportional–integral (PI) controller is used to ensure that $v_d = 0$ in the steady state and the grid voltage vector is perfectly aligned along the q-axis. The output of the controller is added with the nominal frequency of the grid and fed to the integrator. The integrator acts on the frequency error signal and outputs the phase angle θ value.

This phase angle θ value is fed back to the transformation block resulting in a closed control loop. The unit vectors ($\sin\theta$ & $\cos\theta$), ω (estimated frequency) and θ (estimated phase) are the outputs of the SRF-PLL.

The three-phase voltage signals $v_{sa.}, v_{sb}$ and v_{sc} are connected to the input of the first block of PLL where Clark's transformation is applied to convert the three phase voltages in *abc* reference frame into $\alpha\beta$ stationary reference frame as shown in (1).

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \tag{1}$$

The voltages in d-q frame are obtained by Park transformation with the help of (2).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2}$$

The q-axis component is the voltage of interest as it provides the phase error information and is given by (3).

$$v_q = v_\alpha cos(\theta) + v_\beta sin(\theta) \tag{3}$$

The estimated frequency ω is given by (4).

$$\omega = k_p v_q + k_i \int v_q dt + \omega_n \tag{4}$$

Where ω_n is the nominal value of the grid frequency, k_p and k_i are the gains of proportional and integral controllers.

B. MAF_PLL

The harmonic filtering capability and response speed of SRF-PLL is decreased for adverse grid conditions [43]. The phase estimation of SRF-PLL can be improved by lowering the bandwidth but this will result in a slow dynamic response. Different techniques have been worked out to improve the performance of SRF-PLL under adverse grid conditions by applying pre-filtering techniques to the input signal. Moving average filter PLL is a good solution for adverse grid conditions. Moving average filter is a linear-phase filter that allows the dc component to pass through and completely blocks frequency components of integer multiples of $1/T_w$ in Hertz [44]. The MAF technique is the most popular and widely used technique as this filter has significant advantages including easy implementation, complete rejection of low order harmonics and low computational load. But the response slows down in the presence of MAF in the closed loop of PLL. The schematic diagram of MAF-PLL is shown in Fig.2.

MAF can be described in continuous domain and discrete domain as shown in (5) & (6) respectively.

$$Y(t) = \frac{1}{T_w} \int_{t-Tw}^{t} X(\tau)\, d\tau \tag{5}$$

$$Y(k) = \frac{1}{N} \sum_{n=0}^{N-1} X(k-n) \tag{6}$$

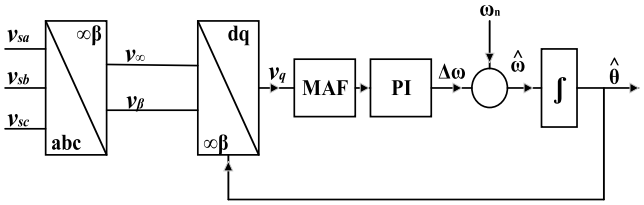

FIGURE 2. Schematic diagram of MAF-PLL.

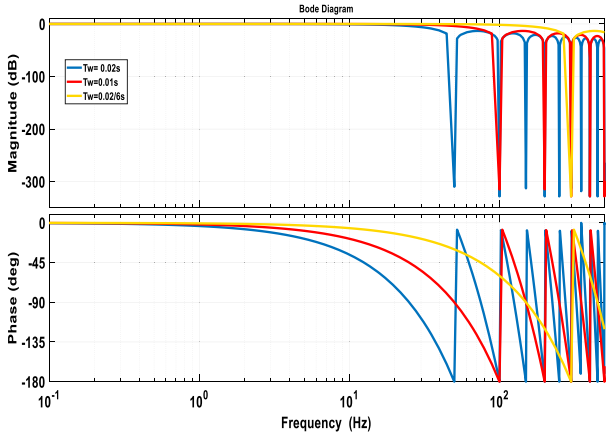

FIGURE 3. Bode diagram of MAF.

Where T_w is the window length of MAF. In Laplace domain the MAF is described as:

$$MAF_G(s) = \frac{Y(s)}{X(s)} = \frac{1 - e^{-T_w s}}{T_w s} \tag{7}$$

It can be seen from (7) that the MAF needs a time equal to its window width to reach steady-state condition. Hence, a wider window width will result in a slower MAF transient response and it will also result in a smaller MAF-PLL open-loop bandwidth. According to Padè approximation the delay time of (7) can be approximated as shown below:

$$e^{-T_w s} \approx \frac{1 - (-T_w s/2)}{T_w s + (-T_w s/2)} \tag{8}$$

The substitution of (8) in (7) results in

$$MAF_G(s) \approx \frac{1}{1 + (T_w s/2)} \tag{9}$$

Substituting $s = j\omega$ in (9), the magnitude and phase margin of the MAF can be expressed as:

$$|MAF_G(j\omega)| = \left| \frac{\sin(\omega T_w/2)}{\omega T_w/2} \right| \angle -\omega T_w/2 \tag{10}$$

The MAF-PLL effectively block the grid disturbances, but at the cost of slowing down its transient response. This characteristic can be visualized through its open loop bode plot shown in Fig.3 for different window lengths. Selection of *Tw* is the most important issue to be considered in designing a MAF because *Tw* can determine the dynamic response speed and filtering capability of MAF-PLL. *Tw* is chosen according to the perturbation. For example, *Tw* should be selected to

1/6 cycle in a 50 Hz grid system to eliminate the harmonics of order 5, 7, 11, 13…etc. For triplen harmonics (3, 9, 27….) the bandwidth must be selected to 1/2 cycle and for even harmonics (2, 4, 6…) the bandwidth must be selected to 1 cycle.

Small Signal Model: In order to simplify the stability analysis and dynamic performance study, small signal model of MAF-PLL is developed. The three phase input voltages of MAF-PLL are represented as:

$$\begin{aligned} v_{sa} &= \sum\nolimits_{ih} \left[V_{ih}^{+} \cos\left(\theta_{ih}^{+}\right) + V_{ih}^{-} \cos\left(\theta_{ih}^{-}\right)\right] \\ v_{sb} &= \sum\nolimits_{ih} \left[V_{ih}^{+} \cos\left(\theta_{ih}^{+} - \frac{2\pi}{3}\right) + V_{ih}^{-} \cos\left(\theta_{ih}^{-} + \frac{2\pi}{3}\right)\right] \\ v_{sc} &= \sum\nolimits_{ih} \left[V_{ih}^{+} \cos\left(\theta_{ih}^{+} + \frac{2\pi}{3}\right) + V_{ih}^{-} \cos\left(\theta_{ih}^{-} - \frac{2\pi}{3}\right)\right] \end{aligned} \tag{11}$$

where $V_{ih}^{+}(V_{ih}^{-})$ and $\theta_{ih}^{+}(\theta_{ih}^{-})$ are the amplitude and phase angle of the interharmonics component of the input voltages. Clark's transformation is applied to yield

$$\begin{aligned} v_{\alpha}(t) &= \sum\nolimits_{ih} \left[V_{ih}^{+} \cos\left(\theta_{ih}^{+}\right) + V_{ih}^{-} \cos\left(\theta_{ih}^{-}\right)\right] \\ v_{\beta}(t) &= \sum\nolimits_{ih} \left[V_{ih}^{+} \cos\left(\theta_{ih}^{+}\right) - V_{ih}^{-} \cos\left(\theta_{ih}^{-}\right)\right] \end{aligned} \tag{12}$$

The q-axis component is attained using Park's transformation.

$$v_q(t) = \sum\nolimits_{ih} \left[V_{ih}^{+} \sin\left(\theta_{ih}^{+} - \hat{\theta}\right) + V_{ih}^{-} \sin\left(\theta_{ih}^{-} + \hat{\theta}\right)\right] \tag{13}$$

Under a quasi-locked state (i.e $\omega = \hat{\omega}$ and $\theta = \hat{\theta}$) (13) can be approximated by

$$v_q(t) \approx V_1 \left(\theta - \hat{\theta}\right) + f(2\omega, 4\omega, 6\omega, \ldots) \tag{14}$$

Where $f(2\omega, 4\omega, 6\omega \ldots)$ represents the disturbance. Using (14) and Fig.2 the small signal model of MAF-PLL is developed as shown in Fig.4.

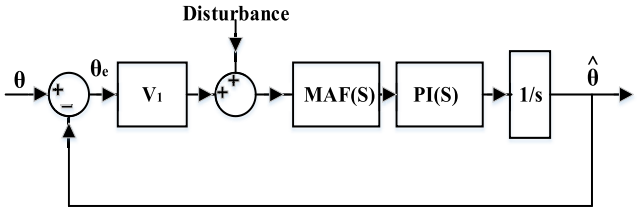

FIGURE 4. Small signal model of MAF.

C. CASCADED DELAYED SIGNAL CANCELLATION

In order to improve the performance of PLL in adverse grid conditions, initially delayed signal cancellation (DSC) technique is used. The positive and negative sequence components of the grid voltage are detached according to the voltage vector in a stationary ($\alpha\beta$) reference frame and the voltage vector is delayed by a quarter of a cycle.

The basic idea of the delayed signal cancellation method is to cancel a signal by adding the signal to its time-delayed opposite phase version of the signal [45]. Generally, two signals of opposite phase cancel each other when added. This method can be used to create a harmonic free input signal. Therefore, it is necessary to create a 180 degrees phase shift through time delay in the harmonics of the input signal to cancel them. Further adding the input signal and the time-delayed harmonics signal cancels the harmonics present in the signal, and the input signal is free from harmonics. In the process, two signals of the same magnitude are added, therefore to maintain the DC gain of the input signal, the resultant signal is divided by 2 [46]. The general expression of the single block of DSC operator is shown in (15).

$$y(t) = \frac{1}{2}[x(t) + x\left(t - \frac{T}{m}\right)] \tag{15}$$

Where m is the delay factor, x (t) is the input and y (t) is the output of the block. The single DSC module can eliminate parts of harmonic meanwhile do not amplify others simultaneously. The block diagram of a single DSC module operating on the voltages in $\alpha\beta$ frame is shown in Fig.5.

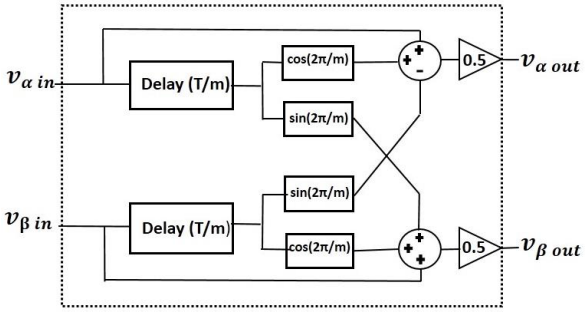

FIGURE 5. Single DSC module.

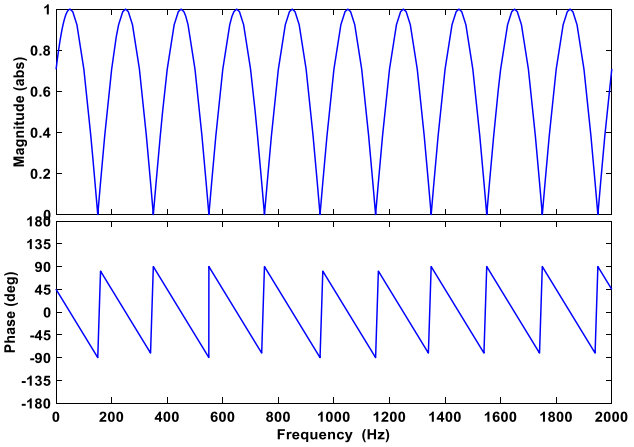

FIGURE 6. Frequency response of DSC4 operator.

The DSC block can be expressed mathematically by (16).

$$v_{\alpha\beta\ out} = \frac{1}{2}[v_{\alpha\beta in}(t) + e^{\frac{j2\pi}{m}} v_{\alpha\beta\ in}\left(t - \frac{T}{m}\right)] \tag{16}$$

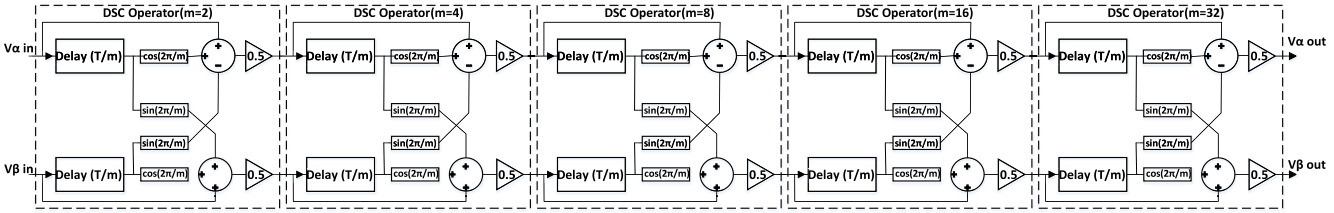

FIGURE 7. Structure of CDSC.

The Laplace transform of (16) results in (17).

$$v_{\alpha\beta\ out}(s) = \frac{1}{2}[1 + e^{\frac{j2\pi}{m}} e^{\frac{-T}{m}s}]v_{\alpha\beta\ in}(s) \tag{17}$$

Where

$$\frac{1}{2}\left[1 + e^{\frac{j2\pi}{m}} e^{\frac{-T}{m}s}\right] = \alpha\beta\mathrm{DSC}_m(s) \tag{18}$$

Substituting $s = jw$ in (18) and applying mathematical simplifications, the magnitude and phase angle can be determined as

$$\alpha\beta\mathrm{DSC}_m(j\omega) = \left|\cos(\frac{\omega T}{2m} - \frac{\pi}{m})\right| \angle(\frac{\omega T}{2m} - \frac{\pi}{m}) \tag{19}$$

Frequency response of DSC operator for m = 4 and T = 0.02s is shown in Fig.6. The $\alpha\beta\mathrm{DSC}_4$ allows the positive sequence components to pass through and blocks the negative sequence component and rejects harmonics of the order h = 4k-1 (k = 1, 2, 3…). However harmonics of the order h = 4k + 1 are not eliminated.

The DSC operator can be cascaded to cancel wide range of harmonics. The cascaded delayed signal cancellation (CDSC) filter is very flexible in adjusting the delay time by selecting the number of DSC blocks in series.

The k cascaded $\alpha\beta$DSC operator with delay factors $m_1, m_2, m_3, \ldots, m_k$ can be approximated by

$$\alpha\beta\mathrm{DSC}_{m_1,m_2,m_3,\ldots,m_k}(s) = \prod_{i=1}^{k} \alpha\beta\mathrm{DSC}_{m_i}(s) \tag{20}$$

In our case single DSC module with delay factor m = 2, 4, 8, 16 and 32 respectively are cascaded as shown in Fig.7. The resultant operator $\alpha\beta$ $\mathrm{DSC}_{2,4,8,16,32}$ is described in s-domain as:

$$\alpha\beta\mathrm{DSC}_{2,4,8,16,32}(s) = \prod_{m=2,4,8,16,32} \alpha\beta\mathrm{DSC}_m(s) \tag{21}$$

Each DSC is configured to eliminate certain harmonics, and the CDSC collectively eliminates all undesired harmonics resting in the input. The cascading of DSC blocks results in elimination of all dominant harmonic.

The transfer function $\alpha\beta\mathrm{DSC}_m$ as shown in (18) can be re-written as

$$\alpha\beta\mathrm{DSC}_m(s) = \frac{1}{2}[1 + e^{-(\frac{sT}{m} - \frac{j2\pi}{m})}] \tag{22}$$

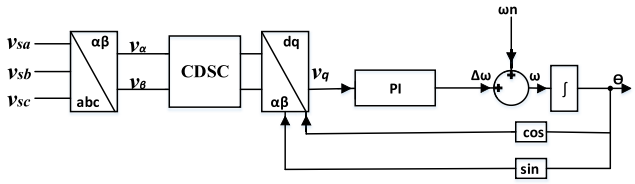

FIGURE 8. Block diagram of CDSC-PLL.

Using Padè approximation the delay term of (22) can be approximated as

$$e^{-(\frac{sT}{m} - \frac{j2\pi}{m})} = \frac{1 - (\frac{sT}{2m} - \frac{j\pi}{m})}{1 + (\frac{sT}{2m} - \frac{j\pi}{m})} \tag{23}$$

Thus the transfer function $\alpha\beta\mathrm{DSC}_m$ can be approximated as

$$\alpha\beta\mathrm{DSC}_m(s) \approx \frac{1}{1 + \frac{T}{2m}(s - \frac{j2\pi}{T})} \tag{24}$$

where $2\pi/T = \omega_n$ is the nominal value of grid frequency.

The transfer function of two cascaded $\alpha\beta$ DSC operators with delay factors m_1 and m_2 can be written as

$$\alpha\beta\mathrm{DSC}_{m_1,m_2}(s) = \alpha\beta\mathrm{DSC}_{m_1}(s)\,\alpha\beta\mathrm{DSC}_{m_2}(s) \tag{25}$$

$$\begin{aligned}\alpha\beta\mathrm{DSC}_{m_1,m_2}(s) &\approx \frac{1}{1 + \frac{T}{2m_1}(s - j\omega_n)} \frac{1}{1 + \frac{T}{2m_2}(s - j\omega_n)} \\ &= \frac{1}{1 + \frac{T}{2}\left(\frac{1}{m_1} + \frac{1}{m_2}\right)(s - j\omega_n) + \frac{T^2}{4m_1m_2}(s - j\omega_n)^2}\end{aligned} \tag{26}$$

The second order term in (26) is negligible at frequencies close to the nominal frequency. Therefore it can be further simplified as

$$\alpha\beta\mathrm{DSC}_{m_1,m_2}(s) \approx \frac{1}{1 + \frac{T}{2}\left(\frac{1}{m_1} + \frac{1}{m_2}\right)(s - j\omega_n)} \tag{27}$$

Similarly the transfer function for k cascaded operators with delay factor $m_i (i = 1, 2, 3, \ldots, k)$ can be approximated by

$$\alpha\beta\mathrm{DSC}_{m_1,m_2,m_3,\ldots,m_k}(s) = \frac{1}{1 + \frac{T}{2}\sum_{i=1}^{k}(\frac{1}{m_i})(s - j\omega_n)} \tag{28}$$

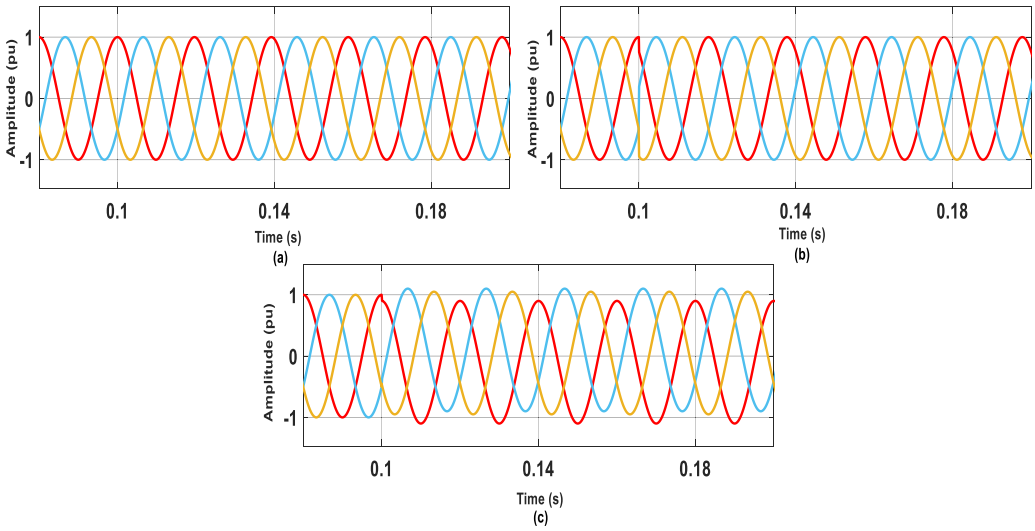

FIGURE 9. Grid voltage test conditions. (a) Frequency jump. (b) Phase jump. (c) Presense of dc offset.

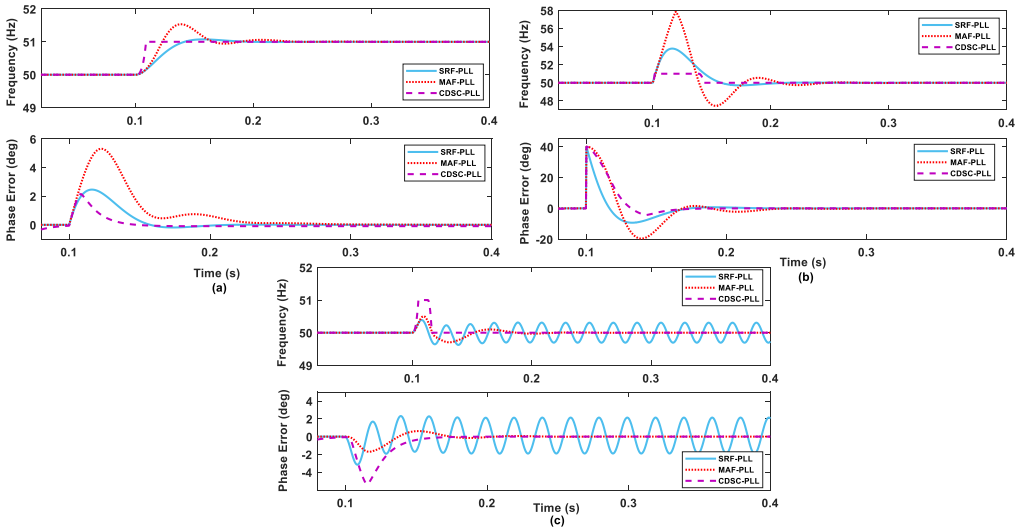

FIGURE 10. Harmonics free grid voltage under. (a) Frequency Jump. (b) Phase jump. (c) Presense of dc offset.

Using (28) the transfer function for $\alpha\beta\text{DSC}_{2,4,8,16,32}$ operator is given by (29).

$$\alpha\beta\text{DSC}_{2,4,8,16,32}\,(s) = \frac{1}{1 + \frac{31T}{64}\,(s - j\omega_n)} \tag{29}$$

The CDSC-PLL control block is shown in Fig. 8 which comprises of a transformation block, a delay operator, a PI controller and an integrator. The delayed signal cancellation is applied to α-β co-ordinates of the voltage signals. After the implementation of CDSC block the voltage signals are again transformed from α-βco-ordinates to d-q co-ordinates.

III. SIMULATION RESULTS

In this section, the three PLL techniques overviewed in the previous section are evaluated in the presence of different grid conditions. The comparison between these three techniques is performed under Matlab/Simulink environment. The nominal grid frequency is set to 50 Hz. Three test cases are considered for performance evaluation.

A) **Test Case 1**: In this test the grid voltage undergoes a $+1$ Hz frequency step change. The performance index taken in this case is 2% settling time, i.e., the time after which the estimated frequency reaches and remains within 0.02x1 Hz $= 0.02$ Hz. The frequency overshoot and peak phase error is also calculated for performance evaluation.

B) **Test Case 2:** A phase angle jump of $+40°$ is added at 0.1s to further evaluate the techniques. The 2% settling time, i.e., the time after which the phase error reaches and remains within $0.02 \times 40° = 0.8°$ is the main

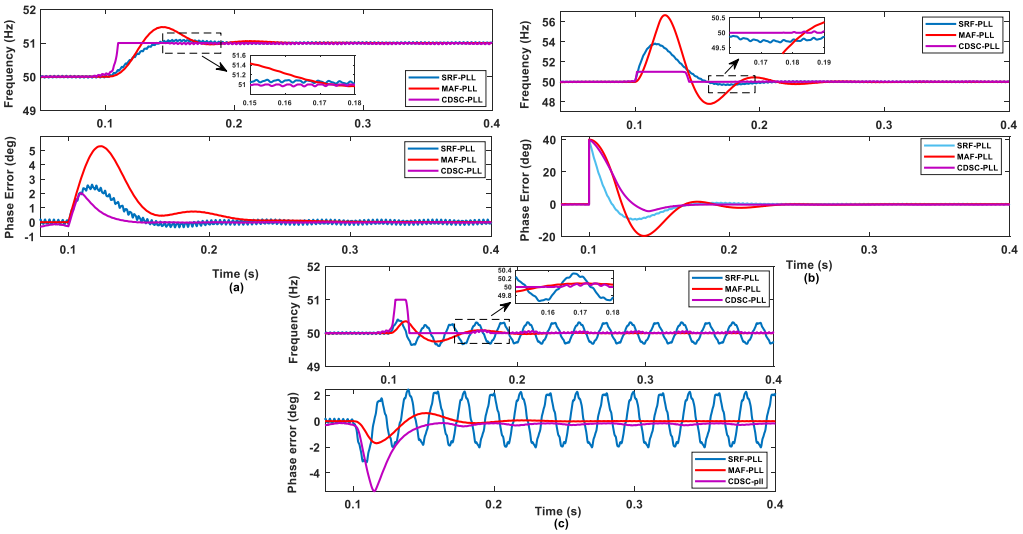

FIGURE 11. Distorted grid voltage (Low amplitude interharmonics) under. (a) Frequency jump. (b) Phase jump. (c) Presense of dc offset.

TABLE 1. Summary of results (harmonics free grid voltage).

Harmonics free grid voltage	SRF-PLL	MAF-PLL	CDSC-PLL
Frequency jump of +1 Hz			
2% settling time	82.735ms	64.716 ms	9.573 ms
Frequency overshoot	1.07 Hz	0.53 Hz	0 Hz
Peak phase error	2.46º	5.3º	2.14º
Phase angle jump of +40º			
2% settling time	124 ms	128.3ms	65.4 ms
Phase overshoot	9.32º	19.61º	4.08º
Peak frequency error	3.69 Hz	7.84 Hz	1 Hz
Presense of DC offset			
2% settling time frequency	--	82.6 ms	16.63 ms
2% settling time phase	--	97.6 ms	68.3 ms
Frequency overshoot	3.82 Hz	0.5 Hz	1 Hz
Phase overshoot	3.129º	1.697º	5.38º0

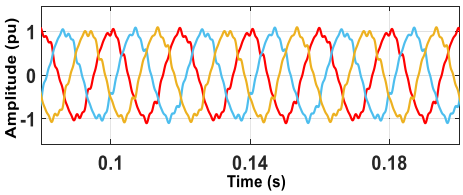

FIGURE 12. Low amplitude interharmonics in grid voltage.

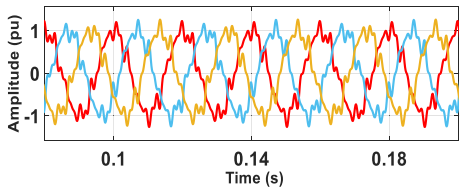

FIGURE 13. High amplitude interharmonics in grid voltage.

TABLE 2. Parameters of low amplitude interharmonics.

Voltage component	Amplitude (pu)
Fundamental positive sequence	1
Harmonic order (5.5)	0.04
Harmonic order (7.5)	0.04
Harmonic order (11.5)	0.03
Harmonic order (13.5)	0.03

performance index in this test. The phase overshoot and peak frequency error are also calculated for performance evaluation.

C) **Test Case 3:** In this test the grid voltage is contaminated with the dc offset ($v_{a,dc} = -0.1$ pu, $v_{b,dc} = 0.1$ pu, $v_{c,dc} = 0.05$ pu). The 2% settling time in case of frequency estimation and phase error approaching to zero degrees is calculated. The overshoot in frequency and phase is also considered to evaluate the performance of PLL techniques.

The main objective of this paper is to evaluate the performance of three PLL techniques in the presence of interharmonics. Initially, simulations are performed to evaluate the techniques for harmonics free grid voltage. The techniques are further simulated in the presence of interharmonics in two steps, first with a low amplitude of interharmonics and then with an increased amplitude. The grid voltages under three test conditions are shown in Fig.9 and the achieved results for the PLL techniques under three test conditions are shown in Fig.10. Table 1 shows the results of PLL techniques for harmonics free grid voltage under three test conditions.

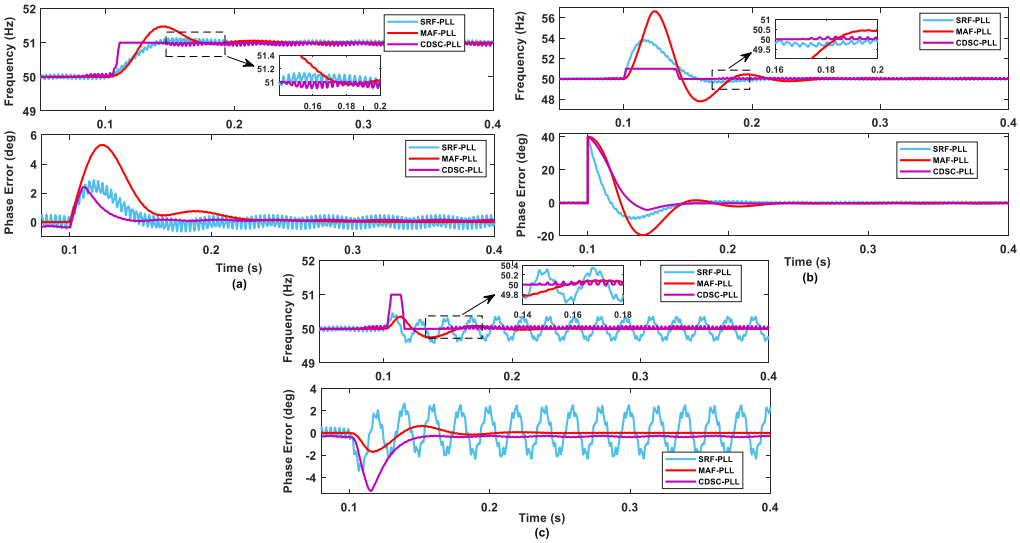

FIGURE 14. Distorted grid voltage (High amplitude interharmonics). (a) Frequency jump. (b) Phase jump. (c) Presense of dc offset.

It is observed from the simulation results that for test case 1 CDSC-PLL takes less than a half cycle to settle down in estimating the frequency, whereas SRF-PLL and MAF-PLL settle to frequency jump in more than four cycles and three cycles respectively. The frequency overshoot and peak phase error of CDSC-PLL is also less than the other two techniques. When a phase angle jump is added, the performance of CDSC-PLL is again better among the three techniques in terms of settling time. The phase overshoot and peak frequency error is again less than the other techniques. For further evaluation, dc offset is added as per test case 3. In this case the CDSC-PLL has better dynamic response but the overshoot in frequency and phase of CDSC-PLL is larger than SRF-PLL and MAF-PLL. In this case the performance of SRF-PLL is greatly affected as it fails to settle down to a change in frequency and phase.

The three tests are performed again by adding interharmonics of low amplitude to the grid voltages. The parameters of interharmonics are listed in Table 2. The simulation results for the PLL techniques in three test cases are shown in Fig.11 and the three phase grid voltages contaminated with interharmonics are shown in Fig.12.

When a frequency jump is added at 0.1s the CDSC-PLL again give a quick response in estimating the grid frequency and phase but the filtering capability of SRF-PLL and CDSC-PLL is reduced as compared to MAF-PLL as indicated in the zoomed view. The MAF-PLL shows a very slow response in estimation of frequency and phase. The addition of phase jump and dc offset to the grid voltage results in almost the same behavior in terms of dynamic response as in the case of harmonics free voltages but in this case ripples appear in the response of SRF-PLL and CDSC-PLL, and the SRF-PLL is not able to estimate the frequency and phase in the presense of dc offset. The simulation results obtained in this case are shown in Table 3.

TABLE 3. Summary of results (interharmonics).

Interharmonics (Low Amplitude)	SRF-PLL	MAF-PLL	CDSC-PLL
Frequency jump of +1 Hz			
2% settling time	83.89 ms	71.35 ms	10.152 ms
Frequency overshoot	1.08 Hz	0.47 Hz	0 Hz
Peak phase error	2.55º	5.31º	2.25º
Phase angle jump of +40º			
2% settling time	73.49 ms	142.83ms	64.3 ms
Phase overshoot	9.148º	19.61º	4.33º
Peak frequency error		5.66 Hz	1 Hz
Presense of DC offset			
2% settling time frequency	--	56.12 ms	16.3 ms
2% settling time phase	--	97.8 ms	59.38 ms
Frequency overshoot	0.39 Hz	0.35 Hz	1 Hz
Phase overshoot	6.345º	1.708º	5.4º

TABLE 4. Parameters of high amplitude interharmonics.

Voltage component	Amplitude (pu)
Fundamental positive sequence	1
Harmonic order (5.5)	0.1
Harmonic order (7.5)	0.1
Harmonic order (11.5)	0.08
Harmonic order (13.5)	0.08

Finally the PLL techniques are evaluated by increasing the amplitude of interharmonics in the grid voltage. The parameters of interharmonics used for simulation of PLL techniques in this case are given in Table 4 and the distorted grid voltages are shown in Fig.13.

TABLE 5. Summary of results (inter harmonics).

Interharmonics (High Amplitude)	SRF-PLL	MAF-PLL	CDSC-PLL
Frequency jump of +1 Hz			
2% settling time	83.7 ms	71.4 ms	12.88 ms
Frequency overshoot	0.01 Hz	0.47 Hz	0 Hz
Peak phase error	2.35º	5.3º	2.4º
Phase angle jump of +40º			
2% settling time	79.61 ms	142.83 ms	72.14 ms
Phase overshoot	9.49º	19.57º	4.28º
Peak frequency error	3.87 Hz	6.65 Hz	1 Hz
Presense of DC offset			
2% settling time frequency	--	85.6 ms	12.14 ms
2% settling time phase	--	104.2 ms	57.17 ms
Frequency overshoot	0.46 Hz	0.36 Hz	1 Hz
Phase overshoot	3.42º	1.71º	5.22º

The three test conditions are again applied and the behavior of PLL techniques is elaborated in Fig.14. The summary of results is given in Table 5. It can be observed that response time and overshoot in frequency and phase of all the techniques are almost the same as in previous test but the number of ripples is increased in the response of SRF-PLL and CDSC-PLL in the estimation of frequency and phase and also in the presense of dc offset. These ripples may lead to wrong estimation of frequency and phase and even failure in the case of SRF-PLL.

IV. CONCLUSION

In this paper a detailed comparison is made between three PLL techniques used for synchronization of grid connected power converters, specifically in the presence of interharmonics. The performance is evaluated on the basis of estimated frequency and phase in the presence of frequency drift, phase angle jump and dc offset. It is observed from the simulation results that the performance of SRF-PLL is good under harmonics free grid voltage but is greatly affected in the presence of interharmonics. The presence of dc offset also significantly reduces its filtering capability. The filtering capability of MAF-PLL is good but its dynamic response is slow under three test conditions. The overshoot in frequency and peak phase error at the event of frequency jump for MAF-PLL is also larger. On the other hand CDSC-PLL comparatively shows fast dynamic response in estimating the frequency and phase but the presence of interharmonics reduces its filtering capability and the performance declines further with increased amplitude of interharmonics. The overshoot in frequency and phase of CDSC-PLL is also larger as compared to the other two techniques in the presence of dc offset.

In future work the CDSC-PLL technique having the fast dynamic response among all can be applied in applications that contain interharmonics, such as speed drives of shipboard power systems and grid connected PV inverters.

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