A Single-Phase Transformer-Based Cascaded Asymmetric Multilevel Inverter With Balanced Power Distribution

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ABSTRACT This paper introduces a method to enforce balanced power distribution between the stages of a single-phase transformer-based cascaded multilevel inverter using the new asymmetric ratio 6:7:8:9 between stages. Since the inverter is fed by a single DC source, asymmetry is enforced by means of the transformer turns ratio providing multiple redundant switching patterns to synthesize an output signal of until 35 levels. As it is developed in the paper, optimum switching patterns for the proposed ratio allow reducing typical power unbalance produced by commonly used ratios in four stage multilevel inverters (1:2:4:8 and 1:3:9:27). The proposed method consists on determining off-line the best switching patterns for minimizing deviation error, and then, storing them as lock-up tables in the digital device controlling the inverter. By permanently reproducing the selected switching patterns, balanced power distribution is achieved. A closed-loop control approach to regulate the RMS value of the output voltage compatible with the proposed method is also developed. The experimental results using a laboratory prototype are presented validating the entire approach.

INDEX TERMS Balanced power distribution, cascaded asymmetrical multilevel inverter, transformer-based multilevel inverter.

I. INTRODUCTION

In the last years, multilevel inverters (MLI) have become a competitive solution against conventional inverters based on pulse-width modulation (PWM), which are still very popular in the market. MLI can be used for uninterruptible power supply (UPS), photovoltaic generators, high voltage direct current (HVDC) networks, and generally any DC-AC conversion application. Among the different advantages attributed to these converters, it is worth mentioning a high-quality output voltage associated to a low harmonic distortion, as well as a high efficiency due to reduced switching frequency in semiconductor devices [1]–[3]. As drawbacks it can be mentioned the large number of elements in the system, the lack

of homogeneity in the voltage and current specifications of power semiconductors and the high complexity of the control electronics. Hence, a great interest prevails today in offsetting these drawbacks.

MLI can be classified into three main groups, according to their typology: a) diode clamped, b) flying capacitor, and c) cascaded MLI (CMLI) [4], [5]. Compared to the other topologies, CMLI have the advantage of using independent stages of voltage source inverters (VSI) (conventionally full-bridges), which reduces complexity regardless of the desired number of levels in the output signal. The cascade connection of the inverter stages can be carried out through different ways depending on the converter topology, keeping in all of them the need for galvanic isolation in either the DC side or the AC side. When galvanic isolation is provided on the DC side, several independent isolated DC sources are necessary to feed

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the stages of the inverter. On the other hand, using a single DC source requires incorporating low-frequency transformers for each inverter stage. These last topologies are known in the literature as transformer –based cascaded topologies. Although their cost can be considerably higher, they are attractive when regarding control simplicity, robustness and reliability provided by low-frequency galvanic isolation [6]–[8].

The configuration of a MLI is defined by the relations between the amplitudes of the input DC sources. If these amplitudes are equal, the inverter is denominated symmetric and if the amplitudes are different, the inverter is denoted asymmetric [9]. On the other hand, for transformer-based cascaded topologies fed by a single DC source such as the studied topology, this definition involves the transformers turn ratio: the configuration of the inverter is symmetric if the turn ratios of all inverter stages are equal and asymmetric if they are different [10]–[12]. Figure 1 depicts the circuit diagram of a cascaded transformer-based multilevel inverter fed by a single DC source.
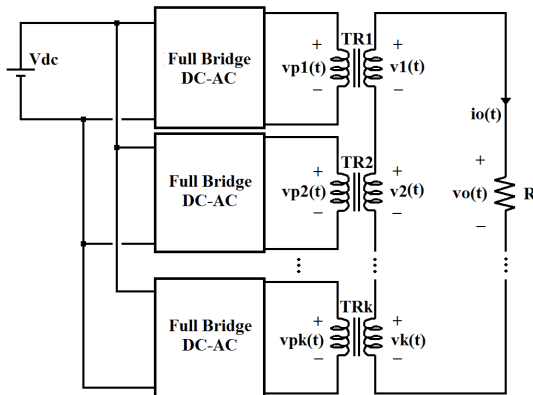

FIGURE 1. Transformer- based cascaded multilevel inverter.

Symmetric configurations of MLI permit obtaining $2N + 1$ output levels from N stages while asymmetrical configurations allow a higher number of levels depending on the ratio between the inverter stages. Using a binary geometric progression to define the ratio between stages, the maximum number of levels at the output will be $2^{N+1} - 1$. Using a ternary geometric progression, the number of levels obtained will be 3^N. For example, considering a multilevel inverter with three stages $(N=3)$, a symmetric ratio 1:1:1 allow obtaining a 7-level signal, an asymmetric binary ratio 1:2:4 allows obtaining a 15-level signal and an asymmetric ternary ratio 1:3:9 allows obtaining a 27-level signal. To obtain each level, the converter stages commutate with positive, negative or null contribution. The way in which the stages of the inverter are commutated to obtain different levels is defined as a switching pattern. As it can be noted, after analyzing the case based on geometric progression of ratios, there is a single way to commutate the inverter stages to obtain each desired level. However, for symmetric ratios, there are multiple possible switching patterns building the same output signal and giving additional properties to the inverter operation [13].
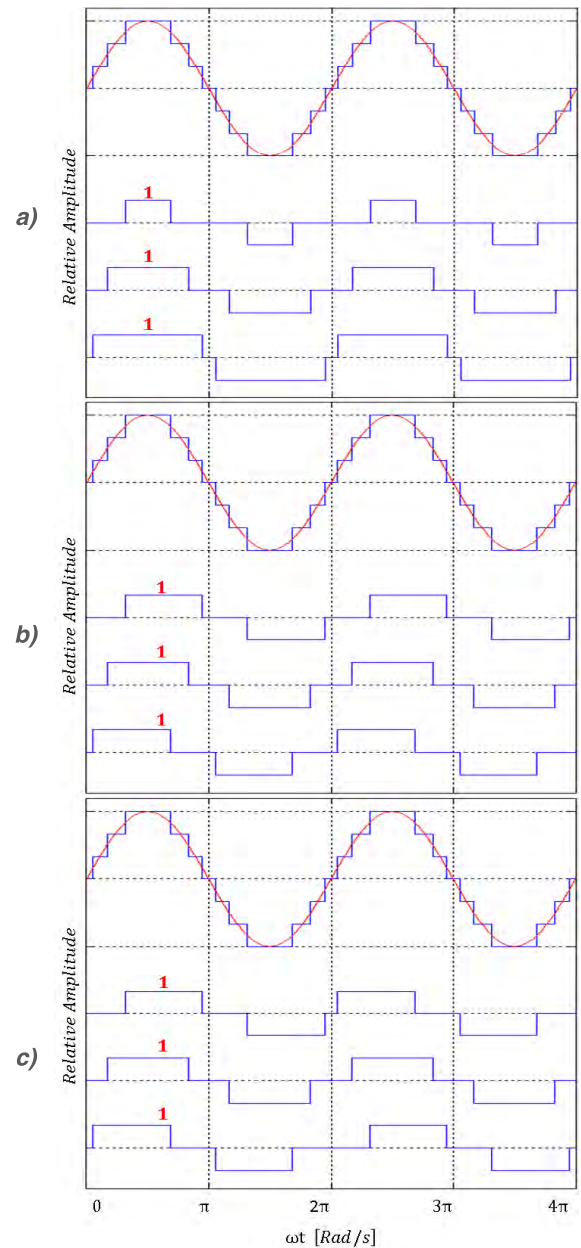

FIGURE 2. Symmetrical configurations for generation of the multilevel sinusoidal signal from three inverter stages: a) conventional switching pattern; b) voltage balanced switching pattern; and c) voltage and power balanced switching pattern.

In Figure 2a depicts the conventional switching pattern for a three stage symmetric MLI. As it is observed, the three stages operate in unbalanced voltage and power regime. In Figure 2b, the switching pattern balances the voltage distribution of the inverter but not the power regime. This feature is evident by regarding that the voltages have a different phase shift with respect to the output voltage and in consequence with respect to the output current. In Figure 2c, the switching pattern yields a balanced operation in voltage showing a two-cycle symmetry.

As a particular case, Figure 3 shows a possible switching pattern balancing voltage and power of the inverter using
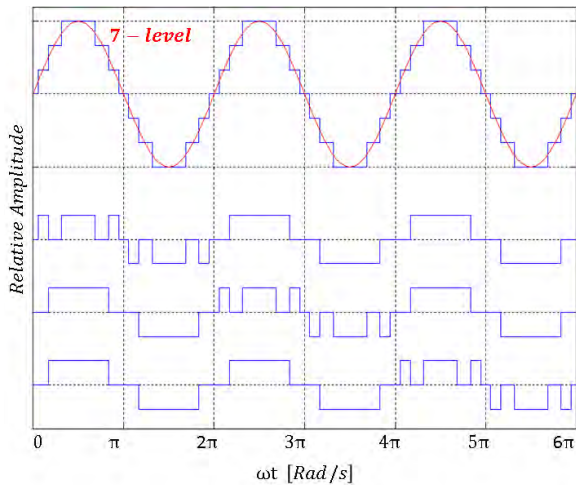
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FIGURE 3. Repeating sequence method for generation of the multilevel sinusoidal signal from three inverter stages.

the repeating sequence method. In this case, balanced power distribution is obtained after a period of three-cycles of the output voltage. Using this method, balanced power distribution for symmetric inverters is relatively easy to be imposed by the control.

For three inverter stages, the simpler asymmetric ratio 1:2:4 depicted in Figure 4 (bottom) allows obtaining a 15-level signal and yields an unbalanced power distribution of 15.01%:36.03%:48.96%. The ternary ratio 1:3:9 shown in Figure 4 (top) allows obtaining 27-levels and results in a deficient power distribution of 3.47%:15.14%:81.39% [8].

To overcome this drawback, other asymmetric configurations have been proposed in the literature using the ratio 1:1:3, namely, 11-levels as depicted in Figure 5 (top) showing a power distribution of 20%:20%:60% and the ratio 1:2:6, providing 9-levels as depicted Figure 5 (bottom) and showing a power distribution of 11%:22%:66% [14]. In this last work, the power balance is slightly improved at expenses of an additional pulse width modulation (PWM) control to ensure a high-quality of the output signal. To the best of the authors' knowledge, combination 16:4:1 is qualified as optimal for three stages corresponding it to the quaternary ratio (43-levels signal). Since not all levels can be produced with this ratio, a high frequency control is required to produce a high quality output signal [14].

The use of four inverter stages in transformer-based MLI topologies is limited because the additional transformer considerably increases the cost and size of the inverter without adding significant advantages to the signal quality. A symmetric relation was used in [15] for a four stage inverter producing a nine levels output signal. Because of the reduced number of levels, the voltage quality without control is poor and requires a feedback control loop and high frequency commutation to reduce the THD. The asymmetric binary ratio 1:2:4:8 was used in [16] providing a 31-level output signal with a power distribution of 7.79%:17.83%:25.79%:50.58%, that result being the closest comparison reference for this
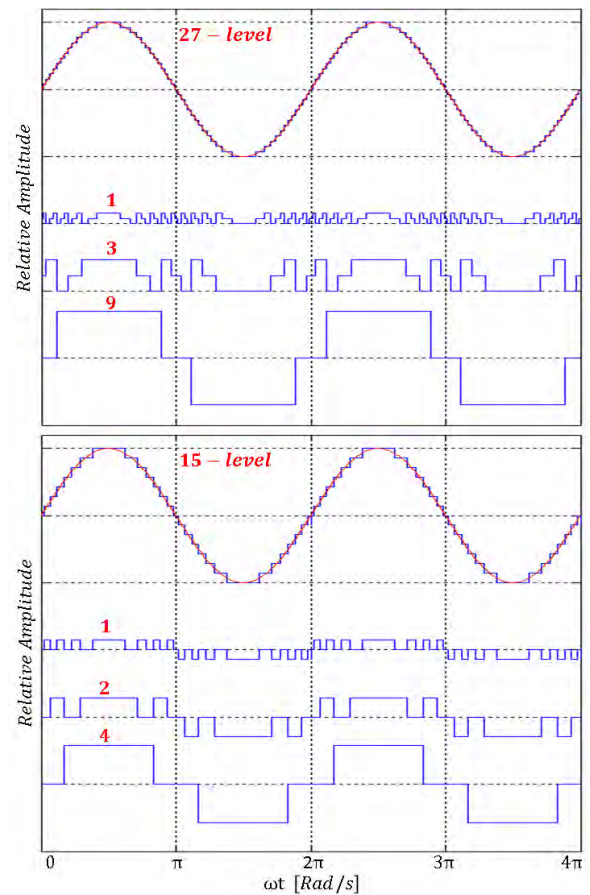

FIGURE 4. Asymmetrical configurations for generation of the multilevel sinusoidal signal from three inverter stages.

work. By using a ternary ratio between stages 1:3:9:27, an 81-level signal is produced increasing considerably the quality of the output voltage. For this ratio also the power distribution between stages of 0.75%:5.39%:16.40%:77.46% is deficient. The output signals of the inverter stages for binary and ternary asymmetric ratios are depicted in Figure 6.

Improving the voltage and power distribution between stages depends on the flexibility of the inverter topology and the ratio between stages. Several methods has been presented until now in literature looking for uniform power distribution or charge balance control as it has been defined by some authors [17]–[20]. Until now, the only way to obtain a highly accurate uniform power distribution has been reported for symmetric inverters using the repeating sequence method depicted in Figure 3. This paper presents for the first time the use of the asymmetric ratio 6:7:8:9 in a four level cascaded multilevel inverter allowing to produce until a 35-level signal in which optimization of the switching pattern leads to a highly balanced power distribution. In order to provide regulation in a wide range of operation conditions. A signal of 31-levels was selected as nominal, producing also 29 or 33 levels when the output voltage increases or decreases outside of a defined range because of variations in the input DC voltage or the load. Although validation of the concept is done using a low-frequency transformer-based topology, it can be
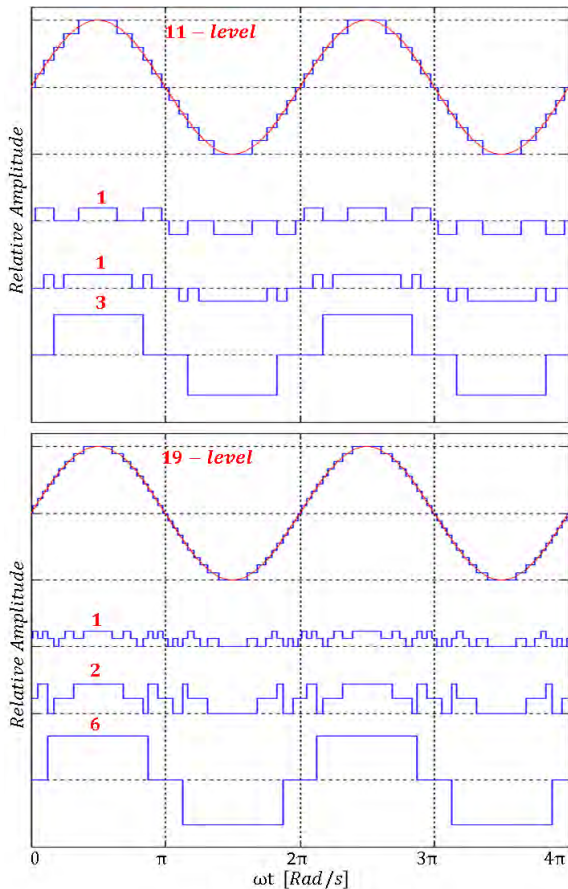
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FIGURE 5. Special asymmetric configurations for generation of the multilevel sinusoidal signal from three inverter stages.

FIGURE 6. Conventional asymmetric configurations for generation of the multilevel sinusoidal signal from four inverter stages.

applied in a converter with the same asymmetric relation between four isolated DC-sources.

The rest of the paper is organized as follows. A complete description of the inverter topology, its principle of operation and design are presented in section II. The synthesis of the optimum switching pattern for nominal conditions is explained in section III and extended for closed-loop operation in section IV. Assessment of the method is illustrated by means of experimental results in section V. Finally, conclusions are given in section VI.

II. CASCADE ASYMMETRICAL TRANSFORMER-BASED MULTILEVEL INVERTER

The selected transformer- based topology corresponds to Figure 1 when the number of inverter stages is four. The following subsections give fundamentals to understand inverter operation and design its components.

A. OBTAINING THE MULTILEVEL OUTPUT SIGNAL

For N cascaded stages, the output voltage of the inverter is computed as follows

$$v_o(\omega t) = v_1(\omega t) + v_2(\omega t) + \cdots + v_N(\omega t)$$
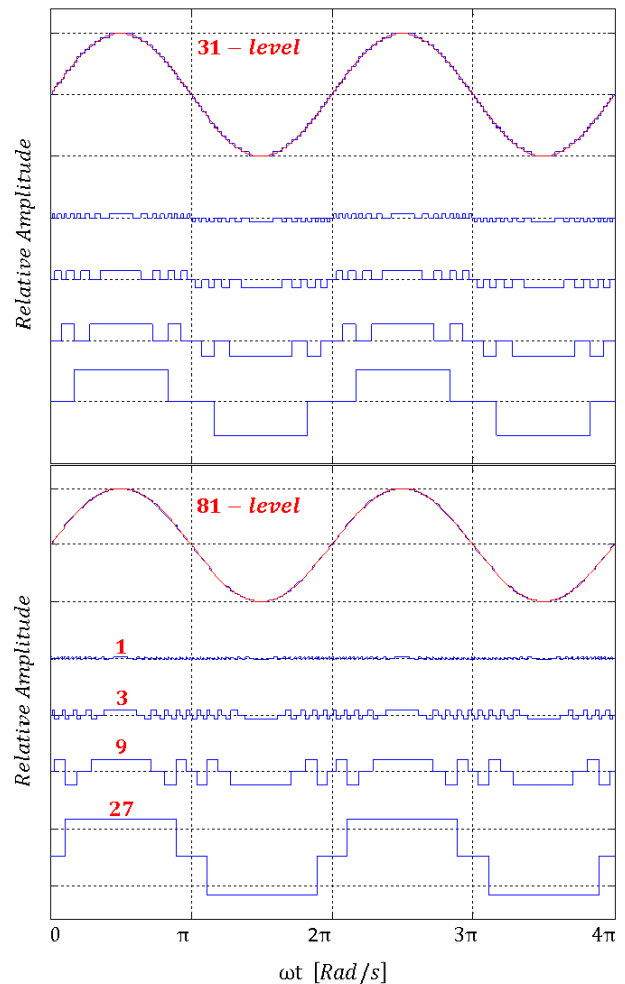$$= \sum_{k=1}^{N} v_k(\omega t), \quad (1)$$

where $v_k(\omega t)$ is the instantaneous output voltage of each stage which is defined by:

$$v_k(\omega t) = V_{dc} T_{R_k} S_{F_k}, \quad (2)$$

where V_{dc} is the magnitude of the DC input voltage, T_{R_k} is the turns ratio of the transformer of each k stage, and S_{F_k} is the instantaneous switching function of each k stage. For the subsequent analysis, S_{F_k} takes the values -1, 0 or 1. Thus, the sum of the output of the stages allows obtaining a signal with M positive integer levels.

Considering that the desired output voltage is $V_{max} \sin \omega t$, the relation between the signal of M positive levels and the amplitude of this reference is defined as $K_m = V_{max}/M$. For example, in Figure 7, the higher positive level of the signal is 5 and the desired amplitude is $V_{max} = 120\sqrt{2}$, then $K_m = 24\sqrt{2}$.

In this paper, the voltage signal is defined considering that the time during which the output voltage signal remains in a voltage level is defined by the coincidence of the middle point between levels with a pure sine wave as it is illustrated
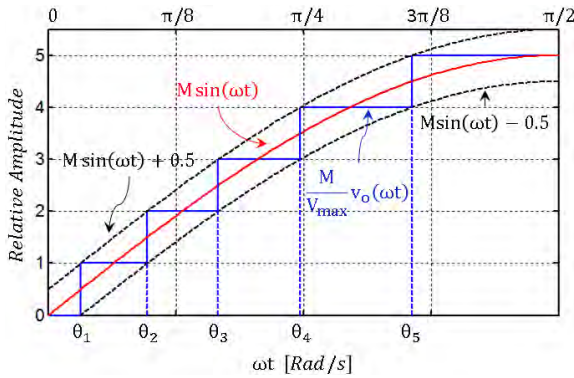
FIGURE 7. 11-level approximation of a sinusoidal signal during the first half of the positive semi-cycle (M= 5).

in Figure 3. In the ωt axis, θ_m determines the end of the m interval and the starting point of the following interval, so that it can be expressed in radians for m = 1, 2, 3…M as follows:

$$\theta_m = \sin^{-1}\left(\frac{2m-1}{2M}\right) \quad (3)$$

Then, each level is defined for the interval $[\theta_m, \theta_{m+1}]$. Because of the symmetry of the sinusoidal signal, the second half of the positive semi-cycle is obtained by inversely reproducing the first half semi-cycle, while the negative semi-cycle is obtained by multiplying by -1 the voltage levels used in the positive semi-cycle. Output signal building based on θ_m angles is summarized in table 1.

TABLE 1. Optimized switching function for 31-levels signal.

Level	Interval start angle	Interval end angle
0	…	θ_1
1	θ_1	θ_2
…	…	…
M-1	θ_{M-1}	θ_M
M	θ_M	$\pi - \theta_M$
M-1	$\pi - \theta_M$	$\pi - \theta_{M-1}$
…	…	…
1	$\pi - \theta_2$	$\pi - \theta_1$
0	$\pi - \theta_1$	$\pi + \theta_1$
-1	$\pi + \theta_1$	$\pi + \theta_2$
…	…	…
-(M-1)	$\pi + \theta_{M-1}$	$\pi + \theta_M$
-M	$\pi + \theta_M$	$2\pi - \theta_M$
-(M-1)	$2\pi - \theta_M$	$2\pi - \theta_{M-1}$
…	…	…
-1	$2\pi - \theta_2$	$2\pi - \theta_1$
0	$2\pi - \theta_1$	θ_1
1	θ_1	θ_2
…	…	…

As it can be observed in Figure 7, the multilevel signal is drawn between two envelopes with one level of difference between them. Thus, the desired signal can be generated by means of either an open loop control based on angles θ_m, or a closed-loop switched control based on the envelopes in the same way as a hysteresis comparator.

Nonetheless, the analysis and results presented in this paper are independent of the control method.

B. THD AND RMS AS FUNCTIONS OF THE NUMBER OF INTEGER LEVELS

The number of levels from which the sinusoidal signal is obtained determines the total harmonic distortion (THD) of the output voltage. Hence, with a higher number of levels, we obtain a lower harmonic distortion, but a greater amount of stages is also required in the inverter. The root mean square (RMS) value of the output signal of the inverter also depends on the number of levels but in a smaller proportion. To evaluate the quality of the output waveform, THD and RMS values are determined. The RMS value considering the symmetry of the signal is defined by:

$$V_o = \frac{V_{max}}{M}\sqrt{M^2 - \frac{2}{\pi}\sum_{m=1}^{M}(2m-1)\sin^{-1}\left(\frac{2m-1}{2M}\right)} \quad (4)$$

On the other hand, the output signal defined from the Fourier series expansion can be expressed as follows:

$$v_o(\omega t) = \sum_{n=1}^{\infty}(a_n\cos n\omega t + b_n\sin n\omega t)$$

Then, considering the odd symmetry of the voltage waveform leads to:

$$v_o(\omega t) = \underbrace{b_1\sin\omega t}_{v_{O_1}(\omega t)} + \underbrace{\sum_{n=2}^{\infty}b_n\sin n\omega t}_{v_{Oh}(\omega t)},$$

where $v_{o1}(\omega t)$ and $v_{oh}(\omega t)$ are the fundamental and harmonic components of the output voltage respectively. Since $v_{o1}(\omega t) = \frac{4V_{max}}{\pi M}\sum_{m=1}^{M}\cos\theta_m$, the RMS value is:

$$V_{o1RMS} = \frac{4V_{max}}{\pi\sqrt{2}M}\sum_{m=1}^{M}\cos\left(\sin^{-1}\left(\frac{2m-1}{2M}\right)\right) \quad (5)$$

Thus, the THD can be exactly determined from (4) and (5) as:

$$THD = \frac{v_{ohRMS}}{v_{o1RMS}} = \sqrt{\left(\frac{v_{oRMS}}{v_{o1RMS}}\right)^2 - 1}$$

$$THD = \sqrt{\left[\frac{M^2 - \frac{2}{\pi}\sum_{m=1}^{M}(2m-1)\sin^{-1}\left(\frac{2m-1}{2M}\right)}{8\left(\frac{1}{\pi}\sum_{m=1}^{M}\cos\left(\sin^{-1}\left(\frac{2m-1}{2M}\right)\right)\right)^2}\right] - 1} \quad (6)$$

As it can be noted, the THD is not dependent on the input voltage V_{dc} or the transformer ratios T_{Rk}. Figure 8 shows the resulting THD as a function of the number of levels for M = 3 and M = 12 respectively, when the expected amplitudes are defined by V_{max}= M. As it can be observed, a number of positive integer levels higher than 14 is required to obtain a THD value lower than 3%. Then, having a signal with
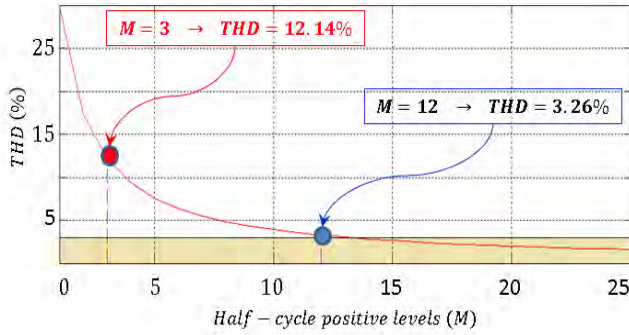
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FIGURE 8. Resulting waveforms and THD for M = 3 and M = 12, and THD as a function of the number of integer levels.

13 positive levels (27-level output voltage) is more than enough to accomplish the international standard requirement of THD<5% [21].

C. TRANSFORMERS TURNS RATIO

The maximum output voltage V_{max} can be obtained as the algebraic sum of the stage output voltages, each of them having a maximum defined by V_{kmax}. Considering a waveform with M positive integer levels which is build using an inverter with N stages, each of one having a weight w_k, these weights define the ratio between stages ($w_1 : w_2 : w_3 : w_4$). Then, the turns ratio for the transformer of each stage 1 :TR_k is obtained as the relation between its maximum output voltage V_{kmax} and the input voltage V_{dc}. Design can be performed by using the following expression:

$$TR_k = \frac{V_{kmax}}{V_{dc}} = \frac{w_k V_{max}}{M V_{dc}} \qquad (7)$$

D. OUTPUT POWER OF THE INVERTER STAGES

The output voltage of each inverter stage is a square-wave that can be modeled using the Fourier expansion as:

$$v_k (\omega t) = V_{1k-max} \sin (\omega t) + \sum_{j=2}^{\infty} V_{j-max} \sin (j\omega t + \theta_j), \qquad (8)$$

where V_{1k-max} is the amplitude of the fundamental component and V_{j-max} is the amplitude of the j-th harmonic. By considering a passive load connected to the output of the inverter, the output current can be defined as:

$$i_o (\omega t) = I_{max} \sin (\omega t + \varphi), \qquad (9)$$

where I_{max} is the amplitude of the output current and φ is the phase shift defined by the load impedance. Current $i_o (\omega t)$ is the same for all inverter stages because of their output series connection. Then, the real power can be computed as:

$$\bar{P} = \frac{I_{max}}{2} \left(\sum_{k=1}^{4} V_{k1-max} \cos \varphi \right), \qquad (10)$$

which is consistent with the superposition principle since voltages V_{k1} have the same frequency.

III. SYNTHESIS OF THE SWITCHING PATTERN

In this work, the proposed asymmetrical relation uses $w_k \in \mathbb{N}$, and configures an arithmetic progression leading to an optimization problem in the discrete field. The selection of w_k implies finding a relation between the levels in the stages that allows obtaining not only the entire signal levels through the algebraic sum of them but also an associated redundancy providing a freedom degree for optimization.

A. REDUNDANCY OBTAINING SIGNAL LEVELS

Because the four stages of the inverter are fed by a single DC source, the voltage stress in semiconductor devices of the stages is the same. Also, in order to preserve similar current stress ratings in the semiconductors, we use in this approach consecutive integer weights adopting the succession w_k= w, w + 1, w + 2, w + 3 to obtain a quarter of cycle of an M-level signal (2M+1 levels inverter). By changing w, it is possible to find more than one solution that yields all voltage levels in an interval between zero and M. This fact implies a redundancy in the way to obtain levels. For example, for M equal to 15, redundancy is found for some values of w in the interval defined by {$w, w \in \mathbb{N}: 3 \leq w \leq 7$}. Figure 9 shows the redundancy distribution as a function of the integer levels in the positive half-cycle of the voltage waveform.
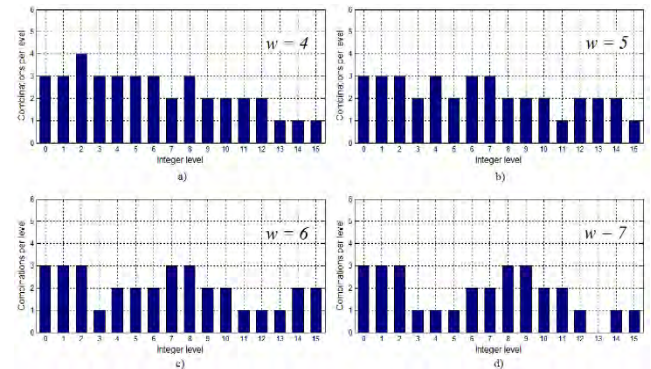

FIGURE 9. Distribution histograms of redundancy vs. levels:
a) 4:5:6:7 ratio; b) 5:6:7:8 ratio; c) 6:7:8:9 ratio; d) 7:8:9:10 ratio.

A value of w = 4 (4:5:6:7 ratio) leads to a major redundancy in the lower levels, which have a lower duration in the voltage waveform, and then lower relevance. Using w = 5 (5:6:7:8 ratio), distributed redundancy is found for almost all levels, but, the maximum level has not redundancy, which compromises the possible advantages of the resulting ratio. With w = 6 (6:7:8:9 ratio), redundancy is obtained in the two more important levels, which has the major duration in the voltage waveform. For w = 7 (7:8:9:10 ratio), the 13-th level is not obtained and there is no redundancy for the highest levels. Thus, defining the redundancy of each level as R_m, the number of possible different sequences to build the output waveform, which is defined as R_{tot}, can be determined as:

$$R_{tot} = \prod_{m=1}^{M} R_m \qquad (11)$$

As a consequence, with 15 positive levels, we have several sequences to obtain a quarter cycle of the sinusoidal signal. The total number of possible switching patterns for cases in which at least fifteen subsequent levels are possible is 279.936 for *w=4*, 186.624 for *w=5,* and finally, 31.104 for *w=6* (see Figure 4). Although, the number of possible switching patterns with lower values of *w* is higher, the absence of redundancy in the maximum level reduces the possibility to achieve a balanced power distribution between stages. It is worth to mention that with selection of w=6, it is possible to obtain also levels 16 and 17, which can contribute to decrease even more the THD of the output voltage in some operation conditions. Also, these two additional levels can be used by a controller to keep regulated the RMS output voltage in a wider range of load or DC input voltage. The possible ways to obtain the seventeen positive integer levels are sketched in table 2.

TABLE 2. Switching functions of the inverter stages for selected ratio.

Positive level	Stage 1 ($w_1 = 6$)	Stage 2 ($w_2 = 7$)	Stage 3 ($w_3 = 8$)	Stage 4 ($w_4 = 9$)
0	0	0	0	0
	1	-1	-1	1
	-1	1	1	-1
1	-1	1	0	0
	0	-1	1	0
	0	0	-1	1
2	-1	0	1	0
	0	-1	0	1
	-1	1	-1	1
3	-1	0	0	1
4	1	1	0	-1
	-1	-1	1	1
5	1	1	-1	0
	1	0	1	-1
6	1	0	0	0
	0	1	1	-1
7	0	1	0	0
	1	-1	1	0
	1	0	-1	1
8	0	0	1	0
	1	-1	0	1
	0	1	-1	1
9	0	0	0	1
	-1	1	1	0
10	-1	1	0	1
	0	-1	1	1
11	-1	0	1	1
12	1	1	1	-1
13	1	1	0	0
14	1	0	1	0
	1	1	-1	1
15	1	0	0	1
	0	1	1	0
16	0	1	0	1
17	0	0	1	1

B. POWER DISTRIBUTION BETWEEN STAGES

Considering the definitions in subsection *II.D*, the average power for each inverter stage can be computed as follows:

$$\bar{P}_k = \frac{I_{max} V_{k1-max}}{2} \cos \varphi, \qquad (12)$$

from which, the mean value of the total output power is obtained as:

$$\bar{P} = \sum_{k=1}^{4} \bar{P}_k = \frac{I_{max} V_{max}}{2} \cos \varphi \qquad (13)$$

The best power distribution between the inverter stages is obtained when the powers $\bar{P}_k$ are equal. Then, for the studied case, the percentage of power processed by each stage is given by (14), having an ideal distribution being obtained when these values are 25% for the four stages.

$$\frac{\bar{P}_k}{\bar{P}} = \frac{V_{k1-max}}{4V_{max}} \times 100\% \qquad (14)$$

For each possible sequence, we can compute this percentage for all inverter stages. For example, for a selected switching pattern, the distribution of an output power of 100 W between four stages is $P_1 = 15$ W, $P_2 = 25$ W, $P_3 = 40$ W, and $P_4 = 20$ W. Then, the ideal distribution of power is $P_k = 100$ W/4 = 25 W, which corresponds to a 25% of the total power. Only the power P_2 has not error compared with the ideal condition since the other stage powers are lower or higher. Stage P_1 has a deviation from the ideal distribution corresponding to a 40% (10 W/ 25 W), stage P_3 has a deviation of 60% (15 W/ 25 W) and P_4 has a deviation of 20% (5 W/ 25 W). Our approach of power equalization finds the sequence which guarantees the minor deviation for all stages. With this aim, the relative error ε_k for the stage k is defined as:

$$\varepsilon_k = \left| \frac{\bar{P}_k - \frac{\bar{P}}{N}}{\frac{\bar{P}}{N}} \right| \times 100\%, \qquad (15)$$

and the set of possible sequences by $W = \{w = \{w_1 S_{F_1}, w_2 S_{F_2}, \ldots, w_k S_{F_k}\}, S_{F_k} = -1, 0, 1\}$. For example, for $w = 6$, from (11), the cardinal of W is Card (W) = 31104. Then, the power balancing problem can be stated as:

$$\min_{w \in W} \max_{i=1,\ldots,N} \epsilon_i \qquad (16)$$

To solve the previous optimization problem, the following algorithm can be used:

- Compute the power of all inverter stages, i.e., obtain P_k for the N stages using (12).
- For each sequence $w \in W$ evaluate $\varepsilon_1, \varepsilon_2 \ldots \varepsilon_N$ and retain $\varepsilon_{w,max}$.
- The optimal solution is obtained by:

$$\underset{w \in W}{\text{Min}} \; \varepsilon_{w,max} \qquad (17)$$

A MATLAB- based algorithm has been implemented to solve this off-line optimization problem. Possible switching patterns from Table 2 were organized in consecutive order in such a way that the first possibility to obtain each of the 15-th values defines the tested combination. All resulting $\varepsilon_{w,max}$ are shown in Figure 10, where it is possible to identify the minimum error which is near 2.6%, which corresponds to the power distribution 25.61%:25.24%:24.70%:24.45% in
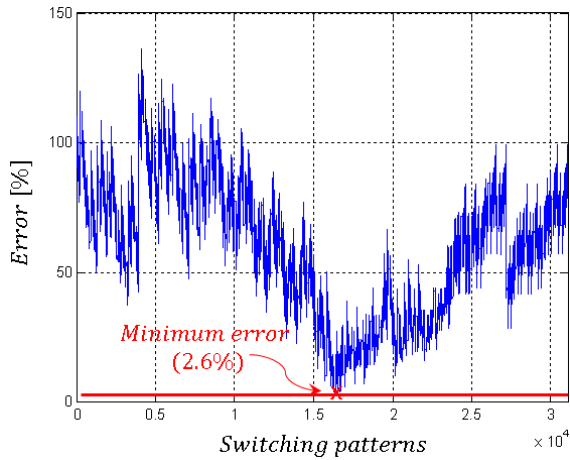
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FIGURE 10. Computed error for the possible 31.104 switching patterns.

FIGURE 11. Output signals of the inverter stages for the optimum switching pattern producing 31-levels signal.

the inverter. The resulting optimized switching function S_{F_k} is detailed in table 3 and the waveforms at the output of the inverter stages are shown in Figure 11.

TABLE 3. Optimized switching function for 31-levels signal.

Positive level	Interval (ms)	Stage 1 ($w_1 = 6$)	Stage 2 ($w_2 = 7$)	Stage 3 ($w_3 = 8$)	Stage 4 ($w_4 = 9$)
0	0.088436	-1	1	1	-1
1	0.17727	-1	1	0	0
2	0.17847	-1	1	-1	1
3	0.18052	-1	0	0	1
4	0.18353	1	1	0	-1
5	0.18762	1	0	1	-1
6	0.19301	1	0	0	0
7	0.20003	0	1	0	0
8	0.20917	0	1	-1	1
9	0.22122	-1	1	1	0
10	0.23752	-1	1	0	1
11	0.26058	-1	0	1	1
12	0.29570	1	1	1	-1
13	0.35719	1	1	0	0
14	0.50958	1	0	1	0
15	0.68681	1	0	0	1

As was mentioned before, the proposed ratio 6:7:8:9 allows to obtain a 31-level signal like the asymmetric binary ratio 1:2:4:8. It can be observed an advantageous balancing in power distribution. Some additional comparison elements are discussed below:

- Although more sophisticated optimization methods can be applied, the proposed method is simple and reliable for the proposed off-line application.
- The number of commutations in the case of ratio 1:2:4:8 is lower than in the proposed case.
- The switching pattern for the proposed ratio implies some bipolar commutations, this not being the case in the binary ratio.
- Using the proposed ratio, the system has the capability to operate with three or two sources and PWM control which is impossible in the case of the binary ratio.
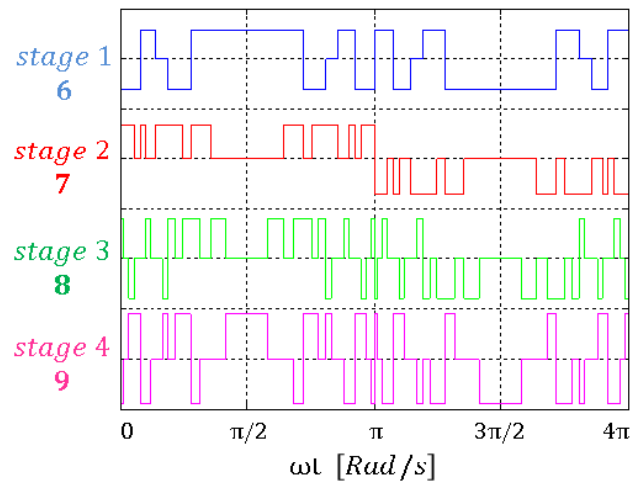
- The amplitude of the output signals in the proposed case is similar which unifies the size of the inverter stages (transformers and semiconductor devices).
- The power distribution is optimal in the proposed case and deficient in the case of the binary relation.
- The size of the required transformers slightly increases with the proposed relation.

C. CLOSED LOOP CONTROL PROPOSAL

A hysteresis control based approach is presented to obtain closed-loop regulation of the output voltage. The idea is to enforce the RMS value of the output voltage to be constrained into an acceptable range around the nominal value of 110 V (amplitude of around 155 V) by using the optimum switching patterns corresponding to produce between 27 and 35 levels. As expected the higher the number of levels the higher the quality of the output signal. Although the power distribution is optimized for the five possible signals, the best balance corresponds to the nominal case of 31-levels. Taking measurement of the output voltage, it is determined if the voltage increases or decreases outside the hysteresis band enforcing the change of the switching pattern as it is depicted in Figure 12.

For example, consider our inverter as example operating at nominal conditions providing 110 V reproducing a 31-level amplitude of 155 V approximately. If the output voltage decreases below the inferior limit of the hysteresis band (Nominal – 5%), the control changes the switching pattern to provide a 33-levels signal obtaining an output voltage near to 111 V. If the output voltage continues decreasing and again falls below the limit of the hysteresis, the switching pattern is changed to provide 35-levels obtaining an output voltage amplitude around 111 V also. The same principle is applied when output voltage increases. This kind of control provides a wide range of operation. It is worth to note that, by applying
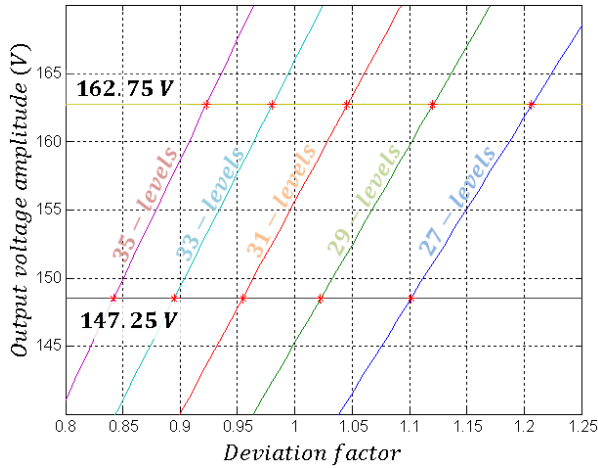
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FIGURE 12. Representation of the proposed hysteresis control dynamic considering a voltage deviation factor.
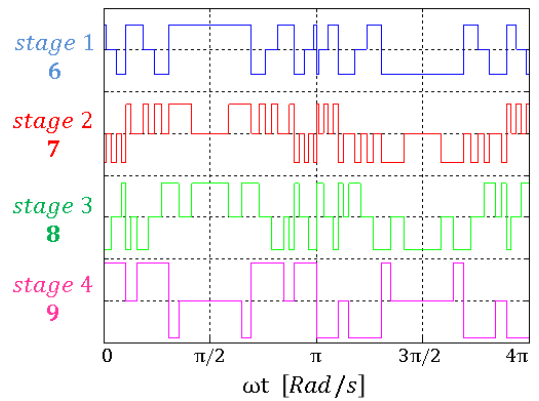

FIGURE 13. Output signals of the inverter stages for the optimum switching pattern generating 29-levels signal.

TABLE 5. Optimized switching function for 33-level signal.

Positive level	Interval (ms)	Stage 1 ($w_1 = 6$)	Stage 2 ($w_2 = 7$)	Stage 3 ($w_3 = 8$)	Stage 4 ($w_4 = 9$)
0	0.08291	1	-1	-1	1
1	0.16614	0	0	-1	1
2	0.16713	-1	1	-1	1
3	0.16881	-1	0	0	1
4	0.17126	1	1	0	-1
5	0.17457	1	0	1	-1
6	0.17889	1	0	0	0
7	0.18443	1	0	-1	1
8	0.19152	1	-1	0	1
9	0.20063	0	0	0	1
10	0.21254	0	-1	1	1
11	0.22856	-1	0	1	1
12	0.25110	1	1	1	-1
13	0.28533	1	1	0	0
14	0.34509	1	0	1	0
15	0.49289	0	1	1	0
16	0.66488	0	1	0	1

this method no modulation is considered as a part of the control.

Table 4 presents the optimized switching patterns for balanced power distribution when the inverter operates generating an output signal of 29-level. Waveforms of different stages are depicted in Figure 13. The power balance for this switching pattern is 25.72%:26.90%:27.09%:20.29%.

TABLE 4. Optimized switching function for 29-levels signal.

Positive level	Interval (ms)	Stage 1 ($w_1 = 6$)	Stage 2 ($w_2 = 7$)	Stage 3 ($w_3 = 8$)	Stage 4 ($w_4 = 9$)
0	0.09475	1	-1	-1	1
1	0.19000	0	0	-1	1
2	0.19148	0	-1	0	1
3	0.19403	-1	0	0	1
4	0.19777	-1	-1	1	1
5	0.20292	1	1	-1	0
6	0.20980	1	0	0	0
7	0.21891	1	0	-1	1
8	0.23106	0	1	-1	1
9	0.24763	0	0	0	1
10	0.27122	-1	1	0	1
11	0.30730	-1	0	1	1
12	0.37067	1	1	1	-1
13	0.52808	1	1	0	0
14	0.71106	1	0	1	0

Table 5 presents the optimized switching patterns for balanced power distribution when inverter operated generating an output signal of 33-level. Waveforms of different stages are depicted in Figure 14. Power balance for this switching pattern is 15.37%:28.84%:28.41%:27.38%.
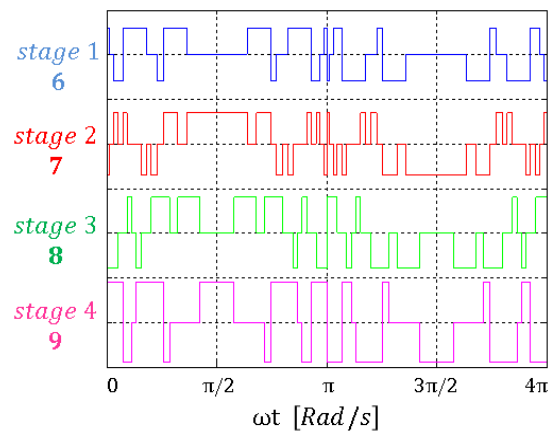

FIGURE 14. Output signals of the inverter stages for the optimum switching pattern generating 33-levels signal.

IV. EXPERIMENTAL RESULTS

A. MULTILEVEL INVERTER PROTOTYPE AND EXPERIMENTAL SETUP

To validate the proposed method, a 240 VA laboratory prototype was built. The nominal input voltage is 40 VDC and the nominal output voltage is 110 V for a frequency of 60 Hz.

The experimental set-up is composed of a programmable power source BK PRECISION XLN6024, a programmable AC load SORENSEN Ametek SLM 300V/4A, an oscilloscope Tektronix TBS1104 with isolated differential voltage probes ADF25, and a Fluke 43B Power Quality Analyzer.
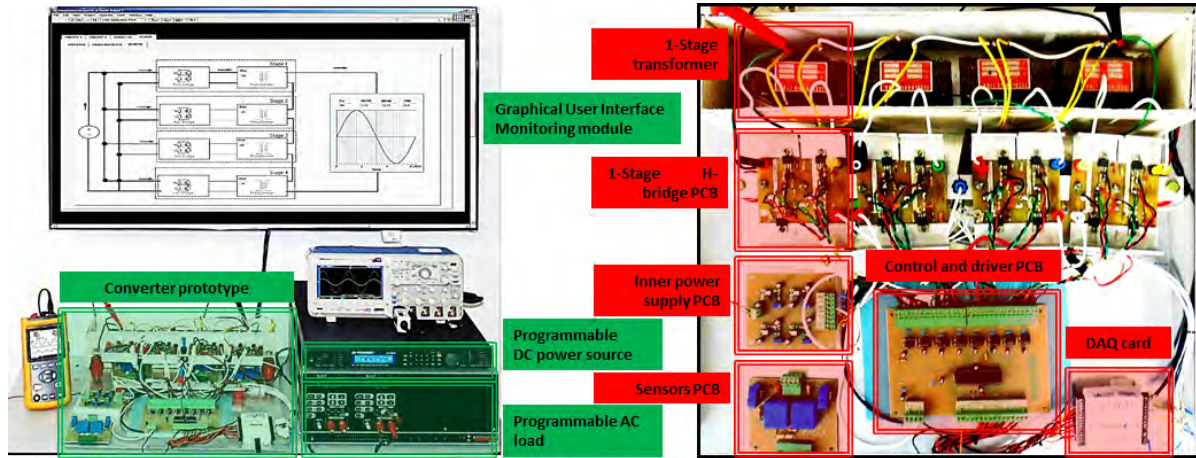
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FIGURE 15. Experimental set-up, inverter prototype and software interface.

The software RT-MLI developed in LabVIEW interacts with the inverter by charging switching patterns using parallel communication, generating analog references for programmable instruments and measuring inverter variables through a DAQ card USB-6002 [22].

The four inverter stages have been implemented using MOSFET IRFZ44 with IRS2004PBF integrated driver circuits. The control was integrated in a PIC16F877A where the switching pattern is stored in the EPROM memory and reproduced in loop using the intervals defined by expression (3) for a 60-Hz frequency (see also Table 2). Figure 15 shows a picture of the prototype and the experimental set-up.

The design parameters for the inverter are $V_{max} = 156V$, $N = 4$, $M = 15$, $S = 250$ VA and $V_{dc} = 40$ V. Transformer turns ratios were obtained by formula (8) as:

$$TR_1 = \frac{w_k V_{max}}{MV_{dc}} = \frac{6(156)}{15(40)} = 1.56$$
$$\implies V_{p1} = 28Vrms \implies V_{s1} = 43.68Vrms$$

$$TR_2 = \frac{w_k V_{max}}{MV_{dc}} = \frac{7(156)}{15(40)} = 1.82$$
$$\implies V_{p1} = 28Vrms \implies V_{s1} = 50.96 \ Vrms$$

$$TR_3 = \frac{w_k V_{max}}{MV_{dc}} = \frac{8(156)}{15(40)} = 2.08$$
$$\implies V_{p1} = 28Vrms \implies V_{s1} = 58.24Vrms$$

$$TR_4 = \frac{w_k V_{max}}{MV_{dc}} = \frac{9(156)}{15(40)} = 2.34$$
$$\implies V_{p1} = 28Vrms \implies V_{s1} = 65.52 \ Vrms$$

B. CONVERTER WAVEFORMS AND OUTPUT VOLTAGE QUALITY

Figure 16 shows the oscilloscope captures of the inverter output voltage feeding an output load of 100 W. It is possible to distinguish the steps in the voltage signal. Also, the output voltage signals of the four stages of the inverter are depicted, showing that implementation is in good agreement with the theoretical assumptions. The RMS value of the output voltage
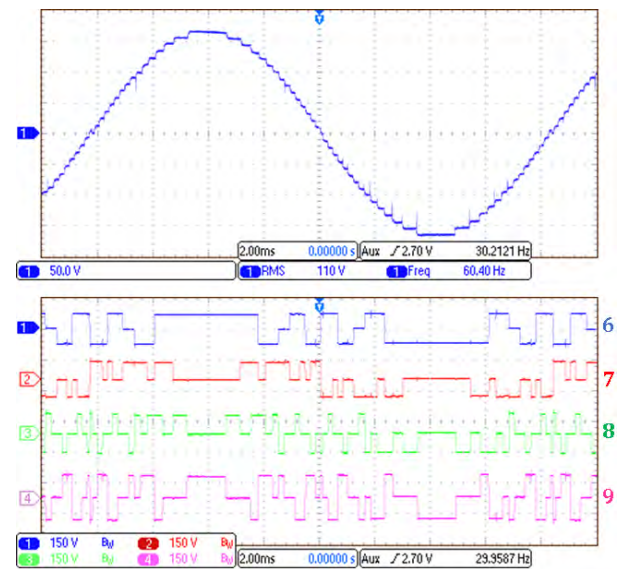

FIGURE 16. Oscilloscope captures: a) output voltage; b) Stage output voltages (The channel number corresponds to the stage number and corresponds to the same organization in simulated signals).

is enforced to 110 V by changing the DC input voltage in the experiment. The measured THD of the output voltage is 1.2% in this case. The same measurements were made for the inverter operating producing the output voltage with the optimized switching pattern for 27, 29, 33 and 35 levels. The corresponding oscilloscope captures are included in Appendix I.

C. BALANCED POWER DISTRIBUTION AND POWER QUALITY MEASUREMENTS FOR RESISTIVE LOAD

To assess the accuracy of the power balancing approach, several tests were realized using resistive loads covering the overall operation range of the inverter. Results for four the tests are shown in Figs.17 and 18 referring to 28, 131, 198 and 250 W resistive loads. In Figure 17, captures of the
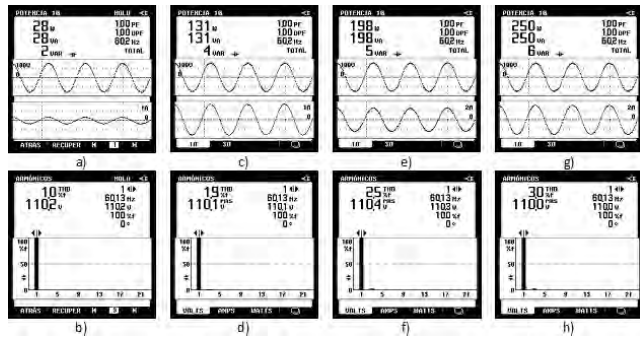
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FIGURE 17. Voltage quality measurements for resistive loads. 430 Ω: a) output power b) THD; 90 Ω: c) output power d) output voltage THD; 61 Ω: e) output power f) THD; 48 Ω: g) output power h) THD.

Power Quality Analyzer FLUKE 43B for power and THD measurement for each load are shown. As it can be noted, the THD increases with the amount of power demanded by the load and shows values between 1.0% and 3.0%. Power factor and displacement power factor are unitary as expected. In Figure 18, measurements of the output voltages of the four stages are organized in a column for each one of the four power levels selected for the test.
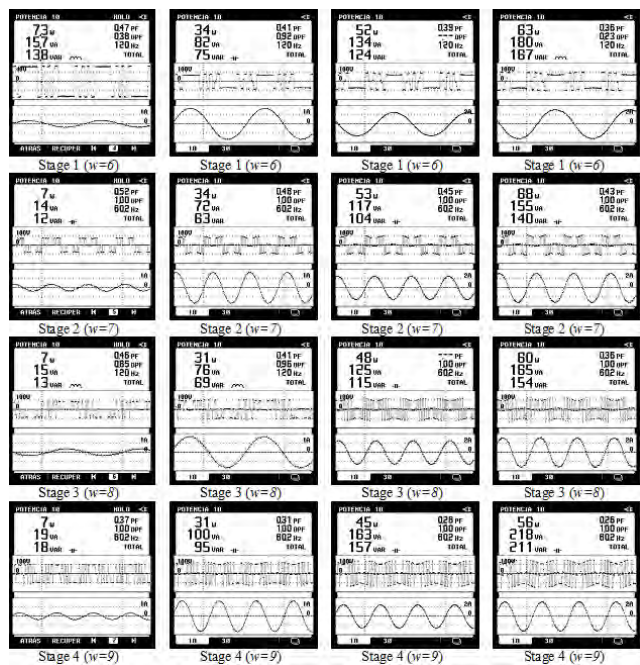

FIGURE 18. Power equalization measurements for resistive loads: a) 430 Ω resistive load (28.3 W); b) 90 Ω resistive load (130 W): c) 61 Ω resistive load (198 W): d) 48 Ω resistive load (247 W).

The maximum power deviation for the load of 28 W is about 4.3%, which appears in the first inverter stage (w=6). For the load of 131 W, a maximum deviation of about 3.5% appears in all stages. For the load of 198 W, a maximum deviation of 7.0% appears in the second inverter stage (w=7). Finally, for a power of 250 W, the maximum deviation is about 10.0% and it is present in the fourth stage of the

inverter (w=9). For all cases, the maximum deviation present in one inverter stage is compensated with lower deviations in the other inverter stages.

The analysis of the results about uniform power balance reveals that the maximum deviation increases with the amount of power demanded by the load, and is related to the differences appearing in the input currents of the converter stages resulting in voltage drops in parasitic resistances.

D. POWER EQUALIZATION AND POWER QUALITY MEASUREMENTS FOR REACTIVE LOADS

To test the immunity of the proposed method to the presence of reactive power, an inductive-resistive load of 237 VA (PF = 0.93) was connected to the inverter. As it can be observed in Figure 19, a maximum power deviation of 8.1% is obtained in the first and fourth stages (w=6 and w=9, respectively).
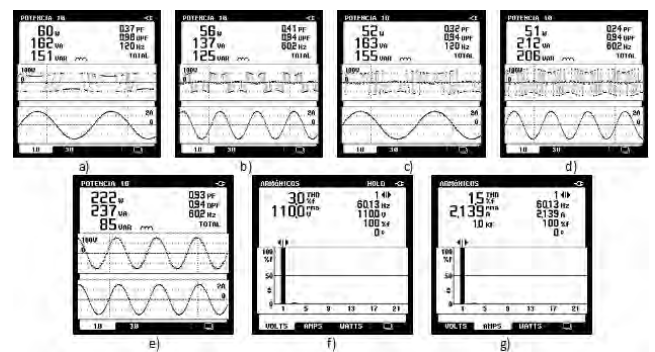

FIGURE 19. Experimental results for a RL load (R= 430Ω, L= 200 mH). Voltage and power per stage: a) w= 6, b) w= 7, c) w= 8, d) w= 9; e) output voltage and power; THD: f) output voltage; g) output current.

Finally, a resistive-capacitive load of 68 VA (PF = 0.73) was connected to the inverter. As it can be observed in Figure 20, a maximum power deviation of 9.8% is obtained in the first stage (w=6). In this case, power deviation increased in comparison with a similar amount of power in a resistive load. Nonetheless, the THD in the output voltage is considerably low (0.9%).
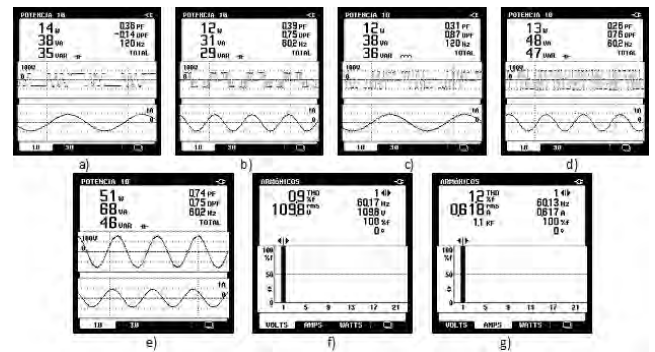

FIGURE 20. Experimental results for a RC load (R= 430Ω, C= 24μF). Voltage and power per stage: a) w= 6, b) w= 7, c) w= 8, d) w= 9; e) output voltage and power; THD: f) output voltage; g) output current.

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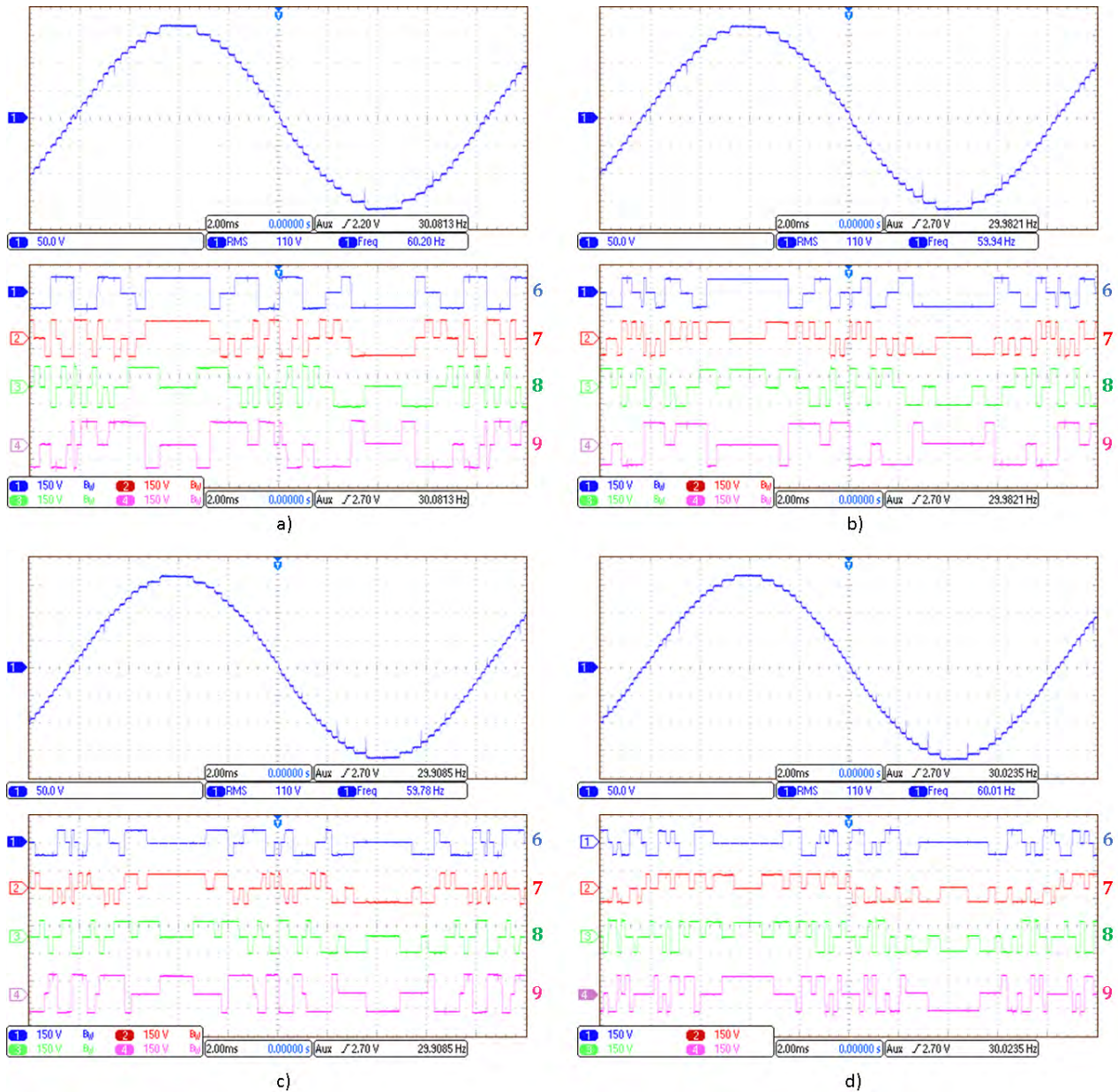
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FIGURE 21. Oscilloscope captures of output signal of the inverter and the inverter stages: a) 27-levels; b) 29-levels; c) 33-levels; and d) 35-levels.

V. CONCLUSION

This paper has presented a method to enforce balanced power distribution on a transformer-based cascaded asymmetrical multilevel inverter. The method is founded on the selection of an optimal switching pattern for each stage of the inverter given by an off-line algorithm. The proposal has been developed using a 31-level output voltage signal obtained from a four- stage common DC source inverter after selecting the best combination of integer weights for the stages of the inverter. The output power and harmonic distortion measurements in a 240 VA prototype have shown THD below 3% and a balanced distribution deviation lower than 10%. This appropriate behavior of the system has been verified for resistive, resistive-inductive and resistive-capacitive loads and improves what has been reported as yet in the technical literature.

It has been demonstrated that the proposed asymmetric ratio 6:7:8:9 allows that the inverter can be controlled using optimized switching patterns for a subsequent number of levels (27, 29, 31, 33 and 35). The patterns can be stored in a digital device to easily support a voltage regulation control loop improving the inverter performance while avoiding the use of high-frequency modulation. Current research and future work are oriented to this goal together with the integration of fault-tolerant properties in one of the inverter stages.
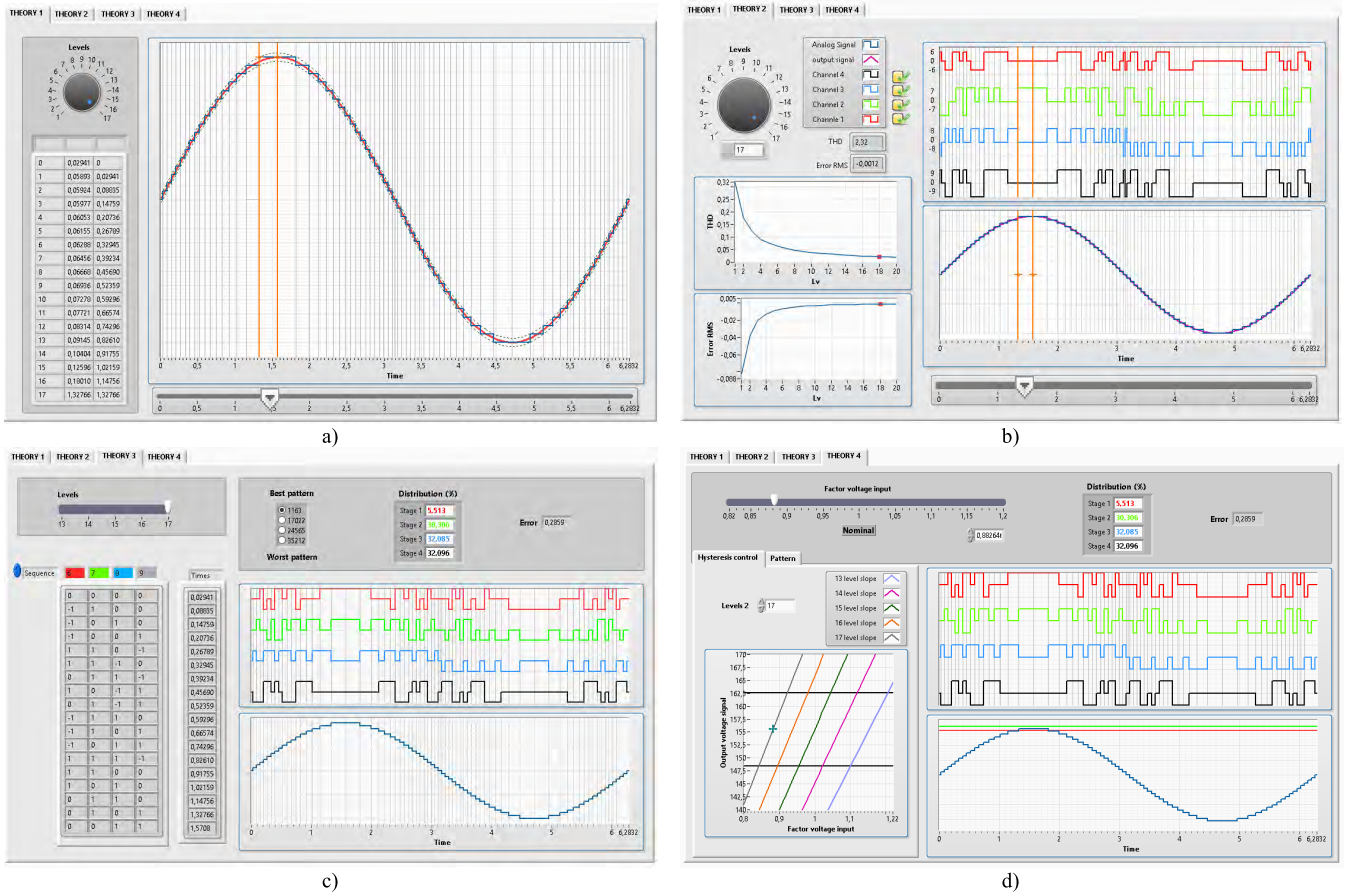
FIGURE 22. Graphical user interfaces of the simulated version of RT-MLI software: a) Frame theory 1; b) Frame theory 2; c) Frame theory 3; and d) Frame theory 4.

APPENDIX 1
OUTPUT SIGNALS FOR BALANCED POWER DISTRIBUTION (27, 29, 33 AND 35 LEVELS)

This appendix shows experimental results for inverter operating with optimized switching patterns for 27, 29, 33 and 35 levels output signal. The RMS value of the output was settled to 110 V by modifying the DC input voltage when inverter fed a 100 W load. The maximum THD measured was 2% while the minimum was of 1%. Power distribution for 27-levels was measured as 29%:23%:26%:22% (Theoretical → 27.13%:23.19%:26.60%:23.08%); 27%: 28%:26%:19% for 29-levels (Theoretical → 25.72%: 26.90%:27.09%:20.29%); 15%:29%:29%:27% for 33-levels (Theoretical → 15.37%:28.84%:28.41%:27.38%). and, 3%:34%:32%:31% for 35-levels (Theoretical → 5.51%: 30.31%:32.08%:32.10%). It is worth to highlight that this results are in good agreement with the theoretical ones showing only slight deviations which can be attributed to voltage drops in parasitic elements. Oscilloscope captures for inverter operating with an output signal of 27, 29, 33 and 35 levels are depicted in Figure 21.

APPENDIX 2
SPECIALIZED SETUP FOR TESTING THE MULTILEVEL INVERTER PROTOTYPE

To detail the explanations given along the paper and provide an interactive tool to understand the majority of the applied concepts, we have developed a laboratory testing tool for the control of the inverter prototype. Some details of the platform can be found in [22]. A reduced version of the software component has been developed to share it as a part of this paper facilitating the use of its contributions. The link below give access to the installer of the LabVIEW application. The simulation version of RT-MLI whose graphical interface is depicted in Figure 22 has been organized in four theoretical frames providing the following functions:

Theory 1: This frame allows building of the multilevel sine signal using the principle presented in section II by configuring a desired number of levels. A slide control provides a visual tracking of the different segments of the signal. The main objective of this frame is to facilitate the understanding of the signal generation process with some interactivity for users (Figure 22a).

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Theory 2: This frame provides the user with a complete overview of the waveforms of the inverter which are synchronously visualized with the output of the inverter as the sum of these signals. Furthermore, the user can activate or deactivate stages regarding fault scenarios. Additionally, this section evaluates the THD and the RMS of the output signal as a function of the number of stages (1-6) and the number of levels (1-17) providing elements to easily understand the selected number of stages and levels (Figure 22b).

Theory 3: This frame allows the user to visualize the waveforms for each stage, as well as the sum of these signals, and the computation of power distribution between stages and the error. The user can change the number of levels between 13 and 17 levels. Also, the user have the possibility to choose between a set of switching patterns including the best ones and the worst ones showing power balance as quality indicator (Figure 22c).

Theory 4: In this frame, the hysteresis-based closed-loop approach is illustrated showing the operation point of the converter as a function of deviation factor (deviation from nominal operation point). The inverter can work producing between 13 and 17 levels changing from a switching pattern to other depending of the measurement of the output voltage amplitude with respect to the defined hysteresis band (Figure 22d).

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