Capacitor-Less Low-Dropout (LDO) Regulator with 99.99% Current Efficiency using Active Feedforward and Reverse Nested Miller Compensations

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ABSTRACT In this paper, an output capacitor-less low-dropout (LDO) regulator with 99.99% current efficiency using active feedforward compensation (AFFC) and reverse nested Miller compensation (RNMC) is implemented. To increase the current efficiency, low quiescent current less than 10 μA is used. The stability problem arising from the low bias current is overcome by applying two kinds of compensation methods. By drawing the pole-zero plot using the open-loop transfer function obtained by the small-signal modeling, the stability of the proposed LDO is guaranteed to be less than 70 mA. By using the proposed compensation methods, two zeros of the right-half plane (RHP) can be placed in the left-half plane (LHP) to prevent lagging and reduce the on-chip compensation capacitor. The current efficiency of the proposed LDO is 99.99% at the load current of 70 mA.

INDEX TERMS Low-dropout regulator (LDO), current efficiency, low quiescent current, nested Miller compensation (NMC), reverse nested Miller compensation (RNMC), active feedforward compensation (AFFC).

I. INTRODUCTION

The low-dropout (LDO) regulator is an important part of power management integrated chips (PMIC) such as portable devices. The power efficiency of the LDO is a critical factor in prolonging the battery cycle life. Figure 1 illustrates the main role of LDOs. The rechargeable battery changes the output voltage depending on the capacity change, which depends on the charge and discharge condition [1]. The DC–DC converter lowers or boosts the voltage supplied by the battery to the voltage level required by the application. Then, LDOs provide the unstable voltage supplied from the DC–DC converter to provide a stable supply voltage with little ripple and noise to the sub-blocks on the backside. They also supply constant voltage regardless of changing load current. Since power consumption is a very important factor in portable devices using batteries, it is necessary to reduce the power consumed

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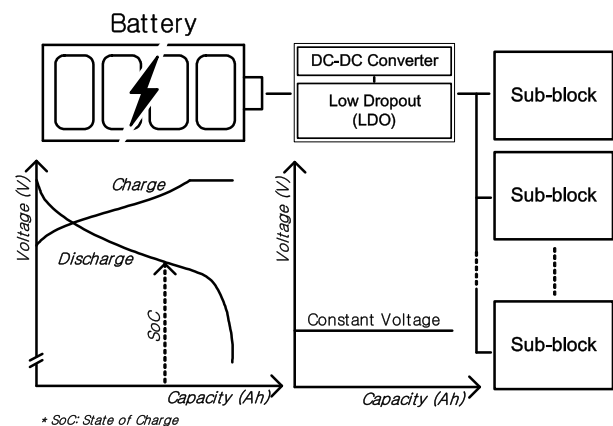

FIGURE 1. Block diagram of LDO delivering voltage from battery to sub-block [2].

by the PMIC part and increase its efficiency. Recent system on chip (SoC) designers have begun to worry about the size of LDOs, as the number of sub-blocks requiring various voltages

and the number of LDOs have increased. Conventional LDOs have a large capacitor in load to ensure loop gain stability. However, it is not easy to on-chip. Therefore, a capacitor-less LDO that can guarantee stability by various compensation techniques without an external capacitor was introduced and highlighted by an on-chip application. Capacitor-less LDOs reduce external components and allow cost-effective systems to be designed. The larger the feedback resistance in Figure 2 (a), the easier it is to improve the current efficiency. However, simply designing a large feedback resistor causes stability problems in an LDO circuit with a feedback path.

In previous studies, various configurations have been conducted in LDO design. Designing an LDO in a two-stage structure makes it easy to compensate for stability, but it does lead to problems associated with insufficient loop gain [3]. The impedance attenuation technique is used to dissipate the low quiescent current and perform current buffer compensation [4]. Some studies have shown that LDOs can be made to consume only 103 nA by reducing the quiescent current [5]. Usually, many dynamic structures are used to reduce the quiescent current and increase efficiency. There is a way to reduce the current consumption by turning on the pass transistor (PT) according to the amount of load current [6]. However, the quiescent current also increases very rapidly when the load current is large. Another study designed with a low quiescent current structure had a very large overshoot and undershoot, making it difficult to use in many applications [7]. In recent state-of-the-art research, most studies are designed to pursue fast settling time [13], [24]–[26] or high PSR [14]–[16]. Regulators designed for a low quiescent current and high current efficiency are mostly digital LDOs [17]–[20]. As such, it is challenging to design LDOs with low quiescent currents that have enough gain with a multistage structure, are not subject to load current magnitude from minimum to maximum and satisfy stability requirements.

In the following parts of the introduction, the difference between the conventional LDO and the capacitor-less LDO is explained in Section A, the compensation methods are introduced in Section B, and the proposed LDO is described in Section C. The transfer function of the LDO proposed in Section II is used to analyze the poles and zeros. Section III presents detailed circuit implementations of the proposed LDO. Section IV describes the measurement results for the proposed LDO transient response and quiescent current in Sections A and B, respectively. Finally, the conclusion is given in Section V.

A. CAPACITOR-LESS LDO

The block diagram of a conventional LDO is shown in Figure 2(a). The LDO consists of an error amplifier (EA), a PT, a feedback network (R_{FB1} and R_{FB2}), and a large off-chip capacitor (C_L). The load current, I_L, is the amount of current required by the load. Conventional off-chip capacitors were used to help LDOs ensure a good transient response
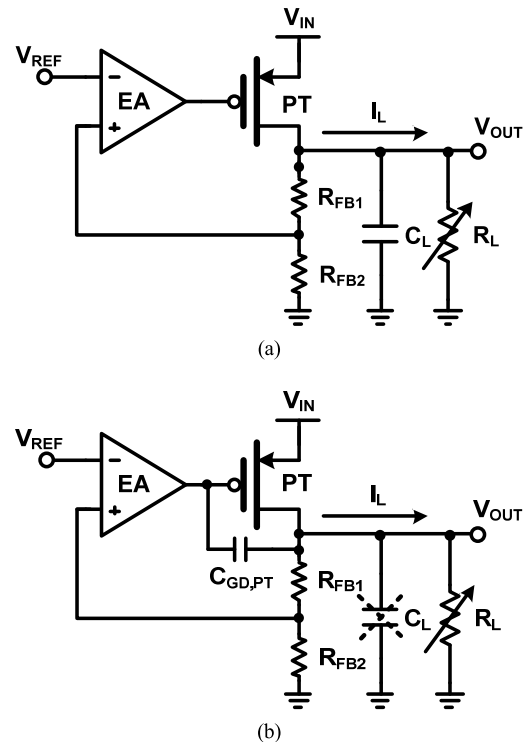

(a)

(b)

FIGURE 2. Block diagram of (a) conventional LDO and (b) capacitor-less LDO.

and stability. Since the capacitor composed largely of the load forms a dominant pole in the closed-loop response, the stability is not greatly affected even if the pole is formed by the PT's parasitic capacitor.

The load capacitor of a conventional LDO has a size of several microfarads, which is not easy to create on-chip, so another solution has been proposed. As shown in Figure 2(b), an LDO with the capacitor removed at the load is proposed. The parasitic capacitors in the LDO circuit play their roles because they removed the capacitors that served them. The size of the capacitor is a few picofarads, which is very large.

The signals V_{IN}, V_{OUT}, and V_{REF} refer to input, output, and reference voltages, respectively. The output of the LDO is determined by the ratio of the resistance of the feedback network and the value of V_{REF} to the input of the EA. The EA amplifies the difference by comparing the reference voltage V_{REF} with the incoming feedback voltage. The output of the EA goes directly into the input of the PT, and the output current to the PT is determined by the DC level. The PT composed of a P-type MOSFET must be designed much larger than the other transistors, because it must contain the amount of current required in the next stage sub-block or more. Since the PT is a common source amplifier, the LDO can be interpreted as a multistage amplifier. The issue of the capacitor-less LDO is that the circuit must have sufficient stability and meets dropout voltage requirements. As well,

TABLE 1. Poles and zeros of NMC and RNMC.

Symbol	NMC	RNMC
gain(A)	$g_{m1} g_{m2} g_{m3} R_1 R_2 R_3$	
ω_{GBW}	g_{m1}/C_{m1}	
ω_{-3dB}	$1/C_{m1} R_1 g_{m2} g_{m3} R_2 R_3$	
ω_p	$\sqrt{g_{m2} g_{m3}/C_{m2} C_3}$	
ω_{z1}	g_{m3}/C_{m2}	
ω_{z2}	g_{m2}/C_{m1}	
Q-factor	$\dfrac{1}{g_{m3} - g_{m2}}\sqrt{\dfrac{C_3 g_{m2} g_{m3}}{C_{m2}}}$	$\dfrac{C_{m1}}{g_{m2}(C_{m1} + C_3) - C_{m1} g_{m3}}\sqrt{\dfrac{C_3 g_{m2} g_{m3}}{C_{m2}}}$

it should increase the current efficiency by reducing the quiescent current. At heavy-load currents, the use of large PTs seems to achieve high efficiency with low dropout voltage, but as the PT size increases, the parasitic capacitor that is present in the transistor reduces the phase margin significantly. When a quiescent current is low, the output resistance of the LDO becomes large, which causes the pole at the output to pull forward to the unit gain bandwidth (UGBW), resulting in a poor phase margin and instability. To compensate for the stability, the capacitance of the compensation capacitor must be large, which results in a large size of LDO.

B. LDO COMPENSATION METHODS

An amplifier consisting of more than two stages is called a multistage amplifier, and while it can have a high gain, the signal is likely to oscillate due to the degradation of the phase margin. Frequency compensation is indispensable to eliminate the possibility of an unstable circuit, and various topologies have been studied, as shown in Figure 3.

The first is nested Miller compensation (NMC), a well-known compensation method for multistage amplifiers. As shown in Figure 3(a), the NMC provides compensation by connecting two capacitors to each other. In the three-stage amplifier, the first output node is connected to the last node through a capacitor, and the other is connected to the output of the last stage from the second stage output. The second is reverse nested Miller compensation (RNMC) introduced in Figure 3(b). The difference from the NMC structure is that there is no problem with stability even with a relatively low g_{m3} value, because the inner compensation capacitor C_{m2} is not shared with the load portion. Finally, the active feedforward compensation (AFFC) structure is shown in Figure 3(c). This structure supplies g_{mff} to the last stage output through the first stage output value. Circuits share the diode connection of the first stage to draw current. The AFFC can obtain two different real zeros. Unlike NMC or RNMC with two zeros in the right-half plane (RHP), the AFFC can bring one zero to the left-half plane (LHP). In addition, the phase margin of the circuit is reduced, because the zero of the RHP is at a frequency lower than that of the LHP.

As shown in Table 1, where the gain, UGBW, pole and zero frequency, and Q values are calculated by obtaining
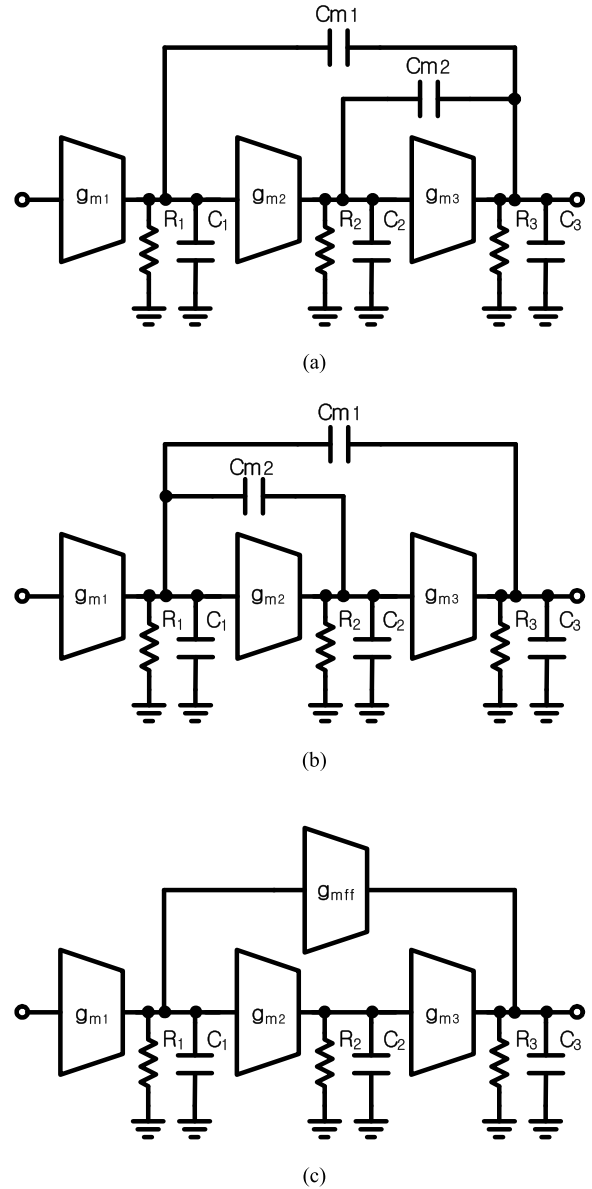

(a)

(b)

(c)

FIGURE 3. Block diagram of compensation methods, (a) NMC [8]–[10], (b) RNMC [11], [12], and (c) AFFC.

the transfer functions of the NMC and RNMC structures, the compensation capacitors C_{m1} and C_{m2} cannot be designed to be small in this structure. The NMC structure shows that the stability condition occurs when the complex pole term of the transfer function, the second complex pole, and the Q value are considered. The gain peaking should be prevented by increasing the C_{m2} value and lowering the Q value. However, since the second pole moves to the lower frequency and a stability issue occurs, the value C_{m1} should be increased to lower the UGBW frequency as well. For this reason, both C_{m1} and C_{m2} are designed to be large in the NMC structure so that a Q value and a phase margin can be secured.

The RNMC structure is suitable for higher load capacitors because C_{m2}, the inner compensation capacitor, is not loaded
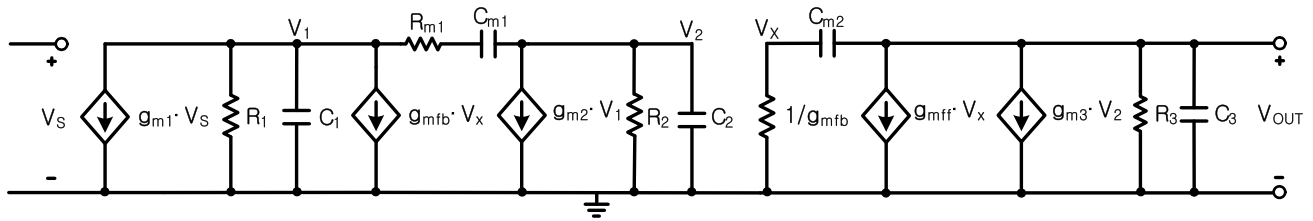
FIGURE 4. Small signal model of the proposed AFF-RNMC LDO.

on the output. According to the transfer function, the real part of the complex term of the denominator is larger than the NMC, so C_{m2} can be designed smaller. The second complex pole then exists at a higher frequency than the NMC structure. This makes it possible to design the UGBW more broadly. Since UGBW is inversely proportional to C_{m1}, it can be designed smaller than NMC structure. The RNMC structure is also suitable for designing with low power targets. This is because the g_{m2} and g_{m3} cannot be designed large according to the stability condition. When the ratio of g_{m2} to g_{m3} becomes larger than the ratio of C_{m2} to C_3, the circuit oscillates. Because the first term of the complex term changes to minus, it becomes an unstable circuit by placing the pole in the RHP. The AFFC structure can shift zero to a lower frequency by adjusting g_{mff}, the transconductance of the feedforward path. This structure improves the phase margin and allows a wider UGBW.

Depending on the load condition, the transconductance of PT, g_{m3}, varies greatly from a few hundred μS to several tens of mS. In the NMC and RNMC structures, the first zero is shifted to a higher frequency according to the increments of g_{m3}.

C. PROPOSED LDO DESIGN
In this paper, we propose a multistage LDO using an AFFC and RNMC structure (AFF-RNMC). By using the AFFC and RNMC structure together, the characteristics are changed, and the influence of the poles and zeros are reduced even when the load condition changes. According to the transfer function of the proposed AFF-RNMC LDO, the second non-dominant complex poles are all formed as a positive term so that the pole is always located in the LHP. Thus, unlike using the RNMC structure alone, there is no limit to the stability issues of g_{m2} and g_{m3} in LDO design. It is possible to maintain a stable state even if g_{m3} varies greatly according to the load condition. It is also suitable for low quiescent current targets. The proposed LDO may take the g_{m3} higher since there is no stability condition by the transconductance. So, it is suitable for high load current scheme. The proposed AFF-RNMC LDO has a large real term, which can reduce the size of Cm2 more than NMC or RNMC, thus reducing the total size of LDO.

II. ANALYSIS OF PROPOSED LDO
Figure 4 shows the small signal model of the proposed LDO. V_S represents the reference voltage of the LDO, V_1 and V_2

TABLE 2. Poles and zeros of NMC, RNMC, and AFFC-RNMC.

	NMC/RNMC	AFFC-RNMC
gain(A)	$g_{m1}g_{m2}g_{m3}R_1R_2R_3$	
ω_{GBW}	g_{m1}/C_{m1}	
ω_{-3dB}	$1/C_{m1}R_1g_{m2}g_{m3}R_2R_3$	$1/(C_{m1}g_{m2}g_{m3}R_1R_2R_3)$
ω_p	$\sqrt{g_{m2}g_{m3}/C_{m2}C_3}$	$\sqrt{C_{m2}g_{m2}g_{m3}/C_1C_2C_3}$
ω_{z1}	g_{m3}/C_{m2}	g_{m2}/C_{m1}
ω_{z2}	g_{m2}/C_{m1}	g_{mfb}/C_{m2}

refer to the output of first and second stage, V_X is defined as the opposite polarity of V_1, and V_{OUT} is the output of the proposed LDO. The transconductance, output impedance, and output capacitors expressed in each stage by the three-stage amplifier structure are denoted as $g_{m1,2,3}$, $R_{1,2,3}$, and $C_{1,2,3}$, respectively. The transconductance of the AFFC path is expressed as g_{mff}, and the transconductance of the active feedback path is defined as g_{mfb}. The two capacitors and one resistor implemented for compensation in the RNMC structure are represented by $C_{m1,2}$ and R_{m1}. Unlike NMC and RNMC, the proposed architecture prevents the flow of current at high frequency by adding a resistor R_{m1} to the active feedback path and the inner compensation path.

The RHP zero generated by C_{m1} in the second stage of proposed LDO, since the importance of the current supplied to the output becomes $1/sC_{m1}$ greater than g_{m2} and the current phase is opposite. To solve this problem, resistor R_{m1} can be added to reduce the pole splitting effect by maintaining a certain degree of impedance with a fixed real resistance at high frequency.

Figure 5 shows a block diagram of the proposed LDO. The transfer function of the proposed LDO can be derived as follows:

$$T(s) = \frac{-A_{DC}(1 + s/\omega_z)}{(1 + s/\omega_{-3dB})(1 + s/Q\omega_p + s^2/\omega_p^2)}, \quad (1)$$

where $A_{DC} = g_{m1}g_{m2}g_{m3}R_1R_2R_3$ stands for DC gain and $\omega_{-3dB} = 1/(C_{m1}g_{m2}g_{m3}R_1R_2R_3)$ denotes the 3-dB dominant pole. Two approximations were applied to simplify the expression. First, the product of transconductance and output impedance at each stage is much greater than 1. Second, as in (3) below, the two capacitors $C_{m1,2}$ used in compensation and the capacitor C_3 in the final output are much larger than the first and second stage output capacitors. The two
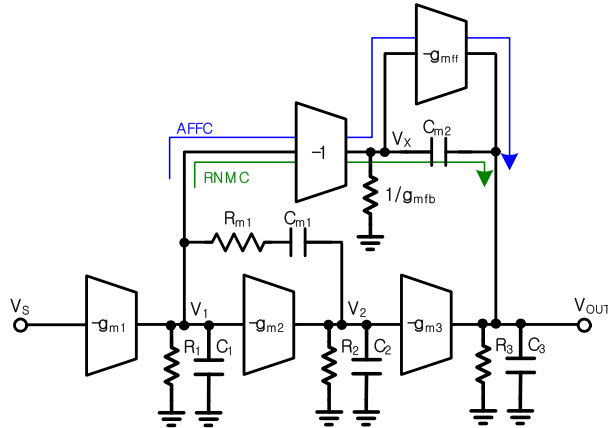
FIGURE 5. Block diagram of proposed LDO.

assumptions are as follows:

$$g_{mi}R_i \gg 1 (i = 1, 2, 3), \qquad (2)$$

$$C_{m1}, C_{m2}, C_3 \gg C_1, C_2. \qquad (3)$$

The transfer function gives the dominant pole and the two complex poles two real zeros in the LHP. It can be seen that the dominant pole is at a much lower frequency than the second complex pole and is located at a frequency lower than the two zeros. The resulting 3-dB bandwidth frequency, complex poles, zeros, and UGBW are derived as follows:

$$\omega_{-3dB} = 1/(C_{m1}g_{m2}g_{m3}R_1R_2R_3) \qquad (4)$$

$$\omega_p \approx \sqrt{C_{m2}g_{m2}g_{m3}/C_1C_2C_3} \qquad (5)$$

$$\omega_{z1} \approx g_{m2}/C_{m1} \qquad (6)$$

$$\omega_{z2} \approx g_{mfb}/C_{m2} \qquad (7)$$

$$\omega_{GBW} = A_{DC} \cdot \omega_{p1} = g_{m1}/C_{m1}. \qquad (8)$$

This allows the zeros in the RHP to be formed in the LHP, thus securing the phase margin and allowing the circuit to operate more stably. As shown in (6) and (7), since g_{mff} of the feedforward path weakens the g_{m3} term, the zeros do not have a g_{m3} term and are affected by g_{m2} and g_{mfb}. Figure 6 shows the result of analysis by pole–zero plot. For the analysis, only three poles and two zeros around the UGBW were represented. Figure 6(a) shows the pole–zero position of the RNMC structure as a real imaginary graph. With three LHP poles, there are two zeros in the RHP. These zeros are located at a higher frequency than the zero of LHP. Figure 6(b) represents the pole–zero when the active feedback path is added to the front of the Miller compensation. An active feedback path is added to limit the current flowing to the Miller capacitor at high frequency, thereby preventing the generation of the RHP zero. Figure 6(c) shows the pole–zero when the AFFC and the active feedback scheme are used together. By using the AFFC structure, one zero in the RHP can be dragged into the LHP, and the transconductance of the feedforward path can be increased to place the zero at a lower frequency than the complex pole and improve the phase margin.
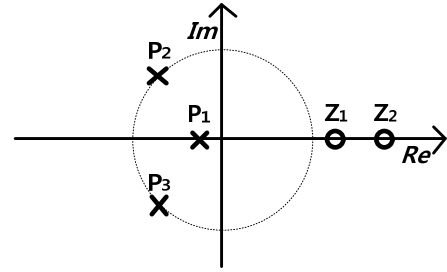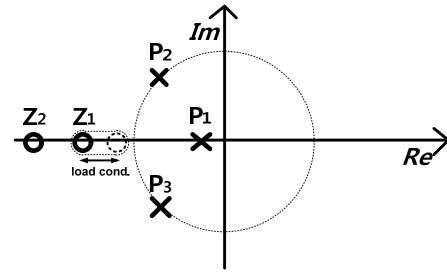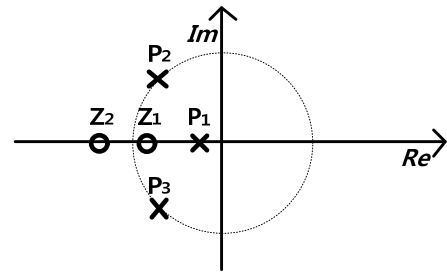
FIGURE 6. Pole–zero plot of proposed AFF-RNMC topology shown in (a) RNMC only, (b) AFFC path only, and (c) both.

The simulation results of the loop gain magnitude and phase of the proposed LDO are shown in Figure 7. When the input voltage is 1.2 V and the load current is at light and heavy, 0 and 70 mA, the DC gain is 81 and 54 dB, respectively, and the phase margin is 63 and 87 deg, which is stable against a low quiescent current. At this simulation, the proposed LDO can withstand load capacitance up to 100 pF in all corner simulations.

III. CIRCUIT IMPLEMENTATION

Figure 8 shows the proposed AFFC-RNMC LDO. The EA consists of two stages with differential to single output. The first stage is comprised of an active current amplifier structure as transistors M10–M14. The second stage is a single stage output consisting of transistors M15 and M16. Both the first and second stages get a negative gain. Since the designed EA has enough gain, it increases the accuracy of regulations, such as load and line regulations. In the output stage, a PT M17,PT and a feedforward path M18 are formed, and there are two feedback resistors R_{FB1} and R_{FB2}.
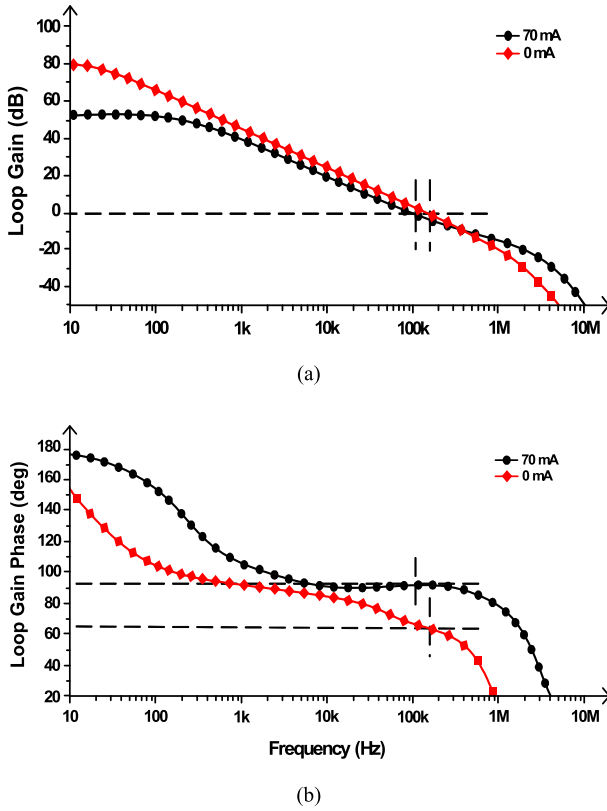
FIGURE 7. Simulation results of open-loop response at different load conditions. (a) loop gain magnitude and (b) loop gain phase.

TABLE 3. Small-signal parameters of proposed AFF-RNMC LDO (Fig.8).

g_{m1}	Transconductance of first stage
R_1	$r_{o,12} \parallel r_{o,14}$
C_1	$C_{gd,12} + C_{gd,14} + C_{gs,16}$
g_{m2}	Transconductance of second stage
R_2	$r_{o,15} \parallel r_{o,16}$
C_2	$C_{gd,15} + C_{gd,16} + C_{gs,PT} \approx C_{gs,PT}$
g_{m3}	Transconductance of third stage
R_3	$r_{o,17} \parallel r_{o,18}$
C_3	$C_{gs,PT} + C_{OUT} \approx C_{OUT}$

In the active feedback path, the first and the last stages are connected through a compensation capacitor C_{m2}. This path is affected by g_{mfb}, the transconductance of transistor M3. Since the gain in the active feedback loop is unity, $1/g_{mfb}$ with a small input impedance value does not exhibit sharing of the drain and gate nodes of M3, the diode-connected part of the first stage. Therefore, g_{mff} has k times the value of g_{mfb}. While using a cross-coupled feedforward path may seem to consume more current, a feedforward path has merits in that it draws more current, reduces output resistance, obtains a higher UGBW than a whole quiescent current, and ensures
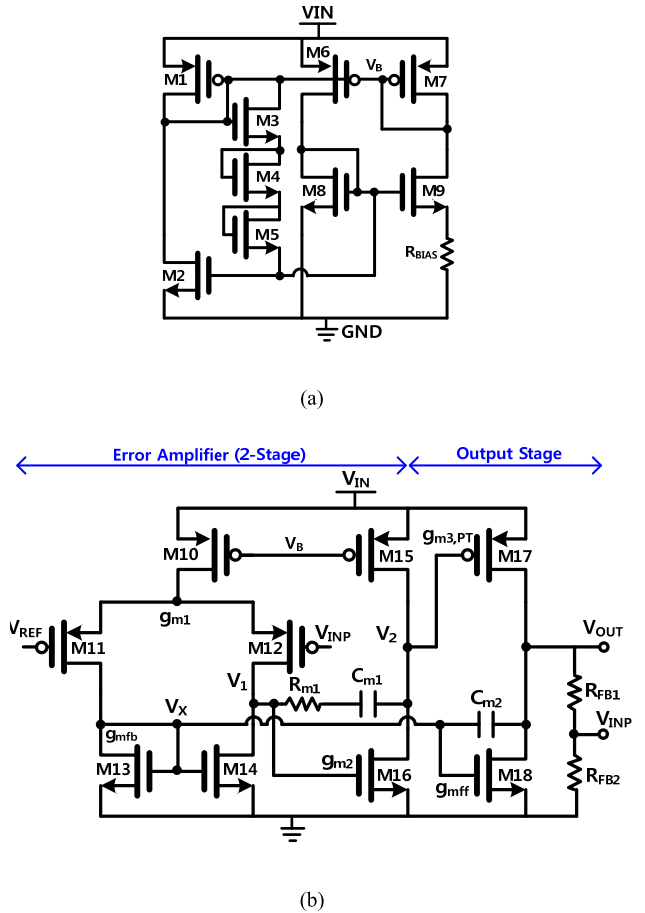

FIGURE 8. Circuit implementation of (a) bias circuit and (b) EA and output stage of proposed AFF-RNMC LDO.

a stable phase margin, where the output resistance R_{OUT} is defined as $r_{o,PT} \parallel r_{o18} \parallel R_L \parallel (R_{FB1} + R_{FB2})$.

Figure 9 shows the result of simulation showing the PSR value at heavy load. The dropout voltage is 200 mV, the input voltage is 1.4 to 2.5 V, and the output voltage is 1.2 V. As expected, the PSR was dominant in the EA gain in the low frequency band, and thus, a relatively low PSR was obtained. As the EA gain decreases and the frequency shifts to higher values, the PSR decreases. In addition, the proposed LDO has a PSR value less than 0 dB in the entire frequency band. The proposed AFFC-RNMC LDO is designed with a low quiescent current and small area as its focus, and it is not designed based on the PSR because the LDO plays the role of supplying voltage to several sub-blocks by lowering the voltage supplied from the battery.

IV. MEASUREMENT RESULT
Figure 10 shows a chip photograph of the proposed AFFC-RNMC LDO fabricated with TSMC 65-nm CMOS technology. The size of the AFFC-RNMC LDO is 0.10 mm × 0.07 mm. It is designed with a small capacity while meeting stability through closed-loop gain and phase analysis, and
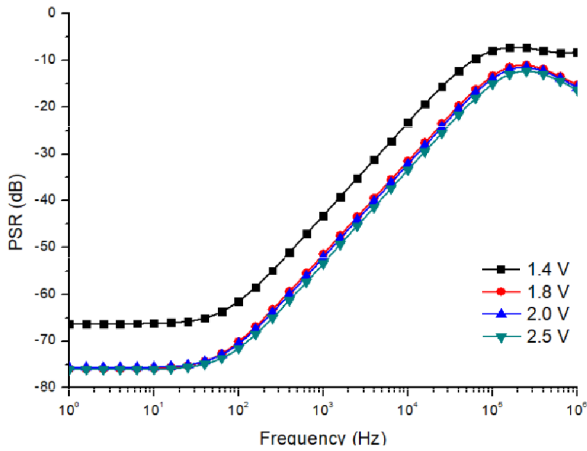
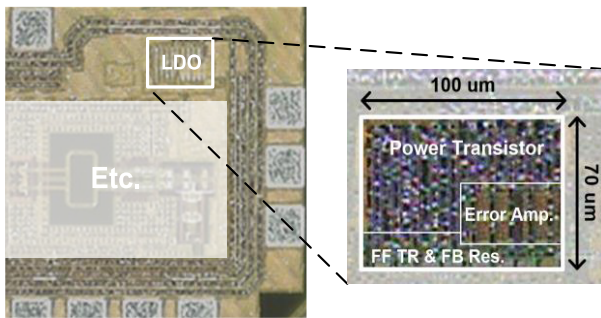**FIGURE 9.** PSR simulation results of proposed LDO at heavy-load condition.

FIGURE 10. Chip photograph.

TABLE 4. Measured capacitor-less LDO performance and comparison.

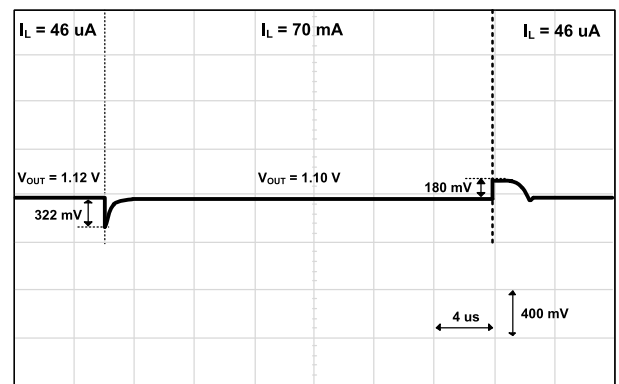| Parameter	[21]	[22]	[23]	This Work
Year	2017	2015	2014	2019
Technology (nm)	65	65	65	65
Active Area (mm^2)	0.087	0.023	0.013	0.007
$I_{Load, max}$ (mA)	25	10	10	70
V_{IN}	1.2	1.2	0.75–1.2	1.2–2.5
V_{OUT}	1.0	1.0	0.55	1.0–1.3
Dropout Voltage (mV)	200	200	200	200
$C_{Load, max}$ (pF)	240	140	10000	100
I_Q (μA)	300	50–90	15.9–487	**9.6–11.5**
Line Reg. (mV/V)	3.8	37.1	4	3.84
Load Reg. (mV/mA)	42	1.1	0.18	0.29
PSR (dB) @10 kHz	-69	-22	-46	-26
PSR (dB) @ 100 Hz	N/A	-21	-53	-67

FIGURE 11. At V_{IN} = 1.3 V and dropout voltage of 200 mV, transient response of V_{OUT} when load current is increased from 46 μA to 70 mA.
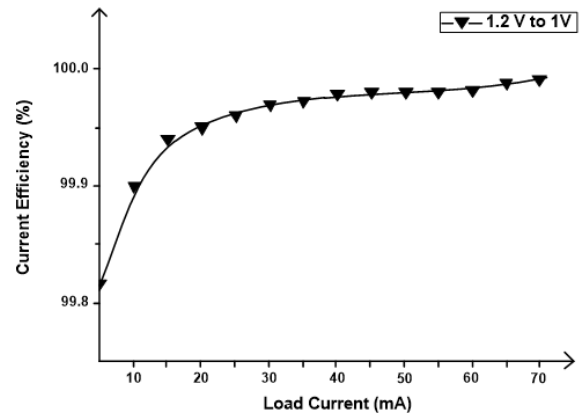
FIGURE 12. Measurement result of current efficiency follows load current in minimum to maximum condition.

it has a small active size despite adding several compensation capacitors. The proposed AFFC-RNMC LDO operates at an input voltage range of 1.2 to 2.5 V and can provide up to 70 mA of load current at the lowest dropout voltage of 200 mV.

The stability of the proposed LDO can withstand load capacitance up to 100 pF. The quiescent current consumes a very small amount of current from 9.6 to 11.5 μA depending on the input level. Using various compensation schemes, the proposed LDO is designed as a stable circuit with a considerable phase margin despite using a low quiescent current.

Table 4 compares the performance of several LDOs with the same 65-nm process parameters and low quiescent current as the target of recent studies. The proposed AFFC-RNMC LDO has several advantages. The proposed LDO has the advantage of high current efficiency with high maximum load and several μA of quiescent current.

A. LOAD TRANSIENT RESPONSE/REGULATION

Figure 11 shows the measured load transient response when the input supply voltage of the proposed AFFC-RNMC LDO is 1.3 V and the output load capacitor is 100 pF. When the load current is changed from 46 μA to the maximum of 70 mA, the settling time is 1.8 us and 2.2 μs, respectively. The

undershoot and overshoot voltages are 322 mV and 180 mV, respectively.

B. CURRENT EFFICIENCY

Figure 12 represents the measurement results of the current efficiency of the proposed LDO. When the input voltage is 1.2 V and the output voltage is 1 V, the current efficiency

is calculated as the quiescent current result when the load current is swept from 0 to 70 mA. When the load current is 70 mA, the quiescent current is 9.6 μA and the current efficiency is 99.99%.

V. CONCLUSION

The proposed AFF-RNMC LDO was designed using a 65-nm CMOS process. A closed-loop pole-zero analysis was performed to match the stability of the proposed LDO. The proposed LDO guarantees stable circuit operation regardless of load conditions. Through analysis, the compensation capacitor can be designed to a small value and designed with a small active size suitable for on-chip. In addition, the capacitance of the load can operate with a stable circuit up to 100 pF. The proposed LDO has high regulation accuracy because it has a high gain due to the structure of a three-stage amplifier. The quiescent current uses a small amount of current of 9.6 μA, and the current efficiency according to the load condition is as high as 99.99%.

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