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A Mesh Downsampling Algorithm for Equivalent Circuit Network Simulation of Multi-Junction Solar Cells

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ABSTRACT Equivalent circuit network simulation is widely used in modeling solar cells in three dimensions. However, the computational time and numerical instability increases dramatically when the number of circuit element increases. This problem is exacerbated by increasing the number of junctions in the solar cells. We propose a downsampling algorithm to reduce the time complexity but retain reasonable accuracy within the appropriate parameter space of multi-junction solar cells. We also publish a full-featured software that implements this algorithm and the full circuit network simulation along with this paper.

INDEX TERMS Circuit simulation, photovoltaic cells, semiconductor device modeling.

I. INTRODUCTION

Equivalent circuit simulation is a very efficient approach to model three-dimensional semiconductor solar cell. The essence of equivalent circuit network simulation is breaking a solar cell into smaller, electrically connected solar cells, which were modeled by a set of current source, diode and a few resistors, as illustrated in FIGURE 1 and 2. Usually, three-dimensional semiconductor modeling involves solving three-dimensional coupled partial differential equations, but this approach generally requires large amount of computational resources [1], [2]. For many applications such as front metal grid optimization, using equivalent circuit network as an approximation provides sufficient accuracy but is much faster to run.

To the best of our knowledge, equivalent circuit simulation or other approaches of this kind have been implemented in many published software packages, such as Griddler [3], [4], PVMOS [5], SPICEGUI [6] and Solcore [7] [8]. However, none of the above package supports the modeling multi-junction solar cell.

Modeling multi-junction solar cell poses other challenges of the equivalent circuit network simulation. A K-junction solar cell increases the number of circuit elements by K times. This increase of circuit elements causes a number of issues of performing this type of simulation. The first challenge is performance. A circuit solver essentially does $N \times N$ matrix inversion [9], where N is the number of nodes in a circuit. Even for linear devices, solving the matrix inversion problem needs a time complexity of around $O(N^{2.807})$ [10]. As the solar cell is a non-linear device, it takes additional iterations to solve the non-linear system equation. A K-junction cell would then increase the dimension of the matrix to roughly NK. State-of-the-art high efficiency multi-junction cells have three or four junctions, which increase the complexity to 10 to 20 times. Therefore, the number of the meshed grids has to be reduced by three or four times in order to keep the computational time close to that of the case of single-junction. The second challenge is numerical instability. Solving the current-voltage characteristics of non-linear electronic devices involves the use of iterative algorithm such as Newton-Raphson method, which becomes easier to fail to converge when the number of the nodes increase. Our experience with ngspice [11] is that the number of nodes should be less than around 10000.

An apparent way to solve this problem is reducing the number of circuit elements in the simulation, in other words, to reduce the resolution of meshing grids in the simulation. This problem has been considered in PVMOS [5]. PVMOS implemented a node-merging algorithm that merges

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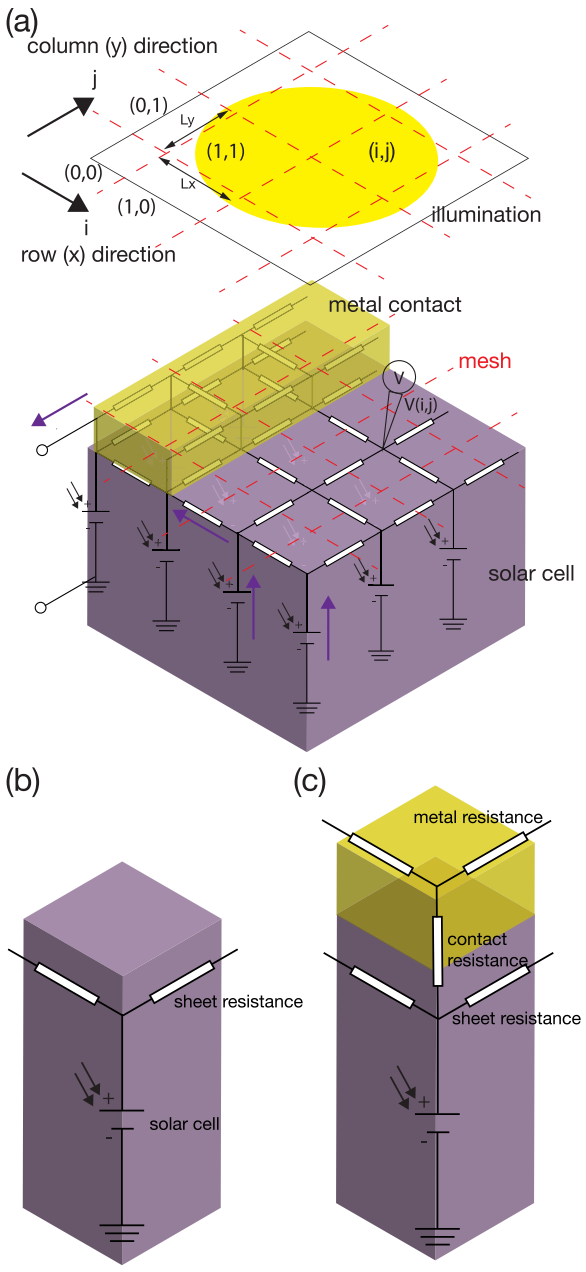

FIGURE 1. (a) An equivalent circuit simulation meshes a solar cell into smaller solar cells. The current generated by the solar cell flows up to the top surface and is collected via the metal contact on the top of the solar cells. The back contact is neglected for simplicity. The smaller unit cells have to types: (b) an unit cell without metal contact on the top and (c) an unit cell with metal contact.

the neighboring pixels of the same kind, followed by an adaptive meshing refinement to increase the meshing resolution with sharp voltage gradient. However, because this reduction approach only merges the pixels of the same kind, the minimum number of nodes that can be reduced to is limited by the features of the front grid pattern. In this work, we propose and implement a more general approximation algorithm to downsample the resolution of the meshes. This method can downsample the resolution of the meshes to an arbitrarily number within the tolerance of accuracy. The computational

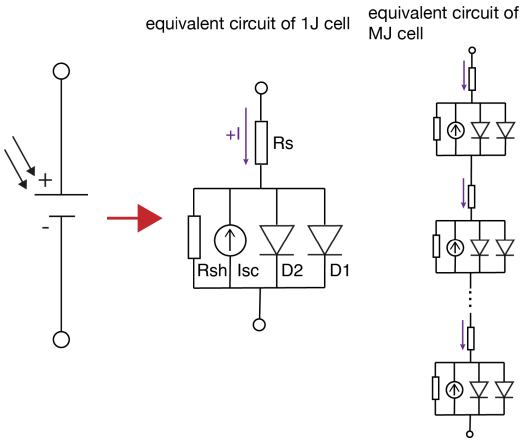

FIGURE 2. A single-junction solar cell is modeled by a set of circuit components comprise of two diodes (D1 and D2), an ideal current source (Isc), one resistor connected in series (Rs) and another resistor connected in parallel (Rsh). In practice, the resistors and the diode D2 can be neglected. A N-junction solar cell can be modeled by N single-junction solar cells.

resource required for modeling multi-junction cell can then be greatly reduced, making it possible to use this equivalent circuit network simulation to perform tasks that requires significant amount of iterations, such as optimizing the design of front metal grid pattern.

In this paper, we will first describe the downsampling algorithm, including the formalism and the details of how to retrieve each modeling parameters for equivalent circuit network. After that, we show the modeling results of various scenarios to verify the accuracy of our approximation algorithm, focusing on the comparison between calculated I-V characteristics of different meshing resolution. Finally, we will discuss the validity and recommend the best practices of using this method.

II. THE ALGORITHMS

A. FORMALISM OF THE PROBLEM

In a three-dimensional equivalent circuit simulation, the solar cell is discretized into $M \times N$ pixels. Based on the definitions of the user, each pixel $P(i, j)$ represents different types of nodes. For example, $P(i, j)$ can either be a solar cell with busbars, a solar cell with fingers, a bare solar cell, or simply nothing if the solar cell is not rectangular.

The solar cell is illuminated by an injection profile $I(i, j, \lambda)$ that has exactly the same dimension as $P(i, j)$, where λ is the illumination wavelength. The illumination of the node $P(i, j)$ is defined by $I(i, j, \lambda)$. The value of the current source is determined by a function f:

$$J_{sc}(i, j) = f(I(i, j, \lambda), P(i, j)) \tag{1}$$

For example, f can be dependent on the quantum efficiency of the solar cell, such as

$$f(I, P) = \int I(i, j, \lambda)\mathrm{EQE}(\lambda)d\lambda \tag{2}$$

A basic unit circuit is formed by the following basic circuit elements:

- contact resistance $r_{c(ij)}$
- metal grid resistance $r_{m(ij)}$
- sheet resistance $r^x_{s(ij)}$ and $r^y_{s(ij)}$
- diode $d_{1(ij)}$
- current source $i_{sc(ij)}$

The physical meaning behind these parameters can be found elsewhere, such as [12]. The values of these parameters are empirical. They can be obtained from other semiconductor simulations or experiments.

B. DOWNSAMPLING ALGORITHMS

In practice, the injection profile **I** and the front metal grid profile **M** are bitmap images obtained from other sources, such as optical ray-tracing simulation or experiments. It is therefore a natural choice to use the pixels in the raw images as an unit in the circuit network simulation. In principle, the minimum number of the nodes is limited by Whittaker-Shannon sampling theorem [13], which states that the minimal resolution should be two times of the spatial frequency of the features on the solar cell. To further reduce the number of nodes, one may use interpolation to downsize the pixels of the image matrix **P**, but this does not work because **P** is not a continuous function. For instance, naive image interpolation cannot merge $P(x_i, y_i)$ and $P(x_{i+1}, y_{i+1})$ if the former is a "metal pixel" (FIGURE 1(b)) and the latter is a "cell pixel"(FIGURE 1(c)). Our goal is to find an approximation function $\mathbf{F}_p$ to map the original set of circuit parameters into a new set of characteristic parameters. This can be formalized as

$$\mathbf{F}_p : \{p_{(ij)} | (i, j) \in \mathbf{D}\} \longmapsto p'_{(i'j')} \tag{3}$$

where p is a circuit element parameter such as r_c or r_m, **D** is a small region of pixels in the raw image, $p'_{(i'j')}$ is the circuit parameters in the downsampled image at the new coordinate (i', j'). FIGURE 3 shows a 2x-downsampled equivalent circuit of FIGURE 1. In this example, we would like to find a function that does the following mapping:

$$\{p_{(ij)} | (i, j) \in \{(0, 0), (0, 1), (1, 0), (1, 1)\}\} \mapsto p'_{(0,0)}$$
$$\cdots\cdots\cdots$$
$$\{p_{(ij)} | (i, j) \in \{(2, 2), (2, 3), (3, 2), (3, 3)\}\} \mapsto p'_{(1,1)}$$

The node merging algorithm demonstrated in PVMOS only merges the set **D** in which its elements have the same $M(i, j)$. Here we propose a more general approach to merge the nodes of different kinds. Our proposed mapping function of each circuit parameter is described as below.

1) METAL GRID RESISTANCE

Our goal is to find the reduced metal grid resistance of an arbitrary metal grid pattern. However, exact solution of this problem only exists in rare cases, for instance, the metal grid pattern is rectangle. We thus propose an approximation to calculate the reduced metal grid resistance of an arbitrary pattern. This approximation assumes that the current flow between each row and column is small. In other words, this approximation decouples the current flow into

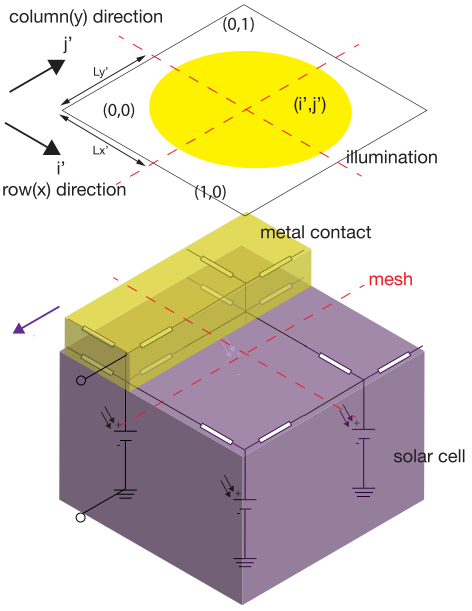

FIGURE 3. The 2x-downsampled equivalent circuit diagram of FIGURE 1(a).

x- and y- direction. In this way, the resistance network in x-direction can be reduced by applying the superposition law:

$$r^x_{m(i'j)} = \sum_{i=0}^{N_I-1} r^x_{m(ij)} \tag{4}$$

$$r^x_{m(i'j')} = 1/\left(\sum_{j=0}^{N_J-1} \frac{1}{r^x_{m(i'j)}}\right) \tag{5}$$

where $r^x_{m(ij)}$ is the metal grid resistance in x-direction at pixel (i, j). We set $r^x_{m(ij)}$ to be numerical infinity if $P(i, j)$ is not covered by a metal contact. Similarly, the resistance in y-direction is:

$$r^y_{m(ij')} = \sum_{j=0}^{N_I-1} r^y_{m(ij)} \tag{6}$$

$$r^y_{m(i'j')} = 1/\left(\sum_{i=0}^{N_J-1} \frac{1}{r^y_{m(ij')}}\right) \tag{7}$$

2) CONTACT RESISTANCE

We assume that the contact resistivity is constant across the solar cell surface. The reduced contact resistance of a downsampled pixel can then be written as

$$r_{c(ij)} = \rho_c/\gamma_m \tag{8}$$

where ρ_c is contact resistivity (Ωm^2) and γ_m is the number of pixels covered with metals divided by the total number of pixels in the selected region, that is,

$$\gamma_m = \frac{\#\{(i, j) | M(i, j) = 1, (i, j) \in \mathbf{D}\}}{\#\{(i, j) | (i, j) \in \mathbf{D}\}} \tag{9}$$

where # is the cardinality of a set.

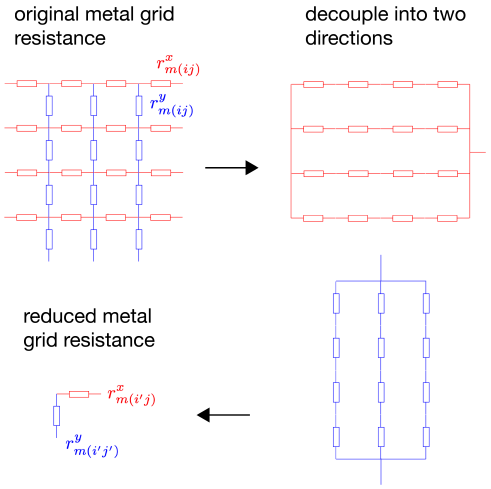

FIGURE 4. Reduction of the metal grid resistance. The network of the resistors in x- and y-directions are decoupled. Each set of the resistors is then merged by resistance superposition law.

3) CURRENT SOURCE

The value of the downsampled current source $i_{sc(i'j')}$ is the sum of the currents in region **D**, namely,

$$i_{sc(i'j')} = \sum_{(i,j)\in\mathbf{D}} i_{sc(ij)} \tag{10}$$

4) DIODE PARAMETERS

The saturation current of the downsampled diode $i_{01(i'j')}$ is the saturation current density multiply by the total pixel area:

$$i_{01(i'j')} = \sum_{(i,j)\in\mathbf{D}} i_{01(ij)} \tag{11}$$

Again, this assumes that the parameters of all the diodes are identical within the region **D**. In this model, the temperature is set explicitly in the diode temperature in SPICE, which takes into account the change of energy distributions of carriers. The diode saturation current is also implicitly affected by other temperature-dependent material properties such as band gap, which can be included if necessary.

5) SHEET RESISTANCE

Assuming that the sheet resistance is uniform, the downsampled sheet resistance can be approximated as

$$r^x_{sh(i'j')} = r^x_{sh(i_0j_0)} \frac{Lx}{Ly}\frac{Ly'}{Lx'} \tag{12}$$

$$r^y_{sh(i'j')} = r^y_{sh(i_0j_0)} \frac{Ly}{Lx}\frac{Lx'}{Ly'} \tag{13}$$

where i_0 and j_0 can be any coordinate within **D**, and Lx and Ly are physical width and height of the pixel (i_0, j_0). Lx' and Ly' are the physical width and height of the new, downsampled pixels. Note that sheet resistance only depends on ratio of the physical height and width of the pixels, its unit is $\Omega/\square$.

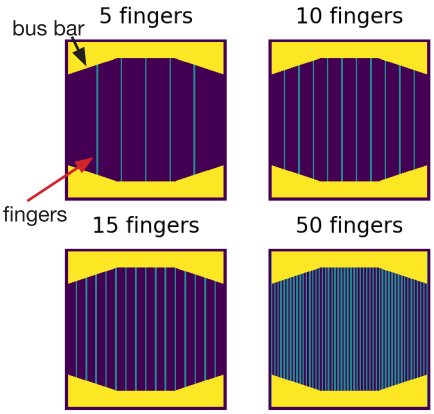

FIGURE 5. The four front contact patterns used in this study. Regions colored in yellow are metal contacts. These four patterns have the same dimension of busbars but differ in the number of fingers. The number of fingers of each pattern is 5, 10, 15 and 50, respectively.

C. POST-PROCESSING OF THE CIRCUIT

The resulting circuit can be further simplified by reducing the circuit elements that has insignificant physical effect. For example, we can short two nodes that are connected by very small value of resistance, or "open" two nodes that have large resistance. The node reduction can be implemented by an union-find algorithm [14].

III. RESULTS AND VALIDATION OF THE IMPLEMENTATION

A. MODELING PARAMETERS

In this section we demonstrate a few representative test cases to show how our downsampling algorithms performs. The aim is to know how the meshing downsampling algorithm affects the I-V characteristics of the solar cell. FIGURE 5 shows the front metal patterns for this demonstration. These patterns similar to typical designs of concentrator photovoltaic solar cells. In these patterns, large metal pad (busbars) sits near the edge of the cell to collect the current. On the center of the solar cells lays the parallel thinner front grids. The four patterns in FIGURE 5 only differ in the number of metal grids in the middle. The dimensions of busbars and metal fingers are the same.

We choose to model three-junction solar cells with a band gap combination of 1.87eV/1.42eV/1.0eV. Each subcell is assumed to perform at Shockley-Queisser limit. Detailed calculations and code implementations are described in [15] [16] [17]. Since our main purpose is to test the validity of the network simulation model, this setting is sufficient to provide reasonable values of saturation current of each subcell to test the accuracy of the downampling algorithm. We also assume uniform ASTM1.5d illumination, i.e., $I(i, j, \lambda)$ is constant, throughout the following examples.

FIGURE 5 demonstrates a front grid pattern that would exceed the node limit of ngspice, i.e., the number of nodes is too large for ngspice to converge. The raw image is 1000×1000 pixels. Simulating this in full dimension results in at least 250×250 nodes even we only take a quarter of the image

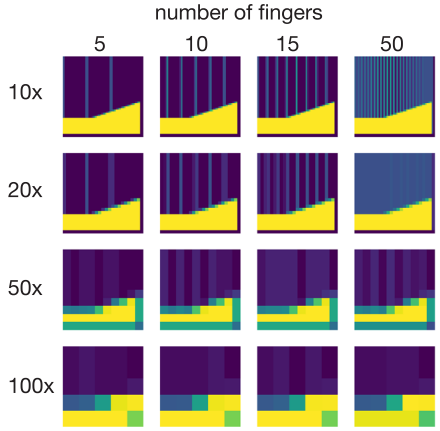

FIGURE 6. The downsampled images of the patterns shown in FIGURE 5.

by taking into account the cell symmetry. As we are mainly interested in higher injection, we can neglect the effect of the diode component D2 (see FIGURE 2). Also, we assume that the series resistance of the solar cells is mainly contributed by the sheet resistance and metal grid, meaning that the series resistance Rs in FIGURE 2 can also be neglected. We also neglected the shunt resistances R_{sh} in our simulation because this value in good quality cells is large.

We tested three different front metal grid patterns, each of which shares the same dimensions of the busbars but with different number of grids in the middle. The height of the front metal grids is set to be 2.2 μm and the resistivity is 2.4×10^{-8} Ωm^{-1}. For each of the pattern, we tested different downsampling ratios ranging from 10x to 20x. The down sampling ratio is defined as the height and width of $\mathbf{D}$ in (3) that being merged into the new pixel. For instance, a downsampling ratio of 2x means that $\mathbf{D}$ is a 2 pixel $\times$ 2 pixel region.

B. LOW-CONCENTRATION, SMALL-SIZED DEVICE

We first tested a 1 mm $\times$ 1 mm cell illuminated at one sun. We can see that the widths of the metal grids are widened in the voltage map image because (5)-(7) distributes the value of $r_{m(ij)}$ into a larger-area pixel, becoming $r_{m(i'j')}$. The left-hand side of FIGURE 7 shows the voltage maps of each case, whereas the right-hand side of FIGURE 7 shows the I-V characteristics. The good match of I-Vs between each downsampling ratio indicates that this meshing algorithm retains the accuracy of the I-Vs well. FIGURE 8 plots the short-circuit current (Isc), open-circuit voltage (Voc), and fill factors (FF) of the I-V characteristics in FIGURE 7 with respect to selected downsampling ratios. Larger number of metal grids increases the fill factors because of lower overall resistance, but it decreases Isc due to larger metal coverage. The figures of merits remain nearly constant against the downsampling ratios, showing that our proposed meshing algorithm is a good approximation with significantly improved computational speed, as shown in FIGURE 8.

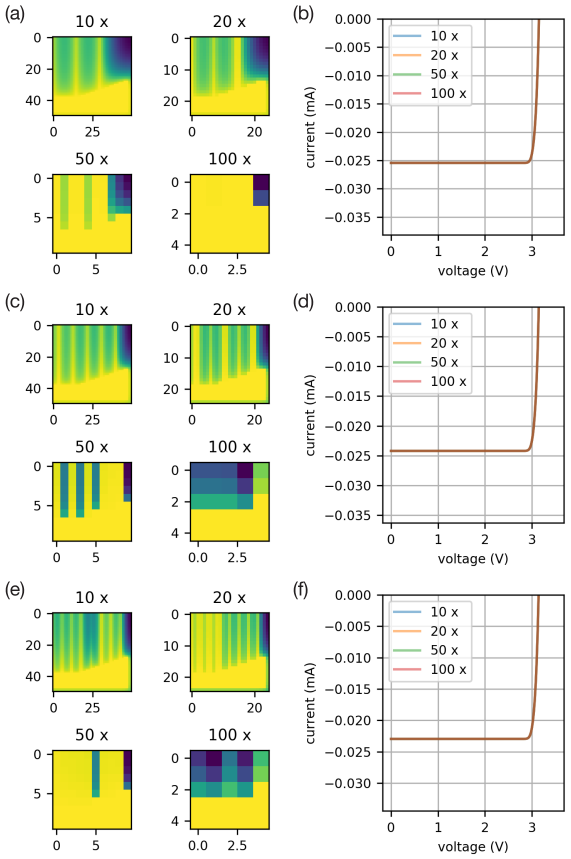

FIGURE 7. The modeled voltage map and I-V characteristics of devices with an area of 1 mm x 1 mm illuminated at one sun (see Section III-B). Left column: Calculated voltage maps of various downsampling ratios of front grid patterns of (a) 5 (c) 10 and (e) 15 fingers at an external bias of 3.5 V. Right column: Modeled I-V characteristics of front grid patterns of (b)5, (d)10 and (f) 15 fingers.

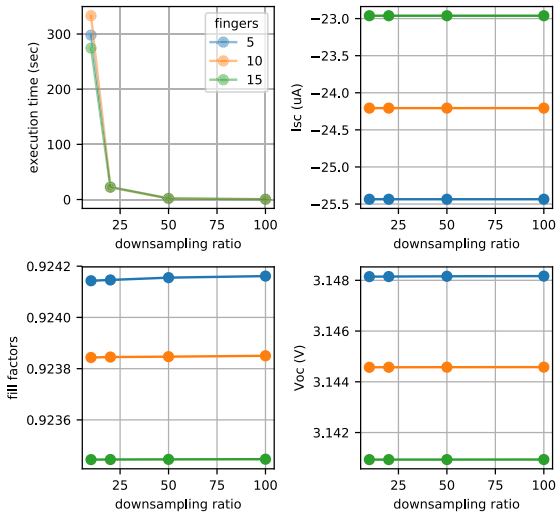

FIGURE 8. Figures of merits against downsampling ratios of a 1 mm x 1 mm device illuminated at one-sun (see Section III-B).

C. HIGH CONCENTRATION, SMALL DEVICE

Next we increase the illumination concentration of the simulated device to 500 suns while keep other modeling

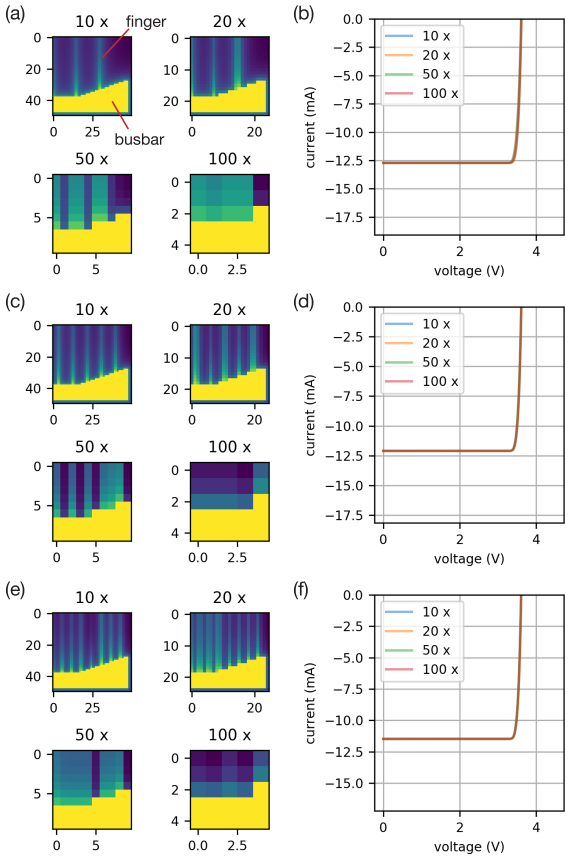

FIGURE 9. (a) The modeled voltage map and I-V characteristics of devices with an area of 1 mm × 1 mm illuminated at 500 suns (see Section III-C). Left column: Calculated voltage maps of various downsampling ratios of front grid patterns of (a) 5 (c) 10 and (e) 15 fingers at an external bias of 3.5 V. Right column: Modeled I-V characteristics of front grid patterns of (b)5, (d)10 and (f) 15 fingers.

parameters the same as Section III-B. Again, the modeled voltage maps, I-V characteristics and figure of merits are shown in FIGURE 9 and FIGURE 10. At this modeling condition, we start to see some deviations of Vocs and FFs when downsampling ratio increases, especially the Vocs and FFs of the devices with only five fingers. This is due to the increase of resulting voltage gradient of each pixel, making the assumptions behind (5), (7) and (13) less valid. Even though, the differences of the Vocs and FFs caused by varying downsampling ratios are very insignificant. Even for the 5-finger device, the change of fill factors is less than one absolute percent when the downsampling ratio increases from 10 x to 100 x, whereas the change of Voc is 0.006 V.

D. HIGH CONCENTRATION, LARGE DEVICE

Here we consider a more extreme case. The size of the solar cell is increased to 1 cm × 1 cm. This is accomplished by increasing the physical height and width of each pixel by ten times in the model setting. The concentration set to be 500x. As shown in FIGURE 12, the Isc of 15- and 20-finger cells still remain constant against different downsampling ratio. The Isc of the 5-finger cell deviates more with the increase of

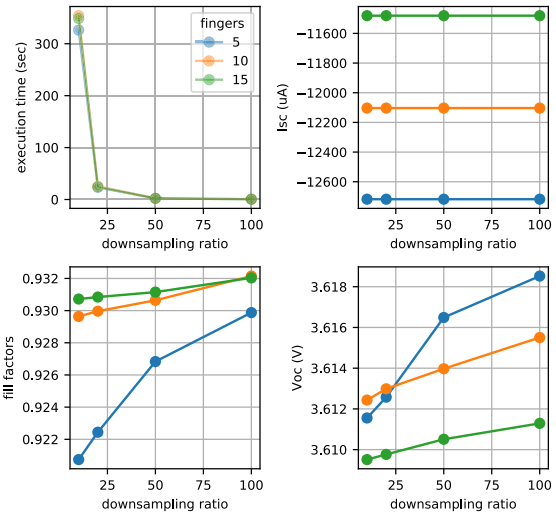

FIGURE 10. Figures of merits against downsampling ratios of a 1 mm × 1 mm device illuminated at 500 suns (see Section III-C).

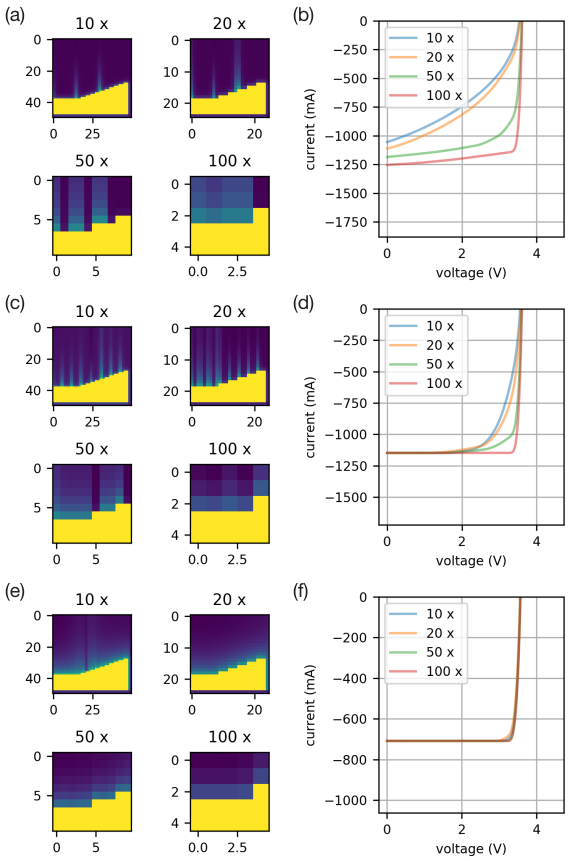

FIGURE 11. (a) The modeled voltage map and I-V characteristics of devices with an area of 1 cm × 1 cm illuminated at 500 suns (see Section III-D). Left column: calculated voltage maps of various downsampling ratios of front grid patterns of (a) 5 (c) 15 and (e) 50 fingers at an external bias of 4.5 V. Right column: Modeled I-V characteristics of front grid patterns of (b)5, (d)10 and (f) 50 fingers.

the downsampling ratio because the sheet resistance makes the I-V very resistive, as shown in FIGURE 12(b). The fill factors of the patterns with less fingers become less accurate

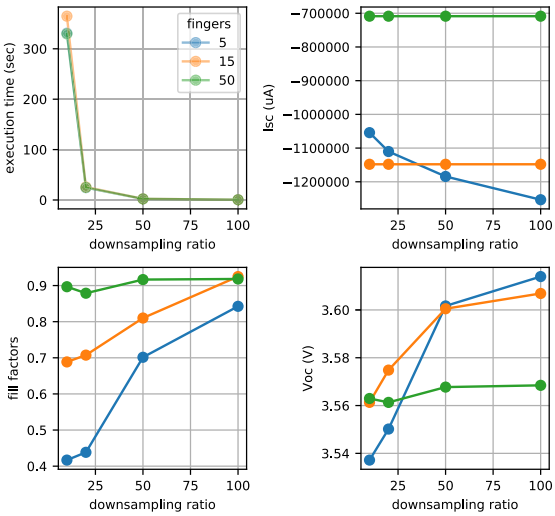

FIGURE 12. Figures of merits against downsampling ratios of a 10 mm × 10 mm device illuminated at 500 suns (see Section III-D).

because the voltage across each pixel becomes very large, which breaks the assumptions of merging metal grid resistance and sheet resistance. For patterns with more fingers more than 25 fingers, the calculated fill factors seem less dependent on the downsampling ratio, however, because high downsampling ratio broadens the pattern and make them completely unrecognized, resulting in high fill factor values. In practice, solar cells operating at such high current density with only five fingers should be out of the usual parameter space of the solar cells and therefore not often considered when modeling or designing. Therefore, although this approximation breaks down at the regimes where the fill factors are low, this does not affect the feasibility of using this approximation to search the optimal solar cell design.

IV. DISCUSSION

The results described in Section III shows that the mesh sampling algorithm causes almost no errors when the voltage gradient within a mesh grid (a pixel) is small. As shown in Section III-B and III-C, the I-V characteristics at different downsampling ratios almost overlaps despite of the grid pattern was slightly altered after downsampling the mesh. The physical intuition behind this is that small "rearrangement" of the resistors wisely in the circuit network will not affect the aggregated I-V results. However, as the current flow increases, the assumptions behind the reduction of metal grid resistances and sheet resistances would fail. Fortunately, the solar cell parameters that may fail this mesh simplification algorithm are unrealistic to use and thus not within our scope of interest. A simple rule of thumb is using fill factors: this mesh downsampling algorithm may not be accurate when the calculated fill factor values are below 0.8. Another way is to calculate the voltage gradient per pixel. Keeping the voltage gradient of the order of 1 mV would ensure the accuracy of this downsampling algorithm.

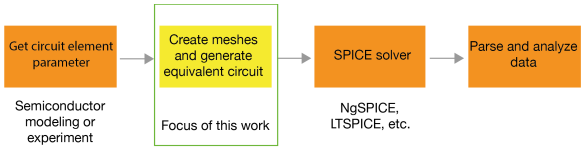

FIGURE 13. The workflow of our implementation of circuit network simulation.

V. CONCLUSION AND FURTHER WORK

We presented and validated a mesh simplification algorithm for equivalent circuit modeling. Within the appropriate parameter space of solar cells, our proposed mesh downsampling algorithm reduces the computational time significantly but retains the accuracy of the modeling. This approach can work in conjunction with other meshing techniques such as adaptive mesh refinement to give more flexibility and accuracy to equivalent circuit modeling.

APPENDIX
THE SOFTWARE

The work flow of the network simulation we implemented is illustrated in FIGURE 13. The main focus of this work takes the circuit parameters from other sources and create a netlist file that is sent to a SPICE solver. The software was uploaded to https://doi.org/10.24433/CO.2397906.v1 for the readers to reproduce the calculations in Section III. Interested readers can also download the code from https://github.com/kanhua/pypvcircuit.

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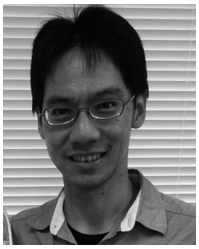

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