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Virtual Resistor-Based Integrated DC Bus Voltage Conditioner for Stability Improvement of Cascaded Power Converters

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ABSTRACT A bidirectional integrated bus voltage conditioner (IBVC) for an isolated phase-shifted full bridge (PSFB) dc/dc converter is proposed to reduce the dc bus voltage oscillations in a cascaded power converter system, where a load converter is controlled tightly with high-control bandwidth. In the proposed method, unlike conventional dc bus voltage stabilization methods for which auxiliary switches are used, the multiplexing utilization of the full bridge switches at the primary side of a PSFB is adopted. In this paper, to improve the dc bus voltage stability, an equivalent virtual resistor is implemented by applying the duty cycle regulation for both legs of the PSFB. The effectiveness of the proposed method on the dc voltage stabilization is examined through simulations and experiments. The achieved results reveal that the dc bus voltage stability is significantly improved with the proposed method.

INDEX TERMS Integrated DC bus voltage conditioner, switch multiplexing utilization, virtual resistor, cascaded power converter, DC bus voltage stability.

I. INTRODUCTION

The DC distribution systems developed based on cascaded and interconnected power converters have been widely used in various engineering systems such as renewable energy systems, more-electric aircrafts, and ship electric propulsion systems. In such systems, the tight control of the load converter with high control bandwidth makes the system to behave like a constant power load (CPL). CPLs consequently present a negative impedance characteristic that results in DC bus voltage oscillations [1]. The improvement of the stability and dynamic performance of DC bus voltage with constant power loads and sudden load change conditions is challenging. Recently, several methods have been proposed to enhance the stability of DC bus voltage. In general, the proposed methods can be classified as passive methods and active methods. The passive methods are mainly based on passive filters such as electrolytic capacitors and decoupling filters [2]–[4]. The large electrolytic capacitors are usually connected across the DC link to stabilize the DC link voltage. The decoupling filters are usually connected between the source converter and the load converter. In this case, the input impedance of the decoupling filter should be higher than the output impedance of the source converter, and filter output impedance should be lower than the input impedance of the load converter to satisfy the requirement defined by the Middlebrook criterion [5]. Although the passive methods can be easily applied, they increase the cost, volume, and weight of the system. Also, the bulky electrolytic capacitors might cause reliability problems.

One of the commonly used active compensation methods is the virtual control method. In this method, the disturbance information on DC bus voltage or current is integrated into the control system of the load converter, a virtual capacitance or virtual resistance can be obtained through a properly designed control scheme to improve the stability of the DC bus

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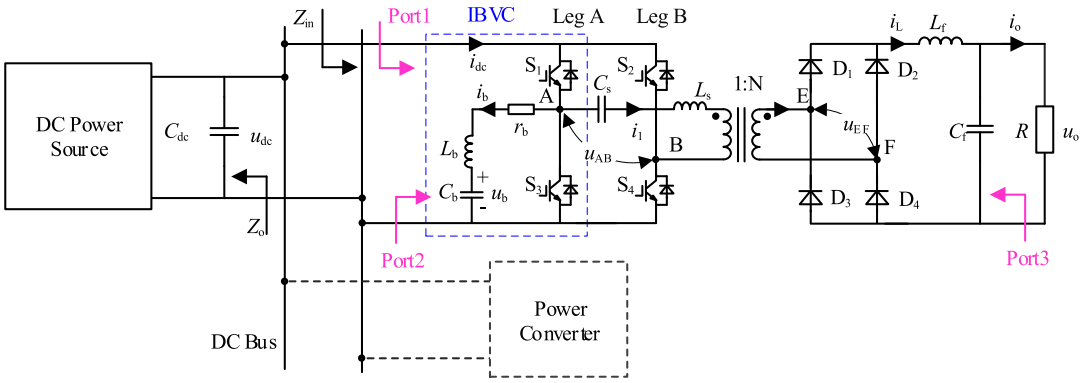

FIGURE 1. The cascaded DC power converter with the integrated bus voltage conditioner.

voltage [6], [7]. Although the stability of the DC link voltage can be improved using these compensation methods, integrating the DC link voltage disturbance into the control system will affect the control performance of the load converter [8]. This means the stabilization of the DC bus voltage is improved at the expense of degradation in the load converter metrics. Another commonly used active method is the method based on a bus voltage conditioner (BVC). The BVC is applied to construct an active damping device to reduce the negative impact of a CPL. In the related literature, a bidirectional half-bridge converter is usually used as a BVC to stabilize the DC bus voltage by controlling the charging and discharging of energy storage components in the converter [9]–[14]. In the bus voltage conditioners, in addition to the capacitors and inductors used as energy storage components, two or more switches are also needed for control purposes, which impose more cost and power losses.

To examine the effectiveness of the stabilization methods, several common techniques have been applied, such as the Middlebrook criterion and minor-loop-gain based forbidden region methods like the Gain and Phase Margin Criterion (GMPM) [15], the Opposing Argument Criterion (OA) [16]–[18], and the Energy Source Analysis Consortium (ESAC) Criterion [19]. In recent years, the passivity-based stability criterion [20], [21] has also been adopted. This criterion transforms a traditional two-port based stability problem into a one-port problem simplifying the stability analysis. However, due to complexity of defining the stability margins, the design process can get complicated resulting in strict stability conditions.

In this paper, an integrated bus voltage conditioner is proposed to stabilize the DC link voltage through multiplexed utilization of the existing full bridge switches, a relatively small capacitor, and an inductor. The proposed power converter behaves like a semi-isolated three-port converter (as denoted in Fig. 1) which is similar to the idea with isolated topology proposed in [22]. Compared to existing standalone bus voltage conditioners that require additional switching components and control systems, the proposed integrated scheme has smaller size, lower cost and less power losses. And according to [23], the current in the LC circuit is helpful to discharge the collector-to-emitter (drain-to-source) capacitor of IGBT (MOSFET) which is beneficial to obtain soft switching in light load conditions.

The rest of this paper is organized as follows. In Section II, the modulation scheme of a PSFB converter, the control-oriented models, the proposed compensation strategy, and the ESAC Criterion are presented along with a Bode plot based stability analysis of the cascaded power converters. The simulation and experimental results that validate the effectiveness of the proposed method are given in Section III. Finally, the conclusion is drawn in Section IV.

II. MODULATION, MODELING AND CONTROL METHOD

A. MODULATION OF PSFB CONVERTER

The proposed integrated bus conditioner is shown in Fig.1. In Fig. 1, Z_o represents the output impedance of the power source converter, it can be a closed loop controlled power converter or a diode rectifier, and Z_{in} represents the input impedance of the load converter. The switches S_1-S_4 are applied to deliver the energy from the DC bus to the load. The turns ratio of high frequency transformer is N. The switches S_1 and S_3 and L_b and C_b are utilized to form the integrated bus conditioner. C_b is used to buffer the transient energy, L_b is used to limit the high-frequency ripple current and r_b represents the equivalent series resistance (ESR) of L_b. C_s has a relatively high value (200μF in this study) and is used to block DC component in the transformer winding. The performance of the proposed voltage bus conditioner is very similar to a bidirectional half-bridge Buck/Boost converter.

In the proposed integrated bus voltage conditioner, S_1 and S_3 are complementary switches, and S_1 is adopted as the main switch in the branch.

In the normal operation mode, the duty cycle of all the switches on leg A and leg B is 50%, and the output voltage u_o is controlled by varying the phase shift between leg A and leg B. In the proposed method, the switching signals of the full bridge converter are shown in Fig. 2. In this figure, it can

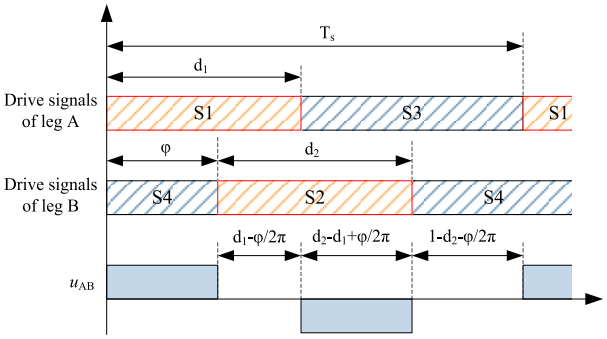

FIGURE 2. The phase shift pulses of the full bridge converter.

be seen that there is a phase shift, φ between the switching signals of leg A (leading leg) and leg B (lagging leg). Also, the duty cycle of leg A is d_1, and the duty cycle of leg B is d_2.

As shown in Fig. 2, the phase shift between the leg A and leg B is always less than $2\pi d_1$ and $2\pi(1\text{-}d_2)$ if the condition given by (1) is satisfied.

$$\frac{\varphi}{2\pi} \le \min(d_1, 1-d_2) \tag{1}$$

If condition (1) is not satisfied, the width of u_{AB} will be determined by d_1 and d_2, and the output voltage u_o cannot be regulated by φ [24]. If the volt-second balance principle is applied to the output filter inductor L_f in the PSFB converter, then, the output voltage u_o can be expressed by (2).

$$\begin{aligned} u_o &= N\left[\frac{\varphi}{2\pi}(u_{dc}+u_{cs}) + (d_2-d_1+\frac{\varphi}{2\pi})(u_{dc}-u_{cs}) \right. \\ &\quad \left. + (1-\frac{\varphi}{\pi}+d_1-d_2)\,|u_{cs}|\right] \\ &= \begin{cases} Nu_{dc}\left[\frac{\varphi}{\pi}(1-\delta_d)+2\delta_d-2\delta_d^2\right], \delta_d > 0 \\ Nu_{dc}\left[\frac{\varphi}{\pi}(1+\delta_d)\right], \delta_d < 0 \end{cases} \end{aligned} \tag{2}$$

In (2), $\delta_d = d_2 - d_1$ and $u_{cs} = \delta_d u_{dc}$. Therefore, u_o can be adjusted by controlling φ and δ_d, and d_1 and d_2. If the constraint condition given by (3) is satisfied, then (2) can be rewritten as (4).

$$d_1 = d_2 = d \tag{3}$$

$$u_o = \frac{Nu_{dc}}{\pi}\varphi \tag{4}$$

According to (4), u_o is completely independent of d_1 and d_2 which means the duty cycle changes will not affect u_o in steady state, and u_o can be controlled only by φ in the steady state. Therefore, the duty cycle, d is an idle variable that can be used for other control purposes, such as DC bus voltage fluctuation reduction that is proposed in this work. By charging and discharging the buffer capacitor, C_b, the voltage oscillation in the DC bus can be suppressed through proper duty cycle regulation.

B. SIMPLIFIED SMALL SIGNAL MODEL

In order to investigate the influence of the resistive load on the DC bus voltage stability, the simplified model of the circuit

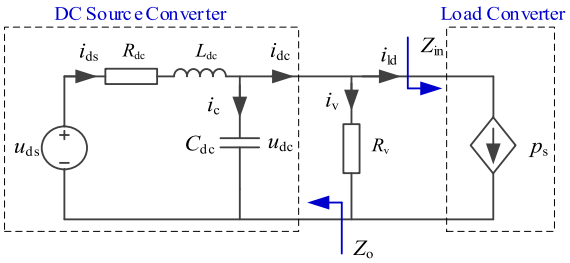

FIGURE 3. The simplified circuit of the cascaded DC power system.

presented in Fig. 1 with an additional parallel resistor R_v on DC bus is shown in Fig. 3 (assuming the DC bus voltage, u_{dc} in Fig. 1 can be rectified by a three-phase diode rectifier as adopted in [6]). In this figure, u_{ds} represents an ideal DC power source, R_{dc} and L_{dc} are the equivalent output resistance and the inductor of the DC power source converter. Also, i_{ds} and i_{dc} are the source current and the DC link current, respectively. C_{dc} is the DC bus capacitor, and p_s is the power absorbed by the load.

In Fig. 2, Z_o represents the output impedance of the source converter, and it can be expressed as (5).

$$Z_o = \frac{L_{dc}s + R_{dc}}{L_{dc}C_{dc}s^2 + R_{dc}C_{dc}s + 1} \tag{5}$$

In order to investigate the impact of p_s on u_{dc}, the differential equations of the circuit presented in Fig. 3 are given by (6).

$$\begin{cases} L_{dc}\dfrac{di_{ds}}{dt} = u_{ds} - R_{dc}i_{ds} - u_{dc} \\ C_{dc}\dfrac{du_{dc}}{dt} = i_{ds} - i_{dc} - \dfrac{u_{dc}}{R_v} \\ i_{dc} = \dfrac{p_s}{u_d} \end{cases} \tag{6}$$

Consequently, the small signal relationship between p_s disturbance and u_{dc} disturbance can be expressed as (7).

$$\begin{aligned} \frac{\hat{u}_{dc}}{\hat{p}_s} &= -\frac{1}{U_{d0}} \cdot (sL_{dc}+R_{dc}) \Big/ [s^2 L_{dc}C_{dc} + s(R_{dc}C_{dc} \\ &\quad + \frac{L_{dc}R_0 + L_{dc}R_v}{R_0 R_v}) + \frac{R_{dc}(R_0+R_v)}{R_0 R_v} + 1] \end{aligned} \tag{7}$$

where $\hat{u}_{dc}$ and $\hat{p}_s$ are the small signal disturbance of u_{dc} and p_s respectively, U_{d0} is the rated voltage of u_{dc}, P_{s0} is the constant load power, R_0 is an ideal negative resistor that corresponds to the constant power load, and it is given by (8).

$$R_0 = -\frac{U_{d0}^2}{P_{s0}} \tag{8}$$

The poles of (7) are given by (9), if these poles are shifted to the right-half of s-plane, the DC bus voltage will be unstable.

$$p_{1,2} = -\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} \tag{9}$$

where ω_n is the natural oscillation frequency, and it can be used to predict the oscillation frequency of the DC bus

voltage, and ζ is the damped coefficient. ω_n and ζ are given by (10) and (11), respectively.

$$\omega_n = \sqrt{\left(\frac{R_{dc}}{R_0} + \frac{R_{dc}}{R_v} + 1\right)\frac{1}{L_{dc}C_{dc}}} \tag{10}$$

$$\zeta = \frac{1}{2\omega_n}\left(\frac{R_{dc}}{L_{dc}} + \frac{1}{R_0 C_{dc}} + \frac{1}{R_v C_{dc}}\right) \tag{11}$$

Usually, R_{dc} is very small, so it can be guaranteed that the coefficients of denominator polynomial in (7) is greater than zero if U_{d0} is high enough. Thus, according to the Routh's stability criterion, to stabilize the DC bus voltage, the following condition given by (12) must be satisfied.

$$\frac{U_{d0}^2}{R_v} > P_{s0} - P_{max} = P_{s0} - \frac{R_{dc}C_{dc}}{L_{dc}}U_{d0}^2 \tag{12}$$

According to (12), it is obvious that a larger DC link capacitance is needed to provide sufficient dynamic energy to support higher constant power load if all other circuit parameters are fixed. Moreover, a smaller value of parallel resistor, R_v can help the DC power source to support constant power load. Under these conditions, the poles given by (9) can be moved to the left-half of s-plane, thus, the stability of the DC bus voltage can be guaranteed. If the conditions given by (1) and (3) are satisfied, the duty cycle regulation and phase shift control are independent, therefore, the output voltage of the PSFB converter can be controlled by phase shift regulation. The small signal circuit model of a phase shifted full bridge converter is shown in Fig. 4 [25].

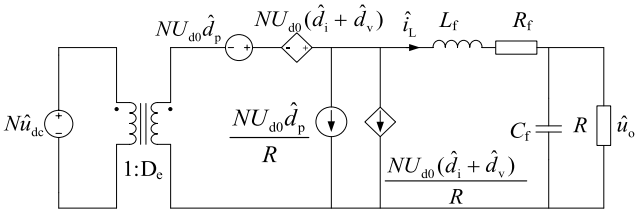

FIGURE 4. The small signal circuit model of a phase shifted full bridge converter.

In the circuit presented in Fig. 4, $\hat{d}_p$ is the small signal disturbance of the equivalent duty cycle (corresponding to φ) of u_{AB} in Fig.1 and D_e is the steady-state value of the effective duty cycle of u_{EF} in Fig. 1 respectively. The small signal disturbances of duty cycle given by (13) are generated as a result of the fluctuation of the inductor current and the input voltage.

$$\begin{cases} \hat{d}_i = -\dfrac{4NL_{lk}f_s}{U_{d0}}\hat{i}_L = -\dfrac{R_d}{NU_{d0}}\hat{i}_L \\ \hat{d}_v = \dfrac{R_d I_L}{NU_{d0}^2}\hat{u}_{dc} \end{cases} \tag{13}$$

where L_{lk} is the leakage inductance, f_s is the switching frequency, and I_L and $\hat{i}_L$ are the steady-state value and small signal disturbance of the inductor current respectively.

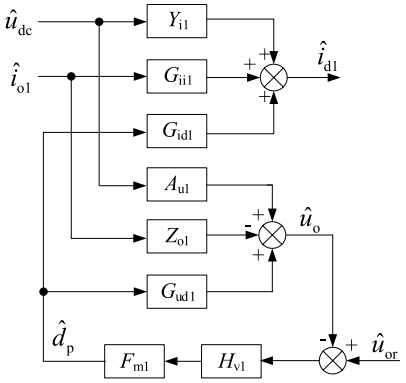

FIGURE 5. The small signal control block diagram of a PSFB.

The small signal transfer function of the control-to-output voltage for the circuit presented in Fig. 4 is adopted to design the voltage controller for a PSFB and is given by (14).

$$G_{ud1} = \frac{\hat{u}_o}{\hat{d}_p} = \frac{NU_{d0}}{L_f C_f s^2 + (L_f/R + R_d C_f)s + R_d/R + 1} \tag{14}$$

The G-parameter small signal control block diagram of PSFB is presented in Fig. 5. In this figure, Y_{i1} is the open loop input admittance, G_{ii1} is the transfer function of $\hat{i}_{o1}$-to-$\hat{i}_{d1}$, G_{id1} is the transfer function of $\hat{d}_p$-to-$\hat{i}_{d1}$, A_{u1} is the transfer function of $\hat{u}_{dc}$-to-$\hat{u}_o$, Z_{o1} is the open loop output impedance, G_{ud1} is the transfer function of $\hat{d}_p$-to-$\hat{u}_{o1}$, F_{m1} is the transfer function of the modulator and H_{v1} is the voltage controller. The transfer functions shown in Fig. 5 can be extracted from literatures [25], [26]. In order to achieve a high bandwidth voltage control system (by which the output voltage can be tightly regulated, and consequently the load converter will show CPL characteristic and negative impedance properties), the voltage controller with two zeros and two poles shown in (15) is employed.

$$H_{v1}(s) = \frac{K \times (s/\omega_{z1} + 1) \times (s/\omega_{z2} + 1)}{s \times (s/\omega_{p1} + 1) \times (s/\omega_{p2} + 1)} \tag{15}$$

In (15), ω_{z1} and ω_{z2} are the angular frequencies of zeros, ω_{p1} and ω_{p2} are the angular frequencies of the poles, and K is the controller gain. According to Fig. 5, (16) can be obtained.

$$\begin{cases} \hat{i}_{d1} = \hat{u}_{dc}Y_{i1} + \hat{d}_p G_{id1} + \hat{i}_{o1}G_{ii1} \\ \hat{u}_o = \hat{u}_{dc}A_{ul} + \hat{d}_p G_{udl} + \hat{i}_{ol}Z_{ol} \end{cases} \tag{16}$$

In (16), $\hat{d}_p = H_{v1}F_{m1}(\hat{u}_{or} - \hat{u}_o)$, by setting $\hat{u}_{or} = 0$ and $\hat{i}_{o1} = 0$ in (16), the closed-loop input admittance can be deduced as (17).

$$Y_{in} = \frac{1}{Z_{in}} = Y_{i1} - \frac{A_{u1}H_{v1}F_{m1}G_{id1}}{1 + G_{ud1}H_{v1}F_{m1}} \tag{17}$$

The simulation parameters are given in Table 1. By utilizing these parameters, the Bode plots of the PSFB voltage control system with and without correction are presented in Fig. 6. In this figure, it is obvious that the crossover frequency of the corrected system is about 1.5 kHz with -20 dB/dec attenuation

TABLE 1. Simulation model parameters.

Parameter	Value
u_{dc}	135V
u_o	40V
R_{dc}	0.02Ω
L_{dc}	3mH
C_{dc}	900μF
L_f	150μH
C_f	1100μF
C_b	560μF
L_b	1mH
r_b	0.1Ω
R	8/1.7Ω
f_s	20kHz
Turns ratio 1:N	1:2/3

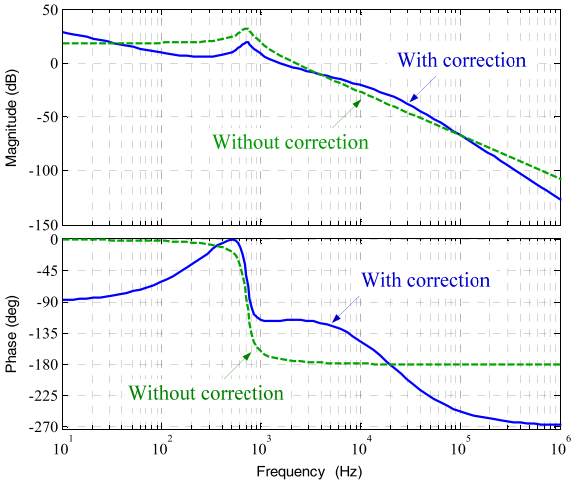

FIGURE 6. The Bode plot of a PSFB voltage control loop with and without correction.

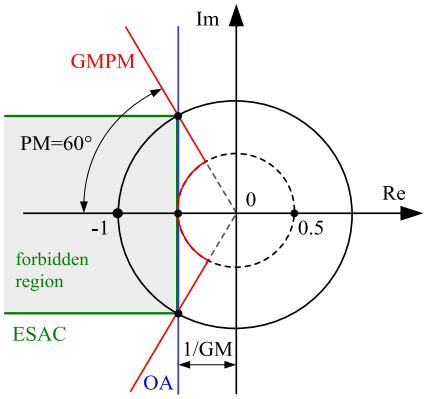

FIGURE 7. The forbidden region boundaries of different criteria.

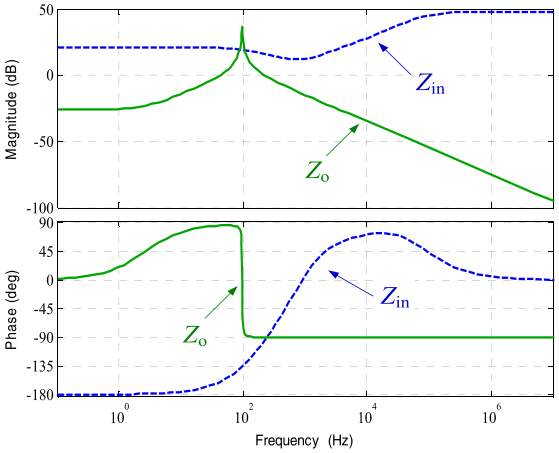

FIGURE 8. The Bode diagram of Z_{in} and Z_o.

rate, the phase margin is about 63°, and the gain margin is about 31dB.

C. ESAC CRITERION AND ANALYSIS

The stability of a cascaded system can be guaranteed by keeping the Nyquist contour of Z_o/Z_{in} outside its forbidden region [27]. The ESAC criterion allows not only imposing the desired minimum gain margin (GM) and phase margin (PM) similar to the GMPM criterion and Opposing Argument (OA) criterion, but also it can generate more accurate and realistic conditions close to the practical conditions by specifying a smaller forbidden region [28]. The forbidden region of the three mentioned criteria for the same values of the GM (6 dB) and PM (60°) is shown in Fig. 7. In this figure, it can be seen that the ESAC criterion has the smallest forbidden region, which means the ESAC criterion has the lowest conservativeness in the stability analysis and design of cascaded power converter among all criteria.

The ESAC criterion can be used to derive load impedance design specifications for a given source output impedance, Z_o. Stability analysis can be conducted in terms of the three-dimensional admittance space where frequency, phase and magnitude are the three axes. The ESAC criterion based stability analysis toolbox is available on Purdue University website [29], by using the ESAC criterion to evaluate the DC bus voltage stability of the cascaded power converter system, the voltage of the cascaded DC bus will be unstable if the input admittance of load converter intersects its forbidden region for a given source admittance.

The Bode diagram of (5) and (17) are plotted in Fig. 8. In this figure, it can be seen that the resonant peak of Z_o intersects Z_{in} around 90 Hz, which is lower than the crossover frequency, 1.5kHz of voltage control loop that is shown in Fig.6. Therefore, the DC bus voltage is likely to be unstable [30]. Furthermore, as shown in this figure, the phase of Z_{in} is very close to -180° at the frequencies lower than 100Hz, which indicates the PSFB converter behaves like a CPL in this frequency region. The corresponding analysis results obtained by using the ESAC criterion toolbox are displayed in Fig. 9. As it also can be seen in Fig. 9, the DC bus voltage of the cascaded system is not stable because Y_{in} intersects its forbidden region.

D. VIRTUAL RESISTOR BASED CONTROL STRATEGY

According to (11) and (12), the damping ratio can be increased by introducing a parallel R_v to cancel the negative

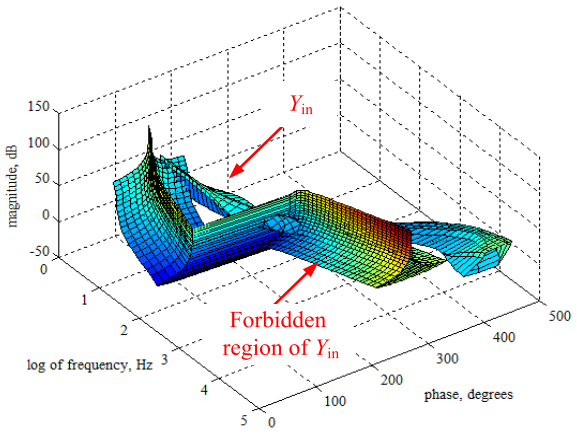

FIGURE 9. The load side input admittance (Y_{in}) and its ESAC forbidden region without the IBVC.

impact of R_0, thereby, the capability of the power converter to resist the constant power load can be enhanced. Thus, if the IBVC shown in Fig. 1 can present the characteristics of a positive resistor through special control strategy, the stability of the DC bus voltage can be improved.

In Fig. 1, the two switches of leg A together with L_b and C_b are utilized to form a bidirectional Buck/Boost converter based integrated bus voltage conditioner, the decoupling operation of the PSFB and IBVC can be obtained, if the conditions defined by (1) and (3) are held (assuming $d_1 = d_2 = d$), therefore, the control system design of the IBVC and PSFB can be considered separately. From this point of view, the whole control block diagram of the cascaded power converter system is presented in Fig. 10. The modeling of the IBVC and the relevant transfer functions are given in [31].

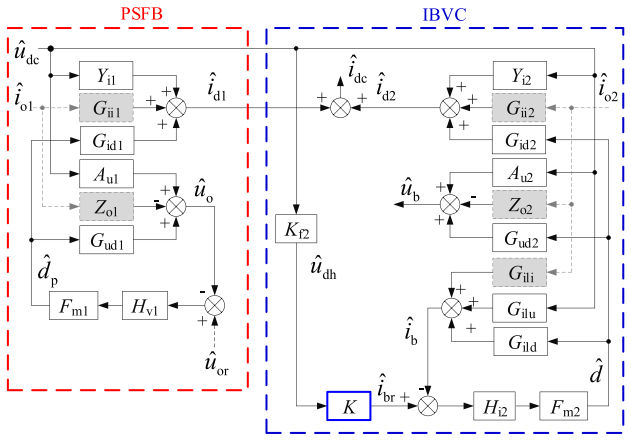

FIGURE 10. The control block diagram of the whole power converter system.

The G-parameter based small signal control block diagram of IBVC is shown in the right side of this figure, Y_{i2} is the open loop input admittance, G_{ii2} is the transfer function of $\hat{i}_{o2}$-to-$\hat{i}_{d2}$, G_{id2} is the transfer function of $\hat{d}$-to-$\hat{i}_{d2}$, A_{u2} is the transfer function of $\hat{u}_{dc}$-to-$\hat{u}_b$, Z_{o2} is the open loop output impedance, G_{ud2} is the transfer function of $\hat{d}$-to-$\hat{u}_b$, G_{ili} is the transfer function of $\hat{i}_{o2}$-to-$\hat{i}_b$, G_{ilu} is the transfer function of $\hat{u}_{dc}$-to-$\hat{i}_b$, G_{ild} is the transfer function of $\hat{d}$-to-$\hat{i}_b$, F_{m2} is the transfer function of the modulator and H_{i2} is the current controller of IBVC to make i_b track the fluctuation of u_{dc}.

In Fig. 10, a high pass filter K_{f2} is employed to extract the fluctuation component, $\hat{u}_{dh} = K_{f2}\hat{u}_{dc}$ of the DC bus voltage. As seen in Fig. 1, the voltage at point A is about half of the DC bus voltage. Therefore, (18) can be deduced according to the power conservation law.

$$\frac{\hat{u}_{dh}}{2} \cdot \hat{i}_b = \frac{\hat{u}_{dh}^2}{R_v} \tag{18}$$

Then, the disturbance of the inductor current reference signal $\hat{i}_{br}$ is given by (19).

$$\hat{i}_{br} = \frac{2\hat{u}_{dh}}{R_v} = K\hat{u}_{dh}, (K = \frac{2}{R_v}) \tag{19}$$

In this case, the virtual resistor based control strategy can be implemented by controlling the i_b phase change according to the u_{dc} fluctuation, by which the dynamic changes of i_b and u_{dc} can be kept approximately in phase. Theoretically, a larger value of K in Fig. 10 is beneficial to obtain higher damping, however, it might cause an excessive duty cycle change that may deteriorate the condition given by (1) and results in interaction between the output voltage control and DC bus voltage stabilization control. In practice, first the value of K is calculated using $K = 2/R_v$, and then it can be appropriately modified according to practical requirements and test results.

As mentioned before, if S_1 on leg A is taken as the main switch (the duty cycle, d is used as a control variable), then, the IBVC can be operated in the Buck mode, and the small signal transfer function of $\hat{d}$-to-$\hat{i}_b$ shown in (20) can be used to design the corresponding control system of IBVC.

$$G_{ild}(s) = \frac{\hat{i}_b(s)}{\hat{d}(s)} = \frac{U_{d0}C_b s}{L_b C_b s^2 + r_b C_b s + 1} \tag{20}$$

The current controller H_{i2} is selected as (21)

$$H_{i2} = \frac{K_c(s/\omega_z + 1)}{(s/\omega_p + 1)} \tag{21}$$

In (21), K_c denotes the controller gain, and ω_z and ω_p are the angular frequencies of the zero and pole respectively. Here, ω_p is designed to reduce the phase of the corrected open loop system around the resonance frequency ω_n (it is about 628 rad/s in this work) of DC link. The ω_z is utilized to guarantee the corrected open loop system has a sufficient phase margin at the crossover frequency. The zero phase of the corrected current closed loop around ω_n can be obtained by properly adjusting the values of ω_z, ω_p and K_c respectively. In this way, i_b can be controlled to be approximately in phase with the fluctuation of u_{dc}, and the proposed virtual resistor based control strategy can be effectively realized. The closed

loop transfer function of the corrected IBVC control system can be expressed as in (22).

$$G_{\mathrm{cl}}(s)=\frac{G_{\mathrm{ild}}H_{\mathrm{i2}}F_{\mathrm{m2}}}{1+G_{\mathrm{ild}}H_{\mathrm{i2}}F_{\mathrm{m2}}} \tag{22}$$

By substituting (20) and (21) into (22), the phase of the IBVC current closed loop control system can be formulated in (23).

$$\theta(\omega)=\text{-arctg}(\frac{\omega_{\mathrm{z}}}{\omega})\text{-arctg}(\frac{c_1}{c_2}) \tag{23}$$

where

$$\begin{cases} c_1=a_1\omega+b_1K_{\mathrm{c}}\omega+\omega/\omega_{\mathrm{p}}-a_2\omega^3/\omega_{\mathrm{p}} \\ c_2=1-\left(a_2+a_1/\omega_{\mathrm{p}}+b_1K_{\mathrm{c}}/\omega_{\mathrm{z}}\right)\omega^2 \\ a_1=r_{\mathrm{b}}C_{\mathrm{b}} \\ a_2=L_{\mathrm{b}}C_{\mathrm{b}} \\ b_1=U_{\mathrm{d0}}C_{\mathrm{b}}F_{\mathrm{m2}} \end{cases} \tag{24}$$

In design process, the values of the controller parameters, ω_{z}, ω_{p} and K_{c} can be roughly designed first according to desired crossover frequency and stability requirements using frequency design method, then the value of one parameter (such as K_{c}) can be fixed as its designed value, while the other two parameters (for example, ω_{z} and ω_{p}) are considered as variables. The three-dimensional plot can be used to find more proper controller parameters. Fig. 11 shows an example of the mentioned method.

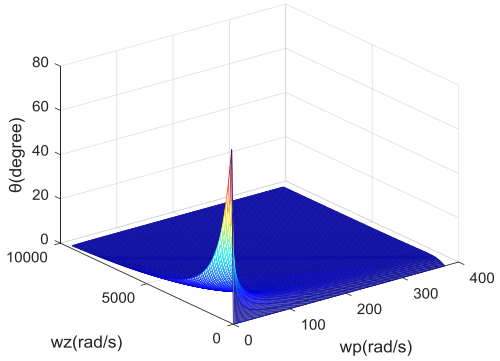

FIGURE 11. Three-dimensional phase of IBVC current closed loop control system.

In Fig. 11, K_{c} is fixed as a constant and it can be seen that the phase of the IBVC current closed loop control system can be approximated to zero with the wide changes of ω_{z} and ω_{p}. By selecting proper values of ω_{z}, ω_{p} and K_{c} ($\omega_{\mathrm{z}}=60$rad/s, $\omega_{\mathrm{p}}=500$rad/s and $K_{\mathrm{c}}=3500$ are used in this case), the current control loop with and without correction is shown in Fig. 12. In this figure, it can be seen that the crossover frequency of the corrected open loop is about 1.65 kHz, the gain margin is about 16 dB, and the phase margin is about 61°. As desired, the phase of the closed loop control system tends to be zero near 100 Hz, that means the current of IBVC, i_{b}, can be controlled to well track the fluctuation of u_{dc}, therefore, the IBVC behaves like a virtual resistor.

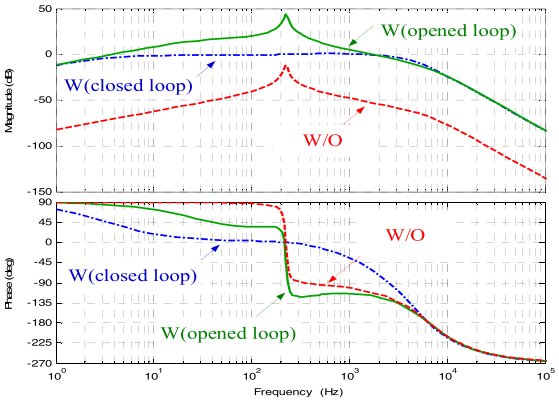

FIGURE 12. The Bode diagram of the IBVC current control loop with and without correction.

According to Fig. 10, (25) can be obtained.

$$\begin{cases} \hat{i}_{\mathrm{d2}}=\hat{u}_{\mathrm{dc}}Y_{\mathrm{i2}}+\hat{d}G_{\mathrm{id2}}+\hat{i}_{\mathrm{o2}}G_{\mathrm{i2}} \\ \hat{i}_{\mathrm{b}}=\hat{u}_{\mathrm{dc}}G_{\mathrm{ilu}}+\hat{d}G_{\mathrm{ild}}+\hat{i}_{\mathrm{o2}}G_{\mathrm{ili}} \\ \hat{d}=\left(\hat{u}_{\mathrm{dc}}KK_{\mathrm{f2}}-\hat{i}_{\mathrm{b}}\right)H_{\mathrm{i2}}F_{\mathrm{m2}} \end{cases} \tag{25}$$

By setting $\hat{i}_{\mathrm{o2}}=0$, the IBVC input admittance can be derived from (25), and it is given by (26).

$$Y_{\mathrm{v}}=\frac{\hat{i}_{\mathrm{d2}}}{\hat{u}_{\mathrm{dc}}}=Y_{\mathrm{i2}}+\frac{\left(KK_{\mathrm{f2}}-G_{\mathrm{ilu}}\right)H_{\mathrm{i2}}F_{\mathrm{m2}}G_{\mathrm{id2}}}{1+G_{\mathrm{ild}}H_{\mathrm{i2}}F_{\mathrm{m2}}} \tag{26}$$

Combining (17) with (26), the load side input admittance can be calculated as (27).

$$Y_{\mathrm{in1}}=Y_{\mathrm{in}}+Y_{\mathrm{v}} \tag{27}$$

In Fig. 1, the value of DC link capacitor, C_{dc} can be roughly selected according to (28) in general application conditions.

$$C_{dc}\geq\frac{P_{s0}}{\left(u_{\mathrm{dcmax}}^2-u_{\mathrm{dcmin}}^2\right)f_r} \tag{28}$$

where u_{dcmax} and u_{dcmin} are the maximum and minimum value of rectifier dc voltage respectively, $u_{\mathrm{dcmin}}=(0.9\sim0.95)u_{\mathrm{dcmax}}$, f_{r} is 300Hz for three-phase diode rectifier.

Considering the parameters given in Table 1 and equation (12), the maximum CPL can be supported by the source converter with $C_{\mathrm{dc}}=900\mu$F (this value is obtained assuming $P_{\mathrm{s0}}=1$kW, $u_{\mathrm{dcmax}}=1.05u_{\mathrm{dc}}$ and $u_{\mathrm{dcmin}}=0.9u_{\mathrm{dcmax}}$in general application condition, and it should be higher than 1700μF if $u_{\mathrm{dcmin}}=0.95u_{\mathrm{dcmax}}$ is required) is $P_{\mathrm{max}}\approx$280W under the assumption of ideal constant power load. The original load resistor is $R_{\mathrm{L}}=8\ \Omega$, the corresponding power is $P_1=200$W which is less than P_{max}. The control system is stable under these conditions, while the DC bus voltage will become unstable if R_{L} is changed to 1.7 Ω, then $P_2\approx$940W which is greater than P_{max} where the power difference is $P_{\Delta}=P_2$-$P_{\mathrm{max}}=660$ W. In this condition, the value of DC bus capacitor, C_{dc} should be increased to 3100μF according to (12) without R_{v} ($R_{\mathrm{v}}=\infty$). Suppose P_{Δ} can

be actively compensated by the virtual resistor based IBVC control strategy under ideal constant power load conditions. R_V can be derived from (12) and should be less than 28 Ω, and K should be larger than $2/R_v$ ≈0.071. However, since most of the load converters do not really act like an ideal constant power load in actual applications, the value of K can be reasonably lower than its designed value determined according to the requirements or the practical test results.

The load side input admittance, Y_{in1} and its ESAC forbidden region using the proposed IBVC with $K = 0.07$ are shown in Fig. 13. In Fig. 13, it can be seen that Y_{in1} does not intersect its forbidden region, which indicates the stability improvement of the DC bus voltage.

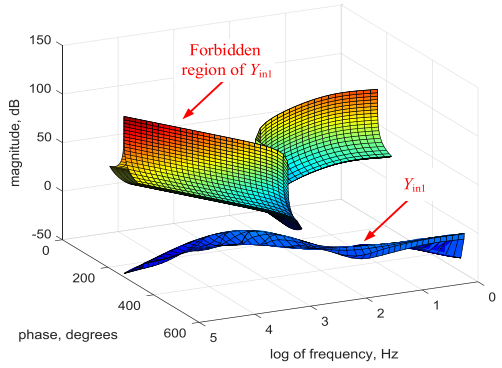

FIGURE 13. Y_{in1} and its ESAC forbidden region with the IBVC.

III. SIMULATION AND EXPERIMENTAL VALIDATION

A. SIMULATION VALIDATION AND ANALYSIS

To verify the effectiveness of the proposed integrated bus voltage conditioner in the DC bus voltage stabilization, a simulation model of the proposed system was developed in MATLAB Simulink. The simulation model parameters are listed in Table 1.

The simulation results without any compensation are shown in Fig. 14, where it can be seen that when the load resistor R_L suddenly changed from 8 Ω to 1.7 Ω at 0.2 s, there was a significant voltage oscillation in the DC bus voltage due to the CPL characteristic of the PSFB converter with a relatively high control bandwidth, and there was an obvious voltage fluctuation in the output voltage as well. By increasing the value of the DC bus electrolytic capacitor, C_{dc} from 2000 μF to 3400 μF, the voltage oscillation of u_{dc} associated with the same load change is reduced significantly as shown in Fig. 15. The fluctuation of u_{dc} is gradually damped in about 0.25 s, and the output voltage, u_o is much better controlled.

The simulation results obtained by using the proposed virtual resistor based control strategy under the same load change condition are presented in Fig. 16. In this case, K is set to 0.08. It can be seen that the fluctuations of u_{dc} and u_o decrease and disappear in about 0.2 s. Though the original magnitude of u_{dc} fluctuation is higher than that in Fig. 15, the transient recovery time is reduced significantly.

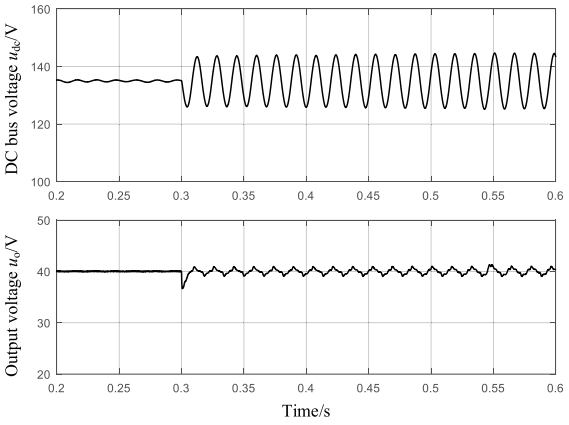

FIGURE 14. Simulation results without the IBVC compensation.

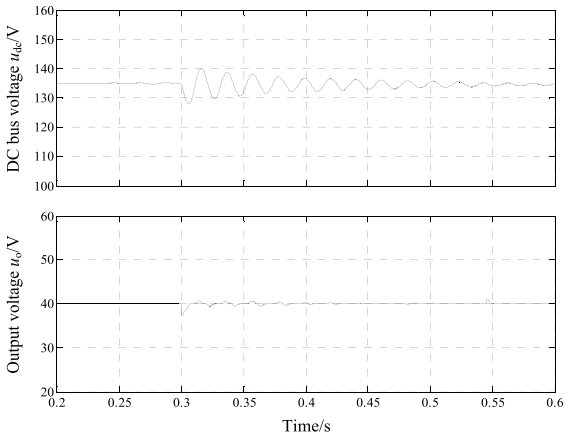

FIGURE 15. Simulation results with 3400μF DC bus electrolytic capacitor.

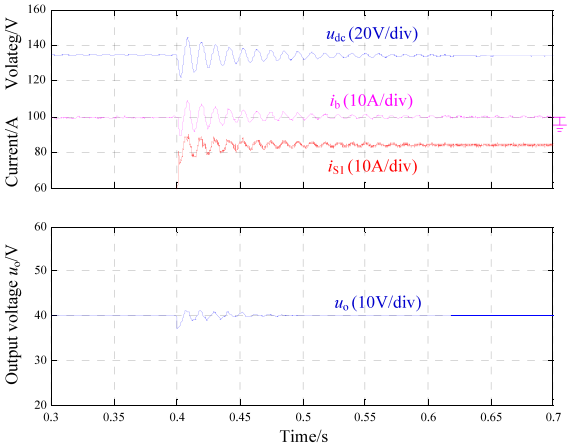

FIGURE 16. Simulation results of the proposed IBVC method.

In addition, the fluctuations of u_{dc}, i_b and i_{S1} (the current that flows through S_1) are almost in phase which indicates the IBVC behaves like a resistor as expected. It can be concluded that the proposed method is effective in voltage oscillation rejection.

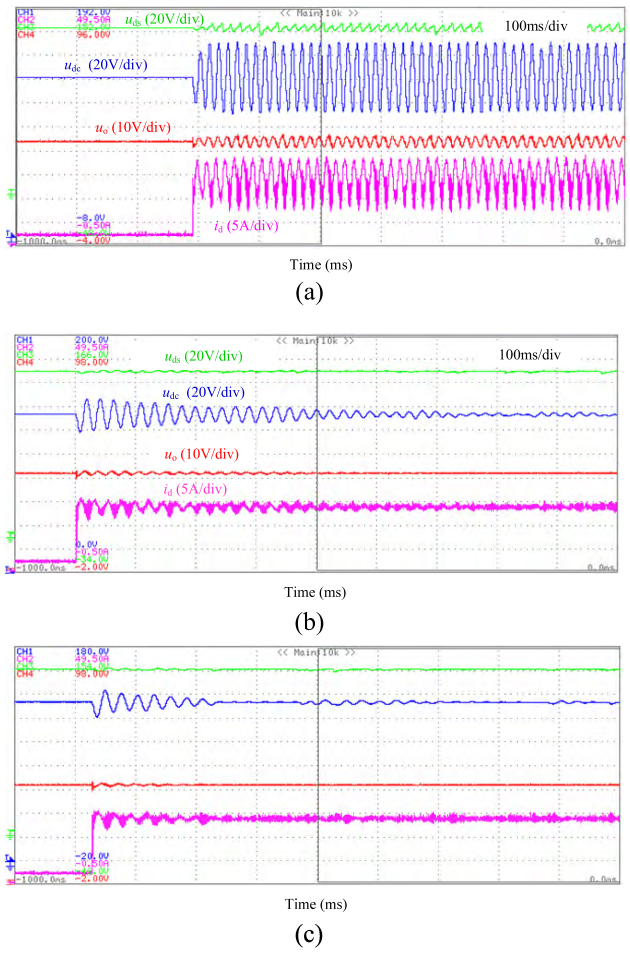

FIGURE 17. Experiment results with different values of C_{dc} (a) 2200 μF, (b) 3400 μF, (c) 4700 μF.

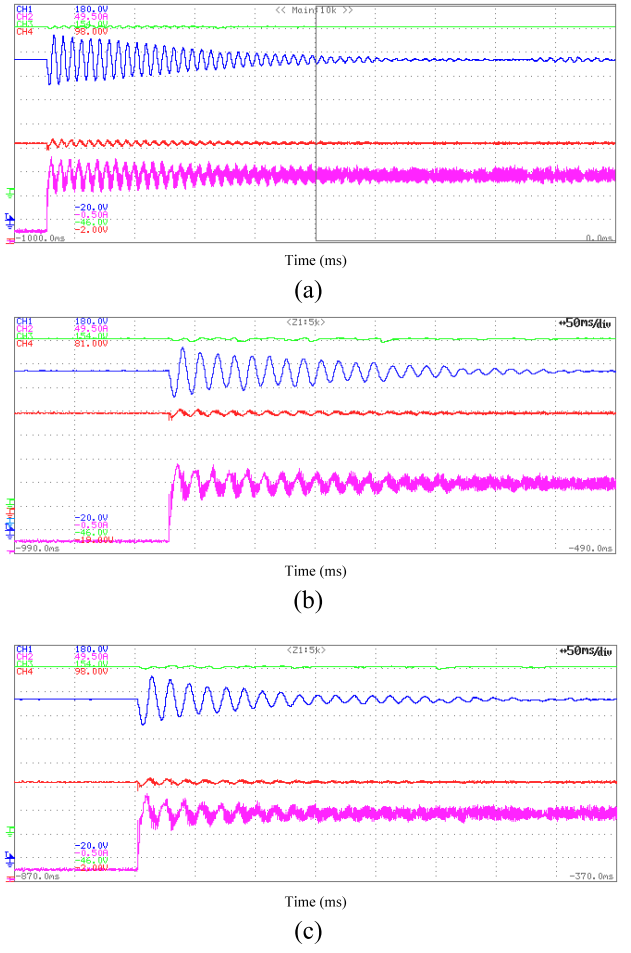

FIGURE 18. Experiment results of the proposed virtual resistor- based control method with (a) $K = 0.065$, (b) $K = 0.072$, (c) $K = 0.08$.

B. EXPERIMENTAL RESULTS AND ANALYSIS

A hardware circuit is developed to validate the theoretical analysis and simulation results. The power circuit is composed of a three-phase diode rectifier and a PSFB converter with the proposed LC branch. The three-phase rectifier together with an adjustable autotransformer can be modeled by a DC voltage source (as u_{ds} shown in Fig. 3), the equivalent u_{ds}, R_{dc} and L_{dc} equations can be found in [6]. The parameters used in the simulation model and experimental test are almost identical. A 32-bit ARM Cortex-M4 core microprocessor was used for experimental tests to implement the proposed control strategy. The experimental results are shown in Fig. 17 and Fig. 18.

Fig. 17 shows the experimental results without using the proposed active method. In Fig. 17(a), the value of C_{dc} is 2200μF, and a large DC bus voltage oscillation is obvious when the load power is suddenly changed from about 200 W to 940 W. In this case, the voltage oscillations could not be attenuated as the DC bus capacitance is not large enough to guarantee the stability of the DC bus voltage. The DC bus voltage oscillation also deteriorates the control performance of the output voltage of PSFB converter that resulted in large output voltage fluctuations in u_o. Fig. 17(b) shows the experimental results when a 3400 μF DC bus capacitor was used. Compared to the results presented in Fig. 17 (a), the DC bus voltage oscillation can be eventually damped in about 0.6s. When the value of C_{dc} is further increased to 4700 μF, as presented in Fig. 17 (c), the DC bus voltage oscillation can be further attenuated.

The experimental results obtained by implementing the proposed virtual resistor based control strategy is shown in Fig. 18. As it can be seen in this figure, the proposed IBVC method can effectively stabilize the DC bus voltage of tightly-controlled load power converter. In addition, as shown in Fig. 18, it significantly improves the stability and dynamic performance of the DC bus voltage, it can be noticed that the transient recovery times of u_{dc} in Fig. 18 (a) to (c) are decreased when larger values of K are adopted using the developed virtual resistor method.

IV. CONCLUSION

A virtual resistor based integrated bus voltage conditioner was developed through multiplexed utilization of the converter switches to stabilize the front end DC bus voltage in

a phase shifted full bridge converter. The main advantages of the proposed conditioner include improving converter power density, reducing overall converter cost, and decreasing the size of DC bus capacitor. The mathematical models and control-oriented analysis are presented to develop a proper control strategy. The obtained simulation and experimental results demonstrate that the proposed control strategy is effective in stabilizing the DC bus voltage.

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