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A Novel Method Using a Rectangular Groove to Reduce Far-End Crosstalk in Microstrip Lines Covered With a Dielectric Layer

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ABSTRACT Microstrip signal lines covered with a dielectric layer are used to reduce far-end crosstalk (FEXT) noise from adjacent lines. When minimizing FEXT noise, the permittivity of the dielectric layer should be higher than that of the substrate. When the permittivity is close to that of the substrate, the thickness of the covering dielectric layer is much larger than that of the substrate. We here present a novel means of reducing FEXT noise in microstrip lines covered with a dielectric layer using a rectangular (R)-shaped groove. When an R-shaped groove is created in the covering dielectric layer or substrate of the microstrip lines, FEXT noise is suppressed in the absence of the above conditions. To analyze the underlying mechanism, we studied the circuit parameters and electric field distribution in the microstrip lines. To confirm the improvements afforded by our methods, we compared simulated and measured data of our new structures to those of other structures.

INDEX TERMS Microstrip lines covered with a dielectric layer, far-end crosstalk noise, rectangular groove.

I. INTRODUCTION

Recently, the use of digital systems has greatly improved the physical compactness of integrated circuits (ICs) and data handling rates. Given these developments, problems associated with electromagnetic interference (EMI) have grown; these include degradation of signal integrity (SI) by crosstalk noise between signal lines inducing ground bounce, delay, and jitter [1]–[4]. Therefore, modeling and analysis of crosstalk in ICs have become more important and are currently attracting much attention [5]–[8].

In general, crosstalk noise is of two types: near-end crosstalk (NEXT) noise and far-end crosstalk (FEXT) noise. In multiple microstrip lines, FEXT noise is predominantly attributable to the inhomogeneous structure of such lines; the capacitive coupling k_C is smaller than the inductive coupling k_L . To reduce FEXT noise, various techniques have been reviewed in [9]–[19].

Placing a guard trace between the microstrip lines was used to reduce FEXT noise [9]. To enhance the performance of noise suppression, the method of a serpentine guard trace was introduced [10], but some noise remained and extra spaces between the lines were required. To enhance the performance and reduce extra spaces between the lines, stubalternating [11] and serpentine [12] microstrip lines have been used. FEXT noise was indeed reduced, but those traceshaping methods have limitations in PCB fabrication as minimum separation between the lines should be very small periodically.

In [13]–[15], FEXT noise was reduced by placing a guard trace with via holes connected to ground between the signal lines. However, a ringing noise emanated from the via holes, and signal distortions were evident at specific frequencies. To minimize such distortions, the distance between the via holes was decreased and the number of via holes thus increased. However, this technique imposed restrictions on printed circuit board (PCB) backside routing. In [16], not only FEXT noise, but also NEXT noise was reduced by placing decoupling capacitors between the lines. However, a number of decoupling capacitors should be used to obtain good performance with respect to insertion and return losses.

Signal lines have been covered with dielectric layers to improve performance [17]–[19]. To reduce FEXT noise induced by structural inhomogeneity, a dielectric layer was

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placed over multiple microstrip lines [17], [18]. This reduced the ringing noise associated with the via holes of a guard trace [19]. However, certain requirements must be met when minimizing FEXT noise. The covering dielectric layer must be much thicker than the substrate when the permittivity of the layer is close to that of the substrate. To reduce the thickness of the dielectric layer, the permittivity thereof should be higher than that of the substrate; however, this increases the complexity and cost of PCB fabrication [20].

Here, we describe a novel layer-shaping method for reducing FEXT noise; this overcomes problems related to the thickness and permittivity of the covering dielectric layer [17]–[19], and can also be an alternative to the trace-shaping methods [11], [12]. Our concept is as follows: when a rectangular (R) groove is created in the covering dielectric layer or the dielectric substrate of the microstrip lines, that groove becomes filled with air ($\varepsilon_r = 1$); by this physical change, the thickness of the upper dielectric layer to minimize FEXT noise can be reduced even when the permittivity of the covering dielectric layer is equal to that of the substrate.

The paper is organized as follows: in Section II, it is shown that how the thickness of the dielectric layer covering microstrip lines affects circuit parameters and reduces FEXT noise. In addition, problems associated with PCB fabrication are discussed. In Section III, the ways to reduce FEXT noise using the R-shaped groove are presented. The mechanism is explained via analysis of electric (E)-field distribution and the circuit parameters of the coupled lines. Section IV shows the simulated and measured results of the method compared to other methods; we verified the reduction in FEXT noise. Section V contains the conclusions.

II. ADJACENT MICROSTRIP LINES COVERED WITH A DIELECTRIC LAYER

Figure 1(a) shows adjacent signal lines termed aggressor and victim lines. The two signal lines can be modeled as coupled transmission lines expressed as a distributed equivalent circuit, where C_s and C_m are the self and mutual capacitances, respectively, and L_s and L_m are the self and mutual inductances, respectively, as shown in Fig. 1(b). For coupled lines, the capacitance matrix C and the inductance matrix L can be expressed as:

$$\boldsymbol{C} = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = \begin{bmatrix} C_t & C_m \\ C_m & C_t \end{bmatrix}, \quad (1)$$

$$\boldsymbol{L} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = \begin{bmatrix} L_s & L_m \\ L_m & L_s \end{bmatrix}.$$
 (2)

where $C_t = C_s + C_m$. From the matrix parameters, the coupling coefficients k_C and k_L can be defined as:

$$k_C = \frac{C_{12}}{C_{11}}, \quad k_L = \frac{L_{12}}{L_{11}}.$$
 (3)

When an input voltage V_g is applied to the aggressor line (port 1), the FEXT voltage at the victim line (port 4), V_{FEXT} ,



FIGURE 1. Adjacent signal lines (aggressor and victim lines): (a) The design scheme. (b) The equivalent distributed circuit model.

can be expressed as follows [21]:

$$V_{FEXT}(t) = \frac{1}{2}(k_C - k_L) \cdot T_D \cdot \frac{dV_g(t - T_D)}{dt},$$
 (4)

where

ı

$$T_D = l\sqrt{L_{11}C_{11}}$$
(5)

is the propagation time through the transmission line and l is the length of the line. For signal lines based on coupled microstrips, k_C is smaller than the k_L of the inhomogeneous structure; V_{FEXT} is induced in the victim line when V_g is applied to the aggressor line. The best way to minimize V_{FEXT} in the aggressor line is to render k_C - k_L equal to zero.



FIGURE 2. Design of adjacent microstrip lines with covering dielectric layer: (a) three-dimensional (3-D) view; (b) cross-section.

Figure 2 shows adjacent microstrip lines covered with dielectric layer to reduce V_{FEXT} [17]. The dimensions of the microstrip lines are: width $w_0 = 1.5$ mm, line spacing s = 4.5 mm, thickness of lower substrate (FR4 epoxy, $\varepsilon_{r1} = 4.4$) $h_1 = 0.8$ mm, and thickness of upper dielectric layer (ε_{r2}) h_2 . Figure 3 shows the extracted values of C_t and C_m with respect to the height ratio h_2/h_1 for $\varepsilon_{r1} = \varepsilon_{r2} = 4.4$, where C_t , C_m , L_s and L_m were extracted from the cross-section of the structures using ANSOFT Q3D software [22]. C_t and C_m increase with increasing h_2/h_1 , but the slope of C_m is larger than that of C_t with respect to h_2/h_1 . These results are explained by the



FIGURE 3. The extracted values of C_t and C_m for coupled lines covered with a dielectric layer, with respect to h_2/h_1 .



FIGURE 4. The differential-mode E-field distributions of microstrip lines (a) without a covering dielectric layer; (b) with a covering dielectric layer.

E-field distributions. Figure 4 shows the E-field distributions of microstrip lines with and without covering dielectric layer for an h_2/h_1 ratio of 3.3 when differential-mode voltages were applied to the coupled signal lines to generate an E-field between the lines. All field distributions in this paper are shown at the same scale of E-field intensity. The E-fields of Fig. 4(b) (those between the signal lines in the upper covered layer) are more strongly distributed than those of Fig. 4(a). When the E-field intensity increases between the lines, the increase ratio of C_m is more than that of C_t . C_t increases from 120.94 pF to 158.09 pF and C_m increases 0.5718 pF to 3.77 pF with a covering dielectric layer. The extracted capacitance and inductance matrices of Fig. 4(a) are:

$$C = \begin{bmatrix} 120.94 & 0.5718\\ 0.5718 & 120.94 \end{bmatrix} \text{ pF/m},$$
$$L = \begin{bmatrix} 305.13 & 7.35\\ 7.35 & 305.13 \end{bmatrix} \text{ nH/m},$$

and the extracted matrices of Fig. 4(b) are:

$$C = \begin{bmatrix} 158.09 & 3.77 \\ 3.77 & 158.09 \end{bmatrix} \text{ pF/m},$$
$$L = \begin{bmatrix} 305.13 & 7.35 \\ 7.35 & 305.13 \end{bmatrix} \text{ nH/m}.$$

Thus, k_C increases from 0.00473 to 0.0243 when a covering dielectric layer is added, and $k_C - k_L$ is almost zero when $h_2/h_1 = 3.3$ because $k_L = 0.0241$ for both cases.

Figure 5 shows the values of $k_C \cdot k_L$ with respect to the height ratio h_2/h_1 for various ε_{r2} values. When $\varepsilon_{r2} = 3$, the $k_C \cdot k_L$ values are much lower than zero for all h_2/h_1 because $\varepsilon_{r1} > \varepsilon_{r2}$. When $\varepsilon_{r2} = 4.4$, the $k_C \cdot k_L$ values increase for all h_2/h_1 ; therefore, $k_C \cdot k_L$ is zero when $h_2/h_1 = 3.3$.



FIGURE 5. Values of $k_c - k_L$ with respect to h_2/h_1 for various ε_{r2} .

Similarly, the values of h_2/h_1 rendering $k_C \cdot k_L$ zero are 1.9 and 1.3 for $\varepsilon_{r2} = 6$ and 8, respectively. This means that the height of the upper covering layer should be much greater than that of the lower substrate to minimize V_{FEXT} when ε_{r2} is close to ε_{r1} . To reduce the required height, ε_{r2} should be greater than ε_{r1} ; however, the use of dielectric materials with higher permittivity than FR4 epoxy increases the complexity and cost of PCB fabrication [20].

III. FEXT NOISE REDUCTION EFFECTS USING AN R-SHAPED GROOVE

A. PLACEMENT OF AN R-SHAPED GROOVE IN THE LOWER SUBSTRATE

Creation of an R-shaped groove in the substrates of microstrip lines changes the E-field distributions because the grooves become filled with air ($\varepsilon_r = 1$). Thus, the thickness of the upper covering layer used to minimize FEXT noise can be reduced when $\varepsilon_{r1} = \varepsilon_{r2}$. A groove was created in the substrate of the microstrip lines $(w_0/h_1 = 1.875, s/h_1 =$ 5.625, $h_2/h_1 = 1.5$). Figure 6 shows the lines with a covering dielectric layer and a groove between the signal lines of the lower substrate (ε_{r1}). The width and height of the groove are shown as w_L and h_L , respectively. Figure 7 shows the E-field distributions of microstrip coupled lines without and with a grooved lower substrate at $w_L/s = 0.85$ and $h_L/h_1 = 0.5$. Compared to the field distribution of Fig. 7(a), discontinuities are evident at the boundaries of the R-shaped groove [Fig. 7(b)]. The discontinuities are attributable to the fact that the groove is filled with air, and the field intensity in the groove are thus larger than that outside the groove. The signal lines and lower substrate with an R-shaped groove



FIGURE 6. Design of adjacent microstrip lines with rectangular (R)-shaped grooves in the lower substrate: (a) 3-D view; (b) cross-section.



FIGURE 7. Differential-mode E-field distributions of coupled microstrip lines (a) without an R-shaped groove and (b) with an R-shaped groove in the lower substrate.

resemble a dielectric slab capacitor composed of a dielectric layer (ε_{r1}) and air. The capacitances generated thus decrease compared to those when the groove is absent; the C_s and C_m values of the lower substrate are decreased by the groove. Also, the groove affects other aspects of the field distribution, as shown in Fig. 7 (b); the E-fields connecting the coupled lines to the upper dielectric layer are more strongly distributed than when the groove is absent. The C_m of the upper covering dielectric layer is increased by the strongly distributed E-field. The extracted capacitance matrix of Fig. 7(a) is

$$C = \begin{bmatrix} 152.49 & 2.19\\ 2.19 & 152.49 \end{bmatrix} \text{pF/m}$$

and the extracted capacitance matrix of Fig. 7(b) is:

$$C = \begin{bmatrix} 146.78 & 3.49 \\ 3.49 & 146.78 \end{bmatrix} \text{pF/m},$$

 C_t thus decreased from 152.49 to 146.78 pF/m and C_m increased from 2.19 to 3.49 pF/m. The increase in C_m of the upper covering dielectric layer was more marked than the decrease in C_m generated by the lower substrate with the R-shaped groove; C_t decreases and C_m increases when the groove is present. The C_t and C_m values with respect to w_L/s and h_L/h_1 are presented in Fig. 8. As shown in Fig. 8(a), C_t decreased with increases of w_L/s and h_L/h_1 , and was minimal when $w_L/s = 1$ and $h_L/h_1 = 0.5$. On the other hand, C_m increased with increased w_L/s and h_L/h_1 ; C_m was maximal when $w_L/s = 1$ and $h_L/h_1 = 0.5$ [Fig. 8(b)]. Therefore, k_C was maximal when $w_L/s = 1$ and $h_L/h_1 = 0.5$, and h_C can thus be controlled efficiently by varying the parameters of the R-shaped groove.

By placing an R-shaped groove in the lower substrate, the optimal parameters for minimizing FEXT noise, w_L/s and h_L/h_1 , can be determined. Figure 9 shows the k_C-k_L values with respect to w_L/s and h_L/h_1 ; we present both two-dimensional (2-D) and three-dimensional (3-D) graphs. These show that values of w_L/s and h_L/h_1 allow k_C-k_L to be near-zero; the optimized parameters are $w_L/s = 0.85$ and $h_L/h_1 = 0.5$ in the present configuration. Thus, h_2/h_1 can be reduced from 3.3 to 1.5 by placing an R-shaped groove in the lower substrate to minimize FEXT noise.

B. TRANSIENT ANALYSIS OF ADJACENT MICROSTRIP LINES WITH R-SHAPED GROOVES IN THE LOWER SUBSTRATE

In the transient simulations, the transmission line length of all tests was set to 10 cm (l = 10 cm) using the ANSOFT HFSS full-wave simulator. In the time domain, V_{FEXT} values were



FIGURE 8. The extracted values of C_t and C_m for coupled lines when R-shaped grooves were placed in the lower substrate, with respect to w_L/s and h_L/h_1 : (a) C_t , (b) C_m .



FIGURE 9. The extracted values of $k_c - k_L$ with respect to w_L/s and h_L/h_1 : (a) two-dimensional (2-D) graph, (b) 3-D graph.

simulated by the area of the R-shaped groove when a 1-V step signal was applied to the input port of the aggressor line (port 1) with a rise time $t_r = 50$ ps. The simulated V_{FEXT} values at the output port of the victim line (port 4) are shown in Fig. 10(a). From (2), the peak V_{FEXT} voltage can be expressed as follows [19]:

$$V_{peak} = \frac{1}{2}(k_C - k_L) \cdot T_D \cdot \frac{V_{g, max}}{t_r},\tag{6}$$



FIGURE 10. Simulated results for adjacent microstrip lines when R-shaped grooves were placed in the lower substrate, by the groove area. (a) V_{FEXT}, (b) S₄₁.

TABLE 1. Comparison between calculated and simulated V_{peak} values with respect to the area of the R-shaped groove in the lower substrate.

	V_{peak} derived using Eq. (6)	V _{peak} derived using EM Sim.
Without R-groove	-0.066 V	-0.060 V
$w_L/s = 0.4, h_L/h_I = 0.2$	-0.055 V	-0.051 V
$w_L/s = 0.55, h_L/h_I = 0.3$	-0.043 V	-0.043 V
$w_L/s = 0.7, h_L/h_I = 0.4$	-0.025 V	-0.031 V
$w_L/s = 0.85, h_L/h_I = 0.5$	-0.002 V	-0.02 V

for $T_{D,e}$ - $T_{D,o} < t_r$ when the even- and odd-mode propagation times $T_{D,e}$ and $T_{D,o}$ are:

$$T_{D,e} = l\sqrt{(L_{11} + L_{12})(C_{11} - C_{12})},$$

$$T_{D,o} = l\sqrt{(L_{11} - L_{12})(C_{11} + C_{12})}.$$
(7)

Therefore, V_{peak} can be obtained from the extracted circuit parameters using (6). The simulated and calculated V_{peak} values are listed in Table 1. V_{peak} decreased with an increased area of the R-shaped groove and was minimal when $w_L/s = 0.85$ and $h_L/h_1 = 0.5$; thus, good agreement was evident between the calculated and simulated V_{peak} data.

In the frequency domain, the S-parameters from the aggressor line (port 1) to the victim line (port 4), S₄₁, were simulated by the area of the R-shaped groove. As shown in Fig. 10(b), S₄₁ decreased with increased groove area over the frequency band of interest and was minimal when $w_L/s = 0.85$ and $h_L/h_1 = 0.5$, reflecting the time-domain transient analysis of Fig. 10(a).

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C. PLACEMENT OF AN R-SHAPED GROOVE IN THE UPPER COVERING DIELECTRIC LAYER

FEXT noise can also be reduced by placing an R-shaped structure in the upper covering dielectric layer rather than the substrate. Figure 11 shows adjacent microstrip lines with a covering dielectric layer and an R-shaped groove in the upper layer. The groove width and height are denoted w_u and h_u , respectively. Figure 12 shows the E-field distributions of microstrip coupled lines with and without the groove in the upper layer; the relevant ratios are $w_u/s = 0.85$ and $h_u/h_1 = 0.3$. As shown in Fig. 12(b), the field intensities inside the R-shaped groove are larger than those outside the groove because the groove is filled with air. The signal lines and upper layer with the R-shaped groove resemble a dielectric slab capacitor; the capacitances are less than those in the absence of the groove; C_s and C_m of the upper layer thus decrease. Also, compared to the field distributions of Fig. 12(a), the E-fields outside the groove that are connected to coupled lines in the upper dielectric layer were more strongly distributed than those in the absence of the groove. Therefore, the C_m value outside the groove in the upper layer was increased by the strongly distributed E-field. The extracted capacitance matrix of Fig. 12(a) is:

$$\boldsymbol{C} = \begin{bmatrix} 152.49 & 2.19\\ 2.19 & 152.49 \end{bmatrix} \text{pF/m},$$



FIGURE 11. Design of adjacent microstrip lines with R-shaped grooves in the upper layer: (a) 3-D view; (b) cross-section.



FIGURE 12. The differential-mode E-field distributions of coupled microstrip lines (a) without R-shaped grooves and (b) with R-shaped grooves in the upper layer.

and the extracted capacitance matrix of Fig. 12(b) is:

$$C = \begin{bmatrix} 149.1 & 2.63\\ 2.63 & 149.1 \end{bmatrix} \text{pF/m},$$

Therefore, C_t decreased from 152.49 to 149.1 pF/m, and C_m increased from 2.19 to 2.63 pF/m. This proved that the increase in C_m outside the R-shaped groove of the upper layer



FIGURE 13. The extracted values of C_t and C_m for coupled lines with R-shaped grooves placed in the upper layer, with respect to w_u/s and h_u/h_1 : (a) C_t , (b) C_m .

was more marked than the decrease in C_m generated by the groove; as C_t decreases, the groove increases C_m . The C_m decrease is dramatic if the area of the groove is larger than a certain value because the decrease generated by the groove is more marked than the increase in C_m outside the groove. The values of C_t and C_m with respect to w_u/s and h_u/h_1 are shown in Fig. 13. Figure 13(a) shows that C_t decreases not only with an increase in w_u/s , but also with an increase in h_u/h_1 . The tendency was thus similar to that described in Section II B. Figure 13(b) shows that C_m increases with increased w_u/s and h_u/h_1 , but C_m decreases dramatically after a specific value is attained. Figure 14 shows the $k_C - k_L$ values with respect to w_u/s and h_u/h_1 using both 2-D and 3-D graphs. From the parametric studies, the value of $k_C - k_L$ is closest to zero when $w_u/s = 0.85$ and $h_u/h_1 = 0.3$; therefore, these values are the optimal parameters in this configuration.

Figure 15 shows the simulated transient results in the time and frequency domains. In Fig. 15(a), V_{FEXT} values are shown with respect to the area of the R-shaped groove when a 1-V step signal with a rise time of $t_r = 50$ ps is applied. The simulated and calculated V_{peak} values are listed in Table 2. We verified that V_{peak} was minimal when $w_u/s = 0.85$ and $h_u/h_1 = 0.3$ in this configuration. Figure 15(b) shows the S₄₁ values by the area of the R-shaped groove in the frequency band of interest; S₄₁ was minimal when $w_u/s = 0.85$ and $h_u/h_1 = 0.3$; however, S₄₁ increased when $w_u/s = 1$ and $h_u/h_1 = 0.4$, as revealed by time- domain transient analysis.

IV. COMPARISONS WITH OTHER STRUCTURES

A. SIMULATED AND MEASURED RESULTS

To confirm the improvements afforded by our methods, four types of microstrip lines were compared in terms of S_{41} , S_{31} ,



FIGURE 14. The extracted values of $k_c - k_L$ with respect to w_u/s and h_u/h_1 : (a) 2-D graph, (b) 3-D graph.



FIGURE 15. The simulated results for adjacent lines with R-shaped grooves placed in upper layer with respect to the groove area: (a) V_{FEXT} , (b) S_{41} .

and V_{FEXT} . Figure 16(a) shows two conventional microstrip signal lines. The dimensions are $w_0 = 1.5$ mm, s = 4.5, $h_1 = 0.8$ mm, and l = 10 cm ($w_0/h_1 = 1.875$, $s/h_1 = 5.625$); a substrate is included ($\varepsilon_{r1} = 4.4$). For comparison, Figure 16(b) shows microstrip lines with guard traces connected to ground

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TABLE 2. Comparison between the calculated and simulated V_{peak} values with respect to the area of the R-shaped groove in the upper layer.

	V_{peak} derived using Eq. (6)	V _{peak} derived using EM Sim.
Without R-groove	-0.066 V	-0.060 V
$w_u/s = 0.35, h_u/h_1 = 0.1$	-0.062 V	-0.057 V
$w_u/s = 0.6, h_u/h_1 = 0.2$	-0.05 V	-0.048 V
$w_u/s = 0.85, h_u/h_l = 0.3$	-0.043 V	-0.044 V
$w_u/s = 1, h_u/h_1 = 0.4$	-0.055 V	-0.054 V



FIGURE 16. Cross-sections of four types of microstrip lines: (a) Conventional microstrip lines. (b) Lines with guard traces and holes. (c) Lines with R-shaped grooves in the upper layer. (d) Lines with R-shaped grooves in the lower substrate.

via holes of radius 0.6 mm [7]. Our new structures are shown in Fig. 16(c) and (d); the R- shaped groove is placed in the upper layer ($\varepsilon_{r2} = 4.4, h_2/h_1 = 1.5$) at $w_u/s = 0.85$ and $h_u/h_1 = 0.3$ in Fig. 16(c), and in the lower substrate at $w_L/s =$ 0.85 and $h_L/h_1 = 0.5$ in Fig. 16(d). A photograph of the microstrip lines is shown in Fig. 17. A Routing machine RU2B with routing accuracy of ± 0.05 mm was used to realize R-shaped grooves in the upper layer and lower substrate. The experimental measurements in the frequency domain and time domain were performed using the E5071C Vector Network Analyzer.



FIGURE 17. A photograph of fabricated conventional microstrip lines, lines with guard traces connected to ground, and lines with R-shaped grooves in the upper layer and lower substrate.

The simulated and measured S_{41} , S_{31} , and V_{FEXT} values for the four types of microstrip lines are shown in Fig. 18; the simulated and measured results are in good agreement.



FIGURE 18. Simulated (left) and measured (right) results from four types of microstrip lines: (a) S_{41} , (b) S_{31} , and (c) V_{FEXT} .

As shown in Fig. 18(a), the S₄₁ values of the conventional microstrip lines were greater than those of the other three types of microstrip lines in the frequency band of interest. The S₄₁ values of microstrip lines with a guard trace connected to ground were less than those of conventional lines but resonance-inducing ringing noise occurred at 8.5 GHz; therefore, S₄₁ increased sharply around this frequency. When the R-shaped groove was present, S₄₁ decreased markedly compared to the two previous two cases and was minimal when the R-shaped groove was in the lower substrate. Figure 18(b) shows the S₃₁ values of the four types of microstrip lines. The impedance of the transmission lines associated with the microstrip lines was kept close to 50 Ω ; therefore, overall, the S₃₁ values indicated good performance except for microstrip lines with a guard trace connected to ground. For these lines, S₃₁ decreased dramatically around 8.5 GHz due to ringing noise. Figure 18(c) shows the simulated and measured V_{FEXT} values of the four types of microstrip lines. The simulated and measured V_{peak} levels are listed in Table 3. In the simulations, compared to conventional microstrip lines, the V_{peak} values of the three other types of line (with the guard trace, an R-shaped groove in the upper layer, or an R-shaped groove in the lower substrate) were reduced by 32, 55, and 79%, respectively. In the measured results, the V_{peak} values fell by 31.5, 58.9, and 77.9%, respectively; V_{peak} was thus lowest when the R-shaped groove was placed in the lower substrate.

	Simulated V _{peak}	Measured V _{peak}
Conventional	-0.10 V	-0.092 V
With a_guard	-0.068 V	-0.065 V
Upper R-shaped groove	-0.045 V	-0.039 V
Lower R-shaped groove lower	-0.021 V	-0.021 V

TABLE 3. Simulated and measured $\mathrm{V}_{\mathrm{peak}}$ values of four types of microstrip lines.

We verified that FEXT noise was adequately reduced when the R-shaped groove was placed in the upper layer or lower substrate compared to conventional microstrip lines and microstrip lines with a guard trace. The simulated and measured results were in good agreement. Also, the FEXT noise reduction when an R-shaped groove was placed in the lower substrate was superior to that when the groove was in the upper layer; it was difficult to render k_C - k_L zero in the latter case.

B. EYE DIAGRAMS

When creating eye diagrams of the four types of microstrip lines, simulation ensured that the line dimensions were those of Section IV A and pseudo-random binary sequence (PRBS) signals were independently applied to the victim and aggressor lines at 8 Gb/s with a rise time $t_r = 50$ ps. Figure 19 shows simulated eye diagrams of the four types of microstrip lines at the output of the aggressor line when PRBS signals were not applied to the aggressor lines. The eye parameters (height, width, and jitter) of the four types of lines were, for conventional lines, 0.84 V, 114.95 ps, and 6.75 ps, respectively; for lines with a guard trace, they were 0.86 V, 115.5 ps, and 8 ps, respectively; and for lines with R-shaped



FIGURE 19. Simulated eye diagrams of (a) conventional microstrip lines; (b) microstrip lines with a guard trace; (c) lines with R-shaped grooves in the upper layer; and, (d) lines with R-shaped grooves in the lower substrate when pseudo-random binary sequence (PRBS) signals were not applied to the aggressor line. grooves in the upper layer and lower substrate, the values were 0.85 V, 115.41 ps, and 6.25 ps, respectively and 0.86 V, 115.06 ps, and 8 ps, respectively. When no signal was applied to the aggressor line, no effect of crosstalk noise on the victim line was apparent and the overall S_{31} values of the four types of microstrip lines evidenced good performance.



FIGURE 20. Simulated eye diagrams for (a) conventional microstrip lines; (b) microstrip lines with a guard trace; (c) lines with R-shaped grooves in the upper layer; and, (d) lines with R-shaped grooves in the lower substrate when PRBS signals were applied to the aggressor line.

Figure 20 shows simulated eye diagrams of the four types of microstrip lines at the output of the aggressor line when PRBS signals were simultaneously applied to the aggressor and victim lines. Eye width and jitter were the parameters predominantly affected by FEXT noise. The eye heights of the four types of lines were 0.81, 0.84, 0.85, and 0.86 V, respectively, thus rather similar. For conventional microstrip lines, the eye width decreased from 114.95 to 92.98 ps, and jitter increased from 6.75 to 22.25 ps, compared to the situation when no PRBS signal was applied to the aggressor lines. FEXT noise was reduced using a guard trace and R-shaped grooves. As shown in Fig. 20(b), the eye width increased to 11.4%, and jitter fell to 24.7%, when the guard trace was used. When an R-shaped groove was placed in the upper layer, the eye width increased to 16.3% and jitter fell to 42.7%. Finally, the eye width increased to 21.8%, and the jitter fell to 51.7%, when the R-shaped groove was placed in the lower substrate. Therefore, for a lower thickness of the upper dielectric layer with $\varepsilon_{r1} = \varepsilon_{r2}$, FEXT noise can be minimized by placing the R-shaped groove in the lower substrate. Although the structure with the R-shaped groove in the upper layer does not reduce FEXT noise as effectively as did the former structure, the latter structure reduced FEXT noise more than did the guard trace. The eye parameters of the four microstrip lines are listed in Table 4.

	Conventional	With the guard	R-shape in upper	R-shape in lower

TABLE 4. Parameters of the simulated eye diagrams of figures 19 and 20.

	Conventional	guard	in upper layer	substrate
]	Eye diagrams without crosstalk (Fig. 19)			
Eye height	0.84 V	0.86 V	0.85 V	0.86 V
Eye width	114.95 ps	115.5 ps	115.41 ps	115.06 ps
Jitter	6.75 ps	8 ps	6.25 ps	8 ps
Eye diagrams with crosstalk (Fig 20)				
Eye height	0.81 V	0.84 V	0.85 V	0.86 V
Eye width	92.98 ps	103.62 ps	108.15 ps	113.3 ps
Jitter	22.25 ps	16.75 ps	12.75 ps	10.75 ps

V. CONCLUSION

We thus devised a novel means of reducing FEXT noise by placing an R-shaped groove in multiple microstrip lines covered by a dielectric layer. FEXT noise was minimized even when the thickness of the upper dielectric layer was reduced; $\varepsilon_{r1} = \varepsilon_{r2}$. To understand the mechanism involved, we explored the circuit parameters and E-field distributions of coupled microstrip lines. As C_t decreased, C_m increased, as expected; FEXT noise could be reduced by placing an R-shaped groove in the upper layer or the lower substrate. To confirm the improvements afforded, the S₄₁, S₃₁, and VFEXT values, and eye diagrams of the various structures, were derived and compared to those of conventional microstrip lines and lines with a guard trace. We showed that FEXT noise was adequately reduced (more so than by other structures) when the R-shaped groove was placed in the upper layer or the lower substrate. The simulated and measured results were in good agreement.

REFERENCES

- [1] J. Buckwalter, B. Analui, and A. Hajimiri, "Data-dependent jitter and crosstalk-induced bounded uncorrelated jitter in copper interconnects," in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2004, pp. 1627-1630.
- [2] J. F. Buckwalter and A. Hajimiri, "Cancellation of crosstalk-induced jitter," IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 621-632, Mar. 2006.
- [3] A. Nieuwoudt, J. Kawa, and Y. Massoud, "Crosstalk-induced delay, noise, and interconnect planarization implications of fill metal in nanoscale process technology," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 3, pp. 378-391, Mar. 2010.
- [4] G.-H. Shiue, C.-L. Yeh, P.-W. Huang, H.-Y. Liao, and Z.-H. Zhang, "Ground bounce noise induced by crosstalk noise for two parallel ground planes with a narrow open-stub line and adjacent signal traces in multilayer package structure," IEEE Trans. Compon., Packag., Manuf. Technol., vol. 4, no. 5, pp. 870-881, May 2014.
- [5] J. A. DeFalco, "Reflection and crosstalk in logic circuit interconnections," IEEE Spectr., vol. 7, no. 7, pp. 44-50, Jul. 1970.
- [6] H. You and M. Soma, "Crosstalk analysis of interconnection lines and packages in high-speed integrated circuits," IEEE Trans. Circuits Syst., vol. 37, no. 8, pp. 1019-1026, Aug. 1990.
- [7] S. H. Hall, G. W. Hall, and J. A. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices. New York, NY, USA: Wiley, 2000.
- [8] Y.-S. Sohn, J.-C. Lee, H.-J. Park, and S.-I. Cho, "Empirical equations on electrical parameters of coupled microstrip lines for crosstalk estimation in printed circuit board," IEEE Trans. Adv. Packag., vol. 24, no. 4, pp. 521-527, Nov. 2001.
- [9] D. Brooks, Signal Integrity Issues and Printed Circuit Board Design. New York, NY, USA: Prentice-Hall, 2003.

- [10] K. Lee, H.-B. Lee, H.-K. Jung, J.-Y. Sim, and H.-J. Park, "A serpentine guard trace to reduce the far-end crosstalk voltage and the crosstalk induced timing jitter of parallel microstrip lines," IEEE Trans. Adv. Packag., vol. 31, no. 4, pp. 809-817, Nov. 2008.
- [11] S. K. Lee, K. Lee, H. J. Park, and J. Y. Sim, "FEXT-eliminated stubalternated microstrip line for multi-gigabit/second parallel links," Electron. Lett., vol. 44, no. 4, pp. 272-273, Feb. 2008.
- [12] K. Lee, H.-K. Jung, H.-J. Chi, H.-J. Kwon, J.-Y. Sim, and H.-J. Park, "Serpentine microstrip lines with zero far-end crosstalk for parallel high-speed DRAM interfaces," IEEE Trans. Adv. Packag., vol. 33, no. 2, pp. 552-558, May 2010.
- [13] D. N. Ladd and G. I. Costache, "SPICE simulation used to characterize the cross-talk reduction effect of additional tracks grounded with vias on printed circuit boards," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 39, no. 6, pp. 342-347, Jun. 1992.
- [14] L. Zhi, W. Qiang, and S. Changsheng, "Application of guard traces with vias in the RF PCB layout," in Proc. IEEE 3rd Int. Symp. Electromagn. Compat., May 2002, pp. 771-774.
- [15] A. Suntives, A. Khajooeizadeh, and R. Abhari, "Using via fences for crosstalk reduction in PCB circuits," in Proc. IEEE Int. Symp. Electromagn. Compat., Aug. 2006, pp. 34-37.
- [16] B.-R. Huang, K. C. Chen, and C. L. Wang, "Far-end crosstalk noise reduction using decoupling capacitor," IEEE Trans. Electromagn. Compat., vol. 58, no. 3, pp. 836-848, Jun. 2016.
- [17] T. R. Gazizov, "Far-end crosstalk reduction in double-layered dielectric interconnects," IEEE Trans. Electromagn. Compat., vol. 43, no. 4, pp. 566-572, Nov. 2001.
- [18] P. Muthana and H. Kroger, "Behavior of short pulses on tightly coupled microstrip lines and reduction of crosstalk by using overlying dielectric." IEEE Trans. Adv. Packag., vol. 30, no. 3, pp. 511-520, Aug. 2007.
- [19] Y.-S. Cheng, W.-D. Guo, C.-P. Hung, R.-B. Wu, and D. De Zutter, "Enhanced microstrip guard trace for ringing noise suppression using a dielectric superstrate," IEEE Trans. Adv. Packag., vol. 33, no. 4, pp. 961-968, Nov. 2010.
- [20] L. W. Ritchey, "A survey and tutorial of dielectric materials used in the manufacture of printed circuit boards," CircuiTree Mag., Nov. 1999. [Online]. Available: https://speedingedge.com/PDF-Files/tutorial.pdf
- [21] H. B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI. Reading, MA, USA: Addison-Wesley, 1990.
- [22] Q3D, Ansoft, Pittsburgh, PA, USA. [Online]. Available: https://www. ansys.com/products/electronics/ansys-q3d-extractor



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