IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 27, 2019, accepted July 9, 2019, date of publication July 11, 2019, date of current version July 30, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2928392

On Neural Networks Based Electrothermal Modeling of GaN Devices

ANWAR JARNDAL, (Senior Member, IEEE)
Electrical and Computer Engineering Department, University of Sharjah, Sharjah 27272, United Arab Emirates
e-mail: ajarndal@sharjah.ac.ae

This work was supported by the University of Sharjah, Sharjah, United Arab Emirates.

ABSTRACT This paper presents an efficient artificial neural network (ANN) electrothermal modeling approach applied to GaN devices. The proposed method is based on decomposing the device nonlinearity into intrinsic trapping-induced and thermal-induced nonlinearities that can be simulated by low-order ANN models. The ANN models are then interconnected in the physics-relevant equivalent circuit to accurately simulate the transistor. Genetic algorithm (GA)-based training procedure has been implemented to find optimal values for the weights of the ANN models. The modeling approach is used to develop a large-signal model for a 1-mm gate-width GaN high-electron mobility transistor (HMET). The model has been implemented in the advanced design system (ADS) and it has been validated by pulsed and continues small- and large-signal measurements. The model simulations showed a very good agreement with the measurements and verify the validity of the developed technique for dynamic electrothermal modeling of active devices.

INDEX TERMS GaN HEMT, electrothermal modeling, neural networks, genetic algorithm optimization.

I. INTRODUCTION

GAN high electron mobility transistor (HEMT) is currently an outstanding device for designing RF and microwave circuits. The higher electron saturation velocity, electron mobility, breakdown voltage, and operating temperature qualify it to be an outstanding device for designing advanced communication-electronic circuits such as power amplifiers and low noise amplifiers [1]. This makes the GaN HEMT an optimal choice for designing transceivers for advanced wireless communication systems such as 5G, WiMAX, ultra-wideband radar systems, and Ku-band space communication systems [2]. One of the main challenges that this device faces especially in high power application is self-heating induced power dissipation. The higher internal temperature (due to self-heating) degrades the electron velocity and mobility, thus reducing the drain channel current. This accordingly reduces the device output power, gain and power efficiency [3], [4]. Even though the thermal performance of GaN HEMTs is better than other technologies such as Si, this effect must be considered in the modeling phase of the device for accurate and reliable circuit design, especially for larger devices under linear- or quasi-linear-mode of operations [5]. Another important effect is the typical inherent surface and buffer trapping of the GaN HEMT, which results in current collapse under RF ($>$ 10 MHz) and kink effects in the dc and pulsed IV measurements [6]. Both thermal and trapping effects are correlated and typically pulsed current-voltage (IV) measurements at well selected quiescent-bias-voltages are used to characterize and model these two effects [7]. To characterize the thermal effect, pulsed IV measurements, at cold quiescent bias condition, are typically used. Furthermore, narrow pulses stimulus voltages are used to just measure the corresponding current without heating up the transistor. In this case, isothermal measurements could be obtained, and the current is mainly depending on the voltages levels and ambient temperature (negligible self-heating). Moreover, double-pulse technique can be used to obtained more accurate characterization for the thermal and trapping effects [8].

Many papers have been published to address the issue of electrothermal modeling of GaN including the dynamic trapping effects [6], [7], [9]–[18]. Some of these works such as the presented ones in [9], [10], [13] depend on the table-based approach, which has limited modeling capability because of its discrete nature. Also, its modeling range is limited by the implemented base measurement. These two

The associate editor coordinating the review of this manuscript and approving it for publication was Azwirman Gusrialdi.

limitations have been overcome by using analytical modeling based on closed formulas [6], [11]. This modeling has higher rate of convergence because of its continuous nature and its ability to predict the device behavior beyond the measured range. However, this technique is technology dependent and proper expressions should be used to fit the curves of the model parameters. Also, more effort is needed to determine the model fitting parameters. Artificial-Neural-Network (ANN) based modeling, such as the ones presented in [14]–[18], can provide an optimal solution in terms of accuracy and cost. The model architecture is based on interconnected neurons in a topology of multilayers (input, hidden and output). In feedforward multilayer-perceptron (MLP) ANN, the outputs from neurons of a layer represent inputs for the next layer. The process in each neuron is implemented by mathematical activation function. In principle MLP is a universal technique that can be used for approximating any nonlinear function [19], which makes it technologically independent and does not require prior knowledge about the modeled device or predefined formulas.

The model topology (number of layer and neurons) is proportional with the degree of nonlinearity for the considered modeling problem. This accordingly, represents a challenge for the ANN based on the mostly used local backpropagation (BP) learning/optimization technique, especially for modeling strong device nonlinearities such as the drain current. During the BP training, the ANN calculates the resulting output current, at certain input voltages, and compares it with the measured current to get the error, which is then propagated back through the system to adjust the weights for best fitting. The main limitation of the backpropagation (BP), as a gradient method, is its higher sensitivity to the initial guess and the solution could get stuck in local minima [20]. To overcome this problem, more effort is needed to find proper initial guess (close to the global minimum), tune the model topology, modify the objective function or change the activation function [21], [22]. This local minima problem becomes more obvious in a non-linear problem of larger scale ANN model such as IV characteristics modeling.

In this paper an efficient modeling technique is proposed to address these issues. The main contributions of this paper with respect to other published works are: (i) decomposing the device nonlinearity into partial weaker nonlinearities that can be represented by simpler topologies ANN models; (ii) genetic algorithm (GA) global optimization [23] is used to train the ANN models; (iii) distributed extrinsic network is used to cover a wider frequency range; (iv) only cold IV and S-parameters are used to characterize and model thermal, trapping and parasitic effects. To the best of the author's knowledge, the presented modeling technique procedure has not been presented previously and this paper will contribute to demonstrate its applicability to nonlinear GaN HEMTs modeling. In the first part of this paper, the characterization and modeling techniques for the temperature-dependency will be introduced. In the second part, the implemented GA based optimization procedure will be presented, along with the output of each combined ANN model will be compared with the actual data. The third part will cover the large-signal model implementation and validation and finally the results will be discussed and the paper will be concluded.

II. MEASUREMENT SET-UP AND MODEL TOPOLOGY

The pulsed drain current can be represented as a function of four parameters: the intrinsic gate voltage V_{gs}, the intrinsic drain voltage V_{ds}, the gate quiescent-bias-voltage V_{gso} and the drain quiescent-bias-drain voltage V_{dso}. The internal power dissipation and thus the associated self-heating is mainly related to the quiescent voltages and current (V_{gso}, I_{gso}, I_{dso} and V_{dso}) and their low frequency components. The quiescent voltages are also stimulating the trapping effects. Therefore, by keeping zero values for V_{gso} and V_{dso} (unbiased condition) one can ensure that there is no further trapping and no self-heating due to quiescent power. The other self-heating contribution from the applied voltage could be avoided by applying a very narrow pulse (in the order of 0.1 μs), which is just enough to stimulate the device and measure the responding drain and gate current. In this case, the device internal temperature is nearly equal to the ambient temperature. Hence, the obtained IVs could be considered as isothermal measurements for the drain current ($I_{ds,iso}$). The device is typically mounted on temperature controlled thermal chuck to heat up the device and therefore the drain current variation can be related to the external temperature. For the considered devices, narrow pulses of 200 ns width are applied to the gate and drain terminals. The peaks pulses are swept from -7 to 1 V for V_{gs} and from 0 to 30 V for V_{ds}, both in steps of 1 V. The measurements have been done at 25, 40, 55 and 70 °C temperature (adjusted by the thermal chuck).

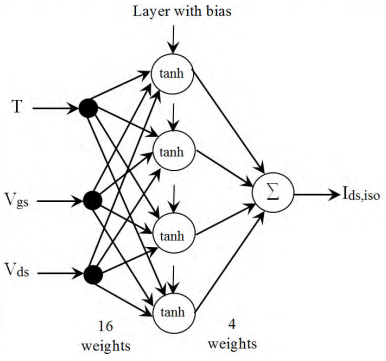

FIGURE 1. Single-hidden layer ANN model for isothermal drain current.

The voltage and temperature dependence of the isothermal drain current $I_{ds,iso}$ is modeled by the model shown in Fig. 1. As it can be seen in the figure, $I_{ds,iso}$ is simulated by the single-hidden-layer ANN model. The total number of input weights, biases and output weights is 20. This shows the difficulty of such quietly large-scale problem and the crucial need to use a global optimization such as genetic algorithm for training larger size ANN. For this modeling (data fitting) problem, the hyperbolic functions (*tanh*)

is used as an activation function. This function is consistent with behavior of the drain current and it can accurately describe it's ohmic-saturation transition and pinch-off (turn-on) nonlinearities [6], [14]. $I_{ds,iso}$ can be formulated in terms of V_{gs}, V_{ds} and Temperature (T) as:

$$I_{ds,iso} = \sum_{k=1}^{4} w_k \tanh\left(w_{1k} V_{ds} + w_{2k} V_{gs} + w_{3k} T + w_{4k}\right). \tag{1}$$

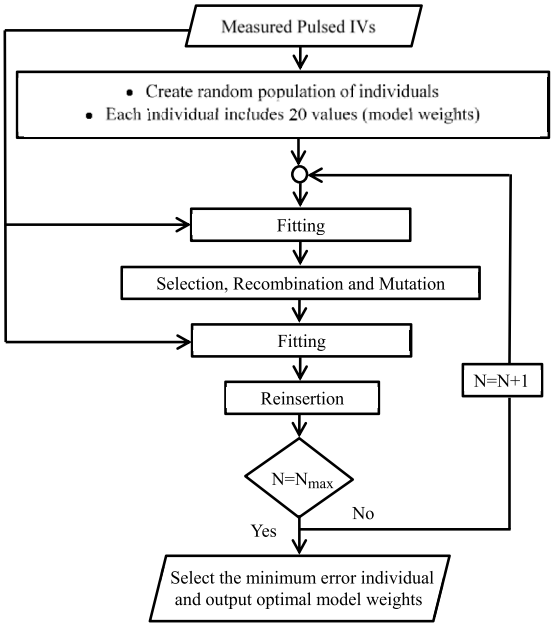

FIGURE 2. Flowchart of the genetic algorithm model learning process.

III. GENETIC ALGORITHM OPTIMIZATION BASED LEARNING

The implemented GA-based learning process is summarized by the flow chart in Fig. 2. In this work, real-coded GA is adopted [23]. The optimization process is started by random generation of initial population of individuals. Each individual consists of 20 values (16 for the input weights and biases and 4 for the output weights). These individuals represent the first generation of parents. The individuals are then evaluated by fitting the pulsed IVs measurements and the worst (maximum error) 10% out of them are rejected. The objective error function is defined as:

$$Error = \frac{1}{N} \sum_{k=1}^{N} \left(I_{ds,meas} - I_{ds,sim}\right)^2 \tag{2}$$

where $I_{ds,meas}$ and $I_{ds,sim}$ are the measured and simulated currents, respectively and N is the total number of data points. The remaining individuals (parents) undergo recombination (crossing) and mutation operations to produce the next generation of individuals (offspring). Double-point crossover has been used to reproduce the offspring. Then, these reproduced individuals are mutated (altered randomly) by low probability of 10% [23]. These individuals are then re-evaluated by fitting the measurements to select minimum errors individuals. These offspring individuals replace the most error parent individuals through the reinsertion step. The new combined individuals will be parents for the next generation and again will undergo selection, crossing and mutation operations. The optimization process will continue over N_{max} generations to find the minimum error individual and the associated optimal values of the model weights and biases.

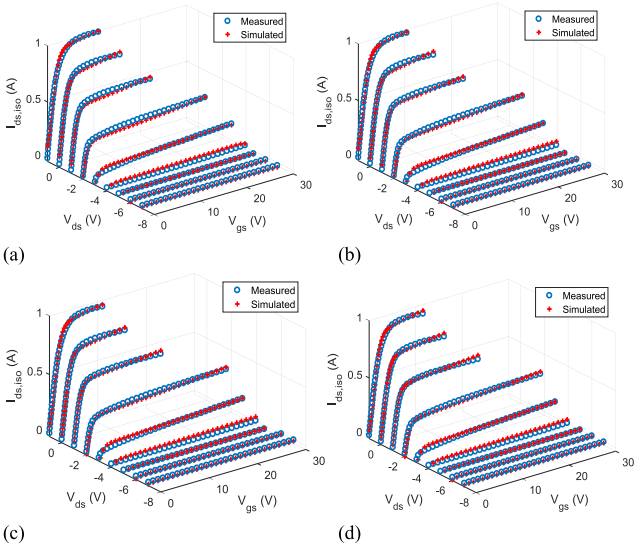

FIGURE 3. Measured and Simulated isothermal drain current of 1 mm GaN HEMT at: (a) 25 °C, (b) 40 °C, (c) 55 °C and (d) 70 °C temperatures.

IV. ISOTHERMAL CURRENT MODEL VALIDATION

The presented procedure in Section III, has been applied to pulsed IV measurements of an on-wafer 1 mm ($8\times125\mu$m) GaN HEMT. It has been fabricated on SiC substrate by the Ferdinand-Braun-Institute [24], and characterized by the Fraunhofer Institute for Applied Solid-State Physics. The pulsed IV measurements have been conducted by stimulating the device by gate and drain pulses of 200 ns pulse-width and 1 ms pulse repetition-time. This narrow (much smaller than the typical thermal time constant) pulse is not enough to heats up the device and it provides stable and reliable measurements [25]. Also the longer pulse repetition-time (1 ms), with respect to the pulse width (200 ns), will keep the device cold and avoid any extra residual heat between consecutive pulses, especially for hot quiescent bias point [25]. As mentioned in the last section, the reference temperature of the measurements is fixed by the thermal chuck (probing of the on-wafer station) and temperature-control unit, with accuracy of $\pm0.1°C$. Fig. 3 shows isothermal measurements (under $V_{gso} = 0$ V and $V_{dso} = 0$ V) at 25 °C, 40 °C, 55 °C and 70 °C external temperatures. Three of these measurements at 25 °C, 40 °C and 70 °C are used to build the model; while the fourth one at 55 °C are used for the model validation.

The optimization (model training) process is started by generating a uniformly distributed random initial population

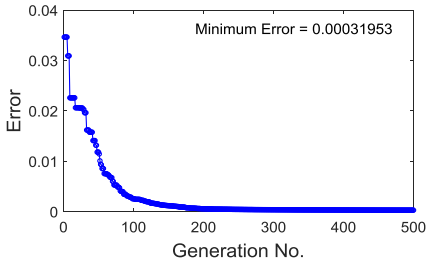

FIGURE 4. Error variation versus number of generation through the model weight optimization.

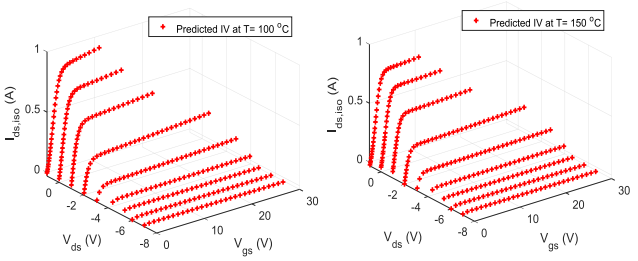

FIGURE 5. Simulated isothermal drain current of 1 mm GaN HEMT at: (a) 100 °C, and (b) 150 °C temperatures.

of 1000 individuals. Each individual consists of 20 values (between −1 and 1) for the model weights. The maximum number of generations is set to 500. Fig. 4 shows the error variation versus the number of generation during the optimization process of the model weights. The convergence of the error clearly shows the effectiveness and efficiency of the implanted optimization.

This results was obtained with elapsed-time of 512 Seconds using 3.6 GHz Computer of 16 GB RAM. This step has to be done offline just to build the model and thus this time is not a big issue. The simple (single-hidden layer of 4 neurons) topology of the model makes it easy to represent it in a simple closed formula that could be directly implanted in CAD with higher rate of convergence and shorter time of simulation. Figs. 3(a) −3(d), present the predicted and measured pulsed IVs at 25, 40, 55 and 70 °C, respectively. The mean-square-error defined in (2) for these four cases is 4.8719×10^{-4}, 3.9829×10^{-4}, 3.5280×10^{-4} and 3.5256×10^{-4}, respectively. The model has been also used to predict the drain current at higher temperature as shown in Fig. 5 for 100 °C and 150 °C. As can be seen, the model shows the typical expected reduction at higher temperature and validates the model accuracy in simulating the temperature dependence of the drain current.

V. ELECTROTHERMAL MODEL FOR DRAIN CURRENT

The longer time delay between consecutive dc IV measurements, (which is typically much longer than trapping time constants), allows even the trapped carriers to release and participate in the conduction mechanism [26]. Thus the drain current variation could be related mainly to the applied dc voltages and the induced self-heating. Pulsed IVs at active quiescent bias voltages will be affected also by self-heating due to quiescent (average) power dissipation. In general, the drain current can be represented by the same model in (1) but the temperature T could be extended to consider also the self-heating as follows:

$$T = R_{th}P_{diss} + (T_{ref} + \Delta T) \tag{3}$$

where ΔT is the rise of ambient temperature with respect to reference ambient temperature T_{ref} (typically at around 25 °C) and P_{diss} is the intrinsic power dissipation ($P_{diss} = V_{ds}I_{ds}$). R_{th} is the thermal resistance and it depends mainly on the device structure and materials. The dc IVs at T_{ref} can be used to characterize and model variation of I_{ds} with P_{diss}. Fig. 6(a) shows dc IVs for the same considered device at room temperature $T_{ref} = 25$ °C. The corresponding power dissipations for the same dc IVs are calculated and illustrated in Fig. 6(b).

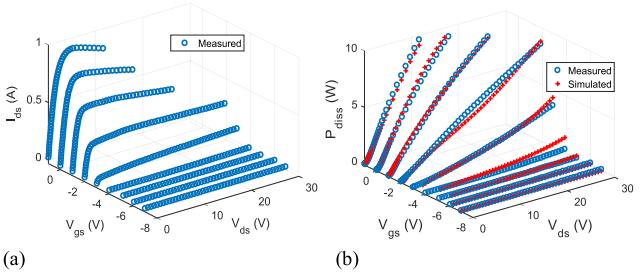

FIGURE 6. (a) Measured dc IVs and (b) measured and simulated dc power (I_{ds} V_{ds}) at 25 °C ambient temperature for 1 mm GaN HEMT.

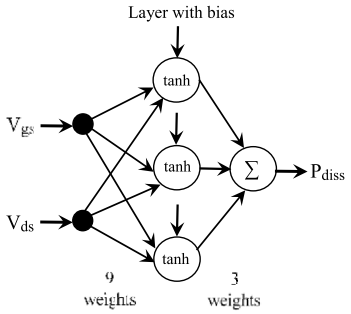

FIGURE 7. Single-hidden layer ANN model for power dissipation.

The power dissipation variation with V_{gs} and V_{ds} can be described by the ANN model of two inputs and single hidden layer of 3 neurons shown in Fig. 7. The same optimization procedure presented in Section III is used to find the model weights. Similar to $I_{ds,iso}$, P_{diss} can be represented analytically as:

$$P_{diss} = \sum_{k=1}^{3} w_k \tanh\left(w_{1k}V_{ds} + w_{2k}V_{gs} + w_{3k}\right). \tag{4}$$

Fig. 6(b) shows the measured and simulated P_{diss} with mean-square-error of 7.2×10^{-2}. The ANN models in Figs. 1 and 7 can be combined to form an electrothermal model for the

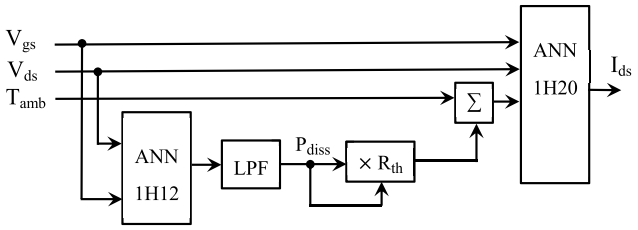

FIGURE 8. Electrothermal model for the drain current.

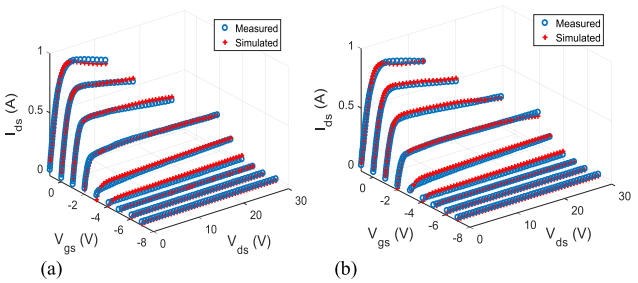

FIGURE 9. Measured and simulated DC IVs of 1 mm GaN HEMT at: (a) 40 °C and (b) 70 °C ambient temperature.

drain current as it is illustrated in Fig. 8. As previously mentioned, the self-heating is induced by the lower frequency components of P_{diss} (static and quasi-static power dissipation). These components are extracted using single-time-constant RC low-pass-filter. The time constant of the RC circuit is in the order of 1 ms (typical thermal time constant of GaN devices) [27]. This implementation is widely used as a simple and efficient technique for simulating the thermal dynamic behavior [7].

The model of Fig. 8 has been implemented in MATLAB and used to predict the dc IVs at different temperatures. The dependence of R_{th} on P_{diss} [28] has been considered by implementing the following formula:

$$R_{th} = [1 + 2(1 + 0.1 \times \tanh(P_{diss} - 9))P_{diss}]P_{diss}. \quad (5)$$

The formula of R_{th} in (5) was empirically extracted and it provided best fitting of the dc IV characteristics at T_{ref}. A tanh(·) function has been used in (5) to restrict R_{th} to a constant value, in smooth manner, at high P_{diss} and improve the model convergence [11]. Figs. 9(a) and 9(b) show the simulated dc IVs at 40 °C and 70 °C ambient temperature with mean-square-error of 5.3585×10^{-4} and 5.1538×10^{-4}, respectively. As it can be seen the model can accurately simulate the ambient temperature and self-heating induced current collapse.

VI. TRAPPING EFFECT MODELING

In general, the trapping effect cannot be ignored, especially for large-size GaN HEMT at high-power operation. In addition to the surface trapping due to polarization induced surface charges [29], the high driving power stimulates some carrier to be injected in the deep levels in the buffer layer below the channel [26]. Under RF (>10 MHz) the longer emission time of trapped carriers (in order of 1 μs) prevents them to participate, which results in current reduction under this condition with respect to static and quasi-static of operation. Thus, the last model of Fig. 8 should be extended by adding another term to consider the current variation due to surface and buffer trapping. The complete drain current can be expressed as:

$$I_{ds} = I_{ds,iso}(V_{gs}, V_{ds}, T) + I_{ds,diff}(V_{gs}, V_{ds}, V_{gso}, V_{dso}) \quad (6)$$

where $I_{ds,iso}$ is determined by (1) and T is calculated using (3)-(5) and it depends on the ambient temperature in addition to the power dissipation P_{diss}. P_{diss} in (3) is predicted by its ANN model and its static/quasi-static values are extracted by a low pass circuit. The main nonlinear behavior of I_{ds} and its inherent thermal effect can be embedded from the measured current at any arbitrary quiescent voltages and the remaining part (the second term of (6)) can be used to characterize the trapping induced dispersion.

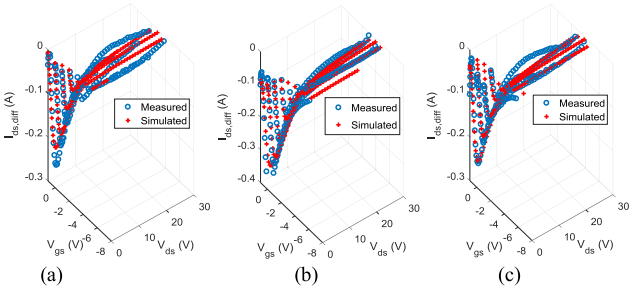

FIGURE 10. Measured and simulated trapping induced current different $I_{ds,diff}$ of 1 mm GaN HEMT at 25 °C under: (a) $V_{gso} = -2$ V and V_{dso} =15 V, (b) $V_{gso} = -4$ V and V_{dso} =25 V and (c) $V_{gso} = -7$ V and V_{dso} =0 V.

The incremental trapping current $I_{ds,diff}$ has been calculated by comparing measured pulsed IVs, at proper cold and active quiescent voltages, with the corresponding predicted ones using the model in Fig. 8. Fig. 10 shows the extracted $I_{\mathrm{ds,diff}}$ from measured pulsed IV at 25°C under ($V_{gso} = -2$ V, $V_{dso} = 15$ V), ($V_{gso} = -4$ V, $V_{dso} = 25$ V) and ($V_{gso} = -7$ V, $V_{dso} = 0$ V) quiescent voltages. Variation of $I_{ds,diff}$ with V_{gs}, V_{gso}, V_{ds} and V_{dso} has been simulated by the ANN model shown in Fig. 11. The mean-square-error for the three cases in Fig. 10 is $3.7466\times^{-4}$, $4.1246\times^{-4}$ and $3.7390\times^{-4}$, respectively.

The model has four inputs with single hidden layer of four neurons. Similarly, it can be represented by the following formula:

$$I_{ds,diff} = \sum_{k=1}^{4} w_k \tanh\left(\begin{matrix} w_{1k}V_{ds} + w_{2k}V_{gs} + \\ w_{3k}V_{dso} + w_{4k}V_{gso} + w_{5k} \end{matrix}\right). \quad (7)$$

The same mentioned genetic algorithm optimization in Section III has been used to train the model to find optimal values for the model weights. The trapping effect, which is characterized here by $I_{\mathrm{ds,diff}}$, depends mainly on the rate of change of the stimulus voltages (ac components) with respect

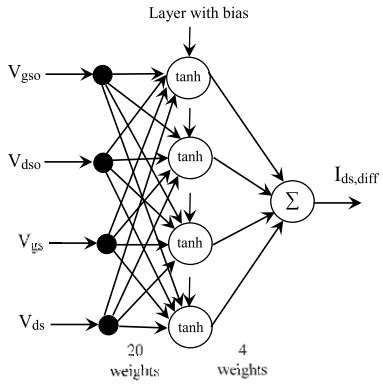

FIGURE 11. Single-hidden layer ANN model for trapping induced dispersion.

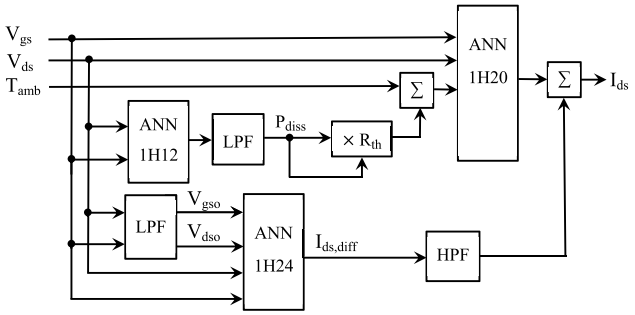

FIGURE 12. Electrothermal and trapping model for the drain current.

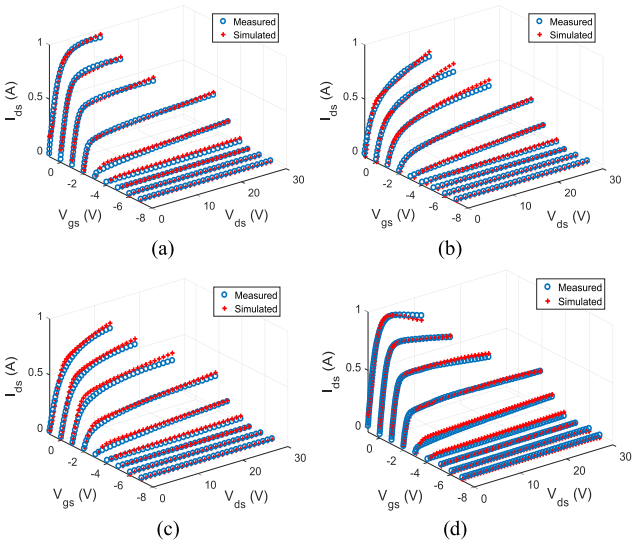

FIGURE 13. Measured and simulated pulsed IV of 1 mm GaN HEMT under: (a)V_{gso} = 0V, V_{dso} =5V and T =25°C, (b) V_{gso} = −4V, V_{dso} =25V and T =70°C, and (c) V_{gso} = −2V, V_{dso} =15V and T =70°C. (d) Measured and simulated dc IV at 25°C.

to their quiescent values (V_{gso} and V_{dso}). Thus, as shown in Fig. 12, this term could be implemented by ANN model with a high pass filter (HPF) of time constant in the order of 1 μs [27] to simulate the dynamic trapping effects. The complete model including the three ANN models is shown on Fig. 12. As presented in Fig. 13, the complete model has been validated by pulsed and dc IVs at different active quiescent voltages and different ambient temperatures. Fig. 13(a) shows the model simulation for pulsed IVs at 25°C under active quiescent biases (V_{gso} = 0V, V_{dso} = 5V). Under this condition the device characteristics will be affected mainly by self-heating (due to quiescent power dissipation) and trapping effects, which as can be seen, are well simulated by the model. As illustrated also in Figs. 13(b) and 13(c), the model also shows very good fitting for cold pulsed IVs at high ambient temperature of 70°C. Fig. 13(d) also presents a very accurate simulation for the dc IVs at room temperature of 25 °C, which are mainly effected by self-heating. The mean-square-error for these four cases is 6.2556×10^{-4}, 5.6769×10^{-4}, 5.6783×10^{-4} and 5.3585×10^{-4}, respectively. These very accurate results clearly justify the advantage of using the non-gradient GA based training. In this model (see Fig. 12), the drain current is not directly related to V_{gs}, V_{ds} and T and thus it is very difficult to calculate the derivatives of the error function in case of using gradient BP based training.

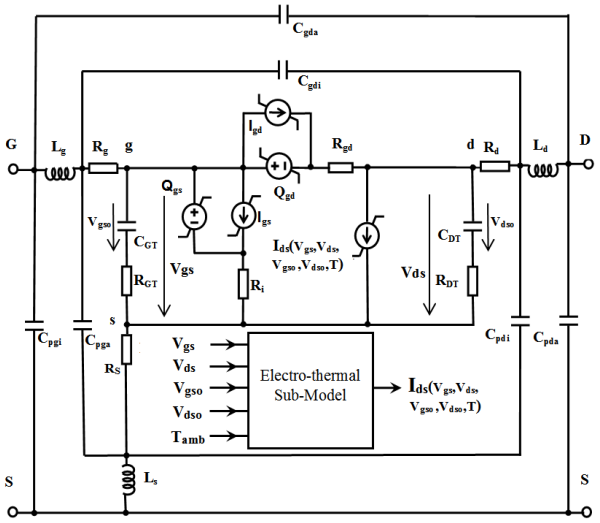

FIGURE 14. Large signal model for GaN HEMT including electro-thermal sub-model for the drain current [16].

VII. LARGE SIGNAL MODELING

The drain current has been embedded in the equivalent circuit large signal model shown in Fig. 14. This model has been reported in [16]. The extrinsic bias-independent part of the model represents the parasitic resistances, inductances and capacitances due to contacts/semiconductor, metallization and pad-connections, respectively. The intrinsic network simulates the nonlinear bias-dependence of the depletion region and channel current. The RC circuits in the drain and gate sides are to represent the trapping time constants ($C_{DT}R_{DT}$ and $C_{GT}R_{GT}$) and to simulate the dynamic trapping. Another RC circuit of thermal time constant is added to simulate the dynamic self-heating. The model extrinsic elements were extracted from cold S-parameters measurements using the same reported approach in [30]. After de-embedding the

extrinsic elements from active measured S-parameters, the intrinsic elements are extracted quasi-analytically from the intrinsic Y-parameters (Y_i) following the same procedure presented in [7]. The intrinsic gate capacitances and conductances are then integrated to find the corresponding currents and charges I_{gs}, I_{gd}, Q_{gs} and Q_{gd} [7].

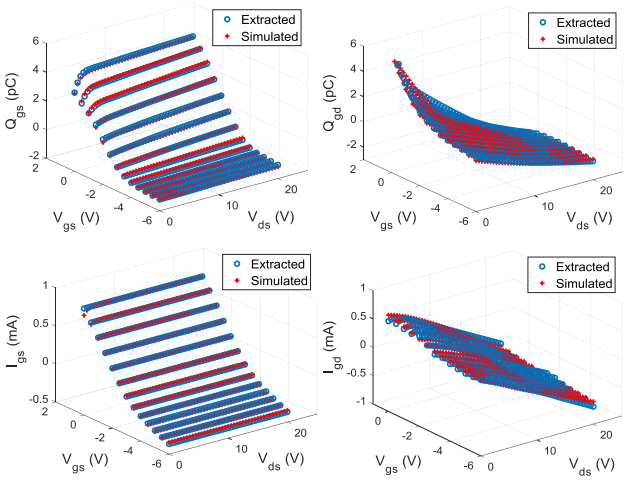

FIGURE 15. Measured and simulated intrinsic gate charges and currents of 1 mm GaN HEMT.

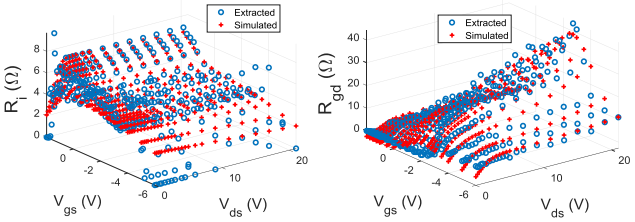

FIGURE 16. Extracted and simulated intrinsic resistances of 1 mm GaN HEMT.

The same neurogenetic modeling approach has been applied to each intrinsic element to simulate its nonlinear behavior with respect to the gate and drain stimulus voltages V_{gs} and V_{ds}. Simple, single hidden ANN topology of three neurons with *tanh* activation function has been used for all models. As it has been mentioned, this function can efficiently simulate sudden or smooth change of the intrinsic elements in the ohmic-saturation and pinch-off regions. Fig. 15 shows the extracted and simulated intrinsic gate currents and charges at room temperature of 25°C. As can be seen, the same model topology based on genetic algorithm optimization provides a very good fitting for different nonlinear behaviors. The same model also shows a good simulation for the intrinsic resistances as presented in Fig. 16. The mean-square-error for the simulated Q_{gs}, Q_{gd}, In_{gs}, and I_{gd}, is 7.5 $\times 10^{-3}$, 2.6 $\times 10^{-2}$, 1.3133$\times 10^{-4}$ and 6.7767$\times 10^{-4}$, respectively.

As it was mentioned, the trapping induced gate-lag and drain-lag are considered in the drain-current model by the additional term of $I_{ds,diff}$. To simulate the dynamic trapping effect, $R_{GT}C_{GT}$ and $R_{DT}C_{DT}$ networks are added to the gate and drain sides, respectively (see Fig. 14). In this representation, symmetrical emission and capture times has been assumed. This approach provides an efficient and simple solution and it has been widely used [7], [9], [31]. The trap emission time-constants can be estimated from the low frequency Y-parameters of the considered device [32]–[34]. The de-embedded intrinsic trans-conductance Y_{gm} and output-conductance Y_{ds} (after removing the extrinsic parasitic elements) can be formulated as [27]:

$$Y_{gm} = Y_{i,21} - Y_{i,12} = \frac{G_m e^{-j\omega\tau}}{1 + R_i G_{gsf} + j\omega C_{gs}} \quad (8)$$

$$Y_{ds} = Y_{i,22} + Y_{i,12} = G_{ds} + j\omega C_{ds}. \quad (9)$$

The trapping induced out-put conductance dispersion can be characterized by low frequency (fraction of MHz) measurements of Y_{ds} [33]. For the considered device, under active bias condition, C_{gs} has values in the order of 1 pF; while G_{gsf} is in the order of 1 mS [34]. Thus, the last two terms of the denominator in (8) can be ignored in the MHz frequency range. In this case, the trapping induced trans-conductance dispersion can be characterized from the magnitude of Y_{gm} versus frequency.

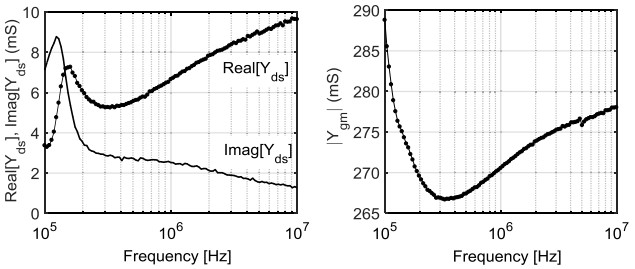

FIGURE 17. Measured intrinsic admittances for 1 mm GaN HEMT at $V_{GS} = -1$ V and $V_{DS} = 12$ V.

Fig. 17 shows the real and imaginary measured values of Y_{ds} for the same investigated 1-mm GaN HEMT. These measurements agree well with the reported ones in [33], [34] and show the expected multiple traps and the typical positive dispersion (growth of out-put conductance with increasing the frequency). The trap mission time constants can be extracted from the frequencies of the peaks of *Imag*[Y_{ds}] or inflexion points of *Real* [Y_{ds}]. In our case, single trap has been considered and its time constant is equal to the inverse of *Imag* [Y_{ds}] peak frequency (in rad/s). From Fig. 17 the estimated time constant is equal to $\frac{1}{2\pi \times 1.2 \times 10^5} = 1.3\mu s$ [33]. The measurements have been repeated at different bias conditions. It was observed that the peak frequency of *Imag* [Y_{ds}] is shifted to 10^4 Hz rang with decreasing V_{DS} and this has been also reported in [32]. For that reason 10 μs has been selected (as an average) and used to fix the values of R_{DT} at 1 M Ω and C_{DT} at 10 pF. Regarding the trans-conductance, positive and negative dispersions can be observed depending on the drain source voltage (V_{DS}) [32]. Fig. 17 shows the measured trans-conductance, which shows the typical lower variation

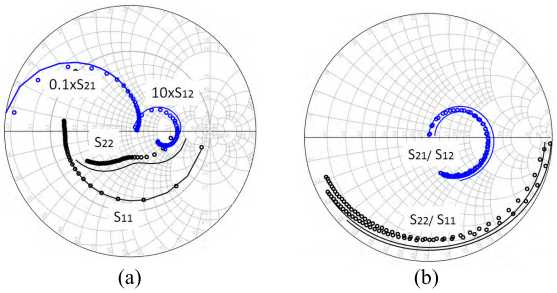

FIGURE 18. Measured and simulated S-parameters of 1 mm GaN HEMT at: (a) $V_{GS} = -2.5V$ and $V_{DS} = 19V$ and (b) $V_{GS} = -6V$ and $V_{DS} = 0V$ from 0.5 GHz to 20 GHz.

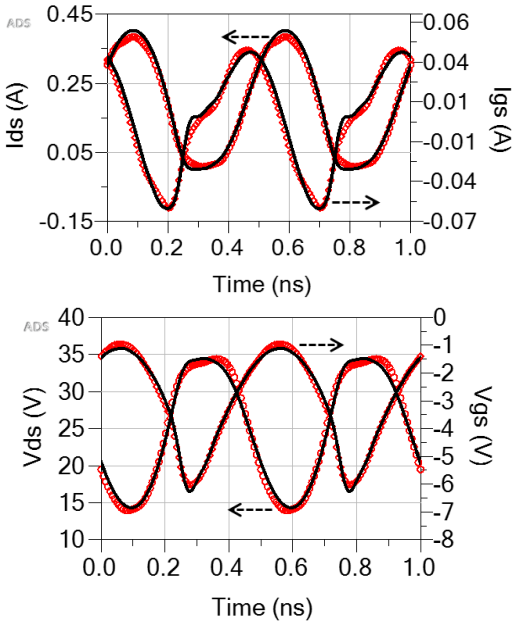

FIGURE 19. Measured (symbols) and simulated (lines) signal waveform at 15dBm input power under $V_{GS} = -3V$ and $V_{DS} = 25$ V bias condition in 50Ω terminations and 25°C room temperature.

(less than 10%) with respect to the output-conductance (> 100%) [32]. Following the same approach, the other trap emission time can be estimated from the frequency of trans-conductance inflexion point to equal $\frac{1}{2\pi \times 3.5 \times 10^5} = 0.45\mu s$ (see Fig. 17). The inflexion frequency of trans-conductance has lower variation, in 10^5 Hz range, with bias voltages. This could be attributed to the implemented surface passivation process, which reduces the surface trapping and the induced trans-conductance dispersion [29]. Here the emission time is fixed at 1 μs and based on that, 1 M Ω was assigned to R_{GT} and 1 pF for C_{GT}.

VIII. MODEL IMPLEMENTATION AND VALIDATION

The simple topologies of the developed ANN models simplifies their implementation in Advanced Design System (ADS). Each ANN model can be implemented as a *tanh* based closed formula in terms of its inputs. The modeling procedure has been applied on the considered 1 mm GaN on SiC substrate and then the developed equivalent circuit model (see Fig. 14) has been implemented in ADS.

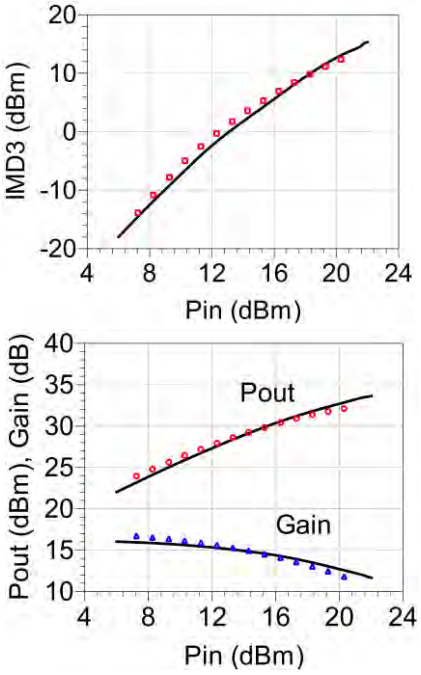

FIGURE 20. Measured (symbols) and simulated (lines) two-tone power sweep versus total input power at carrier frequency of 2.15 GHz and frequency spacing of 100 KHz for class-AB operated 1 mm GaN HEMT ($V_{GS} = -3V$, $V_{DS} = 24$ V, I_{DS} =200 mA) in 50Ω terminations and 25°C room temperature.

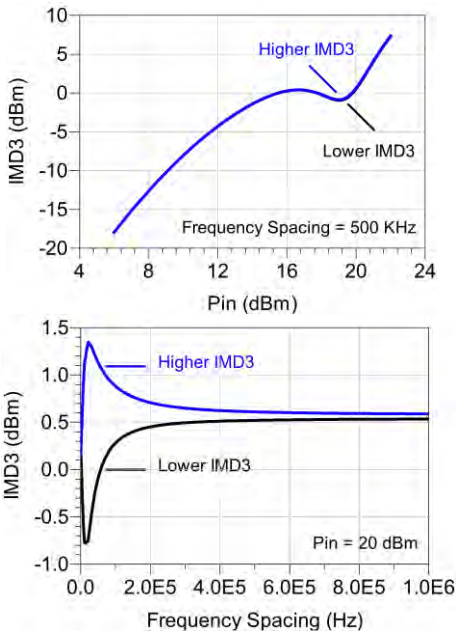

FIGURE 21. Two-tone power sweep (left) and frequency-spacing sweep (right) simulations at carrier frequency of 2.15 GHz and class-C of operation ($V_{GS} = -4.5$ V, $V_{DS} = 24$ V) in 50Ω terminations and 25°C room temperature.

Lumped elements have been used to represent the parasitic resistances, inductances and capacitances. Multiport symbolically-defined device (SDD) has been used to implement the ANN models of the intrinsic elements including I_{ds}, Q_{gs}, I_{gs}, Q_{gd}, I_{gd}, R_i and R_{gd}. In Figs. 18-20, the implemented

model has been validated by S-parameters, signal-waveform and power-sweep measurements for the same considered device. These measurements are independent of the measured data that were used to build/train the model. As can be seen, very good fitting is obtained, which accordingly verifies the validity of the developed model for linear and nonlinear circuits design.

Fig. 21 presents additional simulation to show the model capability of simulating the intrinsic and strong nonlinearities of the device. This could be observed from the predicted third order intermodulation distortion (IMD3) sweet spot (local minimum), which results from the interaction between small- and large signal IMDs [36]. Fig. 21, also, shows variation of the upper and lower IMDs with the frequency spacing and typically the IMDs asymmetry is used as a measure for the memory effects [37]. As can be seen, the model can simulate the expected thermal and electrical memory due to trapping and self-heating effects, respectively [38], [39].

IX. CONCLUSION

In this paper, an elecrothermal neurogenetic modeling approach has been developed and applied to GaN transistor. The method is based on simulating the device's nonlinear behavior by interconnect simple ANN models, which characterize the intrinsic, self-heating-induced and trapping-induced nonlinearities. The model is easy to be implemented in CAD software with equivalent circuit and analytical formulas to represent its nonlinear elements. The modeling technique has been explained as well as the model parameters extraction procedure. The developed model has been implemented in ADS and validated by proper small- and large-signal measurements. A very good result has been obtained and it proves the validity of the developed modeling approach. In the future work, the model will extended to consider the asymmetrical trapping time constants and the model will also be demonstrated by applying it to design application circuits.

ACKNOWLEDGMENT

The author also thanks Fraunhofer Institute for Applied Solid-State Physics (IAF), Freiburg, Germany, for providing the pulsed IV, S-parameters and large-signal measurements.

REFERENCES

[1] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[2] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, "GaN-based robust low-noise amplifiers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013.

[3] J. Kuzmík, M. Ťapajna, L. Válik, M. Molnár, D. Donoval, C. Fleury, D. Pogany, G. Strasser, O. Hilt, F. Brunner, and J. Würfl, "Self-heating in GaN transistors designed for high-power operation," *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3429–3434, Oct. 2014.

[4] O. Arenas, É. Al Alam, V. Aimez, A. Jaouad, H. Maher, R. Arès, and F. Boone, "Electrothermal mapping of AlGaN/GaN HEMTs using microresistance thermometer detectors," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 111–113, Feb. 2015.

[5] A. Jarndal, P. Aflaki, R. Negra, A. B. Kouki, and F. M. Ghannouchi, "Large-signal modeling methodology for GaN HEMTs for RF switching-mode power amplifiers design," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 21, no. 1, pp. 45–51, Nov. 2010.

[6] A. Jarndal and F. M. Ghannouchi, "Improved modeling of GaN HEMTs for predicting thermal and trapping-induced-kink effects," *Solid-State Electron.*, vol. 123, pp. 19–25, Sep. 2016.

[7] A. Jarndal and G. Kompa, "Large-signal model for AlGaN/GaN HEMTs accurately predicts trapping- and self-heating-induced dispersion and intermodulation distortion," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2830–2836, Nov. 2007.

[8] A. Santarelli, R. Cignani, G. P. Gibiino, D. Niessen, P. A. Traverso, C. Florian, D. M. M.-P. Schreurs, and F. Filicori, "A double-pulse technique for the dynamic I/V characterization of GaN FETs," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 132–134, Feb. 2014.

[9] A. Jarndal, A. Z. Markos, and G. Kompa, "Improved modeling of GaN HEMTs on Si substrate for design of RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 3, pp. 644–651, Mar. 2011.

[10] A. Santarelli, D. Niessen, R. Cignani, G. P. Gibiino, P. A. Traverso, C. Florian, D. M. M.-P. Schreurs, and F. Filicori, "GaN FET nonlinear modeling based on double pulse I/V characteristics," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3262–3273, Dec. 2014.

[11] J. B. King and T. J. Brazil, "Nonlinear electrothermal GaN HEMT model applied to high-efficiency power amplifier design," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 444–454, Jan. 2013.

[12] J. Xu, R. Jones, S. A. Harris, T. Nielsen, and D. E. Root, "Dynamic FET model—DynaFET—For GaN transistors from NVNA active source injection measurements," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Tampa, FL, USA, Jun. 2014, pp. 1–3.

[13] A. Jarndal and A. Kouki, "Efficient modeling of GaN HEMTs for linear and nonlinear circuits design," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. 30, no. 1, pp. 1–12, Sep. 2015. doi: 10.1002/jnm.2100.

[14] A.-D. Huang, Z. Zhong, W. Wu, and Y.-X. Guo, "An artificial neural network-based electrothermal model for GaN HEMTs with dynamic trapping effects consideration," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 8, pp. 2519–2528, Aug. 2016.

[15] T.-E. Elhamadi, M. Boussouis, N. A. Touhami, and M. Lamsalli, "Neuro-space mapping modeling approach for trapping and self-heating effects on GaAs and GaN devices," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 27, no. 6, 2017, Art. no. e21106.

[16] A. Jarndal, "Combined genetic algorithm and neural network technique for transistor modeling," in *Proc. Int. Conf. Commun., Signal Process., Appl.*, Sharjah, United Arab Emirates, Feb. 2015, pp. 1–4.

[17] A. Jarndal, "Genetic algorithm-based neural-network modeling approach applied to AlGaN/GaN devices," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 23, no. 2, pp. 149–156, 2013.

[18] A. Jarndal, "Neural network electrothermal modeling approach for microwave active devices," *Int. J. RF Microw. Comput.-Aided Eng.*, Mar. 2019, pp. 1–9, Art. no. e21764. doi: 10.1002/mmce.21764.

[19] Q. J. Zhang and K. C. Gupta, *Neural Networks for RF and Microwave Design*. Norwood, MA, USA: Artech House, 2000.

[20] M. Gori and A. Tesi, "On the problem of local minima in backpropagation," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 14, no. 1, pp. 76–86, Jan. 1992.

[21] X. G. Wang, Z. Tang, H. Tamura, and M. Ishii, "A modified error function for the backpropagation algorithm," *Neurocomputing*, vol. 57, pp. 477–484, Mar. 2004.

[22] Q. Dai and N. Liu, "Alleviating the problem of local minima in back-propagation through competitive learning," *Neurocomputing*, vol. 94, pp. 152–158, Oct. 2012.

[23] M. Melanie, *An Introduction to Genetic Algorithms*. Cambridge, MA, USA: MIT Press, 1996.

[24] R. Lossy, N. Chaturvedi, P. Heymann, J. Würfl, S. Müller, K. Köhler, "Large area AlGaN/GaN HEMTs grown on insulating silicon carbide substrates," *Phys. Status Solidi A*, vol. 194, no. 2, pp. 460–463, 2002.

[25] P. H. Ladbrooke, *Pulsed I(V) Measurement of Semiconductor Devices With Applications*. Milpitas, CA, USA: Accent Optical Technologies, 2004.

[26] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001.

[27] C. Miccoli, V. C. Martino, S. Reina, and S. Rinaudo, "Trapping and thermal effects analysis for AlGaN/GaN HEMTs by means of TCAD simulations," *IEEE Electron Device Lett.*, vol. 34, no. 9, pp. 1121–1123, Sep. 2013.
[28] A. Darwish, A. J. Bayba, and H. A. Hung, "Channel temperature analysis of GaN HEMTs with nonlinear thermal conductivity," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 840–846, Mar. 2015.
[29] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001.
[30] A. S. Hussein and A. H. Jarndal, "Reliable hybrid small-signal modeling of GaN HEMTs based on particle-swarm-optimization," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 37, no. 9, pp. 1816–1824, Sep. 2018.
[31] R. Quay, *Gallium Nitride Electronics*. Berlin, Germany: Springer-Verlag, 2008.
[32] S. D. Nsele, L. Escotte, J. Tartarin, S. Piotrowicz, and S. L. Delage, "Broadband frequency dispersion small-signal modeling of the output conductance and transconductance in AlInN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 4, pp. 1372–1378, Apr. 2013.
[33] C. Potier, A. Martin, M. Campovecchio, S. Laurent, R. Quere, J. C. Jacquet, O. Jardel, S. Piotrowicz, and S. Delage, "Trap characterization of microwave GaN HEMTs based on frequency dispersion of the output-admittance," in *Proc. 9th Eur. Microw. Integr. Circuits Conf.*, Rome, Italy, Oct. 2014, pp. 1408–1411.
[34] M. Bouslama, J. Couvidat, A. Al Hajjar, R. Sommet, and J.-C. Nallatamby, "Novel AlN/GaN HEMT electrical model including trapping effects," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millimetre-Wave Circuits*, Brive La Gaillarde, France, Jul. 2018, pp. 1–3.
[35] A. Jarndal and G. Kompa, "A new small-signal modeling approach applied to GaN devices," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 11, pp. 3440–3448, Nov. 2005.
[36] J. C. Pedro and N. B. De Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits*. Norwood, MA, USA: Artech House, 2003.
[37] J. S. Kenney and P. Fedorenko, "Identification of RF power amplifier memory effect origins using third-order intermodulation distortion amplitude and phase asymmetry," in *IEEE MTT-S Int. Microw. Symp. Dig.*, San Francisco, CA, USA, Jun. 2006, pp. 1121–1124.
[38] J. H. K. Vuolevi, T. Rahkonen, and J. P. A. Manninen, "Measurement technique for characterizing memory effects in RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 8, pp. 1383–1389, Aug. 2001.
[39] F. M. Barradas, L. C. Nunes, T. R. Cunha, P. M. Lavrador, P. M. Cabral, and J. C. Pedro, "Compensation of long-term memory effects on GaN HEMT-based power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3379–3388, Sep. 2017.

ANWAR JARNDAL received the Ph.D. degree in electrical engineering from the University of Kassel, Kassel, Germany, in 2006. From 2007 to 2011, he was an Assistant Professor with the Department of Computer Engineering, Hodeidah University, Hodeidah, Yemen. In 2008, he was a Postdoctoral Fellow with the École de Technologie Supérieure, Quebec University, Montreal, QC, Canada. From 2011 to 2013, he was an Assistant Professor with the Department of Electrical and Computer Engineering, University of Nizwa, Nizwa, Oman. He is currently an Associate Professor with the Department of Electrical and Computer Engineering, University of Sharjah, Sharjah, UAE. He has published around 80 internationally peer-reviewed publications. His current research interests include active devices modeling, measurements and characterization techniques, power and low-noise amplifiers design, local and global optimizations, artificial neural networks' modeling, fuzzy logic modeling, and wireless-power-transfer and radio channel modeling. He received the Annual Incentives Award from the University of Sharjah for distinguished faculty in scientific research for the academic year 2018/2019. He is a member of the reviewing boards of many international journals.