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An Interleaved Soft Switching High Step-Up Converter With Low Input Current Ripple and High Efficiency

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ABSTRACT This paper proposes a high step-up low-ripple dc–dc converter for sustainable energy conversion. A high step-up voltage gain is obtained with an input-current doubler and a switched-capacitor circuit rather than having to use a transformer with a high turn ratio. A low input current ripple is achieved since the current ripples of two input inductors cancel each other out when the primary-side branches work in an interleaving way. A low output voltage ripple is got by charging and discharging complementarily with each other of two output capacitors. In addition, the proposed converter achieves zero-voltage switching (ZVS) for all power switches and zero-current switching (ZCS) for all rectifier diodes, which reduces the switching loss significantly. Moreover, an active-clamp capacitor is installed on the input-current doubler to suppress the voltage spike across the switches. A 400-W prototype converter was realized to demonstrate the above-mentioned performance.

INDEX TERMS DC-DC converter, high step-up, low-ripple, ZVS, ZCS, soft switching.

I. INTRODUCTION

Research activities refer to development of environmental-friendly and sustainable energy like solar energy and fuel cell have attracted extensive attention of academia and industry due to the gradual exhaustion of oil energy and the serious environmental pollution [1], [2]. In some low-voltage and high-current applications, such as photovoltaic (PV) power system and fuel cell (FCEL) power system, the DC-DC converter, which is located between the PV panel (or fuel cell unit) and the DC high voltage bus, is the key component to realize energy conversion and power control [3], therefore it is required to obtain a high voltage gain. Among various DC-DC converters, traditional BOOST circuit has the simplest structure. However, though it is suitable for high power applications, it is not suitable for high static gain applications (higher than 5), because its voltage gain is limited by the duty cycle of the driving signal [4]. Moreover, its conversion efficiency is greatly reduced due to the severe-recovery problem of the rectifier diodes. Relatively, the full-bridge DC-DC converter is more suitable for medium and high-power applications.

In order to extend the gain range, some non-isolated topologies such as switched capacitors and switched inductor coupled inductor have been proposed in the literature [5]–[8]. Although, based on the principle of parallel charging series discharge, the switched capacitors converter can obtain higher gain by cascading switched capacitor units. However, the soft start, as well as the ZVS of the switches and the requirement of large capacitor limit its application. In addition, the switched capacitor converter will generate large current ripple at the time of switching, which is not easy to pass EMI test.

Isolation is required in some applications, and the isolate transformers are also used to extend the gain range. Among the isolated topologies, full-bridge DC-DC is commonly used. The voltage-fed converter and the current-fed converter are the two most common kinds of full-bridge DC-DC converters.

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Voltage-fed converters have been usually proposed in the PV power systems [9]–[14], and the most common topology is the phase-shift full-bridge converter (PSFBC) in which one power switch of each bridge is driven complementarily by the other and the phase difference between two bridges keeps at a constant. PSFBC suffers duty-ratio loss on the secondary side and efficiency loss of whole device owing to the circulation currents. Its rectifier diodes also suffer a high voltage surge. Moreover, it needs to use a transformer with high turns ratio to achieve high step-up voltage gain. Furthermore, its input current ripple is really high, which seriously shortens the life span of PV panel (or fuel-cell stack) [15]. The corresponding solutions to inhibit the voltage spike of the power switches and the rectifier diodes are introduced by adding various auxiliary snubber circuits [16]–[21]. Theoretically, each power switch or rectifier diode needs to be equipped with a snubber circuit, which makes the circuit structure terrifically complicated. In addition, the snubber circuit generally reduces the voltage spike by absorbing the leakage energy, which further increases efficiency loss.

Compared with the voltage-fed converter, the current-fed converter is widely applied in PV power system due to its characteristics of high voltage gain and low input current ripple [22]–[26]. Paper [22] proposed a current-fed DC-DC converter with synchronous rectification which achieves ZCS on primary side switches and ZVS on secondary side switches. However, its step-up voltage gain is not high and its switches on secondary side suffer voltage stress of half the output voltage. Paper [23] presented a double-input current-fed DC-DC converter, which achieves ZVS for switches by using a low magnetizing inductance and obtains low-ripple input current with two input inductors, but it suffers high voltage spike across the switches due to the leakage inductor of transformer. It requires a highly symmetrical structure to avoid DC bias magnetization of the transformer. Paper [25] proposed a current-fed DC-DC converter which achieves ZVS and ZCS for power switches, but the reverse-recovery problem of the rectifier diodes has not been solved, causing a low conversion efficiency.

A RCD snubber circuit referred in [27] greatly reduces the voltage spike of the power switches by means of consuming the energy stored in the snubber capacitor by the resistor. However, it causes efficiency loss consequentially. A flyback snubber circuit proposed in [28] greatly suppresses the voltage spike of the power switches and recycles the energy stored in the snubber capacitor as well. However, the complicated structure and the additional controller of the snubber circuit make it unpractical and difficult to be operated on.

The converters using active clamping are also proposed to obtain soft-commutation. Paper [29] uses an active clamping capacitor C_b and a voltage clamping switch Q_2 to realize ZVS of main switch Q_1. The clamping switch is only used to achieve ZVS of Q_1, whereas bring main switch Q_1 high current stress. In addition, this topology has the problem of energy reflow which reduces battery life. Paper [30] uses an interleaved parallel structure to reduce the stress of the main switch, but still needs extra two auxiliary switches to realize the ZVS of the main switch.

To sum up, most of conventional converters either work in hard-switching which will impose a heavy penalty on the efficiency improvement with high frequency operation [31], [32] or even realizes ZVS/ZCS soft switching by operating the switches above the resonant frequency whereas their input current ripples are large which greatly shorten the life span of the front-end components [33], [34].

In order to solve above problems, a high step-up low-ripple DC-DC converter with all power devices at soft switching is proposed in this paper. It is composed of an input-current doubler, a switched-capacitor circuit, a transformer and its parallel inductor. The proposed high step-up current-fed DC-DC converter obtains a high conversion radio when PPAS is employed. Two input inductors of the current doubler minimize the input current ripple. And more, two output capacitors of the switched-capacitor circuit greatly reduce the output voltage ripple of the converter. In addition, the proposed converter achieves ZVS of all power switches through the resonance of their parasitic capacitance and parallel inductance under the control of interleaved PWM scheme [35], [36]. The switched-capacitor circuit is composed of two symmetrical LCD resonant circuits which make sure the rectifier diodes turned off at ZCS condition. Thus high transformation efficiency was obtained. Meanwhile, the rectifier diodes suffer a small voltage and current stress. The simulation and experimental results have validated the fine characteristics of this novel high step-up current-fed DC-DC converter, including with high conversion efficiency and low switching loss.

The paper is organized in the following manner. Section II describes the principle of operation. Section III presents the simulation and experimental results, and section IV draws the conclusion.

II. PRINCIPLE OF OPERATION

The circuit diagram of proposed converter is shown in Fig. 1(a). It is mainly composed of an input-current doubler, a switched-capacitor circuit, a transformer and its parallel inductor. The input-current doubler contains a voltage source V_{in}, two input inductors L_1 and L_2, a clamp capacitor C_c, two main switches S_2 and S_4 together with auxiliary switches S_1 and S_3, and their body diodes D_{S1} to D_{S4} and parasitic capacitors C_{S1} to C_{S4}. The switched-capacitor circuit contains four rectifier diodes D_1 to D_4, a resonant inductor L_{lk}, two resonant capacitors C_{11} and C_{12}, two output capacitors C_{21} and C_{22}, and the load R. The input-current doubler and the switched-capacitor circuit are connected by a transformer T. The parallel inductor L_m is connected to the primary winding of the transformer in parallel.

In order to analyze the operation principle of the converter, the following assumptions are made:

(1) The on-state resistance of the power switches S_1-S_4 are ignored, and the forward voltage of the diodes D_1 - D_4 is assumed to be zero;

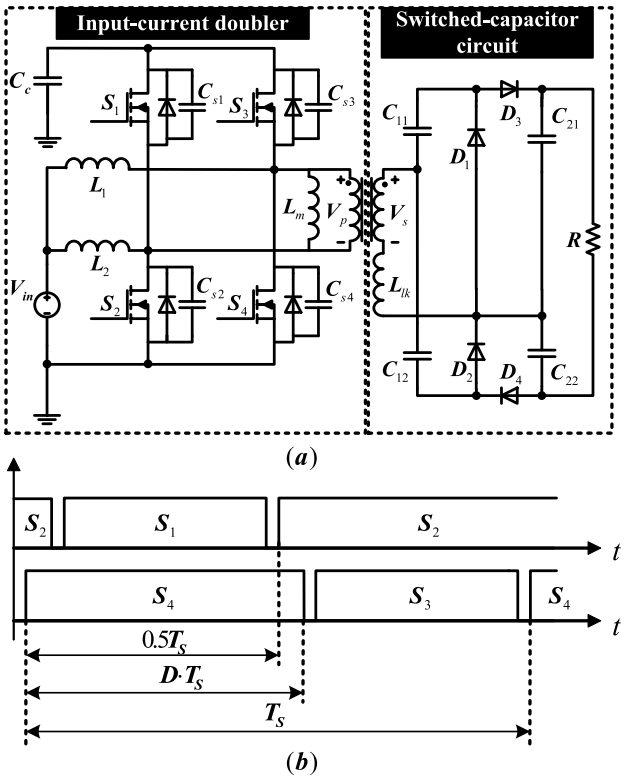

FIGURE 1. The proposed DC-DC converter and its control scheme. (a) The high step-up low-ripple DC-DC converter. (b) The control scheme of pulse-width modulation plus phase angle shift.

(2) The clamping capacitance C_c has a relatively large value, so that its voltage ripple can be neglected;

(3) The magnetizing inductance of the transformer is relatively large, and its magnetizing current is nearly zero, which means the transformer T is equivalent to an ideal transformer with a leakage inductance L_{lk};

(4) All capacitors are considered to be ideal, and the equivalent series resistance (ESR) of the capacitors is assumed to be zero. The resonant capacitance value is identical ($C_{11} = C_{12} = C_1$), and the output capacitors have the same value ($C_{21} = C_{22} = C_2$).

A. MODAL ANALYSIS & SOFT SWITCHING REALIZATION

The pulse-width modulation plus phase angle shift is employed as the control scheme for the proposed converter, as shown in Fig. 1(b), where, D is duty cycle of the main switches S_2 and S_4, and T_s is the switching period. It is noted that one power switch S_1 (or S_3) of each bridge is driven complementarily by the other S_2 (or S_4), and the phase difference between two bridges keeps 180°. The duty cycle is the control parameter which is set to 0.5 for normally input/output in this paper in order to minimize the input current ripple.

The steady-state operation of the proposed converter can be divided into 14 stages during a switching period. The equivalent circuits and waveforms in each stage are shown in Fig. 2 and Fig. 3, respectively. The presentation of ZVS for all power switches and ZCS for all rectifier diodes is included in following modal analysis:

Stage 1 [t_0-t_1]: As shown in Fig. 2(a), S_4 is turned on at t_0, i_{L1} flows through the switch S_4 and the inductor L_m, and i_{L2} flows through the switch S_2. Since the main switches S_2 and S_4 are in the on-state, the voltage v_p across the primary winding of the transformer is zero, and the current i_L of the inductor L_m nearly keeps constant. The currents on both the primary and secondary sides of the transformer are zero. During this stage, the inductor currents i_{L1} and i_{L2} increase linearly as follows:

$$i_{L_1}(t) = i_{L_1}(t_0) + \frac{V_{in}}{L_1}(t - t_0), \tag{1}$$

$$i_{L_2}(t) = i_{L_2}(t_0) + \frac{V_{in}}{L_2}(t - t_0), \tag{2}$$

where, V_{in} is a DC voltage source, e.g. the output voltage of a PV panel.

A circulation loop is formed by the output capacitors C_{21}, C_{22} and the load R. The output capacitor voltage V_{C21} and V_{C22} can be calculated as follows:

$$v_{c_{21}}(t) = v_{c_{21}}(t_0) - \frac{I_0}{c_2}(t - t_0), \tag{3}$$

$$v_{c_{22}}(t) = v_{c_{22}}(t_0) - \frac{I_0}{c_2}(t - t_0), \tag{4}$$

where, I_o is the output current of the converter.

Stage 2 [t_1-t_2]: As shown in Fig. 2 (b), S_2 is turned off at t_1, i_{L2} begins to charge C_{s2} and discharge C_{s1} linearly. C_{s1} ends discharging when C_{s2} is charged to V_{Cc}. The voltage across the primary winding of the transformer rapidly increases to -V_{Cc} in this stage.

Stage 3 [t_2-t_3]: As shown in Fig. 2(c), after i_{L2} fully charges C_{s2} to V_{Cc} and discharge C_{s1} to zero, the current flows through the anti-parallel diode of S_1, which ensures that S_1 will be turned on under ZVS in the next stage. The inductor L_m keeps discharging and i_L keeps decreasing.

Stage 4 [t_3-t_4]: As shown in Fig. 2(d), S_1 is turned on under ZVS at t_3, the voltage across the primary winding of the transformer nearly keeps $v_p = -V_{Cc}$. i_{L1} still increases linearly as in (1), and i_{L2} decreases linearly as follow:

$$i_{L_2}(t) = i_{L_2}(t_3) + \frac{V_{in} - V_{C_C}}{L_2}(t - t_3). \tag{5}$$

During t_1 to t_4, i_L can be calculated by:

$$i_L(t) = i_L(t_1) - \frac{v_{c_c}}{L_m}(t - t_1). \tag{6}$$

The secondary winding voltage of the transformer is:

$$v_s = -N \times V_{c_{c'}} \tag{7}$$

where, N is turns ratio of the transformer, and $N = N_2/N_1$. Two resonant loops are formed during this stage, L_{lk}, C_{11}, D_1, and L_{lk}, C_{12}, D_4,C_{22}, respectively. The resonant capacitor C_{11} is charged by v_s, and C_{22} is charged by v_s in series with C_{12}.

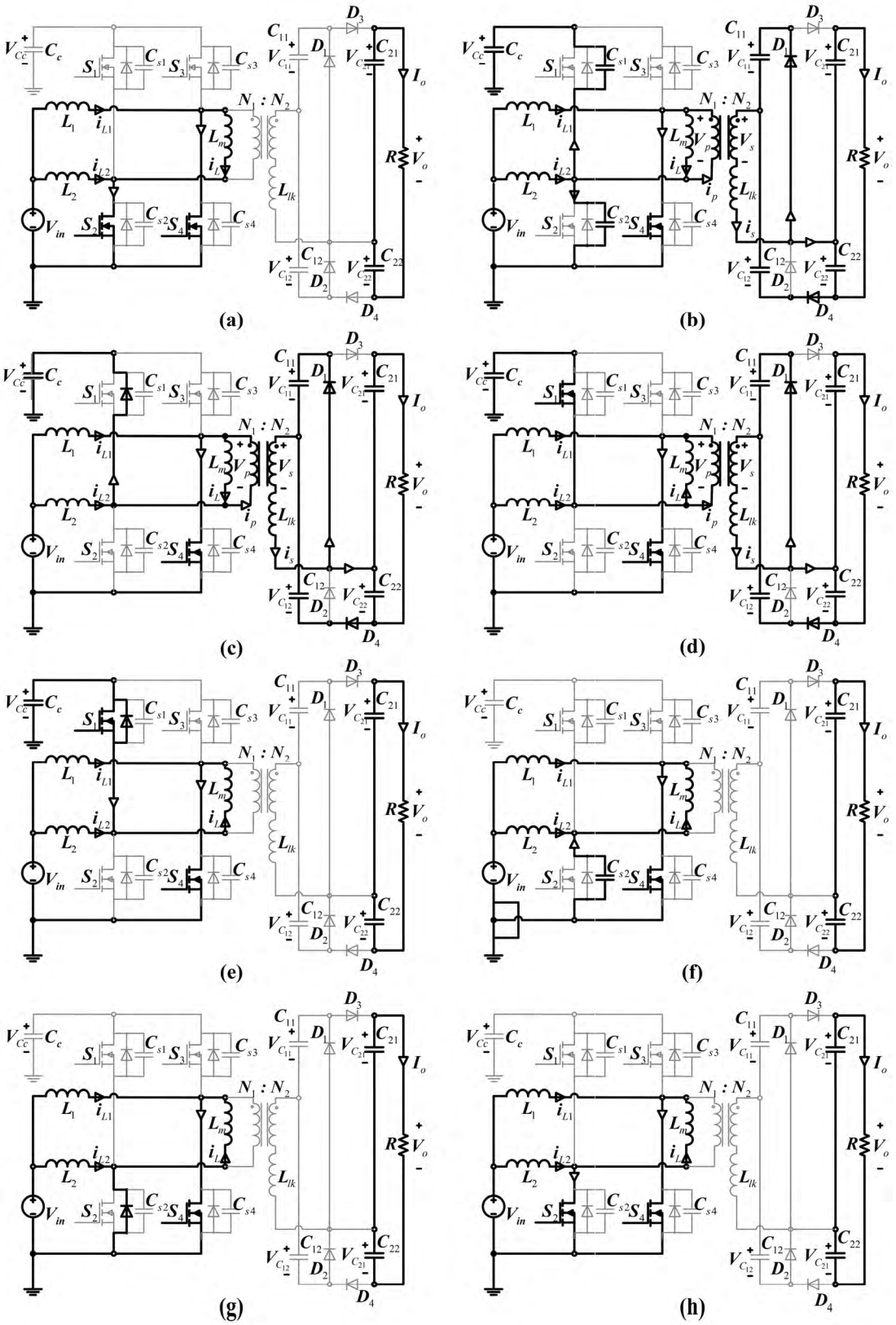

FIGURE 2. Operation stages of the proposed converter. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6. (g) Stage 7. (h) Stage 8.

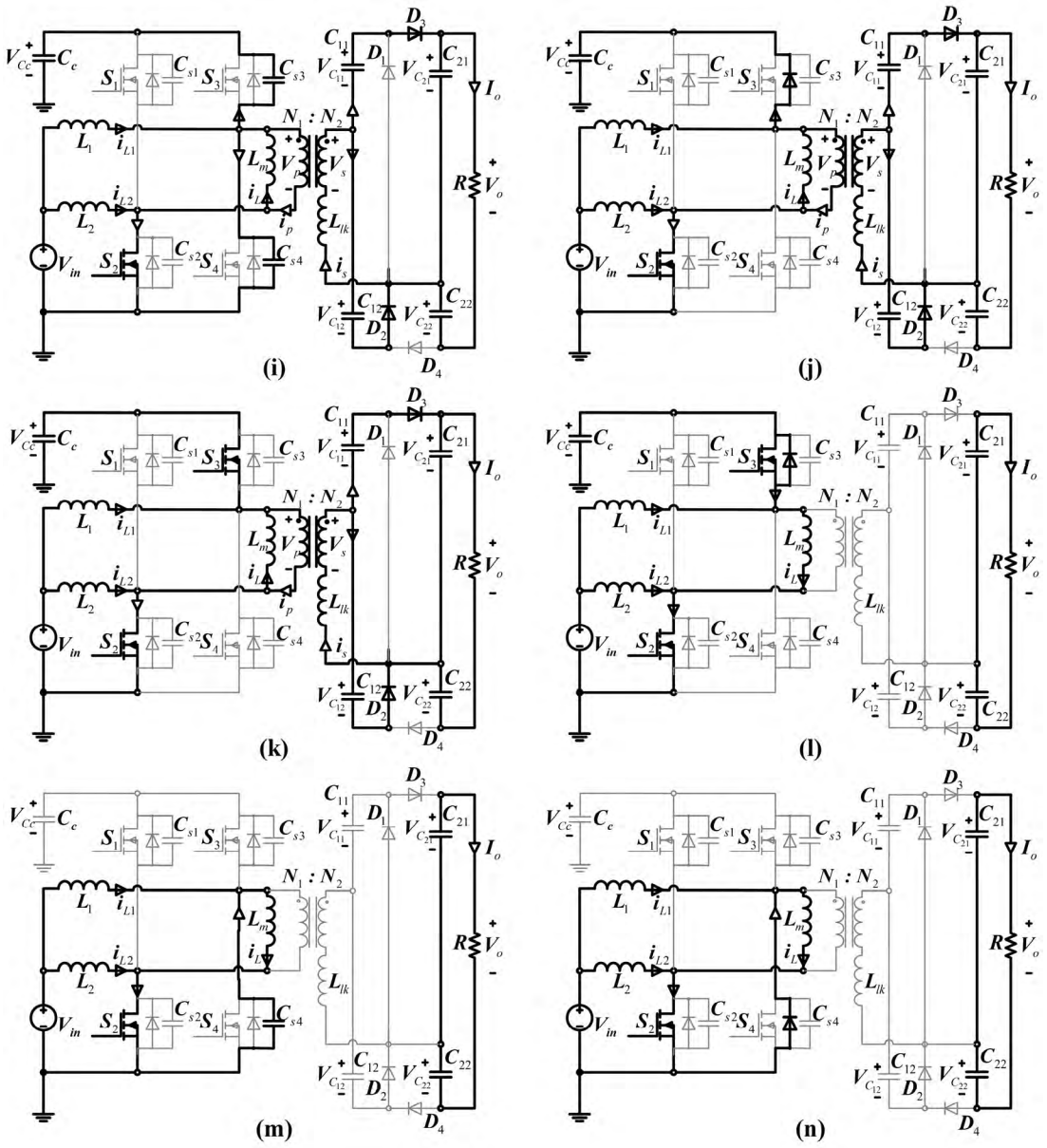

FIGURE 2. *(Continued.)* **Operation stages of the proposed converter. (i) Stage 9. (j) Stage 10. (k) Stage 11. (l) Stage 12. (m) Stage 13. (n) Stage 14.**

The state formulas can be written as follows:

$$N \times V_{C_c} = V_{C_{11}}(t) + L_{lk}\frac{di_s(t)}{dt}, \tag{8}$$

$$i_s = 2C_1\frac{dv_{C_{11}(t)}}{dt}, \tag{9}$$

$v_{C_{11}}, v_{C_{12}}$ and i_s can be obtained as follows:

$$v_{C_{11}}(t) = N \times V_{C_c} - \left[N \times V_{C_c} - v_{C_{11}}(t_1)\right] cos\omega_0 (t - t_1), \tag{10}$$

$$v_{C_{12}}(t) = N \times V_{C_c} + \left[N \times V_{C_c} - v_{C_{11}}(t_1)\right] cos\omega_0 (t - t_1), \tag{11}$$

$$i_s = \frac{N \times V_c - v_{C_{11}}(t_1)}{z_0} sin\omega_0 (t - t_1) = I_m sin\omega_0 (t - t_1). \tag{12}$$

The angular frequency ω_0 and the resonant impedance Z_0 are given by:

$$\begin{cases} \omega_0 = \dfrac{1}{\sqrt{2L_{lk}C_1}} \\ Z_0 = \sqrt{\dfrac{L_{lk}}{2C_1}} \end{cases} \tag{13}$$

The peak current on the secondary winding of the transformer I_m can be obtained as:

$$I_m = I_0\omega_0 T_S. \tag{14}$$

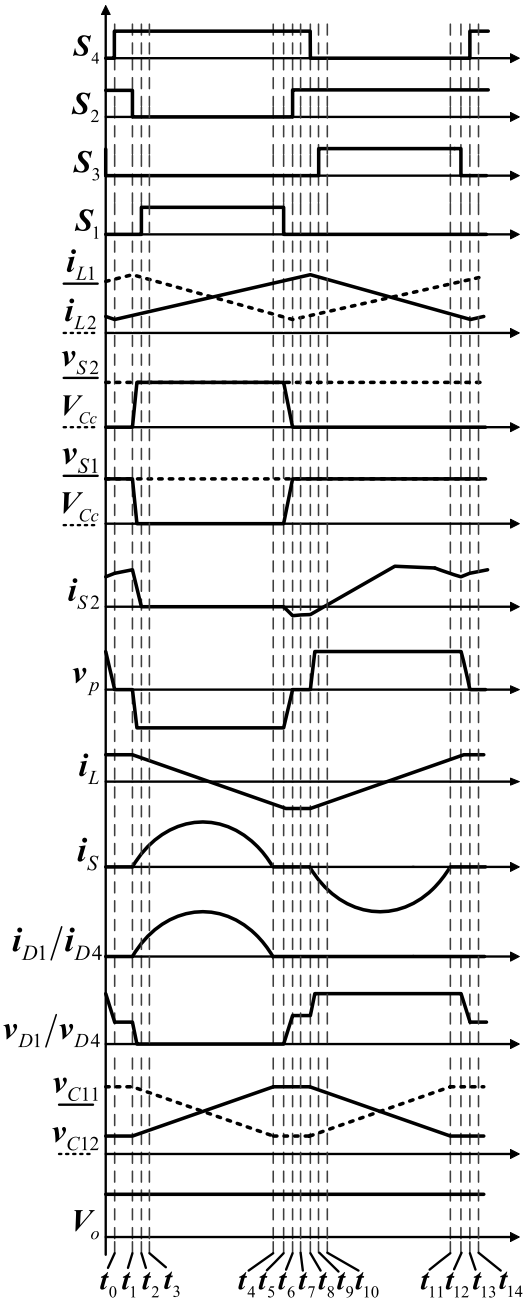

FIGURE 3. The key waveforms of the proposed converter.

$v_{C_{21}}$ still decreases linearly as in (3), and $v_{C_{22}}$ increases as follow:

$$v_{C_{22}}(t) = v_{C_{22}}(t_1) + \int_{t_1}^{t} \frac{0.5i_s - I_0}{c_2} dt. \tag{15}$$

Stage 5 [t_4-t_5]: As shown in Fig. 2(e), two resonant loops L_{lk}, C_{11}, D_1 and L_{lk}, C_{12}, D_4,C_{22}, end their resonance state at t_4. The current of the transformer decreases to zero, and the currents i_{D1}-i_{D4} of D_1-D_4 also decrease to zero. The diodes D_1-D_4 turn off under ZCS. i_{L1} increases linearly as in (1), and i_{L2} decreases linearly as in (5). L_m experiences two processes during t_2 to t_5, first forward being discharged and then reverse being charged, respectively. i_L is varying linearly as in (6).

Stage 6 [t_5-t_6]: As shown in Fig. 2(f), S_1 is turned off at t_5. C_{S2} discharges through L_m and C_{S1} is charged in parallel. Thus, L_m is reversely charged, and i_L reversely increases. In this stage, the voltage across the primary winding of the transformer decreases from -V_{Cc} to zero rapidly.

Stage 7 [t_6-t_7]: As shown in Fig. 2(g), after C_{S2} discharge to zero and C_{S1} is fully charged to V_{Cc}, the current flows through the anti-parallel diode of S_2, which ensures that S_2 can be turned on under ZVS in the next stage. i_L keeps a reverse constant current.

S_2 is turned on under ZVS at t_7. Due to the symmetry of the circuit topology, the steady-state operations of stage 8 to stage 14 are similar to those of stage 1 to stage 7, as shown in Fig. 2 (h) to Fig. 2 (n), respectively. The steady-state at t_{14} is completely consistent with that at t_0, so that the circuit will return to stage 1 over and over again after each period.

B. PERFORMANCE ANALYSIS

1) VOLTAGE GAIN

The volt-second balance law of L_1 during one switching period determines the relationship between V_{in} and V_{Cc} as follows:

$$V_{in} \times D + \left(V_{in} - V_{C_c}\right)(1 - D) = 0. \tag{16}$$

Thus, it can be deduced as:

$$\frac{V_{Cc}}{V_{in}} = \frac{1}{1 - D^*} \tag{17}$$

The volt-second balance law of L_{lk} during one switching period determines the relationship between the resonant capacitor average voltage V_{C11} and V_o as follow:

$$\left(V_{C_{11}} + N \times V_{C_c} - 0.5V_0\right)\frac{T_0}{2} + \left(V_{C_{11}} - N \times V_{C_c}\right)\frac{T_0}{2} = 0, \tag{18}$$

where, T_0 is the resonant period. The average voltages of the resonant capacitors V_{C11} and V_{C12} are obtained as follow in view of the symmetrical circuit:

$$V_{C_{11}} = V_{C_{12}} = 0.25V_0. \tag{19}$$

Since the average voltage V_{C11} is equal to the amplitude of v_s, and the amplitude of v_p is equal to V_{Cc}, it can be deduced that the relationship between V_{Cc} and V_o should be:

$$V_{C_c} = \frac{V_0}{4N} \tag{20}$$

By combining (17) and (20), it can be deduced that the relationship between input and output voltages is:

$$\frac{V_0}{V_{in}} = N\frac{4}{1 - D}. \tag{21}$$

Based on the above analysis, the output voltage can be adjusted by the duty ratio D. Since the characteristics of interleaved parallel, when the duty cycle is not equal to 0.5 the input current ripple becomes large.

2) INPUT CURRENT RIPPLE

Assuming that the input inductors L_1 and L_2 have the same value, the input current ripple is:

$$\Delta I_{in} = \Delta i_{L_1} + \Delta i_{L_2} = \frac{(2D-1)(1-D)T_S}{L_1} \times V_{C_c}. \quad (22)$$

When the duty cycle D=*2/3*, the input current ripple is the maximum, being:

$$\Delta I_{in,max} = \frac{V_{C_c} T_s}{9L_1} = \frac{V_0 T_s}{36NL_1}. \quad (23)$$

3) OUTPUT VOLTAGE RIPPLE

Taking the operation of the half switching period t_0 to t_7 for example, the current of resonance loop L_{lk}, C_{12}, D_4,C_{22} is equal to I_o at a time point τ_1 and a time point τ_2. This current is larger than I_o during τ_1 to τ_2, so V_{C22} keeps increasing and the output voltage keeps increasing too. The output voltage keeps decreasing during other time of the half switching period. The cycle of the output voltage is repeated every half switching period. Thus, the steady output voltage ripple is equal to the output voltage ripple during τ_1 to τ_2, being:

$$\Delta V_o = \Delta V_{C_{21}} + \Delta V_{C_{22}}. \quad (24)$$

The voltage ripples of the output capacitors C_{21} and C_{22} can be calculated as in (25) and (26), respectively.

$$\Delta V_{C_{21}} = \frac{1}{C_2} \int_{\tau_1}^{\tau_2} (-I_o)\, dt, \quad (25)$$

$$\Delta V_{C_{22}} = \frac{1}{C_2} \int_{\tau_1}^{\tau_2} \left(\frac{1}{2} i_s - I_o\right) dt. \quad (26)$$

It can be obtained by combining (24), (25) and (26) that:

$$\Delta V_o = \frac{I_0}{C_2} \left(\frac{cos\theta}{f_s} - \frac{1}{f_0} + \frac{2\theta}{\pi f_o}\right) \quad (27)$$

where, $\theta = sin^{-1}(f_s/\pi f_0)$. It is obvious that the output voltage ripple ΔV_o is inversely proportional to the output capacitance C_2 when other circuit parameters are fixed.

4) DESIGN CRITERIA OF L_M

In order to realize zero voltage turn on (ZVS) of S_2, S_4, a discharge loop for C_{S2} and C_{S4} is provided by the inductor L_m after S_1 and S_3 are turned off. Consequently, after S_1 and S_3 are turned off, it is required that the currents in the input inductors L_1 and L_2 are smaller than that of parallel inductor L_m, then:

$$i_{L_m,max} > i_{L1,min}, \quad (28)$$

$$-i_{L_m,min} > i_{L2,min}. \quad (29)$$

By adding (28) and (29), it obtained:

$$i_{L_m,m\ ax} - i_{L_m,min} > i_{L1,min} + i_{L2,min} = 2i_{L1,m\ in} \quad (30)$$

The left term of (30) can be expressed as:

$$i_{L_m,max} - i_{L_m,min} = \Delta i_L = \frac{V_P}{L}(1-D) \cdot T_S$$

$$= \frac{V_P}{L}(1-D) \cdot T_S \quad (31)$$

The right term of (30) can be expressed by (32), where I_{L1} (I_{L2}) is the average current of the inductor L_1 (L_2). Since the circuit structure is symmetrical, the average currents I_{L1} and I_{L2} are equal, as (33) showed.

$$i_{L1,min} = I_{L1} - 0.5\Delta i_{L1}, \quad (32)$$

$$I_{L1} = I_{L2} = 0.5 I_{in}. \quad (33)$$

Δi_{L1} is the ripple of input inductor L_1, it can be expressed by:

$$\Delta i_{L1} = \frac{V_{in}}{L_1} D \cdot T_S \quad (34)$$

From the formula (28) to (34), the value of L_m can be obtained.

5) PERFORMANCE ANALYSIS

A 400-W design case of the proposed converter is presented as an example in this paper. The parameters of the prototype are as follows: input voltage V_{in}= 25V, power P=*400W*, switching frequency f_s = 50kHz, and leakage inductance L_{lk} = 0.9μH. By applying formula (28-34), when the value of L_m is smaller than 24uH, ZVS can be achieved under duty cycle D = 0.5. In order to improve the ZVS range, we choose L_m = 15uH.

The performance analysis was carried out on the converter, as shown in Fig. 4.

Fig. 4(a) shows the change of voltage gain according to the duty cycle D with the transformer ratio n=*1*, n=*2*,n=*3*, respectively. The voltage gain increases with the duty cycle when the transformer ratio is fixed, and it can get a voltage gain larger than 10 times readily when the duty cycle is 0.5. Fig. 4(b) shows the change of input current ripple according to the input inductance with the transformer ratio n=*1* and the duty cycles D = 0.5, D = 0.6, D = 2/3, respectively. The input current ripple decreases with the increasing of the input inductance, and it is identically equal to zero when the duty cycle D = 0.5. Fig. 4(c) presents the change of output voltage ripple according to the output capacitance when the transformer ratio n=*1* and the duty cycle is D = 0.5. The red points present the output voltage ripple under several typical output capacitances. The output voltage ripple decreases with the increasing of the output capacitance, and the output voltage ripple less than 1V is relatively easy to be obtained.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The simulation was carried out with the software Saber (@Synopsys, Inc) in this section. The simulation parameters are shown in Table 1.

Fig. 5 presents the simulation waveforms of proposed converter. The simulation waveforms are consistent with the theoretical waveforms shown in Fig. 3, which verifies the principle of the proposed converter and the feasibility of the operation. Moreover, soft switching of all switches and

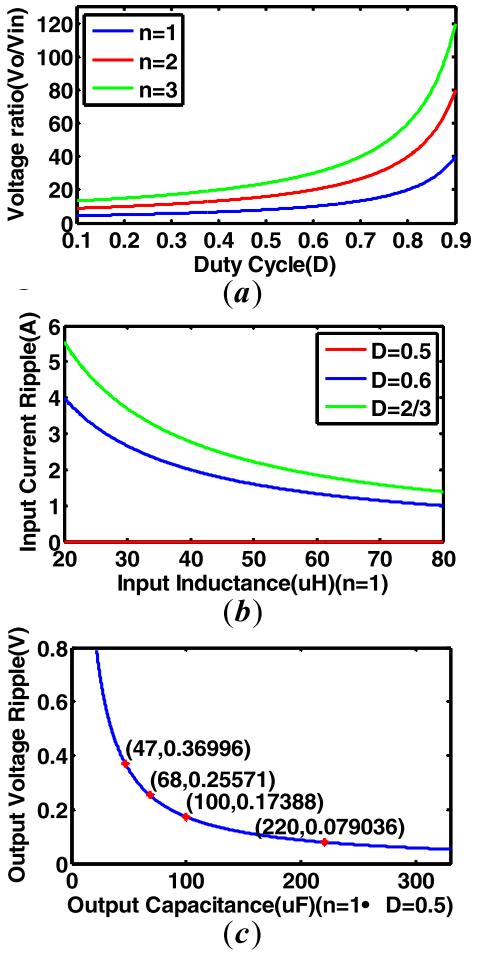

FIGURE 4. Performance analysis of the converter. (a) Voltage gain according to duty cycle. (b) Input current ripple according to input inductance. (c) Output voltage ripple according to output capacitance.

TABLE 1. Simulation parameters of proposed converter.

Parameter	Value
Power (P)	$400W$
Input voltage (V_{in})	$25V$
Switching frequency (f_S)	$50kHz$
Input inductor (L_1=L_2)	$68\mu H$
Parasitic capacitance ($C_{s1}-C_{s4}$)	$2.2nF$
Clamp capacitor (C_C)	$22\mu F$
Leakage inductance (L_{lk})	$0.9\mu H$
Transformer ratio (N)	1:1
Parallel inductor (L_m)	$15\mu H$
Resonant capacitance (C_{11}=C_{12})	$2\mu F$
Output capacitance (C_{21}=C_{22})	$220\mu F$

all rectifier diodes is validated. The ZVS realization of S_2 and S_1 is shown in Fig. 5 as marked by red ellipses. The analysis is as follow: C_{S2} is charged by i_{L2} after S_2 is turned off; due to the clamping function of C_c, v_{ds2} increases to V_{Cc} and then keeps on at this value, which ensures S_1 turn on and off under ZVS; C_{S2} discharges through L_m after S_1 is turned off, and v_{ds2} decreases to zero, which ensures S_2 turn on and off under ZVS. The ZCS realization of D_1 and D_4 is shown in Fig. 5 as marked by green ellipse. It is obvious that the current across the diodes decreases to zero before the rectifier diodes are reverse biased, which means the rectifier diodes reaching ZCS turn-off condition. Thus, the reverse-recovery problem has been solved on proposed converter.

Fig. 6 presents the input current and output voltage waveforms. The output voltage reaches about *200V*, 8 times larger than the input voltage. The output voltage ripple ΔV_o is *0.051V*, which is small as *0.03%* of the output voltage. The input current is *16.15A*. The input current ripple ΔI_{in} is *0.0017A*, which is about *0.01%* of the input current. Hence, the low-ripple input current is obtained.

B. EXPERIMENTAL RESULTS

The hardware prototype of proposed converter with its control system is shown in Fig. 7. The control system is composed of a signal generator (by TMS320F2812), an auxiliary power source and an isolated driving circuit. Where, TMS320F2812 provides 4 ways of PWM output with the frequency of *50kHz* which are fed to the isolated driver, and then two IR2110s generate two pairs of driving signals for two switch bridges, respectively. The proposed converter is mainly composed of an input-current doubler, a switched-capacitor circuit, a transformer and its parallel inductor. A DC power supply provides the input voltage of the input-current doubler, and a *100*Ω ceramic resistor connected to the output port of the switched-capacitor circuit serves as the load. The component models of the proposed converter are listed in Table 2.

TABLE 2. Parameters of the prototype.

Parameters/Specification	Value
U_i	$25\ V$
F_s	$50\ kHz$
$P_{out}/V_{out}/I_{out}$	$400W/200V/2A$
Input inductor (L_1=L_2)	$68\mu H$
Power switches (S_1-S_4)	*IRF*3710
Parasitic capacitance ($C_{s1}-C_{s4}$)	*222J*
Clamp capacitor (C_c)	$22\mu F$
Parallel inductor (L)	$15\mu H$
Resonant capacitance (C_{11}=C_{12})	$2\mu F$
Rectifier Diode (D_1-D_4)	*HER*308
Output capacitance (C_{21}=C_{22})	$220\mu F$

Fig. 8(a) and (b) present the measured voltage and current waveforms of S_1 and S_2 respectively. The amplitude of the measured voltages V_{ds1} and V_{ds2} is around *50V*, which agrees with the theoretical one calculated according to (17).

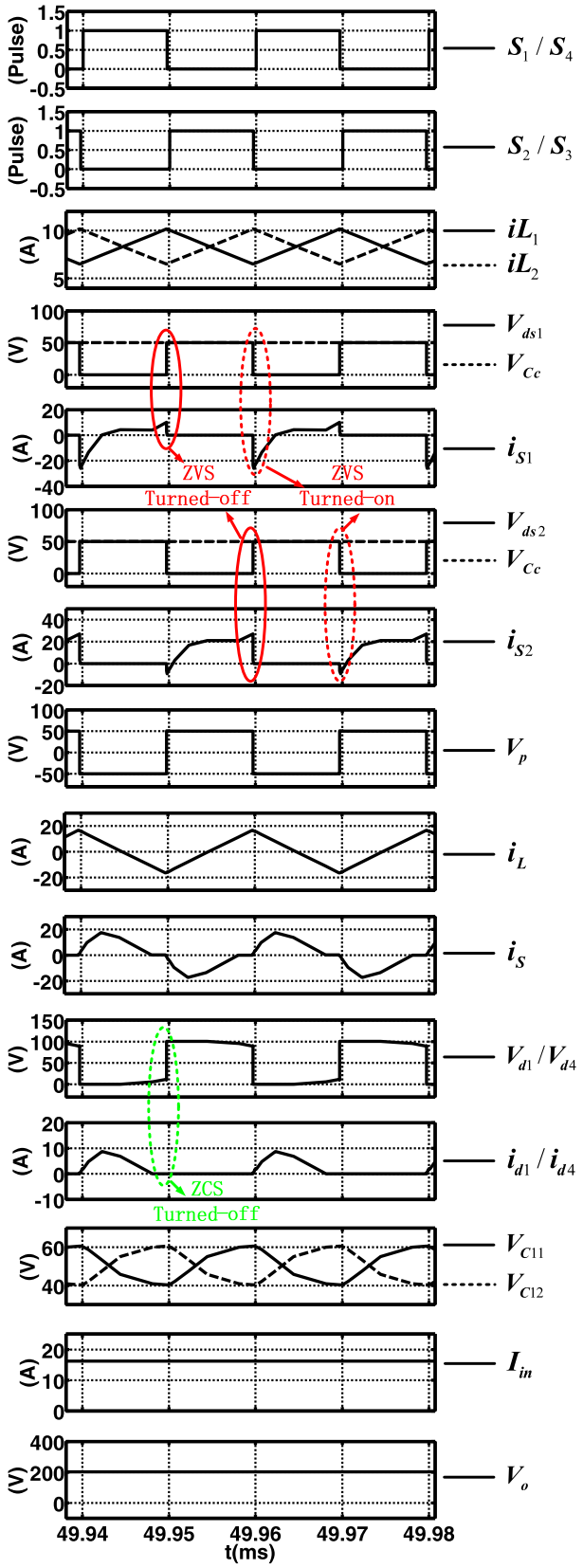

FIGURE 5. Simulation waveforms.

In addition, S_1 and S_2 are turned on and off under ZVS. Similarly, S_3 and S_4 also realized its ZVS switching. Fig. 8(c) and (d) present the measured voltage and current

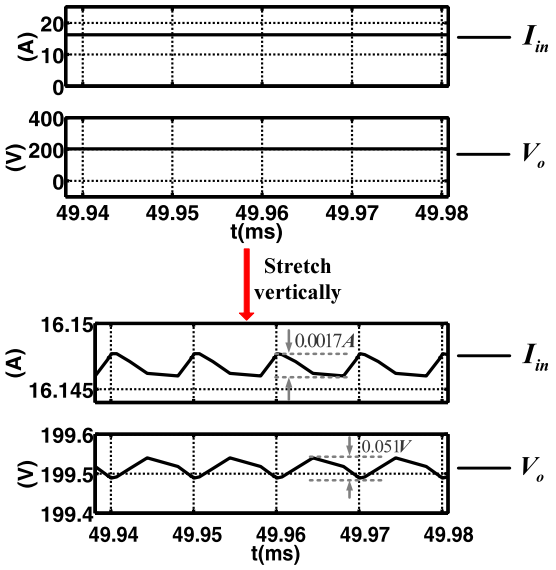

FIGURE 6. Simulation waveforms of the input current and the output voltage.

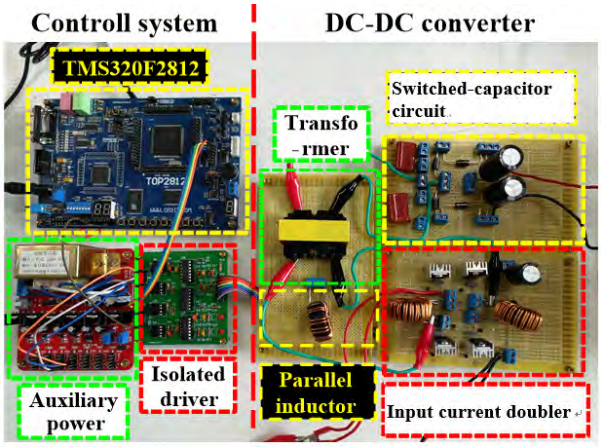

FIGURE 7. Hardware prototype of the proposed converter.

waveforms of the rectifier diodes D_3 and D_4, respectively. It shows that i_{D3} and i_{D4} decreased to zero before the diodes D_3 and D_4 are reverse biased, which means that the rectifier diodes D_3 and D_4 are turned off at ZCS conditions. Hence, the reverse-recovery problem of the rectifier diodes is removed on the proposed converter.

Fig. 9(a) shows the input voltage and current waveforms. The input current ripple is measured to be about *30mA*. It is almost ripple free due to two input inductors working in an interleaved way to be charged and discharged. Fig. 9(b) presents the output voltage and current waveforms. It is noted that the output voltage drops to *192V* from the theoretical *200V*. The voltage drop includes the MOSFETs voltage drop and the rectifier diodes voltage drop. The output voltage ripple is measured to be *0.8V*. It is relatively low due to the alternate charging and discharging of the output capacitors. Both the input current ripple and the output voltage ripple are

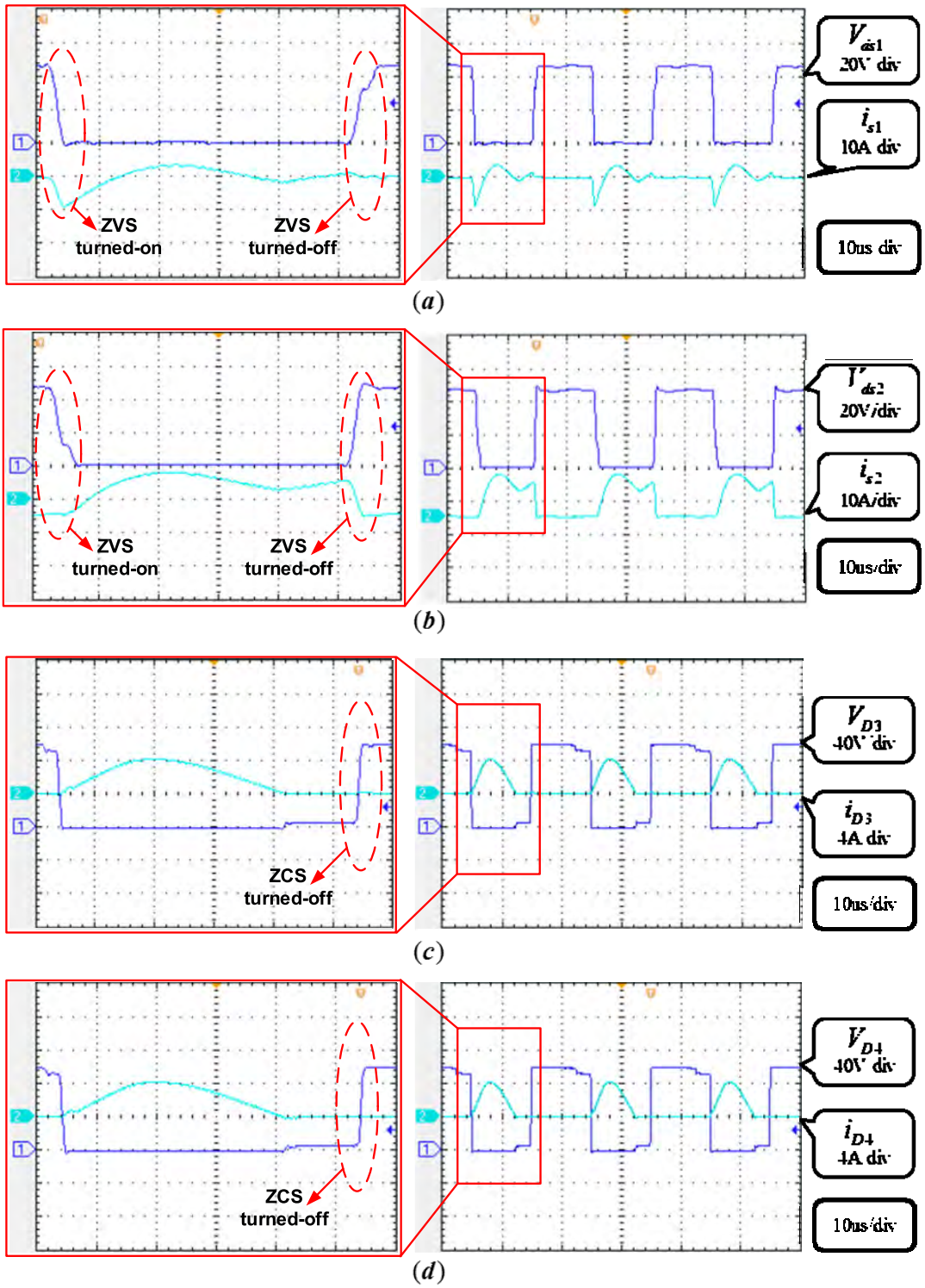

FIGURE 8. The measured drain voltage and current waveforms of switching components. (a) Auxiliary switch S_1. (b) Main switch S_2. (c) Rectifier diode D_3. (d) Rectifier diode D_4.

measured to be larger than the simulation results due to the incomplete symmetry of the hardware prototype.

Fig. 10(a) shows the measured voltage and current waveforms across the primary windings of the transformer and its parallel inductor, which is basically consistent with the theoretical analysis results. The parallel inductor current increases linearly when the voltage is positive, and it decreases linearly when the voltage is negative.

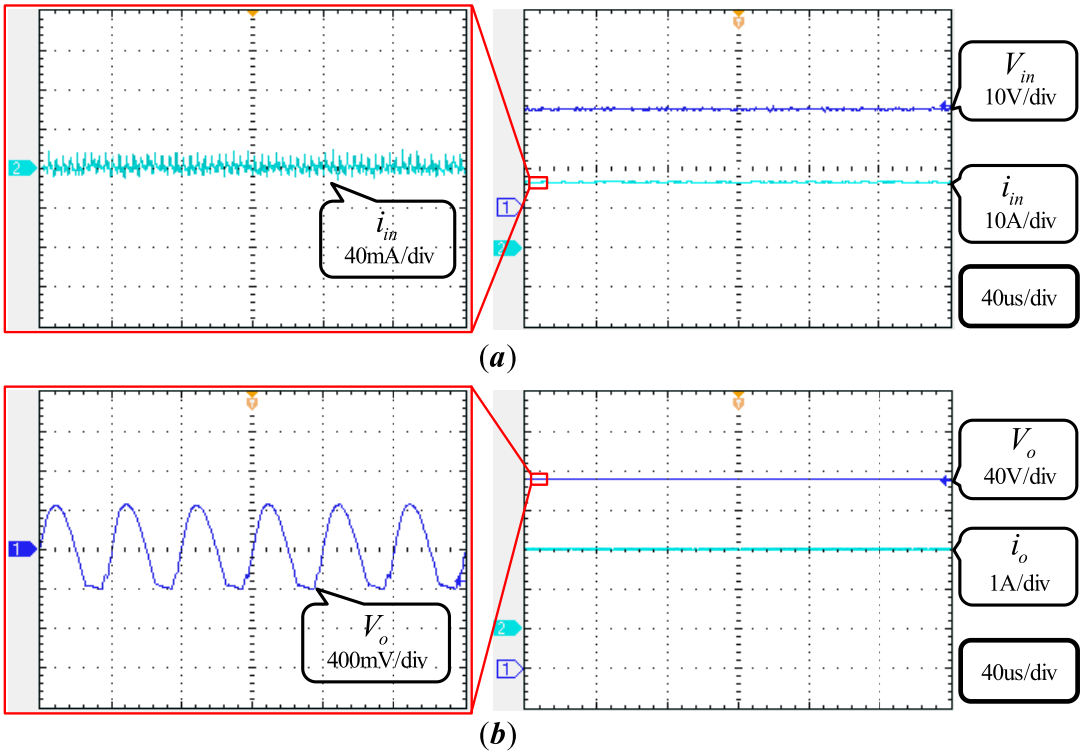

FIGURE 9. Input and output characteristic of the proposed converter. (a) Input voltage and current waveforms. (b) Output voltage and current waveforms.

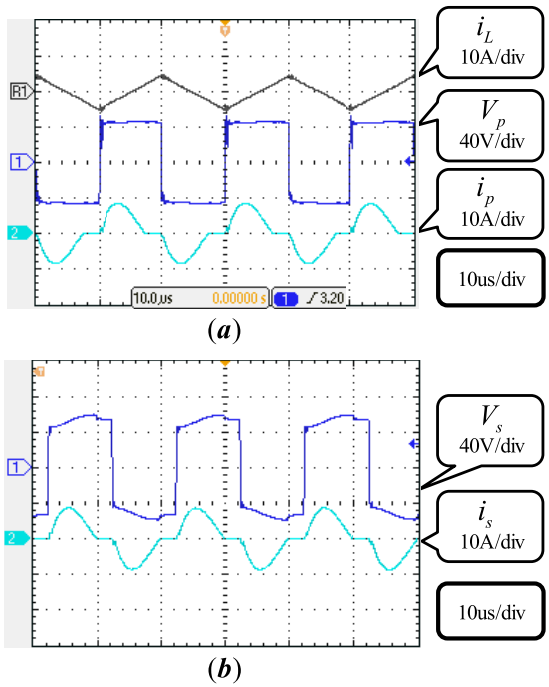

FIGURE 10. The measured voltage and current waveforms of the transformer and its parallel inductor. (a) The primary winding of the transformer and its parallel inductor. (b)The secondary winding of the transformer.

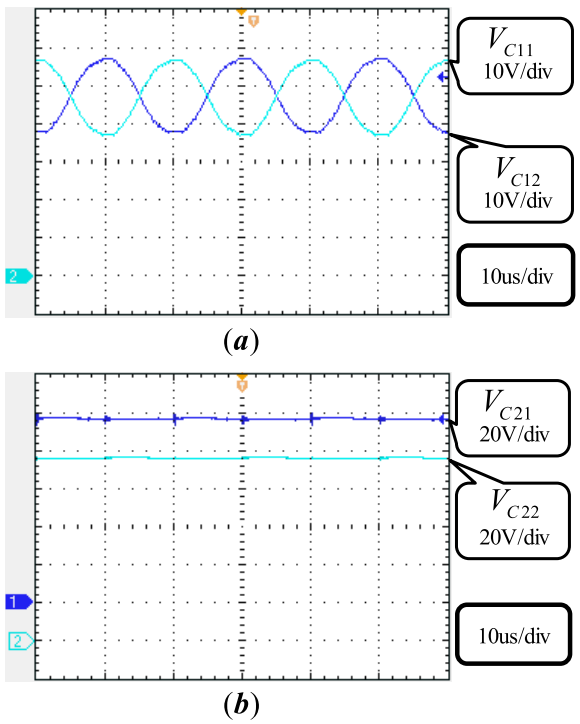

FIGURE 11. The measured voltage waveforms of the switched-capacitors. (a) C_{11} and C_{12}. (b) C_{21} and C_{22}.

Fig. 10(b) presents the measured voltage and current waveforms across the secondary windings of the transformer. It's remarkable that a slight high-frequency resonance occurs on voltage waveforms as shown in Fig. 10(a) and (b) due to the existence of the parasitic capacitance on the transformer.

TABLE 3. Comparison of conventional converters and proposed converter.

Topology	Current-fed full-bridge with synchronous rectification [22]	Bidirectional current-fed isolated full-bridge [24]	Interleaved current-fed full-bridge [37]	Proposed converter
Inductors	1	1	2	3
Capacitors	3	2	5	5
Switches	6	10	12	4
Diodes	0	0	0	4
Transformers	1	1	2	1
Input-current ripple	Low (2.2%)	High (6%)	Low (1%)	0 (D=0.5)
Maximum voltage stress	$\geq \frac{V_o}{4}$	$\frac{V_o}{2N}$	$\geq \frac{V_o}{4}$	$\frac{V_o}{4N}$
Voltage gain	$\frac{N}{1-D}$	$\frac{2N}{1-D}$	$\frac{2N}{1-D}$	$\frac{4N}{1-D}$
Soft switching	ZCS or ZVS	ZCS	ZCS or ZVS	ZCS/ZVS
Circuit design	Simple	Complex	Complex	Simple
Efficiency	/	96.1%	93.3%	96.8%

Fig. 11(a) presents the measured voltage waveforms of the resonant capacitors C_{11} and C_{12}. The voltages v_{C11} and v_{C12} fluctuate sinusoidally in a small fixed range, which are consistent with the theoretical analysis results in section 2.1. Fig. 11(b) shows the measured voltage waveforms of the output capacitors C_{21} and C_{22}. Since the output capacitors C_{21} and C_{22} have relatively large capacitances, the voltage V_{C21} and V_{C22} are approximate to a constant. The output voltage is calculated to be *200V* according to (21), so the theoretical value of voltages V_{C21} and V_{C22} should be *100V* at each. As shown in Fig. 11(b), the measured value of voltages V_{C21} and V_{C22} is about *97V*, which is nearly in line with the theoretical one.

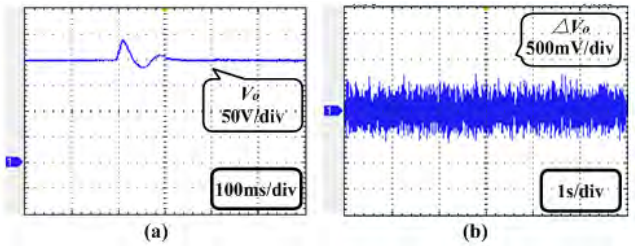

FIGURE 12. Experimental results of the control operation for a load transient. The load was changed from 100Ω to 200Ω. (a) The output voltage. (b) The output ripple.

Fig. 12 presents the close-loop response waveforms under the load changed from 100Ω to 200Ω, where the PID controller is used. The DC output voltage returns to 200V within 0.1s after the load is switched.

The theoretical and measured efficiency of proposed converter under different load conditions is shown in Fig. 13. The maximum measured efficiency occurs up to 96.8% at 300-W load, and the efficiency is 94.7% at 400-W load. The proposed converter achieves a high efficiency due to ZVS realization of all power switches and ZCS realization of all rectifier diodes. The efficiency is relatively low at a light load. The degradation is due to the increase of conduction loss weight with the decrease of PV voltage.

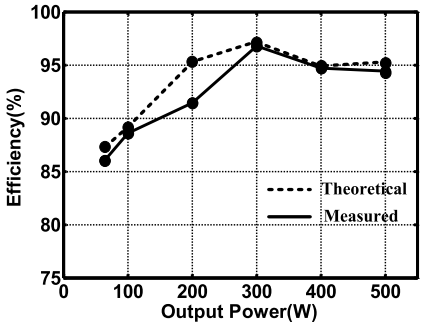

FIGURE 13. Theoretical and measured efficiency under different load conditions.

Table 3 gives a comparison of four different current-fed converters in terms of the number of components, input-current ripple, voltage stress, voltage gain and soft-switching realization, etc. It's obvious that the voltage gain of the proposed converter is four times higher than that of the converter in [22], and twice higher than that of the converters in [24] and [37]. In addition, the voltage stress of the proposed converter is a half of that of the converter in [22], and less than one out of N of that of the converters in [24] and [37]. Moreover, the proposed converter achieves a low-ripple input current when the duty cycle $D = 0.5$ according to (22), compared with 2.2%, more than 6%, and 1% in [22], [24], and [37], respectively.

Furthermore, the proposed converter achieves ZVS turned on and off for all power switches and ZCS turned-off for all rectifier diodes which lead to high converter efficiency (up to 96.8%) while other converters only realize ZCS turned-off or ZVS turned-on condition of each switch. Compared to the converters in [22], [24] and [37], the proposed converter requires less number of power switches. Therefore, the main circuit and its driving circuit are simplified greatly, which makes the circuit design much easier and get low cost.

IV. CONCLUSION

This paper presented a high step-up low-ripple DC-DC converter and its realization of soft switching. The simulation analysis and experiment results have verified that the proposed converter has the following obvious advantages: (1) It has high voltage gain. The output voltage is 10 times larger than the input voltage when the transformer ratio is just 1, which determines the proposed converter is appropriate for low input-voltage and high-output voltage applications, like PV power system for example; (2) The power switches are turned on and off at ZVS and the rectifier diodes are turned off at ZCS, which greatly reduces the switching loss and improves the conversion efficiency (up to 96.8%); (3) The input current ripple is relatively small and the output voltage is almost ripple free, which is conductive to the grid-connected operation of micro power system.

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