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A Fast and Universal RFID Tag Anti-Collision Algorithm for the Internet of Things

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ABSTRACT To address the problems of high computational complexity, inflexible frame length adjustment, and sub-optimal system efficiency of the RFID tag anti-collision algorithms in the Internet-of-Things systems, a low-complexity, and universal fast RFID tag anti-collision algorithm is proposed in this paper. A faster and less-complex tag number estimation method depends less on computing and storage resources, making it easier to integrate into the Internet of Things. Using the concepts of sub-frame and system efficiency priority, after each sub-frame is identified, the number of tags is estimated quickly and the frame length is adjusted dynamically to ensure the algorithm's efficiency. Moreover, the proposed algorithm is fully compatible with the EPC Class-1 Generation-2 standard, which ensures its universality and compatibility with the existing systems. The simulation results show that the proposed algorithm can achieve a system efficiency of 0.3554, a time efficiency of 0.7851, and an identification speed of 433 n/s. Compared with the standard Q algorithm, the performance is improved by 9.691%, 5.002%, and 8.250%, respectively. It is, hence, demonstrated that the proposed algorithm meets the requirements for the rapid identification of the RFID tags in the Internet-of-Things applications.

INDEX TERMS Anti-collision algorithm, Internet of Things, low cost, RFID tag, system efficiency priority.

I. INTRODUCTION

Radio-frequency identification (RFID) technology has been widely used in industrial, agricultural, and commercial production systems such as warehouse management, logistics tracking and supply chains [1], [2], biological asset inventory, and ticketing systems. The integration of RFID and sensing technology makes it possible for RFID sensor tags to function as intelligent sensing nodes in the Internet of Things and has led to additional research results and commercial products [3]. Passive Ultra High Frequency (UHF) RFID technology is based on the EPC Global Class-1 Generation-2 (EPC C1G2) standard. UHF RFIDs have the advantages of fast identification, no need for a power supply, and a long communication distance. They have been widely studied and applied in Internet of Things systems [3], [4].

In RFID technology, tags and readers implement two-way communication through a shared wireless channel. When multiple tags simultaneously respond to the command of a reader, the signals collide and no tag can be identified. Therefore, the tag anti-collision algorithm, which enables the rapid identification of multiple tags, plays an important role in RFID technology and has been widely studied [4]–[14]. Most RFID tag anti-collision algorithms can be divided into tree-based, ALOHA-based anti-collision [7], [11], [15], and hybrid algorithms [16], which integrate the advantages of the tree- and ALOHA-based algorithms. For example, a tree-based Q-ary searching anti-collision algorithm using a tag ID bit encoding mechanism was proposed [15] that implements multi-bit collision arbitration. Based on the query tree, a new algorithm was proposed, which uses conflict bits to generate short, temporary new IDs, and subsequent identification based on new IDs to reduce energy consumption [17]. It assumes that all tags respond at the same time and return

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the tag's real ID to the reader. The reader detects conflict bits based on the received real ID and notifies all tags to generate a short temporary new ID. However, when the IDs all conflict, the new ID is the same as the real ID, resulting in performance degradation. At the same time, because the distance between the reader and the tag is different, the circuit of the tag and the delay are different, so the simultaneous response of the tag is impossible [18]. In addition, the algorithm requires the tag to have an additional register *PC* that is the same length as the real ID to record conflict bits information of the collision, which increases production cost and complexity. Moreover, the algorithm is not compatible with existing standards, such as EPC C1G2 commands and parameters. By using non-collision bits information of the collision slot, an algorithm for identifying tags at both the success slot and the collision slot was proposed, which can improve the performance of the ALOHA based algorithm [18]. The algorithm can't solve the problem of collision of more than three tags, but it can deal with the problem that only two tags collide. When two tags collide, the reader can use the received non-conflicting ID information to realize the identification of the collision tag. However, when the number of tags is large, it is difficult for the reader to determine the number of tags in the collision slot. In addition, since the tags cannot simultaneously answer the ID, the tag ID information streams received by the reader randomly overlap, resulting in strong randomness of the conflict bit positions. More importantly, if the front-end data of the IDs of the two conflict tags are very different, it is difficult to accurately identify the collision tags by using the non-conflicting bits. A hybrid tag anti-collision protocol based on improved collision detection (ACP-ICD) was proposed [16] that uses bit tracking technology and dual prefix matching to arbitrate collisions to eliminate idle slots. A novel tree-based fast splitting algorithm based on consecutive slot status detection (FSA-CSS) was proposed[19], which can reduce collision and idle slots by FS mechanism and shrink mechanism, respectively. Despite their good performance, hybrid algorithms increase the complexity and cost of designing readers and tags [16]. Tree-based algorithms may cause many collision slots when tag IDs are long, which leads to large identification delays [16]. In contrast, ALOHA-based algorithms, especially the typical dynamic frame slotted ALOHA (DFSA) algorithm, are widely used due to their simplicity and speed. Moreover, they are adopted by the EPC C1G2 standard [12], [20]. The EPC C1G2 standard uses the Q algorithm, which is a DFSA algorithm [21], to solve the tag collision problem [20]. Much progress has been made to improve the performance of Q-based algorithms [8],[9],[11]–[13]. However, these algorithms mainly implement frame-by-frame optimization based on an accurate estimation of the number of tags to improve efficiency. They are highly complex [8], and the adjustment of the frame length is inflexible. Energy consumption is becoming more and more important and should be considered in the new algorithm design. An energy-aware frame adjustment strategy algorithm (EAFAS) was proposed to achieve energy efficiency [22]. To reduce the computational complexity, a low-cost tag estimation method has been proposed [8]. In addition, a pre-stored table [12], [13] has been used to store all the estimation results for different frame lengths. By replacing complex computation with a lookup table, the calculation cost is reduced, but the storage cost is increased. The optimal frame length checkpoint strategy [9], [10] and sub-frame strategy [12]–[14] have been used to dynamically adjust the frame length. However, the sub-frame strategy of the algorithm could be improved, and new commands are required, which leads to poor generality [13].

To reduce the computational cost, maintain universality, and improve the flexibility and accuracy of the frame length adjustment, a new RFID tag anti-collision algorithm is proposed. The proposed algorithm is based on the EPC C1G2 standard and sub-frame system efficiency priority and is called the SUBEP-Q algorithm. The main contributions of this paper are summarized as follows:

(1) The optimal frame length adjustment is flexible and efficient. The sub-frame strategy combines the advantages of the frame-by-frame and slot-by-slot strategies to determine the optimal frame length. Moreover, multiple sub-frame decisions replace the single sub-frame decision for optimal frame length, which reduces decision errors and improves efficiency.

(2) The simpler and more flexible tag estimation method estimates the number of tags quickly without the need for pre-stored tables, thus reducing the dependence on device storage and computing resources.

(3) The proposed method does not require additional instructions or parameters, is fully compatible with the EPC C1G2 standard, and meets the upgrade requirements for RFID tags and systems currently in use, ensuring the universality of the algorithm.

Simulation results show that the proposed SUBEP-Q algorithm is superior to other similar algorithms based on EPC C1G2 in terms of system efficiency, time efficiency, and identification speed.

The structure of this paper is as follows. In Section I, some relevant background and motivations for this work are presented. In Section II, the Q algorithm, frame length adjustment strategies, tag number estimation methods, time efficiency, and system efficiency are reviewed. In Section III, the proposed algorithm is described. The basic design idea, low-complexity tag number estimation, and dynamic frame length adjustment strategy are detailed. Then, the pseudocode of the proposed algorithm is presented. The simulation results are discussed and analyzed in Section IV. In Section V, the conclusions of this research work are given.

II. RELATED WORK

A. Q ALGORITHM OF EPC C1G2

As shown in Fig. 1, the Q algorithm adjusts the frame length $L\ (2^{Q})$ by increasing or decreasing the Q value in each slot. The adjustment of the Q value depends on parameter C.

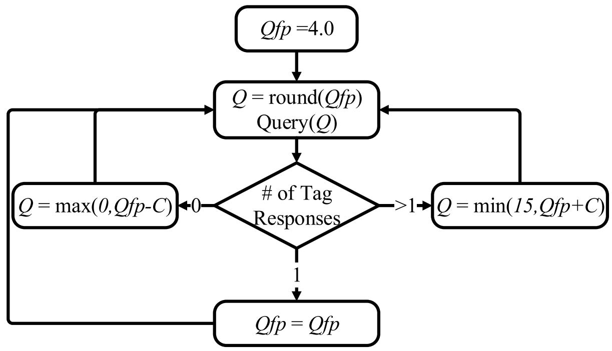


FIGURE 1. Q algorithm of EPC C1G2.

When there is no tag response, C is subtracted from Q, and when there are multiple tag responses, C is added to Q. Otherwise, the Q value does not change. Obviously, parameter C is a key factors affecting the frame length, but this is not clearly explained in EPC C1G2 [8]. The typical range of C is from 0.1 to 0.5. When the Q value is large, C decreases. Conversely, if the Q value is small, C increases [20]. Therefore, for the Q algorithm, the adjustment of parameter C and the optimal frame length adjustment strategy are the focus of research.

B. FRAME LENGTH ADJUSTMENT STRATEGY

Frame length adjustment strategies can be roughly divided into two categories: frame-by-frame [7], [21], [23] and slot-by-slot [13], [20] strategies.

To determine the Q value accurately, the number of tags is estimated accurately in each slot, and then a scheme that selects the optimal Q value based on the estimated results was proposed [8]. However, the computational complexity of this scheme is higher than that of the Q algorithm. To reduce the complexity of estimation for each slot and obtain the optimal frame length adjustment position, the strategy of setting the optimal frame length checkpoint is an important breakthrough. For instance, points such as 1/4, 1/2, and 3/4 of the frame length L have been used as checkpoints. In each frame identification process, only one optimal frame length checkpoint is set in a certain slot for adjusting the optimal frame length [9]. Because the EPC C1G2 standard uses slots of unequal length, when the duration of the collision slot is five times that of the idle slot, $L/5$ is used as a checkpoint for adjusting the optimal frame length while retaining system efficiency [10]. The duration and probability of occurrence of the collision and idle slots are two important factors affecting the identification time, where the probability of a collision slot and idle slot is e-2 [24]. The performance of the algorithm can be improved by using a collision slot adjustment parameter C_{coll} and idle slot adjustment parameter C_{idle} to replace the single parameter C [11]. At the same time, algorithms based on the sub-frame idea have been proposed [12]–[14]. Sub-frame-based dynamic frame slotted ALOHA (SUBF-DFSA) [12], which uses empirical correlation to estimate the number of tags, has low accuracy [13]. The detected-sector-based dynamic framed slotted ALOHA (ds-DFSA) using Schoute's tag number estimation method was also proposed [14], but the existing standard needs to be modified to add a new command [13]. To solve the above problems, dynamic sub-frame based maximum a posteriori probability decision (DS-MAP) was proposed [13], which divides a frame into several sub-frames. Then, the number of all tags in the frame is estimated only at the end of the first sub-frame. If the number of tags matches the optimal interval of numbers corresponding to the ongoing frame length $L\,(2^{Q})$, the algorithm jumps to the traditional DFSA mode, and runs in this mode until the end of the frame. Otherwise, the Q value is adjusted according to the number of remaining tags and a new frame is opened.

C. TAG NUMBER ESTIMATION METHOD

At present, the conventional tag number estimation method is based on probability distribution theory [7], [21], [25]. Assume that n tags are evenly distributed in a frame of length L and the number of tags that may be distributed in each slot obeys the binomial distribution, i.e., the *n Bernoulli* experiment with a probability of $1/L$ [7].

$$B\,(r) = \binom{n}{r}\left(\frac{1}{L}\right)^{r}\left(1-\frac{1}{L}\right)^{n-r} \tag{1}$$

Here, when $r = 0$, there is no tag response corresponding to the idle slot. When $r = 1$, the tag response corresponds to a successful slot. When $r > 1$, this indicates multiple tag responses corresponding to the collision slot. The probabilities of successful, collision, and idle slots in the identification process are represented by P_S, P_C, and P_E, respectively. The expected values of the number of successful, collision, and idle slots in the L slots are E_S, E_C, and E_E, respectively. The calculation of these values is as follows.

$$P_S = B\,(1) = \frac{n}{L}\left(1-\frac{1}{L}\right)^{n-1} \tag{2}$$

$$P_E = B\,(0) = \left(1-\frac{1}{L}\right)^{n} \tag{3}$$

$$P_C = 1 - P_S - P_E \tag{4}$$

$$E_S = LP_S = n\left(1-\frac{1}{L}\right)^{n-1} \tag{5}$$

$$E_E = LP_E = L\left(1-\frac{1}{L}\right)^{n} \tag{6}$$

$$\begin{aligned} E_C &= LP_C \\ &= L\left\{1-\frac{n}{L}\left(1-\frac{1}{L}\right)^{n-1}-\left(1-\frac{1}{L}\right)^{n}\right\} \end{aligned} \tag{7}$$

The problem can be modeled using a multinomial distribution with repeated independent trials, where each trial has one of three outcomes: empty, successful, or collision. Therefore, the maximum a posteriori probability decision (MAP) method has been used to estimate the number of tags [7].

$$P\left(\hat{n}\middle|\,E_E, E_S, E_C\right) = \frac{L!}{E_E E_S E_C} P_E^{E_E} P_S^{E_S} P_C^{E_C} \tag{8}$$

Here, is the result of the estimation, which maximizes the probability P when E_S, E_C, and E_E events occur. However, it is believed that the occurrence of successful, collision, and idle events are interdependent. Therefore, an improved MAP method [26] was proposed.

$$P\left(\hat{n}\middle| E_E, E_S, E_C\right) = \frac{L!}{E_E E_S E_C} P_1\left(E_E\right) P_2\left(E_S|E_E\right) P_3\left(E_C|E_E, E_S\right) \quad (9)$$

Vogt [25] estimates the number of tags based on the minimum distance between the expected value and actual identification vector. All these methods are used to estimate the number of all tags, whereas Schoute's method only estimates the number of tags that collide. The theoretical limit of the number of tags that are not identified is 2.39 times the number of collision slots [21] when the system efficiency is maximized. This is because, assuming that the number of tags participating in one frame identification is n, the number of tags successfully identified after the end of frame is E_S, the number of collision slots is E_C, and the number of unidentified tags is $n - E_S$. Therefore, the average number of tags in each collision slot N_{avgC} is calculated as

$$N_{avgC} = \frac{n - E_S}{E_C} \quad (10)$$

Substituting formulas (5) and (7) into the above formula yields

$$N_{avgC} = \frac{n - n\left(1 - \frac{1}{L}\right)^{n-1}}{L\left\{1 - \frac{n}{L}\left(1 - \frac{1}{L}\right)^{n-1} - \left(1 - \frac{1}{L}\right)^{n}\right\}} \quad (11)$$

For the DFSA algorithm, the rationality of the frame length adjustment determines its system efficiency. Theoretical analysis shows that when n is equal to L, the algorithm maximizes the system efficiency [7], [23], i.e.,$1/e \approx 0.368$. Meanwhile, when n is large enough, the limit $\lim_{n\to\infty} \approx \lim_{n\to\infty}\left(1 - \frac{1}{n}\right)^{n-1} \approx \frac{1}{e}$. When both conditions are satisfied, $N_{avgC} = 2.39$. Hence, formula (11) has also been used to analyze the number of tags that collide in each collision slot under EPC C1G2 standard [23].

Although an improved MAP could further improve the accuracy, the MAP method can control the error within 5%, which is the smallest value of several methods [27]. For the EPC C1G2 standard, a theoretical analysis shows that 18% of the tag number estimation error only affects 0.7% of the algorithmic system efficiency [8]. Therefore, the MAP algorithm is still widely used. However, the biggest advantage of Schoute's method is that it is simple to calculate and more suitable for resource-constrained Internet of Things systems.

D. TIME EFFICIENCY AND SYSTEM EFFICIENCY

For UHF RFID technology that follows the EPC C1G2 standard, the durations of the successful, collision, and idle slots in the identification process differ [20]. Therefore, a performance evaluation based on the time factor is also necessary.

Time efficiency U_T is defined as the ratio of the identification time occupied by successful slots to the total identification time [10], [23].

$$U_T = \frac{N_S T_S}{N_S T_S + N_E T_E + N_C T_C} \quad (12)$$

Here, N_S, N_E, and N_C represent the number of successful, idle, and collision slots when the identification ends, respectively. In addition, T_S, T_E, and T_C indicate the durations of successful, idle, and collision slots, respectively. Although the theoretical analysis concludes that the optimal system efficiency can be obtained when the number of tags is equal to the frame length, obviously, the values of T_S, T_E, and T_C will affect the time efficiency of the algorithm. For example, when $T_C/T_E = 5$, the optimal frame length should be 1.89 times the number of tags [10].

The system efficiency U_S is defined as the ratio of the number of successful slots to the total number of slots [8], [9], [13]. That is to say, when T_S, T_E, and T_C are equal, formula (12) simplifies to

$$U_S = \frac{N_S}{N_S + N_E + N_C} \quad (13)$$

In the theoretical analysis, assuming that the expected value is consistent with the actual value, formulas (5), (6), and (7) are substituted into the above formulas to yield

$$U_T = \frac{n}{L}\left(1 - \frac{1}{L}\right)^{n-1} \quad (14)$$

Here, n, L, and U_S represent the number of tags participating in the identification of the frame, the length of the frame, and the system efficiency, respectively. It can be seen that when the number of tags is the same, different frame lengths L can achieve different system efficiencies. Fig. 2 shows the system efficiency of different frame lengths for the same number of tags. For example, when frame length $L = 256$, the system efficiency peaks when the number of tags is between 180 and 340. Similarly, when the frame length is close to the number of tags, the system efficiency is maximized.

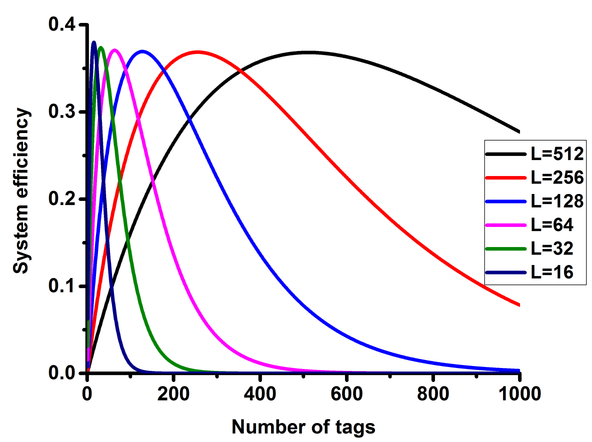


FIGURE 2. Theoretical system efficiency.

III. ALGORITHM DESCRIPTION

In this section, the proposed fast RFID tag anti-collision algorithm, the SUBEP-Q algorithm, is described. SUBEP is suitable for EPC C1G2 standard. This algorithm mainly divides a frame into shorter sub-frames. After each sub-frame is identified, the number of all tags in this frame is estimated quickly and accurately. Then, the estimated results are used to determine if the current frame length is optimal. If it is optimal, the execution continues, otherwise, the current frame is terminated. When the optimal frame length is reset, a new frame is opened.

A. BASIC DESIGN IDEA

Because RFID technology based on the EPC C1G2 standard has been widely used in various Internet of Things devices and management systems, to achieve compatibility and maintainability between the algorithm and existing infrastructure, the proposed algorithm adheres to the following design guidelines: (1) The commands and parameters of the algorithm are fully compatible with the EPC C1G2 standard to ensure its universality. (2) To guarantee the performance of the algorithm, the computational complexity is as low as possible. (3) A more flexible frame length adjustment strategy is adopted to improve the algorithm's system efficiency.

B. LOW COMPUTATIONAL COST TAG NUMBER ESTIMATION METHOD

To reduce the computational complexity of the tag number estimation method, a sub-frame-based estimation method called the DS-MAP method was proposed [13]. First, a frame is divided into K sub-frames, and the tags are evenly distributed in each sub-frame. Therefore, the MAP method is used to estimate the number of tags $\hat{n}$ in the sub-frame at the end of the first sub-frame. Then, the total number of tags in this frame is estimated as $\hat{n}k$. Although the accuracy of the MAP estimation method is high, the estimation error is still amplified by a factor of K. Moreover, at the end of any slot, the number of successfully identified tags N_S is a known quantity. Therefore, the interference of known factors should be excluded as far as possible during the estimation, and only the number of unidentified tags needs to be estimated. Schoute's estimation method can solve this problem, and a simpler method for estimating the number of tags in any slot has been proposed and is called the Chen estimation method [8].

$$\hat{n} = (N_{Si} + kN_{Ci})\left(\frac{L}{i}\right) \tag{15}$$

Note that $\hat{n}$ is the number of all tags that participate in the identification of this frame, which can be estimated at the end of any $i - th$ slot in this frame. In addition, N_{Si} and N_{Ci} represent the number of tags that are currently successful slots and collision slots, and L and i denote the frame length of the frame and current slot number, respectively. Parameter k is the number of tags N_{avgC} in each collision slot, which is 2.39 according to Schoute's method.

Therefore, the DS-MAP method can estimate the number of all tags by sub-frame, and the Chen method can estimate the number of all tags by slot. Both can achieve good results. Obviously, the Chen method is more flexible and computationally less complex. Using the proposed algorithm, these two estimation methods are simulated, and the results are shown in Fig. 3. To ensure the validity of the results, the average value of the algorithm after 500 executions is shown.

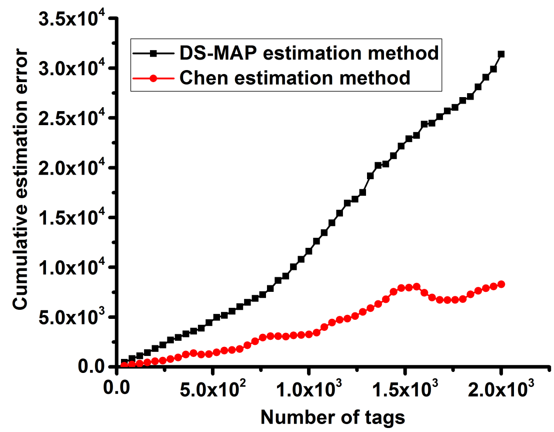


FIGURE 3. Comparison of the estimation error of the DS-MAP and Chen estimation methods.

As shown in Fig. 3, the Chen method has less error and better stability than the DS-MAP method. This is mainly because, although both methods estimate the total number of tags, the Chen method excludes the interference of known factors, i.e., the number of tags that have been successfully identified, and only estimates the number of unknown unidentified tags. In contrast, DS-MAP estimates the known factors, resulting in larger errors. Therefore, the Chen method is adopted in the proposed SUBEP-Q algorithm. This method is successfully applied to the anti-collision algorithm based on sub-frame and system efficiency priority. The results show that it can achieve higher system efficiency and fast identification.

C. DYNAMIC ADAPTIVE FRAME LENGTH ADJUSTMENT STRATEGY

For the DFSA algorithm, the frame length directly determines its system efficiency. According to formula (14), the optimal system efficiency curves with different frame lengths can be obtained by simulation, as shown in Fig. 2. The frame length of the Q algorithm in EPC C1G2 can only be a multiple of 2. Obviously, the Q algorithm cannot guarantee the frame length will be the same as the number of tags, which means the theoretical maximum cannot be achieved. Only a sub-optimal value between two adjacent Q values can be obtained, and the maximum value is 0.361 [8]. However, the frame length corresponding to two adjacent Q values can be calculated to obtain the optimal number of tags for the system. From formulas (16) and (17), the optimal tag number and system efficiency intervals of two adjacent frames are obtained,

TABLE 1. Optimal frame and sub-frame lengths based on system efficiency.

Q	Frame length (2^Q)	Sub-frame length	Optimal number interval	System efficiency interval
1	2	2	1∼3	–
2	4	4	4∼5	0.4091∼0.3759
3	8	4	6∼11	0.3759∼0.3618
4	16	4	12∼22	0.3618∼0.3536
5	32	8	23∼44	0.3536∼0.3501
6	64	8	45∼88	0.3501∼0.3483
7	128	16	89∼177	0.3483∼0.3474
8	256	16	178∼355	0.3474∼0.3470
9	512	32	356∼710	0.3470∼0.3468
10	1024	32	711∼1420	0.3468∼0.3467
11	2048	64	1421∼2839	0.3467∼0.3466
12	4096	64	2840∼5678	0.3466∼0.3466
13	8192	64	5679∼11355	0.3466∼0.3466
14	16384	64	11356∼22713	0.3466∼0.3466
15	32768	64	22714∼45426	–

as shown in Table 1. For example, when $Q = 8$, the frame length is 256. If the number of tags is between 178 and 355, the system efficiency is optimized.

$$\frac{n}{L_{i-1}}\left(1-\frac{1}{L_{i-1}}\right)^{n-1} = \frac{n}{L_i}\left(1-\frac{1}{L_i}\right)^{n-1} \tag{16}$$

$$\frac{n}{L_i}\left(1-\frac{1}{L_i}\right)^{n-1} = \frac{n}{L_{i+1}}\left(1-\frac{1}{L_{i+1}}\right)^{n-1} \tag{17}$$

The Q algorithm does not consider the relationship between the system efficiency of the current frame and the frame length. After each slot identification, the Q value is adjusted by adding or subtracting the parameter C corresponding to the collision or idle slot. If a certain slot is a collision slot, the estimated number of tags is located in the optimal tag number interval of the current Q value. At this time, if the Q value changes after adding parameter C, it will lead to an unreasonable adjustment of the frame length, which will decrease system efficiency. Therefore, to avoid the sub-optimal efficiency caused by frequent Q value adjustments slot-by-slot as well as the problem that the traditional frame-by-frame approach does not adjust the frame length in time, a more reasonable dynamic adaptive frame length adjustment strategy based on sub-frame and system efficiency priority is proposed. The aim is to ensure the flexibility of the frame length adjustment and high efficiency of the algorithm.

First, the frame length L of each frame is divided into several sub-frames. For each sub-frame length L_{sub}, after each sub-frame has been identified, formula (13) is used to estimate the number of tags N_{est} in the frame. Then, N_{est} and the optimum range of numbers corresponding to the Q values in Table 1 are used to determine whether the current frame is optimal.

$$Q = \begin{cases} change, & N_{est}\ not\ in\ optimal\ interval\ of\ Q \\ no\ change, & N_{est}\ in\ optimal\ interval\ of\ Q \end{cases} \tag{18}$$

That is, if the current number of tags is within the optimal range of the current Q value, then it is not necessary to adjust the Q value; otherwise, according to the optimal range corresponding to N_{est}, a new Q value should be selected to open a new frame.

Obviously, the length of the sub-frame determines the frequency of frame length adjustments. If it is too long, the frame length adjustment is too late. In contrast, if it is too short, the frequent adjustment of frame length will decrease system efficiency. Therefore, the selection of sub-frame length has an important impact on the system efficiency of the algorithm. As shown in Table 1, when the Q value exceeds 6, the influence of frame length on system efficiency decreases gradually and the gap is very small, whereas when the Q value exceeds 9, the system efficiency remains about 0.3467, i.e., almost unchanged. Therefore, based on the optimal system efficiency corresponding to the Q value, the algorithm adopts the following sub-frame length L_{sub} selection strategy.

$$L_{sub} = \begin{cases} 2, & Q = 1 \\ 4, & 2 < Q \leqslant 4 \\ 8, & 4 < Q \leqslant 6 \\ 16, & 6 < Q \leqslant 8 \\ 32, & 8 < Q \leqslant 10 \\ 64, & 10 < Q \leqslant 15 \end{cases} \tag{19}$$

As shown in Table 1, when the sub-frame length is 64 and the optimal number of tags is 1,421, the system efficiency of the sub-frame can be guaranteed to be above 0.3483. Therefore, this selection approach can meet the needs of scenarios with a large number of tags and also ensures that the algorithm has a high system efficiency.

D. SUBEP-Q ALGORITHM

The proposed SUBEP-Q algorithm is described in detail in this section. The algorithm is compatible with the EPC C1G2 standard, so the algorithm flow for the tag is consistent with that of EPC C1G2. Therefore, Fig. 4 only shows the flowchart of the reader.

As shown in Fig. 4, during the identification process of each frame, the number of tags is estimated at the end of each sub-frame or frame, thereby determining whether the current frame length is optimal. If it is not the optimal value, the current frame is terminated, and the optimal frame length, i.e., Q, is reselected according to the backlog of tags. Then, the sub-frame length is reset, and a new frame is started. This avoids erroneous adjustment of the frame length caused by inaccurate estimation only once in a certain sub-frame. At the same time, the communication overhead caused by checking or adjusting the frame length for each slot is avoided. More importantly, the flexibility of the frame length adjustment is guaranteed.

IV. SIMULATION RESULTS AND DISCUSSION

In addition to the influence of the technology itself, the parameter setting strategy, such as sub-frame checkpoint strategy, communication parameter T_3, and initial Q value also has an important impact on the performance of the

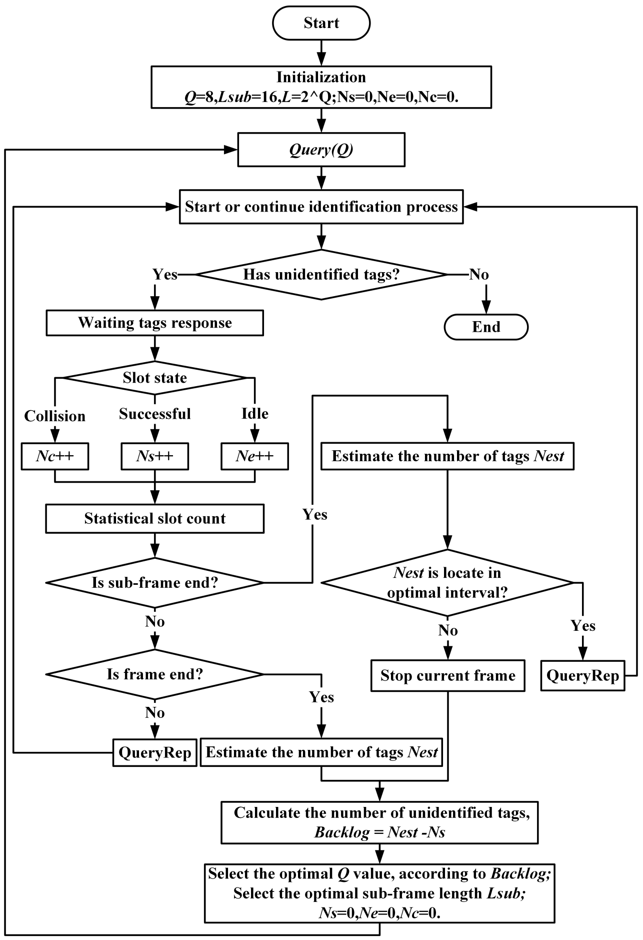


FIGURE 4. Flowchart of SUBEP-Q for the reader.

algorithm. To measure the impact of the above factors on the SUBEP-Q algorithm and explore its applicability, the above contents are discussed and analyzed separately in this section. Then, the optimal operating parameters are selected.

Based on the optimal parameters, the SUBEP-Q algorithm is compared with the similar Q [20], FastQ [11], FEI-Chen [8], and DS-MAP [13] algorithms by Monte Carlo simulation. For better comparative analysis, the theoretically derived optimal ideal DFSA (Ideal DFSA) algorithm is also listed. To ensure the accuracy of the data, all the results are the average of 500 runs of the algorithm. The simulation parameters based on the EPC C1G2 standard are shown in Table 2.

TABLE 2. Simulation parameters.

Parameters	Value(μs)	Parameters	Value(μs)
T_1	62.50	T_{EPC}	912.50
T_2	62.50	T_{ACK}	337.50
T_3	50.00	T_{RN16}	212.50
T_{QUERY}	412.50	T_S	1375.00
$T_{QUERYADJUST}$	168.75	T_E	112.50
$T_{QUERYREPEAT}$	0.75	T_C	337.50

According to the EPC C1G2 standard and parameters in Table 2, the durations of successful, collision, and idle slots T_S, T_C, and T_E, respectively, can be calculated as

$$\begin{aligned} T_S &= T_1 + T_{RN16} + T_2 + T_1 + T_{EPC} + T_2 = 1375.00\mu s \\ T_C &= T_1 + T_{RN16} + T_2 = 337.50\mu s \\ T_E &= T_1 + T_3 = 112.50\mu s \end{aligned}$$

Table 6 lists the simulation results of the algorithm and the performance improvement relative to the standard Q algorithm. Note that the value of the identification speed only retains the integer part of the real value, and the maximum (Max) and average (Avg) of each indicator are given, respectively.

A. OPERATING PARAMETER DISCUSSION

1) SUB-FRAME CHECKPOINT STRATEGIES

Sub-frame checking for optimal frame length ensures the flexibility of the frame length adjustment while avoiding excessive communication overhead. As described in Section II-B, the frame length adjustment strategy depends on the setting strategy of the sub-frame checkpoints. To evaluate the effect of different sub-frame checkpoint setting strategies on the performance of the algorithm, this experiment compares two strategies, one that checks only after the first sub-frame (first sub-frame), and the other that checks after all sub-frames (all sub-frames). Fig. 5 and Table 3 give the Max and Avg results of different evaluation indicators. Compared with the first sub-frame strategy, the all sub-frames strategy improves system efficiency by 0.45%, time efficiency by 0.27%, and identification speed by 0.23%.

TABLE 3. Results of the first sub-frame and all sub-frame strategies.

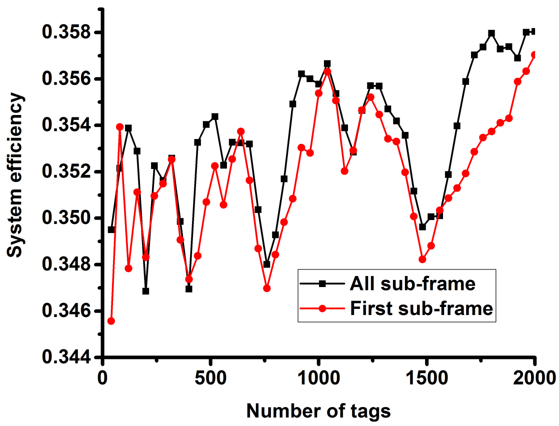
Strategy	System efficiency (Max, Avg)	Time efficiency (Max, Avg)	Identification speed(n/s) (Max, Avg)
First sub-frame	0.3570,0.3519	0.7873, 0.7796	435,431
All sub-frame	0.3580,0.3535	0.7936, 0.7817	438,432

From the perspective of system efficiency, as shown in Fig. 5(a), the all sub-frames strategy is better than the first sub-frame strategy, but the overall behavior of the two is the same. According to Fig. 5(b), the strategy of all sub-frames is better for the time efficiency of the algorithm. This is mainly because the probability of misjudgment is higher in the first sub-frame than after all sub-frames. On the contrary, the probability of misjudgment can be reduced by checking every subsequent sub-frame. Similarly, the results for identification speed in Fig. 5(c) occur for the same reasons.

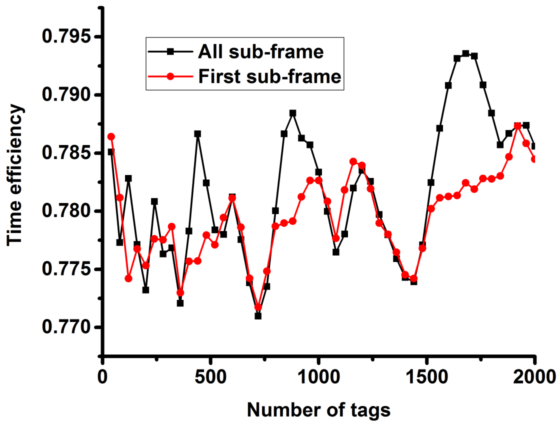
Therefore, it can be concluded that the strategy of dynamically adjusting the frame length after all sub-frames is more reasonable and can further improve the system performance of the algorithm.

2) INITIAL Q VALUE

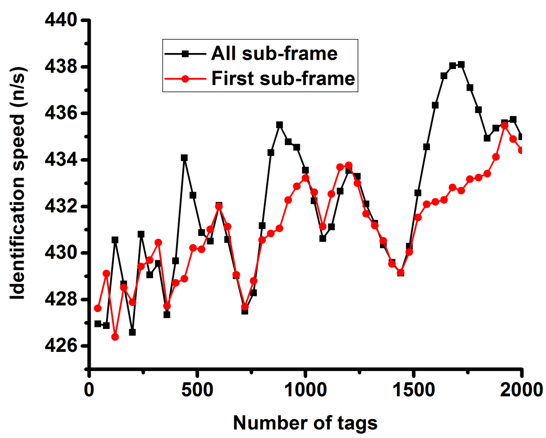
Fig. 6 shows the simulation results of different initial Q values, and Table 4 gives the Max and Avg values of the different evaluation indicators. The results show that, three different



(a) System efficiency.

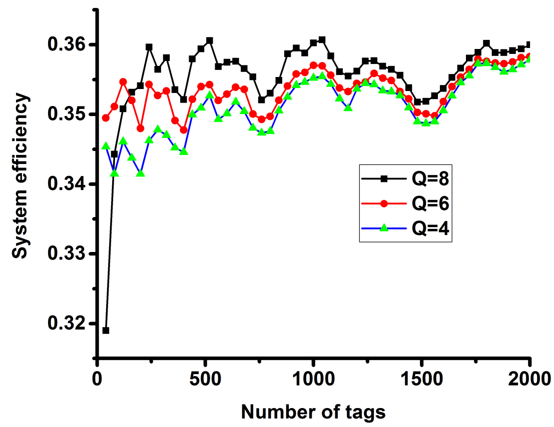


(b) Time efficiency.

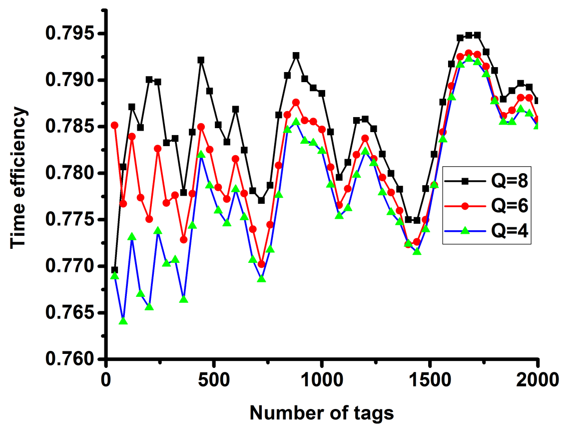


(c) Identification speed.

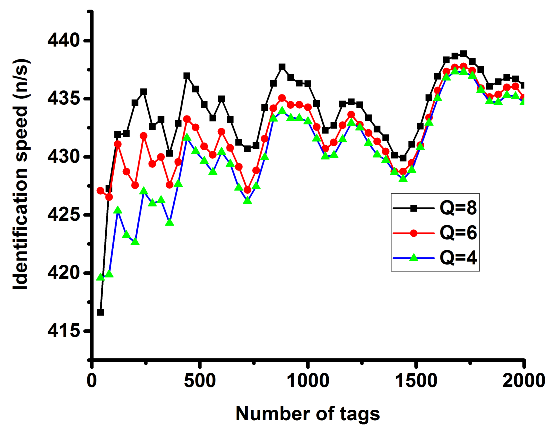
FIGURE 5. **Comparison of the first sub-frame and all sub-frame strategies.**



(a) System efficiency.



(b) Time efficiency.



(c) Identification speed.

FIGURE 6. **Comparison of initial frame lengths Q = 4, Q = 6, and Q = 8.**

initial Q value schemes can achieve a system efficiency of over 0.35. However, compared with $Q = 4$, $Q = 8$ improves the system efficiency, time efficiency and identification speed by 1.25%, 0.89%, and 0.70% respectively.

Overall, Fig. 6 shows that $Q = 8$ is superior to other values for system efficiency, time efficiency, and identification speed. However, when the number of tags is less than 160, $Q = 6$ optimizes system efficiency. Fig.6(b) and (c) show that when the number of tags is less than 80, $Q = 6$ also obtains better performance.

According to the theory that the system efficiency is optimal when the frame length is equal to the number of tags [7] [23], each Q value corresponds to the optimal range

TABLE 4. Results of initial frame lengths Q = 4, Q = 6, and Q = 8.

Initial Q value	System efficiency (Max, Avg)	Time efficiency (Max, Avg)	Identification speed(n/s) (Max, Avg)
Q=4	0.3578, 0.3512	0.7923, 0.7784	437,430
Q=6	0.3583, 0.3536	0.7929, 0.7816	437,432
Q=8	0.3607, 0.3556	0.7948, 0.7853	438,433

of the number of tags and is not suitable for all situations. As shown in Table 1, when $Q = 6$,the optimal number of tags ranges from 45 to 88. Therefore, when the number of tags is small, a smaller Q value can be used to achieve higher efficiency. On the contrary, when the number of tags is large, a larger Q value performs better. Hence, $Q = 8$ is chosen as the initial value in this study. It can be concluded that the selection of the initial Q value has a significant impact on the performance of the system.

3) T3 PARAMETER VALUE

According to EPC C1G2, T_3 is the waiting time for the reader to send the next command [20]. Therefore, the value of T_3 will affect the communication overhead, resulting in significant differences with time-related evaluation indicators such as time efficiency and identification speed. Usually, T_3 takes the values of 5 μs, 50 μs, or 62.5 μs.

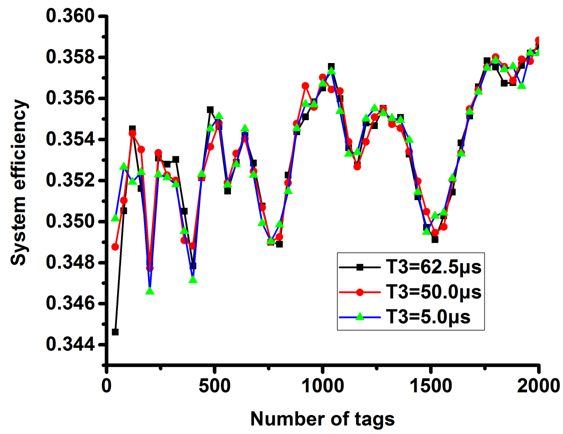
Fig. 7 shows the results of the SUBEP-Q algorithm for different values of T_3. Table 5 shows the Max and Avg values of different evaluation indicators. The results show that although the three different value schemes can achieve a system efficiency of above 0.35 and identification speed above 400 n/s. The time efficiency and identification speed of $T_3 = 5$ μs can still achieve 3.47% and 2.56% performance improvement compared with $T_3 = 62.5$ μs.

TABLE 5. Results of T3 = 5 μs, T3 = 50 μs, and T3 = 62.5 μs.

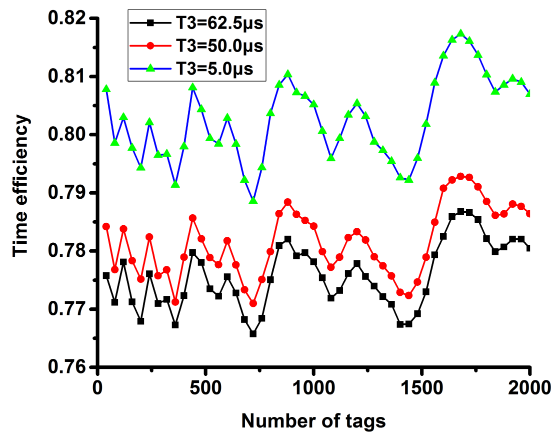
T_3(μs)	System efficiency (Max, Avg)	Time efficiency (Max, Avg)	Identification speed(n/s) (Max, Avg)
5.00	0.3582, 0.3535	0.8173, 0.8027	447,440
50.00	0.3588, 0.3536	0.7928, 0.7816	437,432
62.50	0.3585, 0.3534	0.7868, 0.7758	435,429

As shown in Fig. 7(a) and Table 5, the different values of T_3 have very little effect on the maximum and average values of system efficiency. This is mainly because, according to formula (13), the system efficiency is the ratio of successful slots to total slots. Frame length is the main factor affecting system efficiency, and the value of communication parameter T_3 has no effect.

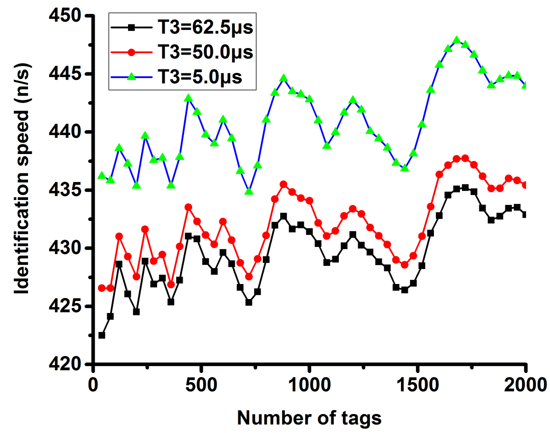
Obviously, a smaller value of T_3 means that communication takes less time. As shown in Fig. 7(b), when $T_3 = 5$ μs, the time efficiency is the highest, and when $T_3 = 62.5$ μs, the time efficiency is the lowest. Similarly, as shown in Fig. 7(c), the value of T_3 has the same effect on identification speed. A smaller value of T_3 increases identification speed. It is concluded that to improve the system efficiency of the algorithm, a lower value of T_3 leads to a higher time efficiency and faster identification speed.



(a) System efficiency.



(b) Time efficiency.



(c) Identification speed.

FIGURE 7. Comparison of T3 = 5 μs, T3 = 50 μs, and T3 = 62.5 μs.

B. PERFORMANCE DISCUSSION

1) SYSTEM EFFICIENCY

The results of system efficiency are shown in Fig. 8, the Ideal DFSA, Q, and FastQ algorithms show strong stability for different tag numbers. On the contrary, the FEI-Chen, DS-MAP, and SUBEP-Q algorithms have consistent fluctuations. More importantly, compared with the standard

TABLE 6. Simulation results of different algorithms and performance improvements compared with the standard Q algorithm.

Algorithm	System efficiency (Max, Avg)	Improvement & Ranking	Time efficiency (Max, Avg)	Improvement & Ranking	Identification speed(n/s) (Max, Avg)	Improvement & Ranking	Overall Ranking
Ideal DFSA	0.3760,0.3687	–	0.8063,0.7963	–	440,439	–	–
Q	0.3257,0.3240	–	0.7646,0.7477	–	401,400	–	–
FastQ	0.3308,0.3284	+1.358%, (4)	0.7918,0.7872	+5.283%, (1)	421,420	+5.000%, (4)	(4)
FEI-Chen	0.3541,0.3436	+6.049%, (2)	0.7872,0.7730	+3.384%, (4)	431,422	+5.500%, (3)	(3)
DS-MAP	0.3489,0.3375	+4.167%, (3)	0.7929,0.7835	+4.788%, (3)	436,430	+7.500%, (2)	(2)
SUBEP-Q	0.3599,0.3554	+9.691%, (1)	0.7952,0.7851	+5.002%, (2)	438,433	+8.250%, (1)	(1)

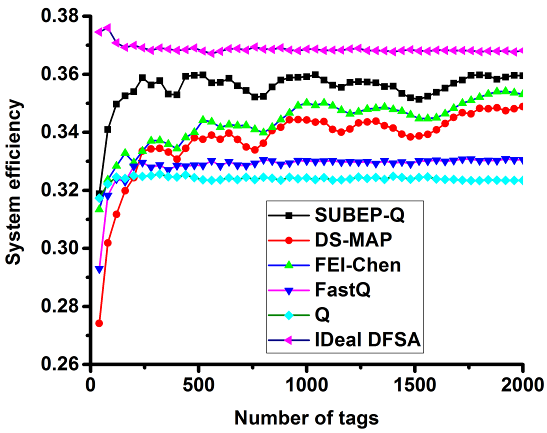


FIGURE 8. System efficiency.

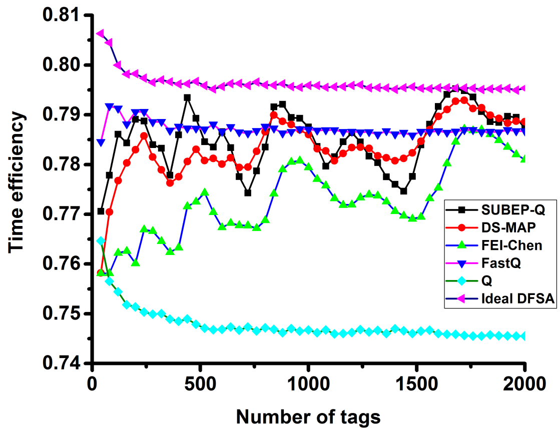


FIGURE 9. Time efficiency.

Q algorithm, the performance of these algorithms is improved. As shown in Table 6, the improvement of the SUBEP-Q algorithm is the most significant, reaching 9.691%.

Generally speaking, the error of sub-frame division and tag number estimation influences the stability of the system efficiency. Algorithms using these technologies, such as SUBEP-Q, will be unstable in terms of system efficiency compared with those that do not use them. However, they can accurately estimate the number of tags and optimize the optimal frame length, i.e., Q, to improve system efficiency. The data in Table 6 confirm the above conclusion.

Sub-frame checkpoint strategy is an important factor affecting system efficiency. The SUBEP-Q algorithm can achieve higher system efficiency than the FEI-Chen algorithm, which dynamically adjusts the Q value slot-by-slot, and the DS-MAP algorithm, which checks the optimal frame length only once at the end of each sub-frame. Obviously, the SUBEP-Q algorithm checks the length at the end of each sub-frame, which reduces the frequency of checking compared with slot-by-slot checking and is more accurate than checking only once. At the same time, although the accuracy of the MAP method adopted by the DS-MAP algorithm is higher, the Chen method combined with the idea of sub-frame checking can still ensure higher system efficiency. These are the main reasons for the best performance of the SUBEP-Q algorithm.

2) TIME EFFICIENCY

As shown in Fig. 9 and Table 6, SUBEP-Q algorithm and similar algorithms, such as FEI-Chen and DS-MAP, have the same trends for time efficiency. Moreover, the average and maximum values of SUBEP-Q are the best. The time efficiency of the SUBEP-Q algorithm is improved by 5.02%, reaching 0.7851. However, it is still lower than that of FastQ on the whole.

According to formula (12), the time efficiency is determined by the delay time and number of different types of slots. Therefore, collision slots and idle slots are also important factors. However, SUBEP-Q and other similar algorithms mainly focus on the optimization of the successful slots, while ignoring the other two. On the contrary, FastQ algorithm gives full consideration to the ratio of collision slot to idle slot duration and the probability ratio of the two. This is the main reason why FastQ can optimize time efficiency.

3) IDENTIFICATION SPEED

Identification speed is an important indicators of algorithm performance. In practice, most logistics management systems require that tags be identified faster than 300 n/s [28]. As shown in Fig. 10 and Table 3, the Q algorithm and its improved algorithm can achieve identification speeds faster than 400 n/s. Of them, the identification speed of SUBEP-Q algorithm is 433 n/s, which is 8.25% higher than that of the standard Q algorithm.

There is no doubt that the identification speed is proportional to the number of successful slots, i.e., system efficiency. When there are more successful slots, the identification speed is faster. As mentioned in the previous section, SUBEP-Q and similar algorithms strive to obtain the optimal system efficiency through optimizing frame length. Therefore, they can achieve higher identification speed.

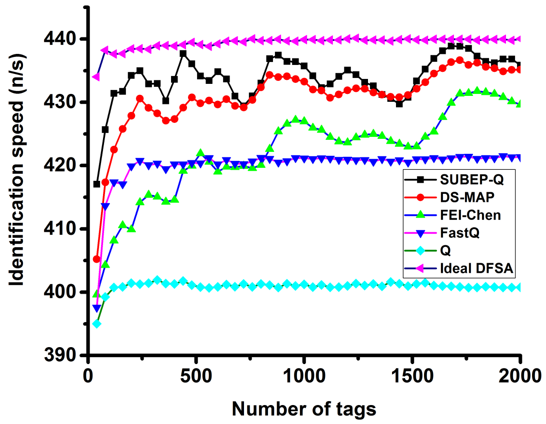


FIGURE 10. **Identification speed.**

The accuracy of multiple optimal frame length checks is higher than that of a single check, so the accuracy of the SUBEP-Q algorithm is higher and its identification speed is faster than those of the DS-MAP algorithm. Frequent adjustment of the frame length for each slot increases the communication overhead. Therefore, the identification speed of SUBEP-Q is significantly faster than that of the FEI-Chen algorithm. This fully demonstrates that the strategy of dividing the frame into sub-frames and dynamically adjusting the frame length after each sub-frame has an important influence on identification speed.

Fig. 11 compares the performance improvement obtained by different algorithms with respect to the standard Q algorithm. From the perspective of system efficiency and identification speed, the SUBEP-Q algorithm proposed in this paper has the highest improvement. In terms of time efficiency, the SUBEP-Q algorithm is suboptimal, mainly because FastQ focuses on time efficiency and the probability of collision and idle occurrence, thus optimizing the parameters of frame length adjustment. Overall, the proposed SUBEP-Q algorithm performs significantly better than similar algorithms.

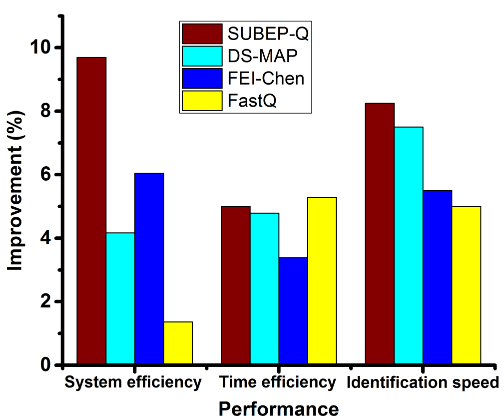


FIGURE 11. **Performance improvement comparison.**

V. CONCLUSION

In this paper, a universal fast RFID tag anti-collision algorithm with low computational cost was proposed. By using a simpler tag number estimation method and adjusting the optimal frame length after each sub-frame, the proposed algorithm avoids the problems caused by slot-by-slot frequent adjustments or insufficient frame-by-frame adjustments. Moreover, the algorithm does not rely on the computing and storage resources of the device. Using the idea of sub-frame and system efficiency priority, the dynamic and accurate adjustment of frame length after each sub-frame can be realized, which significantly improves the performance of the algorithm. More importantly, the algorithm is fully compatible with the existing EPC C1G2 standard, which ensures a seamless connection between the algorithm and existing Internet of Things systems.

Moreover, this study systematically compared and analyzed the effects of different sub-frame checkpoint strategies, initial Q values, and communication parameter T_3 on the performance of the algorithm. In conclusion, the system efficiency and identification speed of the SUBEP-Q algorithm are the best of similar algorithms, but the time efficiency still needs to be improved. In addition, the performance of the proposed algorithm was demonstrated by simulation. Future work will include the hardware implementation and verification of the algorithm as well as further optimization of its time efficiency.

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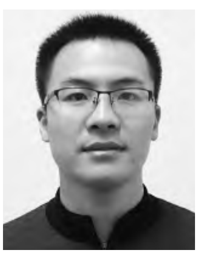

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