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A 2.2 to 2.9 GHz Complementary Class-C VCO With PMOS Tail-Current Source Feedback Achieving −120 dBc/Hz Phase Noise at 1 MHz Offset

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ABSTRACT The performance of low-powered transceivers is required to meet stringent specifications for an advanced wireless radio application. It is critical for a voltage-controlled oscillator (VCO) to meet multi-standard and multiple frequency operation with low-power consumption and amplitude enhanced complementary mode of operation. This paper proposes a novel technique for wide tuning range in a complementary class-C VCO employing a capacitive-source degeneration (CSD) to meet multi-standard operation for low-power transceivers. The technique that employs two sets of symmetrical split PMOS biased current source operating in the subthreshold region achieves the desired low phase noise (PN) performance at a tuning range of 2.2–2.9 GHz with a supply headroom of 1.2 V. The control of the dc bias point reduces the conduction angle, which improves the current efficiency, power consumption, and PN. Concurrently, an auxiliary $-g_m$ NMOS only class-B oscillator is incorporated to mitigate the start-up issue of the class-C VCO. At the center frequency of 2.45 GHz, the proposed VCO achieves a power consumption of 1.73 mW, phase noise of −120 dBc/Hz at the 1-MHz offset, and a figure-of-merit (FoM) of 185.41 dBc/Hz at 1 MHz. The total active chip area is only 0.3-mm^2 excluding bond pads. The proposed VCO serves as a promising solution for low-power wireless communication systems.

INDEX TERMS Class-C VCO, capacitive source degeneration (CSD), CMOS, gate bias, phase noise (PN), start-up.

I. INTRODUCTION

The relentless development of ubiquitous wireless connectivity motivates the development of low-power voltage controlled oscillators (VCOs) with low phase noise (PN) performance to support complex data (de) modulation. Intensive research work towards realizing low-power RF oscillators has improve the overall power efficiency and battery lifetime of transceivers while achieving a stringent PN requirements [1], [2]. Specifically, class-C VCOs prove to be one of the major breakthrough by shaping the current waveform into a tall and narrow pulse. Class-C VCO is able to achieve a power saving of 36% for the same PN performance of that a class-B configuration or 3.9 dB lower under the same power budget [3]. However, class-C VCOs inherently suffers from a trade-off in start-up and maximum oscillation amplitude with respect to PN. On the other hand, the PN and power efficiency of class-B VCOs decreases when the ideal current source is replaced with a single transistor.

Several techniques have been proposed to alleviate these trade-offs to achieve high PN performance. The work in [4] proposed a feedback amplitude control circuit to improve

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the start-up and PN while maintaining a constant signal amplitude. However, the additional control circuit consumes substantial power to sustain the PN performance. In [5], a robust startup is ensured by a class-B switching pair connected in parallel with a class-C core with a low gate bias voltage, $V_{BIAS,N}$. This results in low current efficiency compared to the conventional class-C topology which is undesirable. Chen *et al.* [6] and Deng *et al.* [7] implemented an amplitude detector circuit in the negative feedback to control the amplitude by setting $V_{BIAS,N}$ at a constant value. This implementation degrades the quality factor (Q) of the tank and reduces the tuning range of the VCO.

PN improvement via Q enhancement has been adopted by integrating a novel resonant circuit [8] or through harmonic filtering as proposed by Hegazi *et al.* [9]. The harmonic filtering technique connects a noise filter by adopting a bulky inductor and capacitor at the drain of the tail current source to achieve an even order harmonic filtering which down-converts the VCO oscillation to the fundamental frequency in the mixing process. A harmonic tuned resonant tank employed in [10] creates a third harmonic component via an additional impedance peak, producing a pseudo-square waveform thus improving the zero-crossing slope. This leads to shorter commutation time while achieving a lower effective noise factor. To circumvent the harmonics, Men *et al.* [11] biased the tail current source transistor at $2f_{LO}$ to suppress the cyclostationary noise via accumulation and strong inversion pattern.

Fig. 1 shows a high swing complementary class-C VCO by Fanori *et al.* [12] which exploits a PMOS – NMOS complementary pair operating in class-C mode to enhance the output swing and ensures a fast startup. In reference to Fig. 1, by assuming the parallel resonant tank resistance, $R_p = 2\pi f_{osc} L Q_{ind}$ where $Q_{ind} = (\omega_o L)/R_s$, the startup condition is expressed as

$$\frac{(2\pi f_{osc})^2 L^2}{R_s} > \frac{2\alpha}{g_m} \tag{1}$$

where R_s is the inductor's series resistance, L is the inductance of the LC tank [13], f_{osc} is the VCO's oscillation frequency and α is the design factor selected to be larger than 1 for startup condition taking into account of the process-voltage-temperature (PVT) variation. Therefore, from the startup condition in (1), the frequency of oscillation for a low frequency (LF) band is denoted as

$$f_{osc,low} = \frac{1}{2\pi}\sqrt{\frac{2\alpha R_s}{g_m L^2}} \tag{2}$$

Besides satisfying the startup condition, the flicker noise up-conversion from the tail transistor to the PN is a bottleneck in most conventional cross-coupled VCOs. Various efforts have been adopted to suppress the tail noise and to shape the tail current into a class-C waveform [14], [15]. The technique in [16] utilized a low-pass and a notch filter connected between the tail transistor and the common-source node of the switching transistor to suppress the second harmonic noise from the tail transistor. This prevents the VCO from down-converting to the oscillation frequency which improves the PN but at the cost of using a bulky inductor. Another approach in [17] where the noise cancellation technique applied on the trans-conductance stage results in noise suppression.

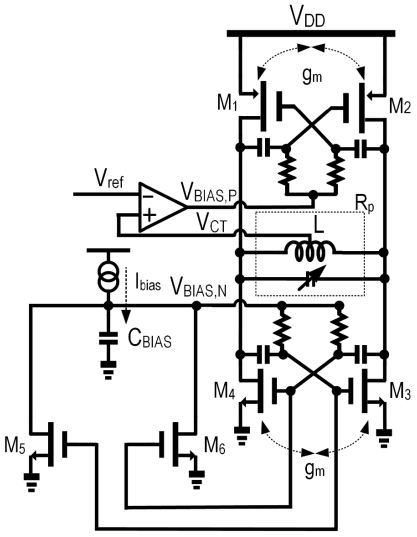

FIGURE 1. Conventional high swing complementary Class-C VCO [12].

Switched capacitor arrays [18]–[20] and switched inductors [21]–[24] are unique solution in VCO design for wide tuning range and multiple frequency operation. However, an extra chip area with higher power consumption is required due to the increase in circuit complexity. An alternative method is by employing a magnetic coupling effect to control the frequency tuning by an inductive switching in order to achieve a wide tuning range [25]. This method requires an additional driving current which subsequently leads to lower energy efficiency.

To overcome the trade-offs in start-up and PN performance of conventional class-C VCOs, a novel wideband complementary class-C architecture has been proposed, utilizing the principle of Capacitive Source Degeneration (CSD) and through the splitting of the PMOS tail current source biased in subthreshold region. As the current efficiency improves, the flicker noise up-conversion of the tail current source simultaneously reduces. Furthermore, an additional NMOS-only class-B cross-coupled oscillator is integrated to alleviate the start-up issue. Section II of this paper expounds on the proposed architecture scheme and analysis, followed by the experimental results in Section III. Finally, Section IV concludes the findings.

II. PROPOSED TOPOLOGY

A. CIRCUIT OPERATION

Fig. 2 shows the proposed wideband complementary class-C VCO architecture accommodated with the class-B NMOS VCO only transistors, M_3 and M_4 as two sets of active core.

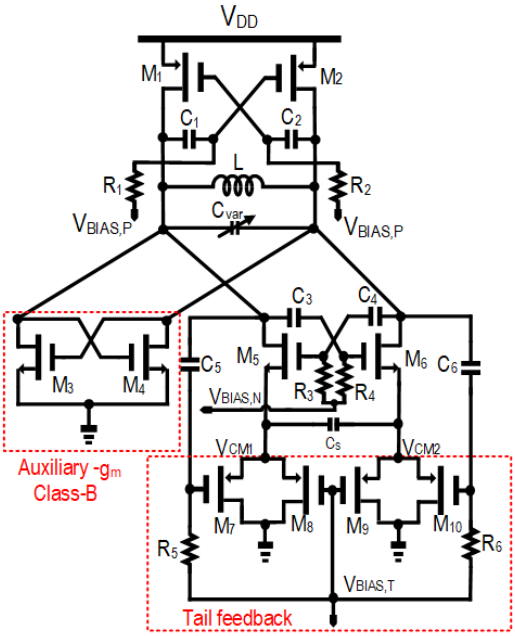

FIGURE 2. Schematic of the proposed architecture.

The RC charging circuit, R_1C_1 and R_2C_2 connected at the active transistor's gates of the PMOS cross-coupled pair, M_2 and M_1 are biased at $V_{BIAS,P}$ to achieve saturation condition of $V_{DS,M1(M2)} < V_{BIAS,P} + \left|V_{th,P,M1(M2)}\right|$. The charger circuit, R_3C_4 and R_4C_3 which are connected at the gates of transistors M_5 and M_6 biased at $V_{BIAS,N} \leq V_{th,N,M5(M6)}$ in subthreshold region controls the dc power consumption of the entire VCO. The RC time constant which satisfy the loop gain to sustain the oscillation is expressed as

$$A_V \cdot R_p \parallel -\frac{g_m}{2} > 1 \tag{3}$$

where A_V is the loop gain approximated to 1 due to the absence of passive gain. The flicker noise, $1/f$ to PN up-conversion is prevented as the even-order harmonics are suppressed with a high impedance path along the biasing gate at $V_{BIAS,N}$. Therefore, a symmetric waveform is attained in the impulse sensitivity function (ISF), yielding to a zero dc value. The minimization of flicker noise is obtained from the advantage of the PMOS current source, $M_7 - M_{10}$ which stabilizes the bias condition at the source voltage (V_{CM1} and V_{CM2}) of the differential switching pair, M_5 and M_6 operating in the subthreshold region. A lower effective noise, N_{eff} improves the phase noise performance consisting noise source contribution from the LC tank, active cross-coupled devices and PMOS as a split current source as given as

$$\begin{aligned} N_{eff} &= N_{LC,tank} + N_{gm} + N_{gm,cs} \\ N_{eff} &= \frac{2k_BT}{R_T}\left(1 + \gamma\left(1 + \alpha_{p/n} g_{m,cs}\right) R_T\right) \end{aligned} \tag{4}$$

where $N_{LC,tank}$, N_{gm} and $N_{gm,cs}$ are the effective noise of the LC resonator, the subthreshold cross-coupled differential pair transistor, M_5 (M_6) and the PMOS current source respectively. k_B is the Boltzmann's constant, T is the absolute temperature, $g_{m,cs}$ is the transconductance of the current source, γ is the channel noise coefficient of the MOS devices and $\alpha_{p/n}$ is the parameter that relates the transition time interval of the complementary PMOS and NMOS conduction. Referring to (4), reduction in $\alpha_{p/n}$ and $N_{gm,cs}$ shall reduce the $N_{eff}.\alpha_{p/n}$ is reduced by ensuring M_5 and M_6 operates in subthreshold region. $N_{gm,cs}$ is minimized by utilizing a PMOS tail current sources, ($M_7 - M_{10}$), taking into advantage of its lower inherent flicker noise. In addition gate biasing, $V_{BIAS,T}$ is added to established low impedance path to ground, shutting off part of the output biasing noise which minimally influence the phase noise. High load impedance is observed in series with the switching pair, M_5 and M_6(M_3 and M_4) which injects current noise into the resonant tank at the zero crossing point. The work in [26] outlays a solution to remove the tail current source in alleviating the noise contribution or by substituting it with a tail resistor as reported in [27]. This technique subjects the oscillator to be sensitive towards the supply voltage variation and driving the differential switching pair active transistors into triode region. Therefore, it is preferred to retain and modify the tail current source in a way to serve minimum noise contribution.

B. CAPACITIVE -SOURCE DEGENERATION, (CSD) WITH 1/f SUPPRESSING EFFECT

Conventional wide-band communication systems for multiple standards application adopts band-switching technique to achieve wide tuning range. This technique observes a penalty of an increase in circuit level and introduces switching loss, causing higher resistive sensitivity which degrades the Q of the circuit [28]. On lossy silicon substrate, the parasitic capacitances (C_{gs}, C_{gd}) of the cross coupled pair adjusted by varactor, C_{var} tunes the oscillation resonant frequency for low frequency, (LF) band in (2) and high frequency, (HF) band in (5).

$$f_{osc,high} = \frac{1}{2\pi\sqrt{L.\left(\frac{2C_{var}+C_{gs}+4C_{gd}}{2}\right)}} \tag{5}$$

Evidently, the parasitic capacitances are the limiting factor towards attaining a higher bandwidth given by the tuning range (TR) expressed as

$$TR = \frac{C_{max} - C_P}{C_{min} - C_P} \tag{6}$$

where C_P is the total parasitic capacitance of the cross couple active MOS transistor and C_{max}/C_{min} refers to the tuning ratio of C_{var}. Hence, a tradeoff persist between a wide band operation and startup efficiency is apparent.

In LF band, the aspect ratio of the transistor are sized larger to increase the g_m to guarantee startup with a significant setback of parasitic effect; i.e., C_{gs} at high $V_{BIAS,N}$ [29]. This is not feasible for HF as the size of the core needs to be minimized in order to widen the operating frequency range.

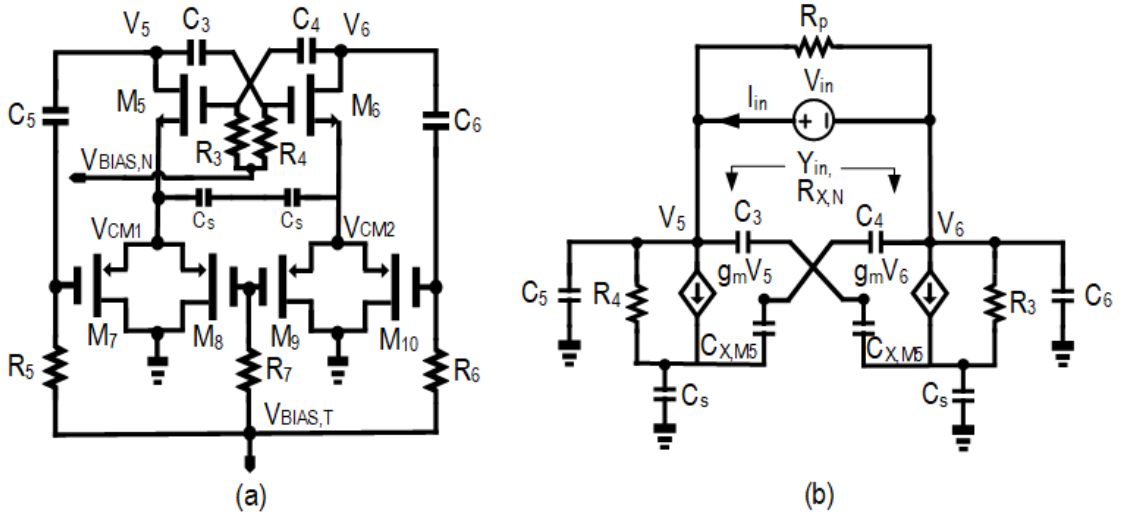

FIGURE 3. Class- C NMOS a) cross coupling pair M_5 and M_6 with capacitive source degeneration, C_s and b) the equivalent circuit model.

Therefore, with the implementation of source degeneration capacitors, C_s as shown in Fig. 3 (a), the equivalent parasitic capacitance can be reduced to achieve the desired frequency bandwidth. Depending on the transition frequency of a signal, the parasitic capacitances and resistance need to be diligently sized concurrently to achieve a wideband operation with a small chip area. Considering a half circuit analysis as shown in Fig. 3 (b), the parasitic capacitances of the NMOS class-C transistor, $C_{X,M5}$ lowers the capacitance tuning ratio and degrades the tuning range. The equivalent parasitic capacitance, $C_{X,M5}$ with the tank admittance, Y_P and the negative resistance, $-R$ of the NMOS class-C VCO consisting of $R_{X,N}$ are derived as

$$C_{X,M5} = \frac{-\omega^2}{2}\left[4C_{gd}+C_{sb,M5}+C_{db,M5}+C_{gs,M5}\right] \quad (7)$$

$$Y_P = \frac{2}{j\omega L}+\frac{2}{R_p}+\frac{j\omega C_{var}}{2} \quad (8)$$

$$R_{X,N} = \frac{V_{in}}{I_{in}} = 2\left[\frac{1}{g_{d,M5}}-\frac{1}{g_{m,M5}}\right] \quad (9)$$

$g_{m,M5}$ is the trans-conductance of the transistor M_5 and C_s is the source degeneration capacitor. The input impedance, $Z_{in(j\omega)}$ is derived as

$$Z_{in(j\omega)} = \frac{2}{j\omega\left(C_s + C_{X,M5}\right) - g_{m,M5}} \quad (10)$$

Therefore, by converting $Z_{in(j\omega)}$ to $Y_{in(j\omega)}$, the admittance of the transition frequency that contribute to achieve wide tuning range is given as (10).

$$Y_{in(j\omega)} = Re\left(Y_{in}\right) + jIm\left(Y_{in}\right) = \frac{\left\{\begin{array}{l}-\omega^2 C_s\left(2C_{X,M5}+C_s\right)g_{m,M5} \\ +j\omega^2 C_s\left[-g_{m,M5}^2-\omega^2\left(C_{X,M5}+C_s\right)\right]\end{array}\right\}}{2\left[g_{m,M5}^2+\omega^2\left(C_{X,M5}+C_s\right)^2\right]} \quad (11)$$

The parasitic of gate-to-drain $\left(C_{gd,M5}\right)$, source-to-bulk $\left(C_{sb,M5}\right)$ and drain-to-bulk $\left(C_{db,M5}\right)$ capacitance are neglected to simplify the transit frequency analysis. Hence, the equivalent resistance, R_{eq} and reactance, X_{eq} in (11) and (12) are attained as in [28], given as

$$R_{eq} = -\frac{2C_{X,M5}}{g_{m,M5}C_s}\left[\frac{1+\left(\frac{\omega}{\omega_T}\right)^2\left(1+\frac{C_s}{C_{X,M5}}\right)^2}{\left(\frac{\omega}{\omega_T}\right)^2 2\left(1+\frac{C_s}{2C_{X,M5}}\right)^2}\right] \quad (12)$$

$$X_{eq} = \frac{2}{\omega^2}\left[\frac{1+\left(\frac{\omega}{\omega_T}\right)^2\left(1+\frac{C_s}{C_{X,M5}}\right)^2}{1-\left(\frac{\omega}{\omega_T}\right)^2 C_s\left(1+\frac{C_s}{C_{X,M5}}\right)^2}\right] \quad (13)$$

where $\omega_T = g_{m,M5}/C_{gs,M5}$ is the unity gain frequency and $\omega_{tran} = \left(g_{m,M5}/C_{gs,M5}\right)\left(C_{gs,M5}/C_{gs,M5}+C_s\right)^{1/2}$ is the transition frequency which determines the mobility (inductive to capacitive) of the impedance. As observed in (10), the transition frequency reduces when C_s increases adding into the denominator and setting as $\omega^2\left(C_{X,M5}+C_s\right)^2 > g_{m,M5}^2$. Through this implementation, the negative resistance reduces. Therefore, the transistor size of M_5 and M_6 need to be sized diligently to reduce the feedback path effect (Fig. 6) contributed by the parasitic capacitances at a large $V_{BIAS,N}$, thereby, reducing both $1/f^2$ and $1/f^3$ noises.

Fig. 4 shows the simulated nonlinear equivalent capacitance of $C_{X,M5}$ and negative resistance, $R_{X,N}$ with different values of the source degeneration capacitor, C_S. At the range between 0.38 pF to 0.8 pF, $C_{X,M5}$ falls under <0.03 pF. For simplicity of $C_{X,M5}$, a particularly nonlinear gate to source capacitance, $C_{gs,M5}$ is taken into account as it brings significant effect towards the change in the instantaneous transit frequency expressed in (12) and (13). A well balanced point is attained in the defined range with suitable value of C_s. If C_s is sized optimally large, the VCO will be unstable leading towards squegging phenomenon which will deteriorate

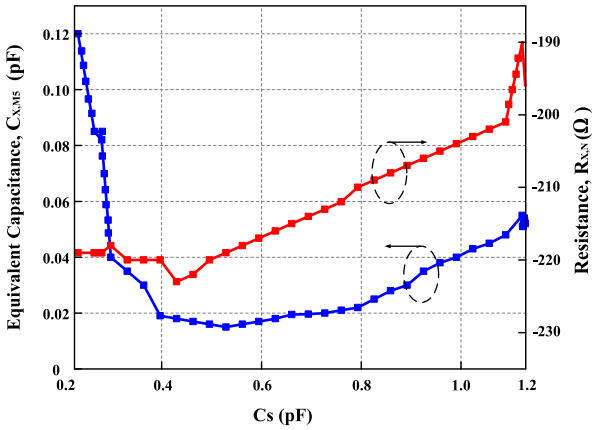

FIGURE 4. Simulated equivalent capacitance, $C_{X,M5}$ and negative resistance, $R_{X,N}$ in subthreshold conduction with different values of source – degeneration capacitance, C_s.

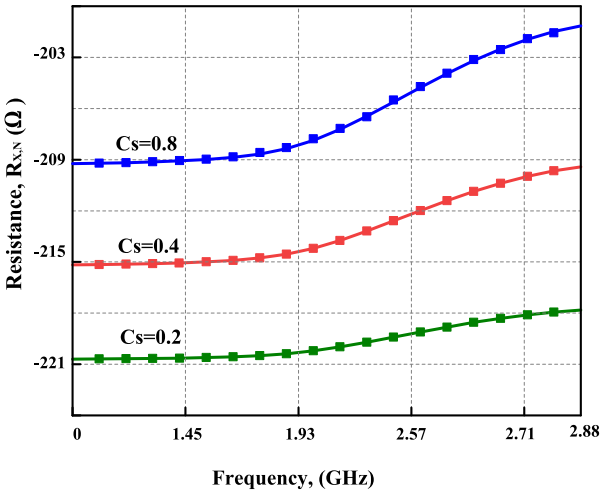

FIGURE 5. Simulated large-signal negative resistance, $R_{X,N}$ in subthreshold conduction under wide tuning range with different values of source – degeneration capacitance, C_s in particular value of 0.2, 0.4 and 0.8 pF.

the PN performances and cause startup problem. This CSD technique solely reduces the nonlinear equivalent capacitance of $C_{X,M5}$ while increasing the negative resistance, $R_{X,N}$.It shown that the capacitive source, C_s becomes a dominant factor towards altering the impedance of the negative resistance and also plays significant role towards widening the tuning range. In the absence of CSD, the negative resistance becomes low and imposes a difficulty in sustaining a prolong startup of the oscillator. However, when the value of C_s increases, the negative resistance increases proportionally but requires diligent transistor sizing to reduce the parasitic capacitance prior to Groszkowski's effect. In Fig.5, the value of C_s at the range of 0.2-0.4 pF, the negative resistance shows a constant value resulting favorably towards adequate startup and as C_s goes beyond 0.48pF, the negative resistance experiences a continuous increment, providing a high gain thus eliminating the impact of the buffer stage parasitic effect on the LC tank.

A conventional VCO commonly utilizes a single current source of stacked NMOS transistor for the tail biasing. By further splitting the tail current source transistors to an equal half, forms a lower amplitude of the common mode voltages, V_{CM1} and V_{CM2} compared to the conventional architecture, benefiting from C_s. To sustain the VCO in class-C operation mode, the output voltage amplitude of the tank in the boundary condition of saturation and subthreshold [30] are expressed as in (14) and (15), respectively

$$A_T < \frac{V_{DD} - \left|V_{BIAS,P}\right| - V_{th,P}}{2} \tag{14}$$

$$A_T < \frac{V_{BIAS,N} - V_{CM1/CM2} - V_{th,N}}{2} \tag{15}$$

A_T is the maximum voltage amplitude, $V_{BIAS,N}$ is the gate bias voltage of the NMOS class-C cross-coupled pairs of M_5 and M_6, V_{th} is the threshold voltage and V_{DD} is the drain supply voltage. Referring to (14) and (15), the overall maximum tank voltage swing attained without transistors driven into triode region is

$$A_T < \frac{V_{DD} + \left|V_{BIAS,P} - V_{th,P}\right| + \left|V_{BIAS,N} - V_{th,N}\right| - V_{CM1/CM2}}{2} \tag{16}$$

Therefore the PN of the class-C VCO is expressed in (17) respective to the overall value of A_T and $R_P\left(Y_p^{-1}\right)$ given in equation (16) and (8), respectively.

$$L(\Delta\omega) = 10\,log\left[\frac{k_B T\,(1+\gamma)\,R_p}{NQ^2A_T^2}\,\frac{\omega^2}{\Delta\omega^2}\right] \tag{17}$$

N is the number of resonators ($N = 1$ for single ended and $N = 2$ for differential oscillator with a single LC tank) [10], k_B is the Boltzmann's constant, T is the absolute temperature, γ is the MOS channel noise factor and R_P is the parallel tank impedance. The conduction angle becomes narrower as both PMOS pair (M_1 and M_2) and NMOS pair (M_5 and M_6) acquire different transistor gain operating in different gate voltage biasing condition at the saturation and subthreshold point of $V_{BIAS,P}$ and $V_{BIAS,N}$, respectively. The aspect ratio of PMOS-NMOS gain can be adjusted to achieve an equilibrium gain and achieve fast startup.

C. LOW NOISE AND LOW POWER CONTRIBUTION IN SUBTHRESHOLD CONDUCTION

Fig. 6 shows the low-power complementary class-C circuit operating under subthreshold region adopting PMOS transistors as the MOS current source. The operation yields a higher trans-conductance to power dissipation ratio which results in a decent noise performance. A substantial low impedance path of resistance to ground is formed at V_{CM1} and V_{CM2} which bypasses the output noise, thus improving the effective ISF [31]. Furthermore, the components of R_5C_5

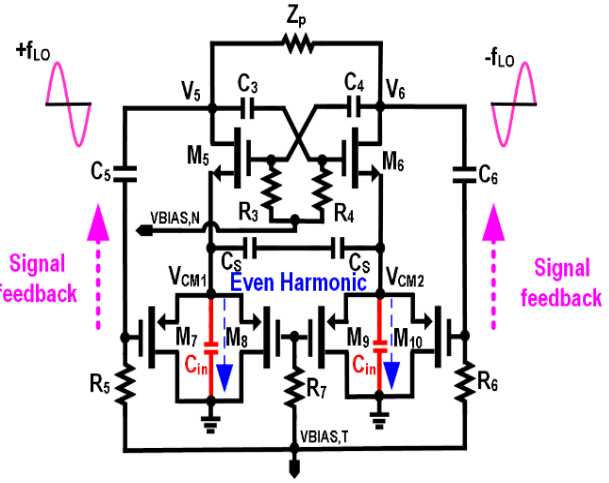

FIGURE 6. Subthreshold conduction with PMOS split current source.

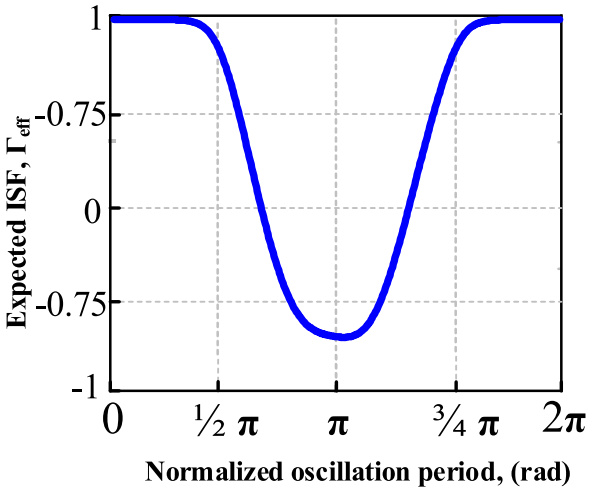

FIGURE 7. Estimated simulated ISF.

and R_6C_6 provide a feedback path for driving the AC signals, $+f_{LO}(-f_{LO})$ from the output to the respective gates of the PMOS tail current source, $M_7 - M_{10}$. The feedback components are sized adequately to be insensitive towards PN and to achieve die area optimization.

The intrinsic parasitic capacitance, C_{in} exist between each split tail current source pair suppresses the even order second harmonic $(2f_{LO})$ from the common mode nodes $(V_{CM1}\text{and}V_{CM2})$, improving the phase noise, (PN) performance. V_{CM1} and V_{CM2} in (15) adjust the threshold voltage of the differential class-C NMOS transistors results in a higher headroom for larger output voltage swing. Furthermore, the dc bias point, $V_{BIAS,T}$ favor towards the subthreshold biasing condition, $V_{GS} \approx V_{BIAS,T} \leq V_{th}$ improving the current efficiency simultaneously with an adequate active subthreshold MOS negative conductance, g_{sub} of the complementary class-C VCO, expressed as

$$g_{sub} = \frac{-g_{m5}}{2} = \frac{I_{DS}.q}{nk_BT} \tag{18}$$

g_{sub} of a class-C VCO in subthreshold region is computed from the subthreshold drain current, I_{DS} and is exponentially related to the gate voltage (V_G), source voltage (V_S) and drain voltage (V_D) of the NMOS transistor, M_5 and M_6 expressed as

$$I_{DS,M5(M6)} = I_0 e^{\frac{V_G}{nU_T}} \left(e^{\frac{V_S}{U_T}} - e^{\frac{V_D}{U_T}} \right) \tag{19}$$

in which subthreshold drain current, I_0 is defined as

$$I_0 = 2n\mu_e C_{ox} \frac{W_e}{L_e} U_T^2 e^{-\frac{V_{th}}{nU_T}} \tag{20}$$

q is the electronic charge, k_B is the Boltzmann's constant, T is the absolute temperature and n is the subthreshold slop factor dependent to process parameters and bias conditions denoted as $n = 1+C_{dep}/C_{ox}$. The capacitors C_{dep} and C_{ox} are the surface depletion and gate oxide capacitor, respectively. It is evident from (17) with a low bias $\left(V_{GS} \approx V_{BIAS,N}\right)$, the efficiency denoted by $\eta = P_{RF}/P_{DC}$ improves linearly which contributes towards a negligible amount of noise. The effective aspect ratio of M_5 and M_6 are adequately sized to improve I_0. The parameter μ_e is an effective carrier mobility in channel and $U_T = kT/q$ is the thermodynamic voltage. The output negative trans-conductance, G_{neg} at the output node voltage, V_5 is derived as

$$G_{neg} = -\frac{g_m + j\omega\left(C_{gs,M2} + C_s + C_{ds,M5}\right)}{2} \tag{21}$$

$$\sum R_{eq} = \left[\frac{-2}{g_m + j\omega\left(C_{gs,M2} + C_s + C_{ds,M5}\right)} \right] \| R_p \tag{22}$$

Therefore, the output voltage under subthreshold bias condition in (17) and (18) reduces to

$$V_5 = \left(R_{eq}\right) \cdot I_0 e^{\frac{V_G}{nU_T}} \left(e^{\frac{V_S}{U_T}} - e^{\frac{V_D}{U_T}} \right) \tag{23}$$

Fig. 7 illustrates the estimated simulated effective ISF waveform for the differential output voltage swing at steady state with $V_{BIAS,N}$ biasing at M_5 and M_6 under operation of subthreshold region.

The estimated effective ISF waveform shown in Fig.7 serve to be part of the ISF manipulation technique implied in [32]. As compared to the previous conventional circuit in [33] which adopts a single-tail transistor, the proposed feature substitutes a symmetrical sized two PMOS transistor to filter the noise out at the low impedance to ground path. This helps in steering the tail current that reduces the switching losses of the cross-couple M_5 and M_6 approaching to an equilibrium state. Prior to that, the conduction angle becomes lower, improving the power efficiency. The effective ISF is derived as

$$\omega_{1/f^3} \approx \frac{1}{2} \cdot \omega_{1/f} \cdot \left(\frac{\Gamma_{\text{EFF,DC}}}{\Gamma_{\text{EFF,H1}}} \right)^2 \tag{24}$$

The equation (24) shows that the improvement of the flicker noise corner at the 30 dB/dec region affected by the purity of

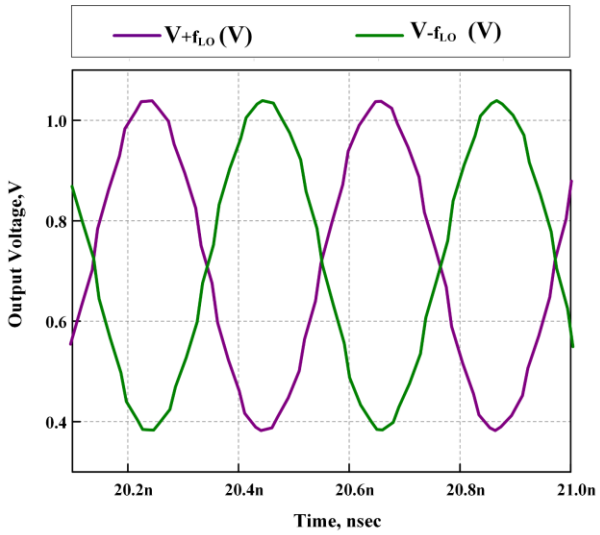

FIGURE 8. Simulated differential output voltage swing.

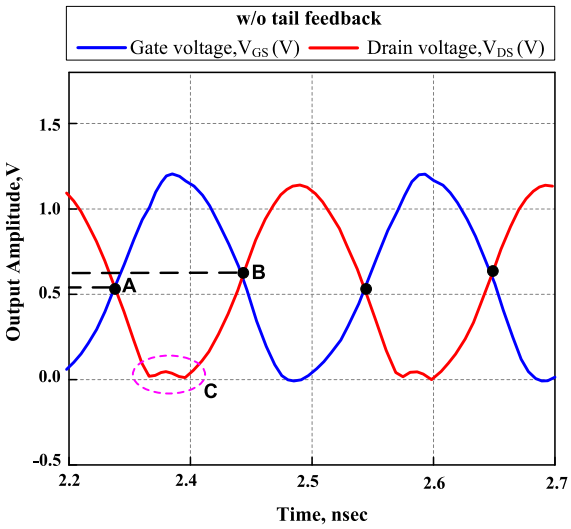

FIGURE 9. Simulated gate and drain voltage without tail feedback.

an effective DC value and effective first harmonic of the oscillation. As, the second harmonic content being suppressed, the tail noise modulation function (NMF) will be reduced to half, achieving a even smaller effective ISF. Fig. 8 shows the differential AC signals of $-f_{LO}$ and $+f_{LO}$ appears to be distorted due to the signal with noise contribution from the complementary non-linear active devices that had feed back to the oscillator via the path generated by the RC components of R_5C_5 and R_6C_6. Alternatively, Fig. 9 shows asymmetric oscillation of the simulated transient voltage waveforms of the drain voltage, $V_{DS,M5(M6)}$ and gate voltage, $V_{GS,M5(M6)}$ of M_5 and M_6. Point A and B shows the $1/f$ flicker noise up-conversion into the $1/f^3$ close in phase noise region. When the gate voltage, $V_{GS,M5(M6)}$ and drain voltage, $V_{DS,M5(M6)}$ are same, the VCO will be more sensitive to the injected noise, thereby resulting in zero crossing point differ in between this two operating voltages. Without the tail

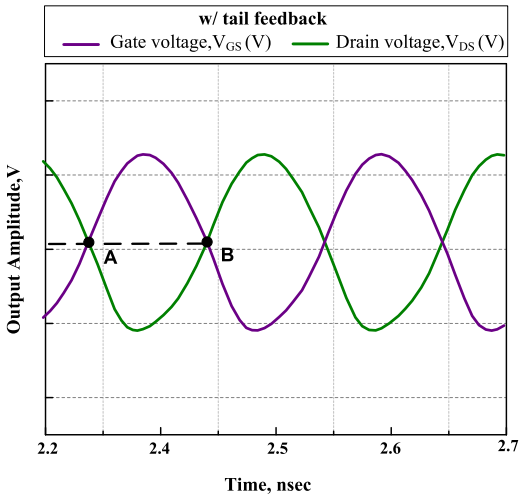

FIGURE 10. Simulated gate and drain voltage with tail feedback.

feedback with external biasing, the cross-coupled transistor are subjected into triode region, generating a significant amount of noise, causing an amplitude distortion as shown in point C. Fig. 10 shows a more balanced symmetric waveform attained with the advantage of the tail feedback and aided through the symmetrical auxiliary $-g_m$ class-B oscillator under low power operation. The PN performance with and without the tail feedback is shown in Fig. 12 where at 1 MHz offset, the proposed architecture demonstrates approximately 14 dB of PN improvement compared to the conventional oscillator [12] operating at 2.45 GHz oscillation frequency. The PN improvement due to CSD technique implied with feedback RC components biasing, reduces the non-linear parasitic capacitance triggering towards lower flicker noise up-conversion via AM to PM conversion mode making it less significant in the far out phase noise region.

D. PHASE NOISE

PN degradation via $1/f^2$ and $1/f^3$ upconversion are mainly contributed by the active noise sources in the oscillator. However, with the subthreshold biasing and substitution of PMOS device as tail transistors, the respective tail noise has dual path flow which is through M_5 and M_6 and back to the signal output shown in Fig. 6. Alternately, the second pathway is via M_7 and M_8 (M_9 and M_{10}) to ground. A low impedance path seen from the each source of M_5 and M_6 attracts considerably the tail noises as compared to the drain of M_7 and M_8 (M_9 and M_{10}). In reference to [31], the effective ISF, Γ_{eff} (Fig. 7) becomes smaller in amplitude since low injection of the tail noise flows to the output leading towards phase insensitivity at the tail transistors. The smaller Γ_{eff} brings an advantage of a lower amplitude in the second order harmonic current noise or negligible with the presence of the low common mode oscillation point, V_{CM1} and V_{CM2}. In weak inversion region, the presence of shot noise and drain current noise of the PMOS (NMOS) has an exponential dependence on the gate voltage, $V_{BIAS,T}$ that are shared within the transistors. Fig. 11 illustrates a

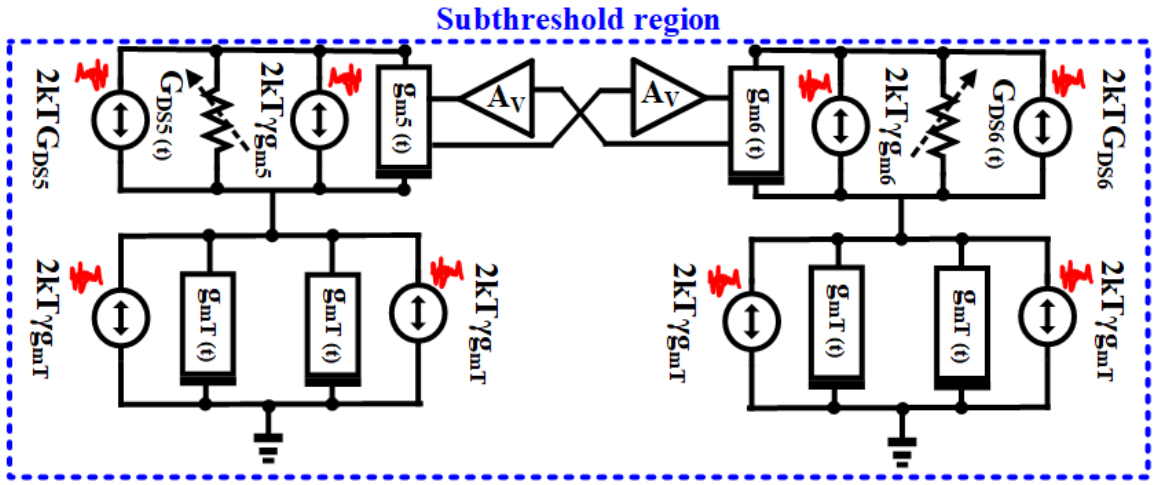

FIGURE 11. Noise sources model of the proposed subthreshold circuit.

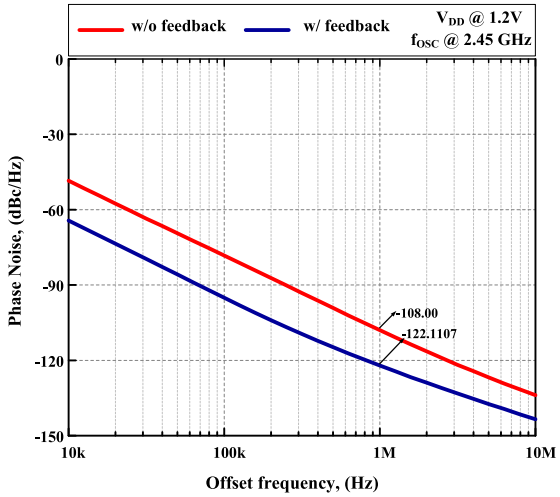

FIGURE 12. Simulated phase noise with and without tail feedback.

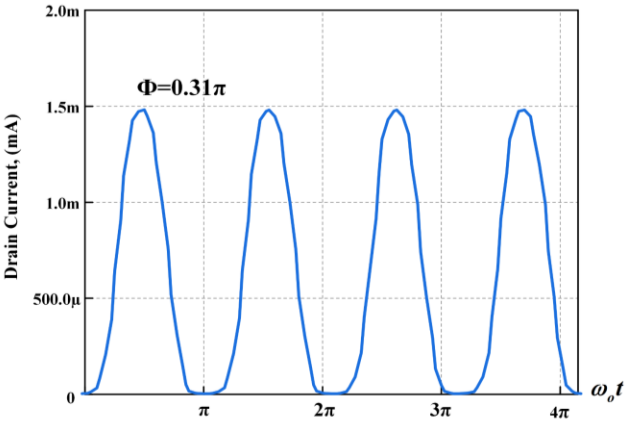

FIGURE 13. Simulated drain current of the proposed architecture.

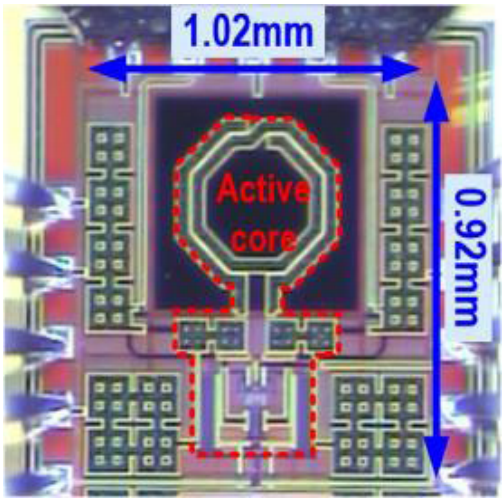

FIGURE 14. Chip photomicrograph of the proposed architecture.

simplified model of the noise sources of the proposed subthreshold architecture classifying the noise contribution from the NMOS cross-coupled trans-conductance and PMOS current biasing transistors. Noise model where $g_{m5(m6)}$ (t) and $G_{DS5(6)}$ (t) represent the trans-conductance and channel conductance of transistor M_5 and M_6 respectively. Apart from it, g_{mT} is the trans-conductance of PMOS current source transistors for M_7 and M_8 (M_9 and M_{10}). Fig. 13 depicts the simulated drain current at $V_{BIAS,N}$ near the transistor's threshold value which is shown to secure sufficient gain while ensuring an appropriate startup with the oscillation swing being enhanced. The current efficiency improves >60% in the effect of a narrower conduction angle with better PN performance.

In order to simplify the noise derivation, the finite trans-conductance of the transistors are ignored. The coupling capacitors, C_3, C_4, C_5 and C_6 are considered as short circuits since they are sized larger than the gate parasitic capacitance of the respective transistors. Since $V_{BIAS,P}$, $V_{BIAS,N}$ and $V_{BIAS,T}$ comprises different dc bias point, unequal output noise currents are attained.

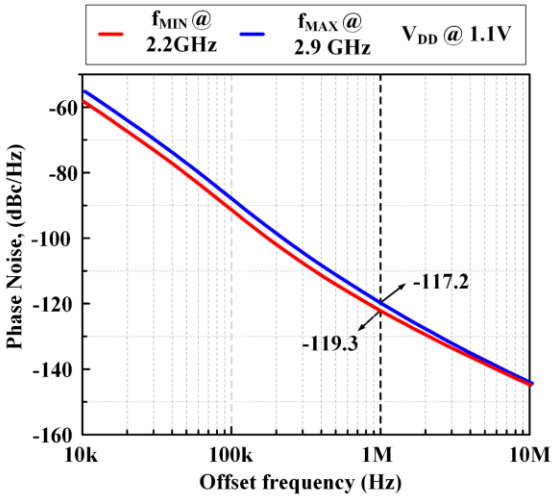

FIGURE 15. Measured PN against offset frequency at V_{DD} at 1.1V.

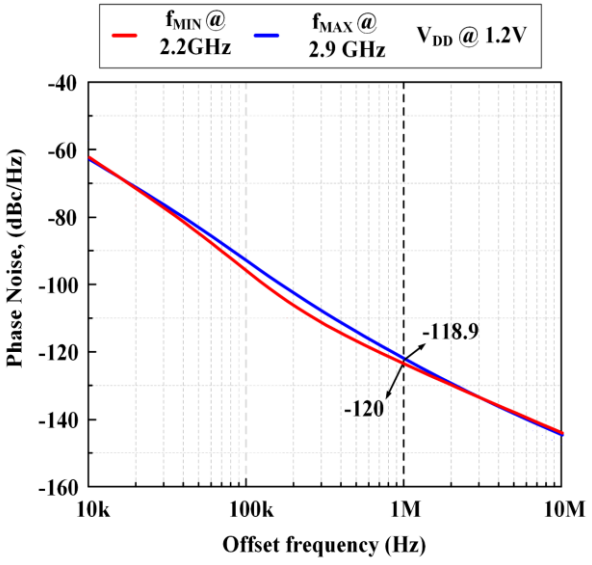

FIGURE 16. Measured PN against offset frequency at V_{DD} at 1.2V.

Equation (25) expresses the weak inversion mode drain noise current in the subthreshold region of M_5 and M_6.

$$\overline{I_{nd}^{2+}} = \frac{4kTC_{ox}\rho}{f} + 2qI_{DS} \tag{25}$$

where $k_f = 4kTC_{ox}\rho$ is the empirical coefficient and I_{DS} is the net drain current. In comparison to the superthreshold regime in proposed in [34], [35], the effective thermal noises, $I_{nd}^{2+}/\Delta f = 4kT\gamma g_m$ are still comparable with the shot noise in weak inversion mode. Equation (25) proves that the shot noise dominates the white noise present in the MOS transistors [35]. In this operation mode, the shot noise component is reduced to be as $2k_BT(g_m + g_{mb})$. The current source biased in subthreshold reduces the overall power consumption of the VCO. Smaller flicker noise upconversion $(1/f)$ reduces the

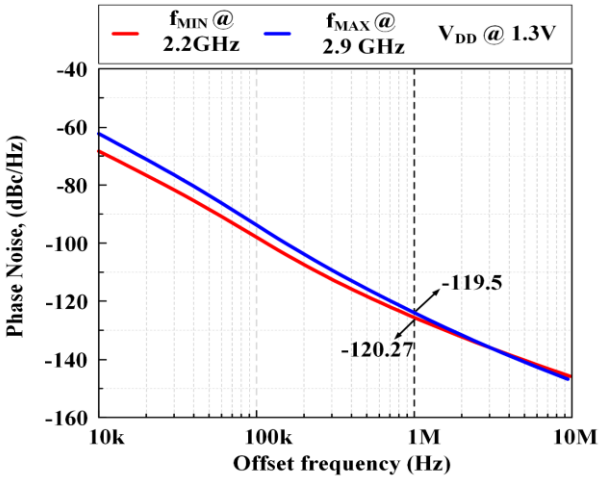

FIGURE 17. Measured PN against offset frequency at V_{DD} at 1.3V.

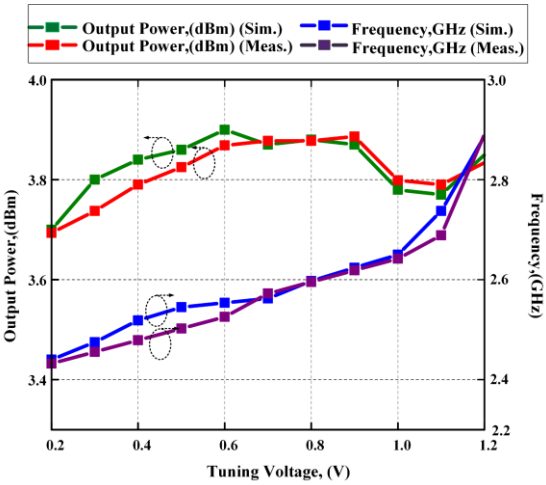

FIGURE 18. Measured and simulated output power, dBm and frequency, GHz against tuning voltage, V.

current noise shown as

$$\frac{\bar{I}_{nd}^{2+}}{\Delta f} = \frac{K_f}{f} + 2qI_{DS,M5(M6)} \tag{26}$$

where q is the electron charge and $I_{DS,M5(M6)}$ is the net drain current of transistor M_5 and M_6. It had been verified in the previous research works [36] that the phase noise of the MOS oscillator in the flicker noise region of $1/f^3$ doesn't depend on the gate bias, $V_{BIAS,N}$. In addition, this conduction with an adequate sizing width of the transistor creates a lower K_f and current noise, thus lowers the phase noise as shown below in equation (27).

$$L(\Delta\omega) = 10\log\left[\frac{\Gamma_{\text{in,rms}}^2\left(\vec{I_{nd}^{2+}}/\Delta f\right)}{2q_{\max}^2\Delta\omega^2}\right] \tag{27}$$

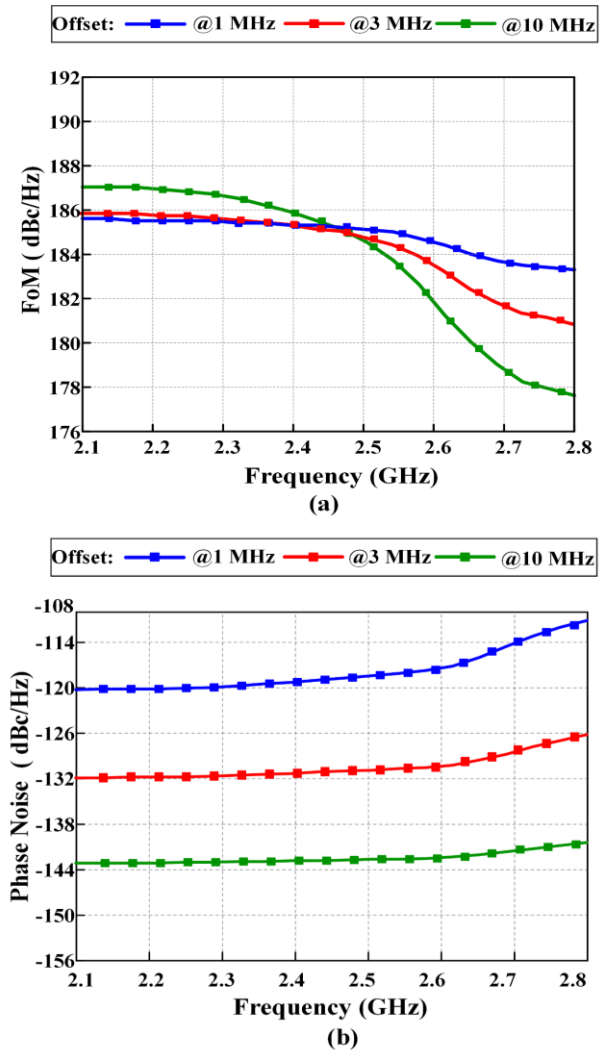

FIGURE 19. Measured a) FoM b) Phase Noise, PN against the tuning frequency of the proposed architecture VCO.

Moreover, as this region accommodates PMOS transistors, reduction in power consumption and a high potential of transconductance to the bias current is observed. The PMOS current source transistors are linearly dependent on the bias condition, $V_{BIAS,T}$ while the $1/f$ up-conversion subsequently reduced by increasing the device dimension expressed as

$$\gamma = \frac{2n_1}{3 + \left(\frac{g_m}{I_{DS}} n_1 U_T\right)} \tag{28}$$

where γ is the correction factor, U_T denotes the thermodynamic voltage and n_1 is the slope factor. Therefore the noise current for the M_5 and M_6 in the subthreshold region is given as

$$\frac{\overline{I_{nd}^{2+}}}{\Delta f} = 2kTqg_m \tag{29}$$

where q is the electron charge.

TABLE 1. Performance summary of the proposed architecture.

Parameters	Results
Submicron Technology, nm	180
Operating Frequency, GHz	2.45
Frequency Bandwidth, GHz	2.2 – 2.9
Phase Noise(PN), dBc/Hz @ 1 MHz	-120
Phase Noise(PN), dBc/Hz @ 3 MHz	-132.10
Phase Noise(PN), dBc/Hz @ 10 MHz	-142.12
Figure of Merit(FoM), dBc/Hz @ 1MHz	185.41
Figure of Merit(FoM), dBc/Hz @ 3MHz	185.45
Figure of Merit(FoM) dBc/Hz @ 10MHz	187.52
Tuning Range(TR), %	28.60
Flicker Noise Corner, kHz (Sim.)	<100
Flicker Noise Corner,kHz (Meas.)	200
Frequency Pushing, MHz/V (Sim.)	<75
Output Power, dBm (Meas.)	3.76
Voltage Supply, V_{DD}	1.2
Power Consumption, P_{DC}	1.73
Current conversion efficiency, α_I	>0.6
Active core area, mm^2	0.3
Startup time, ns	2.0

Hence, the output noise voltages reduced as computed under this region comprises a half circuit analysis as

$$\overline{V_{n,M5(M6)}^2} = 2kT\left(1 + \frac{g_m}{g_{mb}}\right)\left[\frac{Y_P^2 + G_m^2}{\left(Y_P^2 - G_m^2\right)^2}\right]\Delta f \tag{30}$$

where the G_m is the conductance of M_5 and Y_P^2 is the squaring tank admittance equated in (8).

III. EXPERIMENTAL RESULT

Fabricated in 0.18 μm CMOS process, the micrograph of the proposed VCO is shown in Fig. 14. The VCO occupies a 0.3 mm^2 active silicon area and consumes an average power of 1.73 mW under 1.2 V of supply headroom. With on-wafer probing, the measured PN for the proposed architecture at $f_{\mathrm{MIN}} = 2.2$ GHz and $f_{\mathrm{MAX}} = 2.9$ GHz are shown in Fig. 15, 16 and 17 under the supply variation of 1.1 V, 1.2 V and 1.3 V, respectively. Fig.18 shows the measured output power of 3.76 dBm at 2.45 GHz under the tuning voltage of 0.6 V. Finally, Fig.19 depicts the measured PN and FoM across the tuning frequency range. At 1 MHz offset frequency for 2.45 GHz, the proposed VCO achieves an excellent PN performance of -120 dBc/Hz which translates to a FoM of 185.41 dBc/Hz. The VCO is tunable from 2.2 to 2.9 GHz resulting in a tuning range of 28.6%. Table 1 summarizes the performance of the proposed oscillator whereas Table 2 compares the VCO with recent reported state-of-the-art works.

TABLE 2. Performance comparison summary.

Specification		This Work	[37]	[38]	[39]	[40]	[41]
Frequency Range (GHz)		2.2 – 2.9	10.53-11.35	4.92-5.7	4.67-5.18	2.05-2.75	5.4-7.0
Tuning Range (%)		28.6	7.5	14.7	10.3	29	25
V_{DD} (V)		1.2	0.46	1.4	1.8	1.8	1
CMOS Technology (nm)		180	180	180	180	180	40
VCO Core Area (mm²)		0.3	N/A	@0.98	0.285	N/A	0.13
Frequency (GHz)		2.45	10.94	5.31	4.925	2.4	5.4
Power,P_{DC} (mW)		1.73	0.346	2.5[&]	8.46	18	12
PN (dBc/Hz)	1 MHz	-120	-107.8	-118	-120.0	-119.5	-124.5 @ 5 GHz
	10 MHz	-142.12	-123[*]	-120[*]	-145[*]	-139[*]	-144.5
FoM (dBc/Hz)	1 MHz	185.40	193.2	188.52	184.58	174.55	188.36
	10 MHz	187.52	188.39	170.52	189.58	174.05	188.36
FoM_T (dBc/Hz)	1 MHz	194.52	190.70	191.87	184.84	183.80	196.32
	10 MHz	196.65	185.89	173.87	189.84	183.30	196.32
Passives		1 inductor	1 inductor	1 inductor	SVA	1 inductor	1 Inductor and 1 Transformer

[&]Only VCO core considered [*]Normalized from 10 MHz offset @Include test pad

SVA: Switched Varactor Array 1:$FoM - PN + 20\,log(f_o/\Delta f) - 10\log(P_{DC}/1mW)$ 2: FoM_T: $FoM + 20\log\left(TR\%/_{10}\right)$

IV. CONCLUSION

In this paper, a complementary class-C VCO with a modified tail biasing structure adapting a split PMOS as a tail current source feedback has been proposed. To ensure a fast startup, an auxiliary - g_m stage has been integrated to cancel the parasitic resistance of the resonant tank. Dual RC biased network has been implemented in the complementary Class-C VCO operating under saturation and subthreshold region to further improve the PN performance as compared to the conventional architecture in the recent reported work. The proposed VCO achieves a good FoM of 185.41 dBc/Hz with a competitive tuning range of 28.6%.

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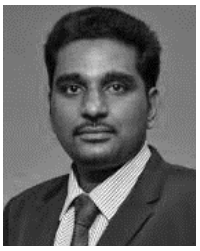

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