HIL-RT Implementation of UHVDC Transmission System Based on Series-Connected VSC Modules

XIAOFAN FU[1], (Member, IEEE), **ALIREZA JAVADI**[1], (Member, IEEE),
KAMAL AL-HADDAD[1], (Fellow, IEEE), **LOUIS-A. DESSAINT**[1], (Fellow, IEEE),
WEI LI[2], (Member, IEEE), AND **BOON-TECK OOI**[3], (Fellow, IEEE)

[1]Department of Electrical Engineering, École de Technologie Supérieure, Université du Québec, Montréal, QC H3C 1K3, Canada
[2]OPAL-RT Technologies Inc., Montréal, QC H3K 1G6, Canada
[3]Department of Electrical and Computer Engineering, McGill University, Montréal, QC H3A 0E9, Canada

Corresponding author: Xiaofan Fu (xiao-fan.fu.1@ ens.etsmtl.ca)

ABSTRACT This paper presents an ultra-high-voltage direct current (UHVDC) transmission system based on the series-connected voltage source converter (VSC) modules. A detailed DC voltage equalization control strategy is developed for the series-connected VSC modules at both terminals of the UHVDC transmission system. Moreover, the phase-shifted triangle carrier concept is applied for generating the pulse width modulation (PWM) signals to eliminate AC line current harmonics and reduce converter switching losses. Besides, harmonic elimination comparison between applying the conventional sine pulse width modulation (SPWM) and the phase-shifted triangle carrier-based pulse width modulation (PSCPWM) techniques is done. Furthermore, a hardware-in-the-loop (HIL) real-time (RT) UHVDC validation model was set up by connecting a real-time simulator of OPAL-RT which ran the power electronics-power system parts and a dSPACE 1103-based prototype controller which was used to implement the control part. Finally, the real-time dynamic performance of the series-connected VSC models UHVDC system is validated in operation at different transient and steady state modes.

INDEX TERMS Series-connected VSC modules, UHVDC, DC voltage equalization, phase-shifted carrier SPWM, hardware-in-the-loop, real-time simulation.

I. INTRODUCTION

Nowadays commercial, industrial, and residential level of energy consumption has become a strategic issue because of the constant increase of energy demand and it is expected to continue as such for many years. The ever need of mashing and interconnecting several neighboring energy providers networks has become a necessity since smart grid and secure energy supply implementation is underway. Another challenge is the need to transit offshore, interstates inter-countries energy resources and deliver large quantities of electricity from power generating stations to urban centers to meet the increasing intense demand of electricity [1]. The so-called ultra-high-voltage DC transmission (UHVDC) means the transmission of energy at ±600 kV to ±800 kV or higher classified as UHVDC [1], [2]. The main features of UHVDC are the long-distance, low-loss and high-capacity

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power transmission. Thus, UHVDC has become a serious option that offers the promise to meet the aforementioned challenge. Some ultra-high voltage direct current projects are in operation in China, for example, the ±800 kV DC voltage, 1935 km Xiangjiaba-Shanghai UHVDC with rated power of 6,400 MW [3]; and the ±800 kV DC voltage, 1373 km Yunnan-Guangdong UHVDC with rated power of 5000 MW [4]. Another example is Ximeng to Taizhou ±800kV UHVDC transmission project, with rated power 10000MW, and that is the first UHVDC project with high voltage and low voltage converter split connection to 500kV and 1000kV power grid [5]. More ultra-high voltage direct current projects are under construction in other countries, such as Brazil and India.

The existing line-commutated thyristor type UHVDC projects such as [5], [6] and [7] and the great interest in modular multilevel converter (MMC), seen in [8]–[12] are the driving forces for this research. For example, in [5] the split connection mode control function was analyzed and the

dynamic performance of the UHVDC system was simulated. In [6], the DC variables, the equivalent powers of the converters, and the mismatch equations are decided. Both [5] and [6] are studied under the hierarchical connection mode and the inverters are connected on two different AC voltages. For reliability analysis to UHVDC systems, in [7], a new sensitivity model after equivalence is proposed, and the latter helps to determine the vulnerable parameters and components of UHVDC system, find countermeasures, or estimate error results from the uncertainty of reliability parameters. Most of these UHVDC systems mentioned above are based on the thyristor converters. However, thyristor based UHVDC converters have the weaknesses that it necessitates an expensive filters on both AC and DC sides and power flow reversal interruption to change voltage polarity [13]. As voltage source converter (VSC) based HVDC are free from the weaknesses mentioned before, so this paper examines the real-time performance of VSC modules based UHVDC transmission system.

In very recent year, with the hot trend of MMC topology, the competition from MMC topology obliged partisans of VSC to examine if the excellent characteristics of VSC-HVDC can be fully realized by adopting multi-modularity approach. However, it should be noted that although MMC reduces high frequency harmonics, a large number of components are required and a large number of control signals need to be sent to the controller. While a conventional VSC-HVDC is well-known to have flexibility such as: (1) decoupled active power and reactive power (P-Q) control [13]; (2) capability of reversal power flow without change voltage polarity [14], [15]; (3) low total harmonic distortion (THD) [16]–[19]. Moreover, [20] examined the feasibility of series-connecting four voltage source converter (VSC) modules, each rated at 200 kV voltage, to form a pole of UHVDC rated at 800 kV DC voltage including the desirable features of the previously mentioned UHVDC system. Based on general analysis of the series-connected VSC modules topology and conventional decoupled power control strategy, it was demonstrated that the equal DC voltages can be obtained by negative feedback as presented in [20]. In this paper, the improved control strategy with DC voltage equalization at both terminals of the UHVDC transmission system is presented.

As we know, phase-shifted PWM technique (PSPWM) is a popular modulation method for MMC topology [21]–[25]. For example, [23] and [24] both adopted conventional phase-shifted pulse width modulation techniques for cascaded H-bridge multilevel converters and in [25], it analyzed the performances of different carrier phase-shifting PWM techniques to be used onto a multilevel cascaded H-bridge converter in case of unbalanced operational conditions. Since the series connection of VSC modules contributes multilevel topology, which allows the PSPWM technique to be applied to this research. The different phase-shifted carrier angles are presented according to the number of the series-connected VSC modules and it is expected to eliminate AC current harmonics and reduce converter switching losses [26], [27].

Additionally, since real-time enables HIL simulation and HIL testing offers an excellent alternative to traditional testing methods, especially in high-voltage application [28], [29]. When performing HIL simulation, the physical plant is replaced by a precisely equivalent computer model running in real-time on a simulator appropriately equipped with inputs and outputs (I/Os) capable of interfacing with hardware control systems and other equipments [30]. Therefore, in this paper a HIL real-time test platform was set up by connecting the real-time digital simulator/target to an external real time controller dSPACE type of controller. The configuration of the OPAL-RT simulator-based HIL test bench for series-connected VSC modules based UHVDC system is shown in Fig. 1. The dynamic performance of the series-connected VSC modules based UHVDC system is validated in various operating conditions and test cases.
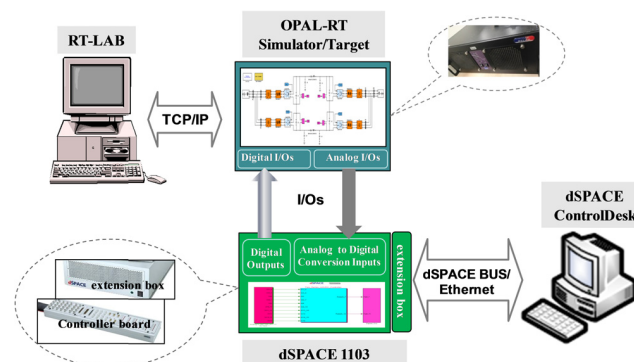
FIGURE 1. Configuration of the OPAL-RT simulator-based HIL test bench for VSC modules based UHVDC system.

The objective of this research is to examine real-time HIL performance of series-connected VSC modules to form a UHVDC system. The three primary reasons for using series connection topologies are: (i) to raise the DC transmission voltage; (ii) to reduce THD and (iii) to reduce switching losses. The contribution of this research shows that this presented UHVDC system, based on connecting VSC modules in series, enjoys the three benefits.

The paper is organized as follow: the characteristics and basic modeling of the series-connected VSC modules for UHVDC system is described in section II. The detailed control strategy of series-connected VSC modules for UHVDC system is presented in section III. In section IV, the method of applying phase-shifted triangle carrier SPWM technique for series-connected VSC modules to eliminate AC current harmonics and reduce switching losses is presented and simulated. Different real-time HIL tests are implemented in section V. Finally, conclusions are made in section VI.

II. MODELING OF VSC MODULES FOR UHVDC
The topology of the series-connected VSC modules UHVDC system (one pole) is depicted in Fig. 2. AC System 1 (receiving terminal) and AC System 2 (sending terminal) are interconnected via a DC transmission line. The UHVDC station
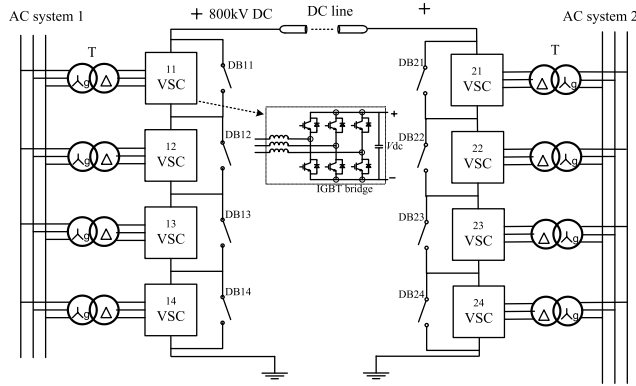
FIGURE 2. Topology of the series-connected VSC modules UHVDC system (one pole) [20].

consists of a series connection of four modules of two-level VSCs rated at DC voltage 200 kV each. The series-connected modules enable the DC voltage to reach 800 kV. Isolation on the AC side is achieved by Y/Δ transformers [20]. For reliability, the DC breaker (DB) switch, across the DC terminals of each VSC module, bypass the terminals when the module fails so that the pole continues to operate, but from 800 kV DC voltage to a lower voltage of 600 kV DC. Thus, one of the merits of the topology shown in Figure 2 is that by using DC breakers it still enables 75% power transmitted when one of the VSC modules is out of work at each terminal. Moreover, it enables flexible options according to the requirements of the power dispatch. For example, when VSC14 in AC system 1 is bypassed, VSC24 or VSC23 or any one of VSC modules in AC system 2 could be bypassed. Besides, AC system 1 and AC system 2 can operate in unsynchronized mode. This UHVDC topology inherits some advantages of robust VSC-HVDC system such as uprating and upgrading instead of rebuilding. Moreover, this topology provides a simple and feasible solution for UHVDC power transmission systems.

To increase the integrity and readability of the content, the circuit analysis and circuit equations, begins with

assigning unequal inductance and resistance values and controlling variables to the jth VSC module, are presented hereafter and a more detailed description can be found in [20]:

$$L_j\left(di_{aj}/dt\right) + R_j i_{aj} = e_a - \left(m_{aj} U_{dc-j}/2\right) \quad (1)$$

$$L_j\left(di_{bj}/dt\right) + R_j i_{bj} = e_b - \left(m_{bj} U_{dc-j}/2\right) \quad (2)$$

$$L_j\left(di_{cj}/dt\right) + R_j i_{cj} = e_c - \left(m_{cj} U_{dc-j}/2\right) \quad (3)$$

where, e_a, e_b, and e_c are the voltages from the AC system referred to VSC side of the transformers; i_{aj}, i_{bj} and i_{cj} are the 3-phase currents; and m_{aj}, m_{bj} and m_{cj} are the modulating signals. U_{dc-j} is the voltage across the DC capacitor C_j, L_j and R_j are the equivalent inductance and resistance on the AC side.

From the view of power balance, the DC current of the VSC is:

$$i_{dc-j} = \left(m_{aj} i_{aj} + m_{bj} i_{bj} + m_{cj} i_{cj}\right)/2 \quad (4)$$

Assuming that the DC line current is i_{DC}, the voltage across the capacitor C_j is:

$$C_j\left(dU_{dc-j}\right)/dt = i_{dc-j} - i_{DC} \quad (5)$$

The total DC voltage across four VSC modules is:

$$V_{tot} = \sum_{j=1}^{4} U_{dc-j} \quad (6)$$

Let the currents i_{aj}, i_{bj} and i_{cj} on the Δ side of the transformers be transformed to i_{aj}^1, i_{bj}^1 and i_{cj}^1 on the Y side.

From Kirchhoff's current law, the AC bus currents from the Y transformer windings are:

$$i_a = \sum_{j}^{j=4} i_{aj}^1 \quad i_b = \sum_{j}^{j=4} i_{bj}^1 \quad i_c = \sum_{j}^{j=4} i_{cj}^1 \quad (7)$$

In general, manufacturers have the ability to produce N units of VSC module which meet identical specifications. This is because they can meet tight tolerances so that $L_j \cong L$, $R_j \cong R$ and $C_j \cong C$ for $j = 1, 2, 3, 4$, and likewise for the modulating signals $m_{aj} \cong m_a$, $m_{bj} \cong m_b$ and $m_{cj} \cong m_c$
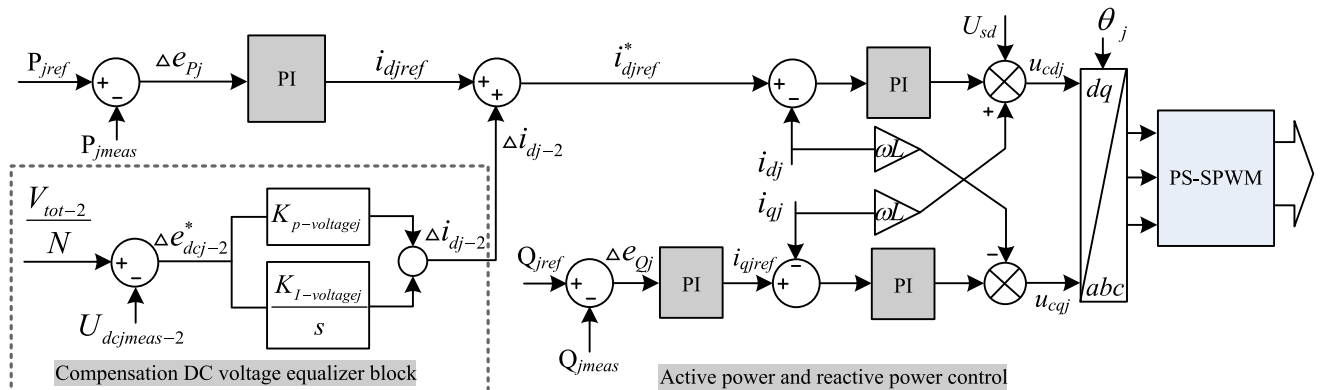

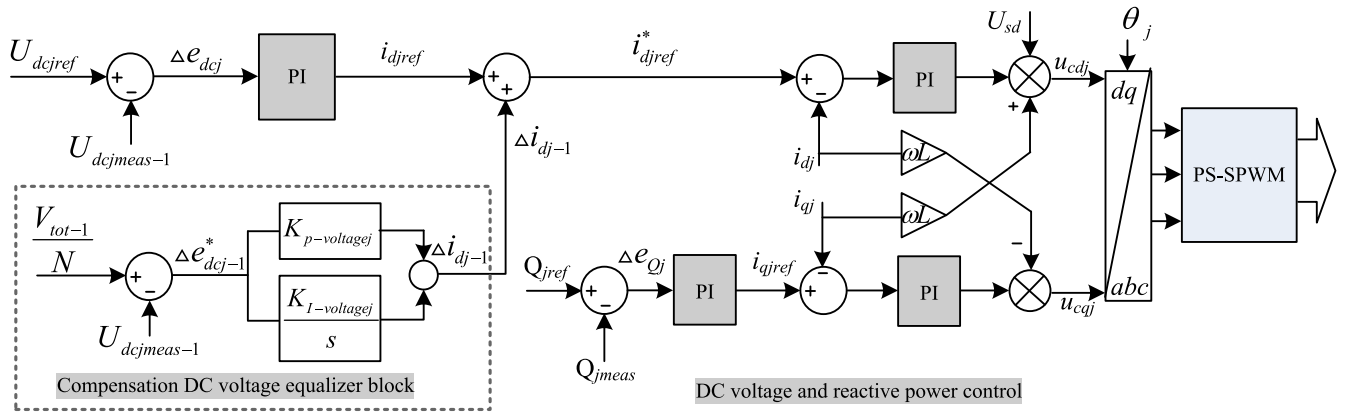**FIGURE 3.** Power control with DC voltage equalization for VSC modules at sending terminal.

FIGURE 4. DC voltage control with DC voltage equalization for VSC modules at receiving terminal.

for $j = 1, 2, 3, 4$. The four VSC modules would operate identically provided in (1), (2) and (3), $U_{dc-j} = U^*_{dcref}$ for $j = 1, 2, 3, 4$, where the DC voltage reference for the compensation is calculated as below:

$$U^*_{dcref} = V_{tot}/4 \qquad (8)$$

So for the series-connected VSC modules, the equalization of DC voltages can be achieved by negative feedback, which will be designed in the following section.

III. DC VOLTAGE EQUALIZATION FOR SERIES-CONNECTED VSC MODULES UHVDC

The conventional decoupled active power and reactive power control strategy was presented in [20]. In this case, all the VSC modules at receiving terminal (AC system 1) work in DC voltage and reactive power regulation mode and all the VSC modules at sending terminal (AC system 2) work in active power and reactive power mode; and VSC modules at the same terminal are used the same control strategy. Based on above mentioned decoupled control strategy and combined with DC voltage equalization control strategy, the detailed control system is designed for both sending and receiving terminals.

A. POWER CONTROL WITH DC VOLTAGE EQUALIZATION AT SENDING TERMINAL

Fig. 3 presents the power control with DC voltage equalization block for VSC modules at sending terminal. In the conventional decoupled active and reactive power control, i_{djref} is sent to command the jth VSC to produce power so that the error Δe_{pj} is nulled. However, with DC voltage equalization, a corrective signal Δi_{dj-2} is added to original current reference i_{djref} so that a new current command is generated i^*_{djref}. The size of the corrective signal Δi_{dj-2} is based on the voltage error Δe^*_{dcj-2} being nulled by the negative feedback.
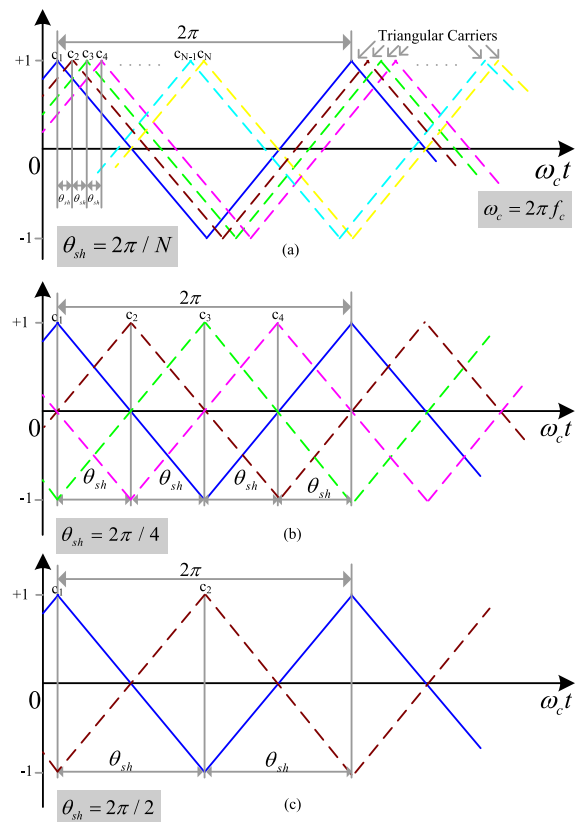

FIGURE 5. Phase-shifted triangular carriers, (a) for N VSC modules; (b) for four VSC modules; (c) for two VSC module.

The DC voltage across the jth VSC module at the sending terminal is measured as $U_{dcjmeas-2}$. The measurement of each individual DC bus voltages are summed up as:

$$V_{tot-2} = \sum_{j=1}^{N} U_{dcjmeas-2} \qquad (9)$$

Thus, the equalization reference is V_{tot-2}/N, which is used in the compensation DC voltage equalizer block of Fig. 3.
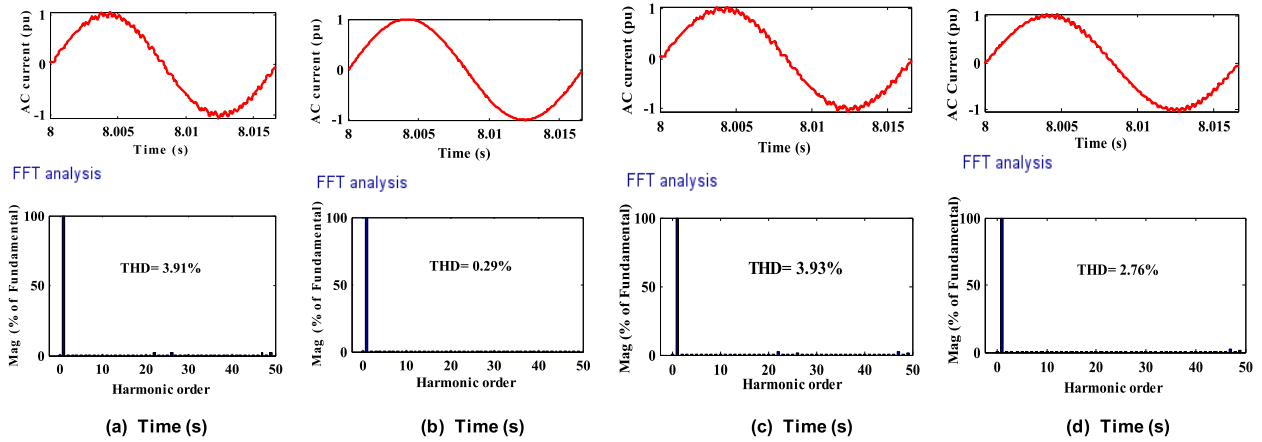
FIGURE 6. AC current and its harmonic spectrum, (a) with regular SPWM of four series-connected VSC modules, (b) with phase-shifted SPWM of four series-connected VSC modules, (c) with regular SPWM of two series-connected VSC modules, (d) with phase-shifted SPWM of two series-connected VSC modules.
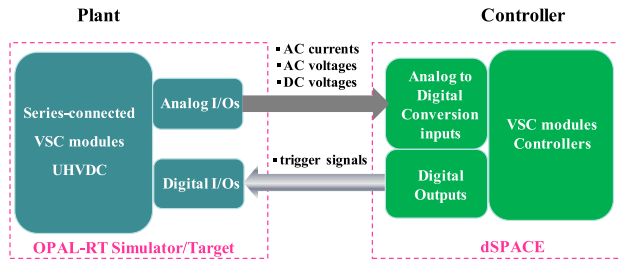
FIGURE 7. Schematic diagram of the plant and controller.

TABLE 1. Parameters of the VSC modules UHVDC system.

Parameters	Value	Unit
Total base power (S_{base})	400	MVA
AC side rated voltage (Us)	100	kV
Individual VSC Reactor resistance(R)	0.075	Ω
Individual VSC Reactor inductance (L)	0.0024	H
Individual VSC DC capacitance (C)	70e-6	F
Individual VSC DC base voltage(U_{dcjref})	200	kV
Individual VSC switching frequency (f_c)	1440	Hz
VSC module base power (S_{jbase})	200	MVA
Total DC side base voltage (U_{dcref})	400	kV
DC-line resistance (R_l)	6.95e-3	Ω/km
DC-line inductance (L_l)	3.18e-4	H/km
DC-line capacitance (C_l)	2.3e-7	F/km
Length of DC line (l)	1000	km
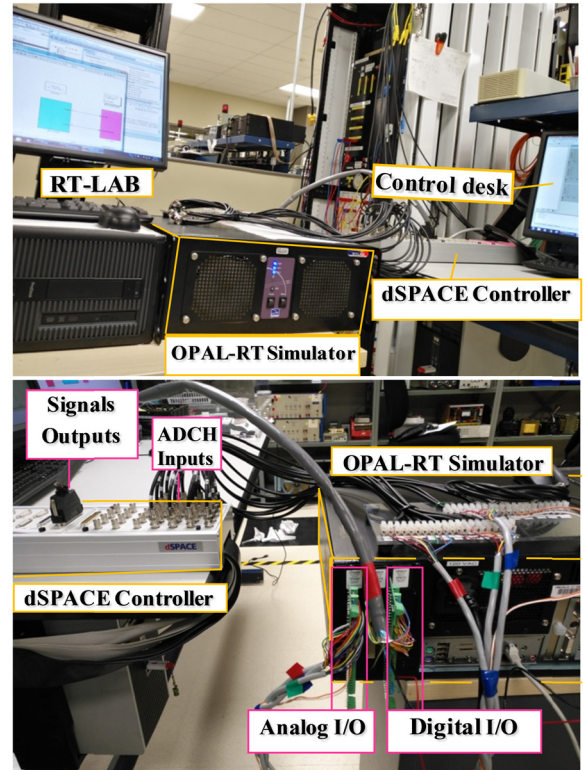
FIGURE 8. Photograph of front and back views of HIL-RT setup.

B. DC VOLTAGE REGULATION WITH DC VOLTAGE EQUALIZATION AT RECEIVING TERMINAL

Fig. 4 shows the DC voltage regulator with DC voltage equalization block for VSC modules at receiving terminal. In the conventional decoupled DC voltage and reactive power controller, i_{djref} is sent to command the jth VSC to keep DC voltage constant so that the error Δe_{dcj} is nulled. Similarly, with DC voltage equalization, a corrective signal Δi_{dj-1} is added to the original current reference i_{djref} so that a new current command is i^*_{djref}. The size of the corrective signal

Δi_{dj-1} is based on the error Δe^*_{dcj-1} being nulled by the negative feedback, which is shown in detail at compensation DC voltage equalizer block of Fig. 4.

The DC voltage across the jth VSC at the receiving terminal is measured as $U_{dcjmeas-1}$. The measurements of each individual DC voltages are summed up as:

$$V_{tot-1} = \sum_{j=1}^{N} U_{dcjmeas-1} \qquad (10)$$

Note that here the voltage compensation reference for each VSC is V_{tot-1}/N, which is different from that of sending terminal control.

IV. REDUCTION OF SWITCHING LOSSES

A. PHASE-SHIFTED TRIANGLE CARRIER-BASED SPWM

To eliminate AC current harmonics and reduce converter switching losses, the corresponding phase-shifted triangle carrier technique is adopted [21]–[23]. In this case, as illustrated in Fig. 5(a), when N number of VSC modules form a complete UHVDC station, each VSC receives successively its carrier with a phase-shifted (PS) angle of $\theta_{sh} = 2\pi/N$ ($N \geq 2$).

When four VSC modules are connected in series their carriers C_1, C_2, C_3 and C_4, as illustrated in Fig. 5(b), are phase-shifted by an angle $\theta_{sh} = 2\pi/4$, respectively. Similarly, when two VSC modules are connected in series, the phase-shifted angle of the carriers is $\theta_{sh} = 2\pi/2$, as illustrated in Fig. 5(c). In conventional SPWM implementation, the effective carrier frequency becomes $F_c = Nf_c$ when each of the N VSC module uses a carrier frequency of f_c. The switching losses are proportional to f_c of each VSC module, switching losses are reduced by increasing N because of $f_c = F_c/N$.

B. HARMONICS AND TOTAL HARMONIC DISTORTION

SPWM technique with carrier frequency $f_c = 24*60 = 1440$ Hz is applied to the simulation cases of Figure 2, developed in MATLAB/Simulink. When four VSC modules connected in series, the AC current harmonic spectrum of fast Fourier transform (FFT) analysis is shown in Fig. 6(a). The 22nd, 26th harmonics correspond to the sidebands for a frequency modulation ratio of 24 (that is, harmonic order 24*1 ± 2). Their magnitudes are given as % of the fundamental. The THD of AC current is 3.91%. Better waveforms are obtainable by increasing the carrier frequency. By using phase-shifted triangle carrier SPWM, as illustrated in Fig. 5(b), it has become apparent that the equivalent carrier frequency is four times of the original one, that is $4*f_c = 5760$ Hz. Fig. 6(b) shows the AC current of the four VSC modules connected in series and its harmonic spectrum. The 22nd and 26th harmonics shown in Fig. 6(a) are eliminated in this spectrum and the THD of AC current is reduced to 0.29%. While the switching losses remain the same as the case of $f_c = 1440$ Hz.

Similarly, when two VSC modules are connected in series, the AC current harmonic spectrum of FFT analysis with regular SPWM is shown in Fig. 6(c). The THD of AC current is 3.93%. While using phase-shifted triangle carrier SPWM, as illustrated in Fig. 5(c), the equivalent carrier frequency is twice of the original one, that is, $2*f_c = 2880$ Hz. Fig. 6(d) shows the AC current of the two VSC modules connected in series and its harmonic spectrum. As we can see that the 22nd and 26th harmonics of Fig. 6(c) are eliminated in this spectrum and the THD of AC current is reduced to 2.76%
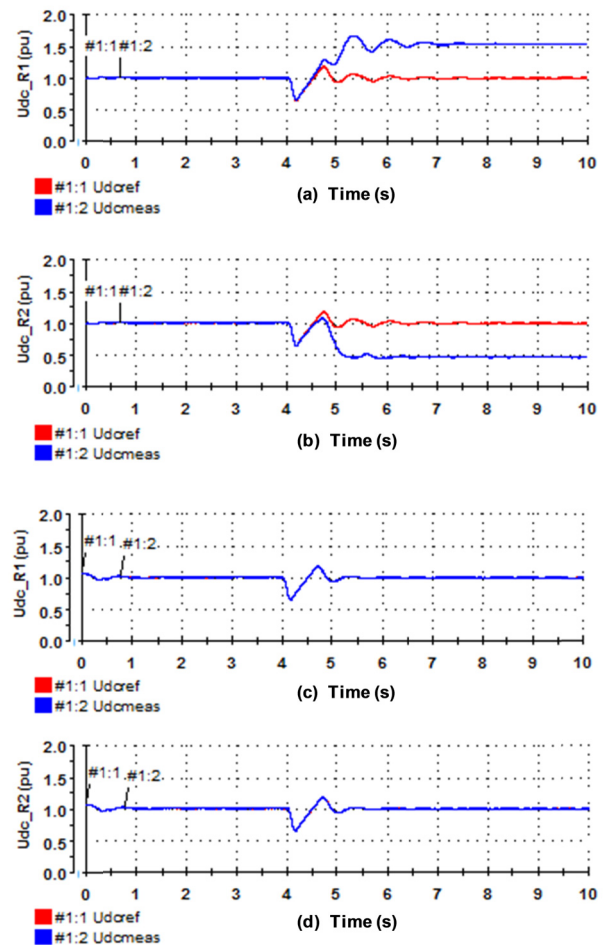

FIGURE 9. DC voltages of each VSC module at sending terminal, (a) without DC voltage compensation equalizer control for VSC1; (b) without DC voltage compensation equalizer control for VSC2; (c) with DC voltage compensation equalizer control for VSC1; (d) with DC voltage compensation equalizer control for VSC2.

and the switching losses remain the same as the case of $f_c = 1440$ Hz as well.

From Fig. 6, it can be known that with the phase-shifted carrier SPWM technique the quality of AC currents becomes better than that with the regular SPWM technique. Besides, compared to Fig. 6(b) and Fig. 6(d), it is worthy noticing that with the phase-shifted carrier SPWM technique the more connected VSC modules in series, the better power quality is reached.

V. HIL TEST VALIDATION

To further verify the effectiveness of the series-connected VSC modules modeling approach and test the control system of the proposed UHVDC system, a HIL-RTS test platform is set up by connecting the real-time Opal-RT simulator/Target to an external dSPACE 1103 controller. The overall series-connected VSC modules UHVDC with the transmission line model is created under the RT-LAB environment. This overall plant simulation model is then compiled into
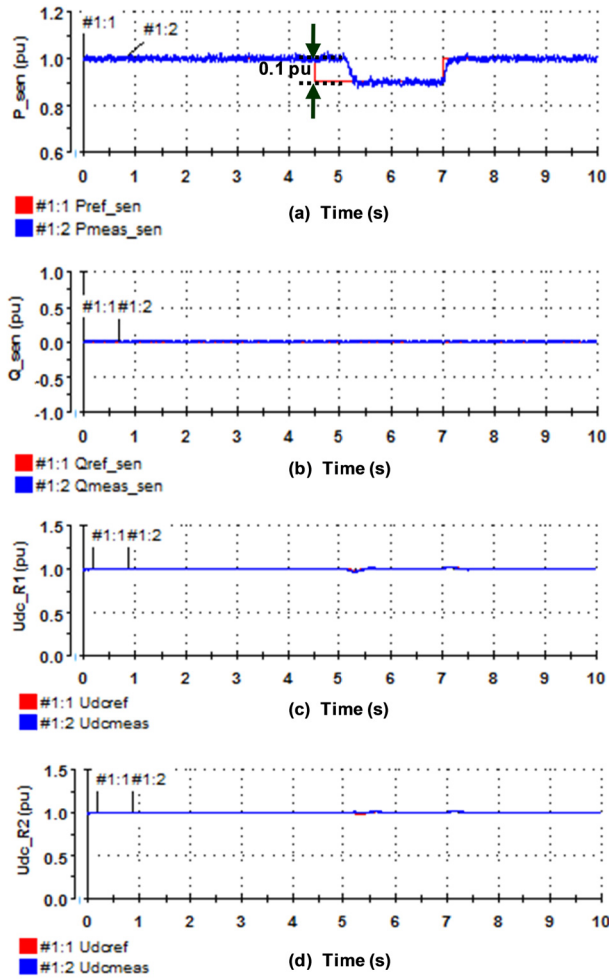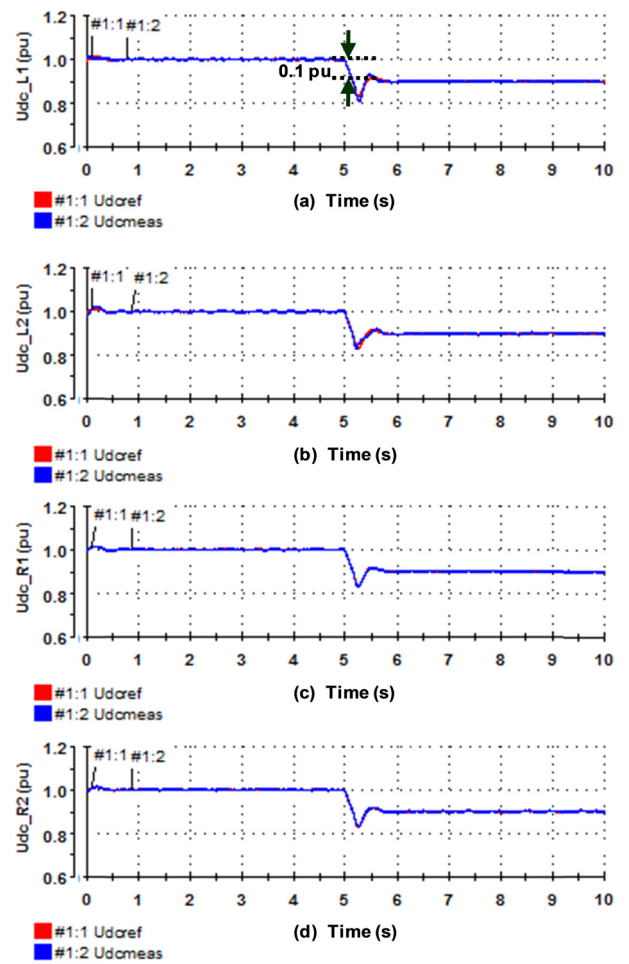
FIGURE 10. Active power, reactive power and DC voltage responses at sending terminal (a) active power response; (b) reactive power response; (c) DC voltage response at sending terminals of VSC1; (d) DC voltage response at sending terminals of VSC2.
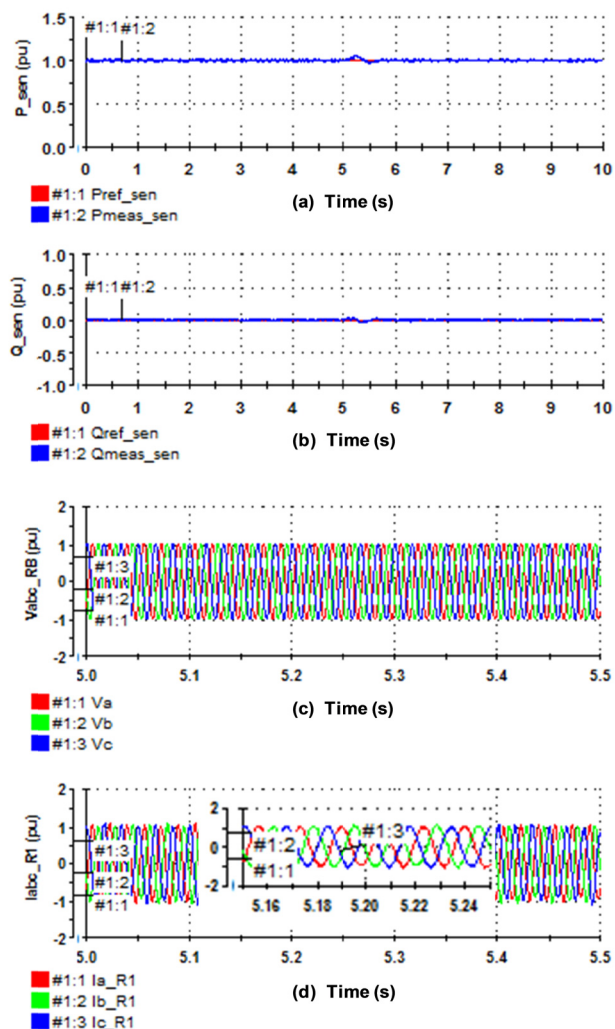

FIGURE 11. DC voltage responses at both terminals (a) DC voltage responses at receiving terminal of VSC1; (b) DC voltage responses at receiving terminal of VSC2; (c) DC voltage responses at sending terminals of VSC1; (d) DC voltage responses at sending terminals of VSC2.

real-time executable codes which are downloaded to the real-time simulator. By the analogue and digital inputs and outputs (I/Os), the simulator is connected to the prototyping controller dSPACE 1103, and the real-time simulator is used as a plant where the dSPACE 1103 is used as an external controller as shown in Fig. 7.

A unique technology, RT-Events (RTE), is used in the RT-LAB simulation platform to avoid the one time-step delay [31]. Moreover, the corresponding time-stamped bridge (STB) block is used as the VSC module in this HIL study. It is noted that all digital signals received from dSPACE controller should be converted into RTE signals to trigger the gates of all the IGBT devices with smaller time step for more accurate results [32]. Combined with the actual simulator performance and VSC modules based UHVDC system model, the real-time simulation time step (Ts) is set $48\mu s$.

Considered the limitation of 16 analog/digital channels in supported driving ports of the OPAL-RT simulator, only two VSC modules connected in series was implemented as

UHVDC station in this HIL test. All the parameters of the HIL-RTS test are shown in Table 1. A photograph of the HIL-RTS test platform is shown in Fig. 8. Different HIL-RTS tests were implemented in the next subsections.

A. DC VOLTAGES EQUALIZATION HIL TEST
At the sending terminal, when the reference value of active power changes from $+1$ pu to -1 pu at $t = 4$ s, the performance of the DC voltage at sending terminals is shown in Fig. 9(a) and Fig. 9(b). It can be noticed that the VSC modules do not have self-DC voltage equalization mechanism. In other words, the DC voltages are unequal and uncontrollable without the DC voltage equalization control. Whereas, the DC voltages shared equally with the DC voltage equalization control, as seen in Fig. 9(c) and Fig. 9(d).

The obtained results of the HIL test showed successful DC voltage equalization at both terminals are reached with DC voltage equalization control strategy, as shown in Fig. 3 and Fig. 4.
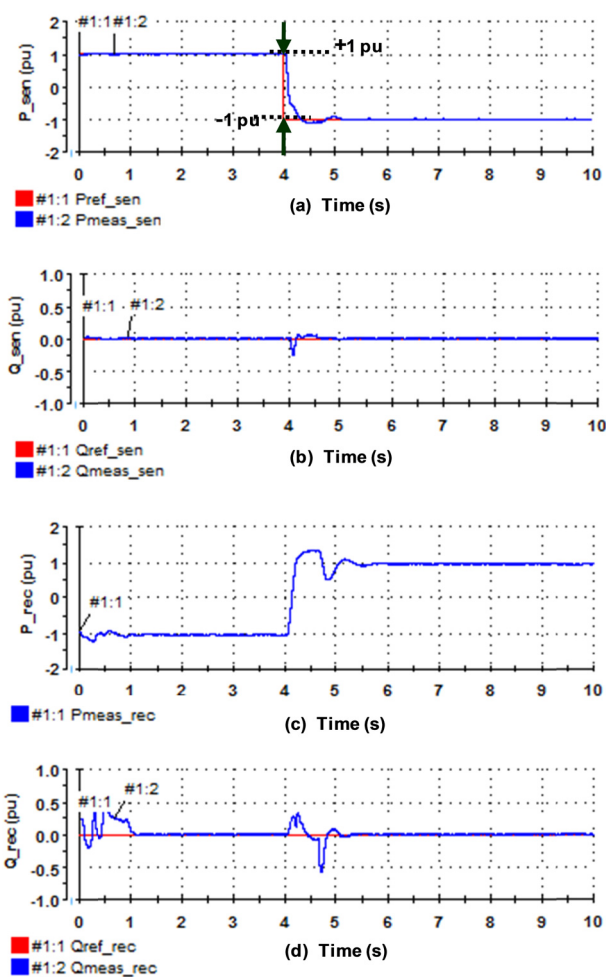
FIGURE 12. Active power, reactive power, AC voltage and AC current responses at sending terminal (a) active power; (b) reactive power; (c) AC voltages, (d) AC currents of VSC1.

FIGURE 13. Active power, reactive power responses of power reversal: (a) active power at sending terminal; (b) reactive power at sending terminal; (c) active power at receiving terminal; (d) reactive power at receiving terminal.

In this case, two VSC modules are connected in series at each terminal. The reference of $0.5V_{tot-2}$ is compared with DC voltages across each VSC module and regarded as the reference of each DC voltage. It should be specially mentioned that V_{tot-2} is the sum of two individual DC voltages at the sending terminal.

The red lines are marked as the reference signals, the blue lines are marked as the measured signals, and the color legends are used in the same way in the following figures of the active power, reactive power and the DC voltages.

B. HIL TEST OF POWER STEP CHANGE

As Fig. 10(a) shows that the active power reference has −0.1 pu power sag that lasts 2.5 s while the reactive power reference keeps 0 pu. From Fig. 10(a) and Fig. 10(b), it can be seen that the active power has a good dynamic performance when the power sag occurs and the reactive power is not affected by the active power sag perturbation.

This HIL test results verified that the active power and reactive power both have good tracking performances and they can be controlled independently.
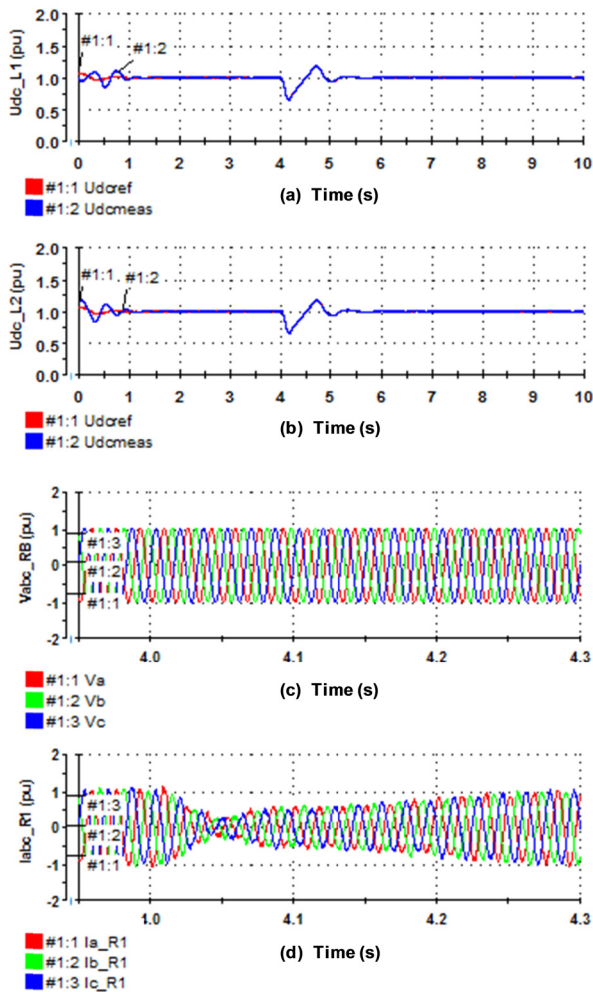
From Fig. 10(c) and Fig. 10(d), it can be seen that all the DC voltages at the same terminal follow their references and keep stable when power sag occurs.

C. HIL TEST OF DC VOLTAGE STEP CHANGE

Fig. 11 shows all the DC voltages responses when the reference of DC voltage has a 0.1 pu step change at the receiving terminal, which VSC modules are to regulate their DC voltages across their DC terminals thereby ensuring active power balance.

All DC voltages at both terminals are shown in Fig. 11. From these results, it can be seen that all the measured DC voltages follow their reference signals and share equally the Vdc. Fig. 12(a) and Fig. 12(b) show the active and reactive power control at sending terminal. It can be easily known that the power control keeps stable when the DC voltage
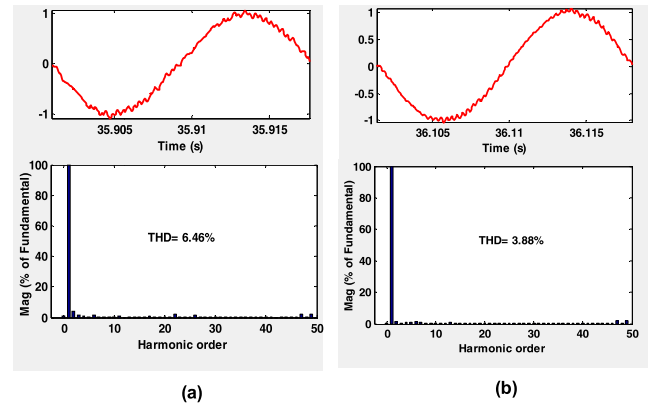
FIGURE 14. DC voltage, AC voltage and AC current responses of power reversal (a) DC voltage response of VSC1 at receiving terminal; (b) DC voltage response of VSC2 at receiving terminal; (c) AC voltage responses at sending terminal; (d) AC current responses of VSC1 at sending terminal.

FIGURE 15. AC current and its harmonic spectrum (a) with regular SPWM; (b) with phase-shifted SPWM.

HIL test verified the proposed UHVDC system has very good bidirectional power delivery capability.

When Fig. 13(a) power reversal occurs, Fig. 14(a) and Fig. 14(b) show the DC voltage responses at receiving terminal using DC voltage equalization control blocks. As it can be seen that the DC voltages keep constant except for one second slight fluctuations at the power reversal instant.

Additionally, successful DC voltage equalizations on sending terminal have already been demonstrated in Fig. 9(c) and Fig. 9(d).

Fig. 14(c) and Fig. 14(d) show the AC voltage and AC current responses at the moment of the power reversal occurring. Based on all above test cases, the results show that the proposed control strategy has good performance under both steady-state and transient-state HIL tests.

E. HIL TEST FOR LINE CURRENT SIGNATURE

Fig. 15 shows the line current and its harmonic spectrum. The THD of AC current comparison between using regular SPWM and phase-shifted SPWM is studied in this HIL test. Using the regular SPWM technique, the current waveform of the carrier frequency $f_c = 1440$ Hz and its harmonic spectrum of FFT analysis are shown in Fig. 15(a). The THD of AC current is 6.46%. Using phase-shifted triangle carrier technique mentioned before, the THD of AC current is reduced to 3.88%, as depicted in Fig. 15(b). The equivalent carrier frequency is twice of the original one, that is, $2*f_c = 2880$ Hz, while the switching losses remain unchanged as for $f_c = 1440$ Hz.

VI. CONCLUSION

This paper presents a detailed control strategy with DC voltage equalization for series-connected VSC models UHVDC system. Moreover, different simulation cases were studied in MATLAB/Simulink, which demonstrated that the series-connected VSC topology with phase-shifted triangle carrier SPWM technique is very efficient to attenuate AC current harmonics and reduce converter switching losses. The real time dynamic performance of the series-connected VSC

has 0.1 pu step change. Moreover, the AC voltages and AC currents, shown in Fig. 12(c) and Fig. 12(d), keep good waveforms as well at the moment of DC voltage step change.

D. HIL TEST OF POWER REVERSAL

The HIL response of the system to power reversal command where active and reactive powers, DC voltages, AC voltages and AC currents at sending terminal are depicted. As Fig. 13(a) shown, the active power reference P_{ref_sen} is ramping from $+1$ pu to -1 pu with the step change. The measured active power P_{meas_sen} tracks its reference quickly, which demonstrates a good dynamic performance of active power. In Fig. 13(c), it can be seen that the receiving active power, P_{meas_rec}, changes according to the change of the sending active power P_{meas_sen}.

At both terminals, the measured reactive powers Q_{meas_sen} and Q_{meas_rec} track their reference signals Q_{ref_sen} and Q_{ref_rec}, shown in Fig. 13(b) and Fig. 13(d), respectively. This

modules based UHVDC system was validated on this HIL test platform under both transient and steady state mode. The results showed that full DC voltages equalization, independent control of active and reactive power, and bidirectional power delivery capability were efficiently performed. The proposed series-connected VSC modules UHVDC topology inherits some merits of the conventional VSC-HVDC system and it provides one of the alternative and feasible solutions for UHVDC power transmission systems.

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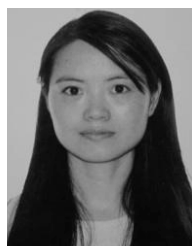
XIAOFAN FU (M'16) received the B.Eng. degree in electrical engineering from the Taiyuan University of Technology, Taiyuan, China, in 2003, and the M.Eng. degree in electrical engineering from Guizhou University, Guiyang, China, in 2006, the Ph.D. degree in electrical engineering from Southeast University, Nanjing, China, in 2009, and the Ph.D. degree in electrical engineering from the École de Technologie Supérieure (ÉTS), Université du Québec, Montréal, Canada, in 2016, where she has been a Postdoctoral Researcher with the GREPCI Laboratory, since 2017. Her research interests include voltage-source converter family of HVDC, multi-terminal VSC-HVDC, grid integration of renewable energy, and microgrid technology.

ALIREZA JAVADI (S'09–M'16) received the B.Sc. degree in power electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2007, the M.Sc.A. degree in electrical engineering from the École Polytechnique de Montréal, Montréal, QC, Canada, in 2009, and the Ph.D. degree in electrical engineering from the École de Technologie Supérieure (ÉTS), Montreal, in 2016.

He is currently an R&D Designer with Suez Water Technologies and Solutions. His research interests include encompass power electronics converters, harmonics and reactive power control using hybrid active filters, power quality of smart grids, renewable energy, fast electric vehicle charging stations, real-time power hardware-in-the-loop applications, and rapid control prototyping.

Dr. Javadi was an Active Member of the IEEE Montreal Section and a former President of the IEEE-ETS.

KAMAL AL-HADDAD (S'82–M'88–SM'92–F'07) received the B.Sc.A. and M.Sc.A. degrees in electrical engineering from the University of Québec à Trois-Rivières, Canada, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from the Institute National Polytechnique, Toulouse, France, in 1988.

Since 1990, he has been a Professor with the Electrical Engineering Department, École de Technologie Supérieure (ÉTS), Montreal, QC, Canada, where he has been the Canada Research Chair in electric energy conversion and power electronics, since 2002. He has supervised more than 170 Ph.D. and M.Sc.A. students in power electronics. He is also a Consultant and has established very solid link with Canadian industries. He has coauthored more than 600 transactions and conference papers and two books. His research interests include high-efficient static power converters, active-hybrid power filters, grid connect, and multilevel converters, including modeling, control, and development of prototypes for various industrial applications.

Prof. Al-Haddad is a member of the Academy of Science, a Fellow of the Royal Society of Canada, and a Fellow Member of the Canadian Academy of Engineering. He was a recipient of the Dr.-Ing. Eugene Mittelmann Achievement Award. He was the IEEE IES President, from 2016 to 2017. He is an IES Distinguished Lecturer and the recipient of the Dr.-Ing. Eugene Mittelmann Achievement Award.

LOUIS-A. DESSAINT (M'88–SM'91–F'13) received the B.Ing., M.Sc.A., and Ph.D. degrees from the École Polytechnique de Montréal, Universite du Quebec, Montréal, QC, Canada, in 1978, 1980, and 1985, respectively, all in electrical engineering.

He is currently a Professor with the École de Technologie Supérieure, Université du Québec, Montréal. He is the author of The MathWorks "SimPowerSystems" (SPS) Blockset.

Prof. Dessaint is a Fellow of the Canadian Academy of Engineering and a member of the Centre d'Excellence de l'Universite du Quebec. He was an Associate Editor of the IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY and *IET Generation, Transmission and Distribution*.

WEI LI (M'06) received the B.Eng. degree from Zhejiang University, China, the M.Eng. degree from the National University of Singapore, and the Ph.D. degree from McGill University, Canada.

He is currently a Senior Power System Simulation Specialist with Opal-RT Technologies, Montréal. His current research interests include power electronics, renewable energy, distributed generation, real-time simulation and controls of modular multilevel converter HVDC systems, and FACTS devices.

BOON-TECK OOI (S'69–M'71–SM'85–F'02–LF'05) received the B.Eng. degree (Hons.) from the University of Adelaide, the S.M. degree from the Massachusetts Institute of Technology, and the Ph.D. from McGill University.

He is currently an Emeritus Professor with the Department of Electrical and Computer Engineering, McGill University, Canada. He has been a Visiting Professor with the University of Malaya, the University of Adelaide, South Australia, and the Nanyang University of Technology, Singapore. His early research had been in linear induction motor, homopolar linear synchronous motor, magnetic levitation by superconducting magnet, sub-synchronous resonance instability, series, and shunt capacitor compensation of long transmission lines. His later research has been in power electronics, including unity power factor PWM rectifiers, the voltage-source converter family of HVDC, multi-terminal VSC-HVDC, controllers for flexible ac transmission systems, power quality and distributed generation, MMC, multi-terminal MMC HVDC, and dc–dc converter. In renewable energy technologies, his research has been in wind turbine generators, doubly fed induction motor (DFIG), impact of wind power on grid frequency, and islanded wind farms.

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