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mm-Wave Waveguide Traveling-Wave Power Combiner Design Using an Equivalent Circuit Model

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ABSTRACT The waveguide traveling-wave power combiner (WTWPC) falls into the category of asymmetrical non-isolated power combiners, and, therefore, the active load modulation occurring within the combiner was investigated. Proper manipulation of active load modulation gave rise to a two-step design method for the combiner. The first step formulated the specifications of the combiner in terms of active load impedance at its input ports, which determined the objective scattering parameters of the combiner, as well as the desired coherent excitation signals. The second step established a versatile equivalent circuit model to provide a mapping relation between the scattering parameters and the physical dimensions of the combiner. The proposed equivalent circuit method not only offered a close-to-reality description of the existing type of traveling-wave power combiners but also broke new ground for combiner variants that accommodate the more general driving amplifiers. A Q-band quasi-planar traveling-wave waveguide spatial combined amplifier was built to demonstrate the proposed method. The measured P_{-1dB} bandwidth of the prototype was 6 GHz (33–39 GHz).

INDEX TERMS Equivalent circuit, load modulation, traveling wave, mm-wave power amplifier, rectangular waveguide, waveguide probe, waveguide iris window.

I. INTRODUCTION

mm-Wave multi-Gbps wireless backhaul is targeted to be a key enabler of 5G roll-out [1]. Additionally, mm-Wave backhaul aiming for a high-speed train (HST) scenario was emphasized in 3GPP 5G New Radio (NR) [2], while conducting experimental research [3]–[5]. The technical challenge of its hardware manifests in three aspects [6]–[10]: the baseband modem, mm-Wave front-end, and high-gain antennas. To reach a rate of 10 Gb/s and beyond, the transmission of a truly wideband modulated signal (>2 GHz) poses a new challenge to the mm-Wave front-end in that the mm-Wave front-end-induced signal impairment must be restricted at a low level. Moreover, to maintain an above Gbps data stream over a spatial distance beyond 1 km (equivalent to a travel distance of 7.2 s for a train running at 500 km/h), the power amplifier (PA) plays a vital role in providing adequate signal-to-noise ratio (SNR) for an uninterrupted link. However, the desired output power of the PA may dramatically exceeds the capacity of a single solid-state device (GaAs or GaN MMIC). Therefore, wideband power-combining techniques have been considered to boost output power. Historically, Sanada *et al.* developed the waveguide traveling-wave power combiner (WTWPC) using E-plane probe coupling structures [11], while in a separate design, Mortazawi *et al.* used slotted-waveguide cross coupling structures [12], [13]. Subsequently, Becker *et al.* planarized the probe-type WTWPC to facilitate batch fabrication [14]. In addition, the probe-type WTWPC was improved using new transmission lines: ridged rectangular waveguide [15] and coaxial waveguide [16], respectively. Moreover, the volume of slot-type WTWPC is reduced in [17].

Overall, the benefits of the WTWPC include compact volume, low insertion loss, wide bandwidth, and the flexibility of a non-binary path number. However, owing to the inherent low inter-port isolation of this combiner, the multiple PAs

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attached to it interact through a coupled network, effectively load-pulling each other. The load impedance seen by each PA is not a constant value but a function of the excitation signal. This mechanism is known as load modulation. To eliminate the risk of unknown hazardous load modulation conditions occurring in the WTWPC and to guarantee all-condition stability, an isolated waveguide combiner based on magic-T [18] and a waveguide Gysel combiner [19] were developed to replace the WTWPC. However, these solutions significantly increase the combiner volume, while complicating the fabrication.

On the other hand, engineered load modulation is also evolving for applications of out-phasing amplifiers. An in-depth understanding of load modulation manipulation has been progressively obtained [21]–[26]. In brief, the objective is a load modulation controlling scheme wherein the usable impedance regions are reached whereas hazardous load impedance conditions are precluded. Proceeding from this understanding, several schemes applicable to dual-way or quad-way asymmetrical non-isolated combiners were successively obtained. Furthermore, an RF-input/RF-output outphasing PA, which enables drop-in replacement of a traditional PA, was recently realized in [26]. Intuitively, the underlying working principle of the RF-input outphasing amplifier is somewhat similar to that of a combined amplifier based on a WTWPC. However, its combiner arrangement and RF-domain signal component separator could not be directly applied to the WTWPC circumstance.

Moreover, the equivalent circuit of a WTWPC provides a useful tool for the analysis and synthesis of the combiner. Specifically, it reveals the quantitative relationship between the waveguide geometries and scattering parameters of the combiner. An incomplete circuit model provided by Sanada [11] has been used extensively. The fundamental unit cell of Sanada's model, known as reflectionless dividing units, is a two-port network. In contrast, this unit is intended to represent a three-port physical structure. The groundless reduction from a three-port network into a two-port network impedes the formulation of the working principle for the unit cell. Since the existing two-port model loses the information of the third port, it only provides an impaired baseline for the entire combiner design. The absence of a three-port network model can be attributed to the challenge in achieving quantitative representation by a circuit model for the coupling mechanism of a waveguide probe or waveguide broadwall slot. Similar problems are encountered regarding the establishment of an equivalent circuit in the case of a waveguide feeder for array antenna, and comparable studies are performed [27], [28].

This paper presents a systematic design procedure for a WTWPC from two perspectives:

1) A load modulation scheme is tailored for the WTWPC. The solution is expressed by a set of scattering parameters, as well as an excitation signal vector (ESV), is developed by extending the dual-way load modulation solution provided by Sengupta [24] to a nonbinary multi-way case.

2) An enhanced versatile equivalent circuit model for the WTWPC is proposed. To emphasize, a three-port circuit model instead of the two-port reflectionless dividing units, [11], [17] is established for the first time. The revised unit circuit is developed based on a shunt inductance impedance inverter presented by Levy [29], as well as a waveguide probe coupling model reported by Kishk [27]. Accordingly, the scattering parameters given in the load modulation scheme are converted to equivalent circuit parameters and are subsequently translated to physical dimensions. The physical dimension synthesis of the WTWPC is performed by a circuit-full-wave hybrid procedure similar to the one widely used for waveguide filters [29]. Once the coarse solution of the physical dimension is obtained, an electromagnetic (EM) simulator is only used for dimension refinement. Since substantial synthesis work is conducted on the circuit simulator instead of an EM simulator, the computational burden of EM simulation is greatly alleviated.

This paper is organized as follows. Section II presents the analytical expression for active load modulation within a non-isolated combiner; wherein the desired loading modulation solutions are derived as a set of combiner scattering parameters and a desired ESV. Section III presents the equivalent circuit extraction and physical dimension synthesis of a WTWPC. Section IV discusses the realization of ESV and associated nonideal factors for the of the active load impedances. Section V describes the fabrication of a Q-band WTWPC prototype and measurement results. Section VI concludes this paper.

II. ACTIVE LOAD IMPEDANCE AND ITS DEPENDENCE ON AN ESV

Fig. 1 shows a combined amplifier architecture, which enabled the interaction of multiple branch PAs through a non-isolated combiner. The combined amplifier was composed of a divider network, an array of uniform branch power amplifiers (UPAs), and a non-isolated multiway power combiner. Each UPA witness an active excitation-signal-dependent load impedance. This mechanism is known as load modulation.

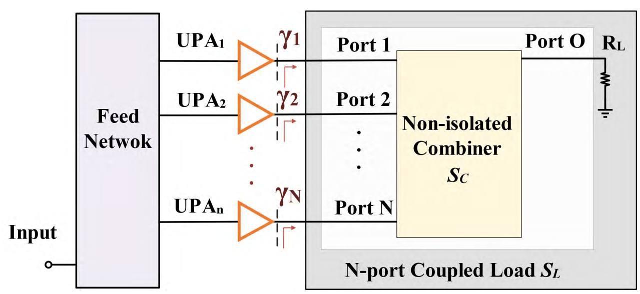

FIGURE 1. Schematic diagram of the active reflections on the non-isolated combiner.

Traditionally, the branch PAs is perceived as voltage sources with constant internal impedance (usually 50 ohm) and thereupon efficiency consists of two portions: the reflection loss at combiner input interface and power transfer factor inside the combiner. In contrast, recent studies in [20] and [21] indicated that the interaction between the branch PAs due to the non-isolated combiner are indeed more complicated when taking into account the nonlinear device model of the PA. The overall efficiency resulted from the power factor of the combiner and the apparent efficiency of the individual branch PAs.

In this paper, the investigation focused on an asymmetric multi-way power combining case since a WTWPC falls into the category of asymmetric non-isolated combiners. For quantitative analysis, an analytical equation describing these dynamics is provided in (1a) to (1d), wherein power waves represented the excitation signal and active reflection coefficients (ARCs) denoted the active load. To clarify, the input ports of the combiner were labeled with sequential numbers whereas its output port was labeled 'o'. Accordingly, the incident power waves were designated $a_j (j = 1, 2, \ldots, \mathrm{N})$, while the reflection coefficients were γ_j s. Additionally, a_js were collectively denoted by an ESV $\vec{a}$, while a diagonal matrix Γ denoted γ_j s. To satisfy the objective active load condition predetermined by the property of UPAs, Γ was usually confined within a circular zone, and the scattering matrix S_C represented the combiner. Moreover, the combiner, as well as its terminating load $\mathrm{R_L}$ were treated as a whole and was represented by a matrix S_L to simplify the equations. The relationship between S_C and S_L is given in (1d).

$$S_L \cdot \vec{a} = \Gamma \cdot \vec{a} \tag{1a}$$

$$\vec{a} = \begin{pmatrix} a_1 & a_2 & \cdots & a_N \end{pmatrix}^T \tag{1b}$$

$$\Gamma = \begin{bmatrix} \gamma_1 & & & \\ & \gamma_2 & & \\ & & \ddots & \\ & & & \gamma_\mathrm{N} \end{bmatrix} \tag{1c}$$

$$S_C = \left[\begin{array}{cccc|c} \multicolumn{4}{c}{\overbrace{\hphantom{s_{11}\quad s_{12}\quad \cdots \quad s_{1N}}}^{S_L}} & \\ s_{11} & s_{12} & \cdots & s_{1N} & s_{1o} \\ s_{21} & s_{22} & \cdots & s_{2N} & s_{2o} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ s_{N1} & s_{N2} & \cdots & s_{NN} & s_{No} \\ \hline s_{o1} & s_{o2} & \cdots & s_{oN} & s_{oo} \end{array}\right] \tag{1d}$$

To explain the restriction over $\vec{a}$ and S_L, equation (1a) was rearranged as a homogenous matrix equation in (2). Moreover, the equation had to be maintained over a wide, continuous frequency span.

$$(S_L - \Gamma) \cdot \vec{a} = 0 \tag{2}$$

Based on the solution space theory for homogenous matrix equations, the solution space for $\vec{a}$ and row space of $(S_L - \Gamma)$ were orthogonal complements. Additionally, the allowable magnitude imbalance among a_js, and the realizable value range of S_L both imposed restrictions on the realizable solution. Therefore, such a problem required a generic solution. The deduction started from the unitary matrix property of S_C expressed as $S_C \cdot S_C^H = I_{N+1}$ [30], arising from the lossless property of the combiner. Through a matrix element expansion of (3), a generic solution was discovered. A desired ESV (termed $\vec{a}_d$), in conjunction with its associated γ_j s values were derived and presented in (4) and (5), respectively. To explain, the phase delay factor Φ_D in (4) was introduced to accommodate a casual signal condition because the conjugate operation incurred a positive slope in the phase frequency curve. The proposed γ_j expressed in (5) consisted of a common factor γ_C and phase rotating factor ψ_j, which established a one-to-one relationship with s_{oo} and s_{oj}, respectively.

$$\left[\begin{array}{cccc|c} \multicolumn{4}{c}{\overbrace{\hphantom{s_{11}\quad s_{12}\quad \cdots \quad s_{1N}}}^{S_L}} & \\ s_{11} & s_{12} & \cdots & s_{1N} & s_{1o} \\ s_{21} & s_{22} & \cdots & s_{2N} & s_{2o} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ s_{N1} & s_{N2} & \cdots & s_{NN} & s_{No} \\ \hline s_{o1} & s_{o2} & \cdots & s_{oN} & s_{oo} \end{array}\right] \times \begin{bmatrix} s_{11}^* & s_{21}^* & \cdots & s_{N1}^* & s_{o1}^* \\ s_{12}^* & s_{22}^* & \cdots & s_{N2}^* & s_{o2}^* \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ s_{1N}^* & s_{2N}^* & \cdots & s_{NN}^* & s_{oN}^* \\ s_{1o}^* & s_{2o}^* & \cdots & s_{No}^* & s_{oo}^* \end{bmatrix} = \begin{bmatrix} 1 & & & & \\ & 1 & & & \\ & & \ddots & & \\ & & & 1 & \\ & & & & 1 \end{bmatrix} \tag{3}$$

$$\vec{a} = \Phi_D \cdot \begin{pmatrix} s_{o1}^* & s_{o2}^* & \cdots & s_{on}^* \end{pmatrix}^T \tag{4}$$

$$\gamma_j = \gamma_C \cdot \psi_j = \left(-s_{oo}^*\right) \cdot \exp\left[j * 2 \arg\left(s_{oj}\right)\right] \tag{5}$$

Turning to the specific case of the WTWPC, the S_C reference impedance at the input ports (denoted by R_0^j) were commonly assigned to a real value R_{MS} whereas its counterpart at the output (denoted as R_0^o) was assigned to another real value R_{WG} (The definition of R_{MS} and R_{WG} is further clarified in Fig. 4). Based on these port reference impedances, the active load impedance value was derived from (5), and given in (6).

$$Z_{IN}^j = R_0^j \cdot \left(1 + \gamma_j\right) / \left(1 - \gamma_j\right) \tag{6}$$

To provide an intuitive understanding of the above equations, Fig. 2 illustrates the value range of γ_j s on a Smith chart. In particular, the design space was divided into three regions according to the objective value of the active impedance. Type-I area aimed for 50-ohm real impedance, Type-II aimed for less than 50-ohm real impedance, and Type-III was intended for a complex impedance. The distinction of the three types stems from the requirement of UPAs. On the other hand, the realizability of these types should be examined for the general asymmetric multi-way case. As revealed in (5) and (6), the attainability of the γ-clusters relied on limiting conditions of s_{oo}, s_{oj} and R_0^j. The specific relationships are listed in Table 1.

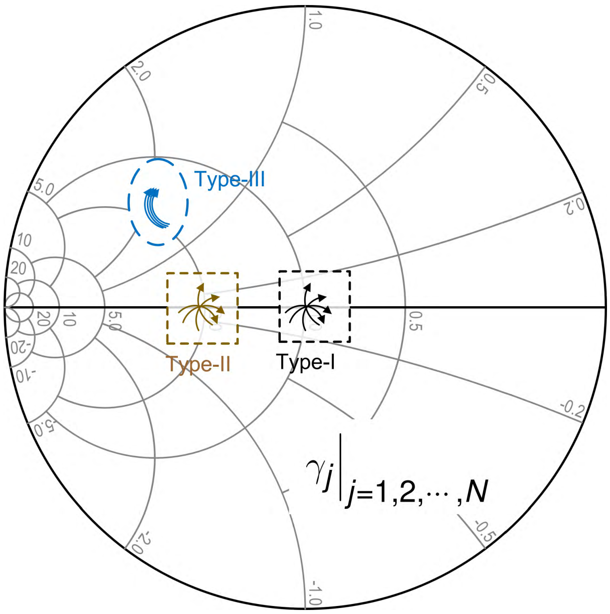

FIGURE 2. Three types of γ_j clusters. (Z_0 = 50 ohms).

TABLE 1. Types of γ-clusters, and their dependent conditions.

γ-cluster type	S_C requirement		R_0^j
	$arg(s_{oj})$	$\lvert s_{oo}\rvert$	
I	Unequal	≈0	50 ohm
II	Unequal	≈0	< 50 ohm
III	Equal	≠0	≤ 50 ohm

The analysis of the WTWPC via load modulation theory resulted in two observations. First, it revealed that the existing design of the WTWPC, which belonged to the type-I catalog, was recognized as one of three subtypes. Furthermore, type-II and type-III WTWPC provided additional design space, which enabled more flexibility for UPAs. Secondly, superimposing the load-pull contour of the UPAs on the Smith chart in Fig. 2, indicated that the phase rotation of γ_j s would induce an inconsistent frequency response from the UPAs. As stated in the theory of the Bode-Fano matching upper bound [31], [32], the magnitudes of γ_j s were inherently finite and, therefore, the discrepancy always existed in γ_j s and became more evident as the operational bandwidth expanded. Such a negative effect was essentially overlooked in previous studies. For experimental investigation and verification, a powerful dedicated measurement system capable of monitoring the active reflection at the UPA outputs might be considered. Although the frame structure of the measurement system was conceived under somewhat similar circumstances [23], the adaptation to a mm-Wave WTWPC still encountered arduous challenges.

Proceeding from the objective parameter of s_{oo} and s_{jo}, the physical dimension synthesis of the WTWPC was performed with the assistance of the circuit model described in section III.

III. EQUIVALENT CIRCUIT EXTRACTION AND PHYSICAL DIMENSION SYNTHESIS OF THE WTWPC

This study presented a new method for physical dimension synthesis and applied it in the wideband design of the WTWPC. The proposed method exploited versatile prototype equivalent circuits as intermediary agents between adjustable waveguide element geometries and combiner scattering parameter specifications. Fig. 3 shows physical structure of the four-way WTWPC employed to delineate the proposed method. Fig. 4 shows the equivalent circuit model of the WTWPC in Fig. 3.

As demonstrated in Fig. 4a, the multi-way combiner consisted of cascaded stages using T-junction combiners, which usually adopts a homologous structure. The schematic diagrams of constituent blocks, namely NWG, NWP, and NWM, were separately presented in Fig. 4b, Fig. 4c, and Fig. 4d. The establishment of the equivalent circuit model for the T-junction combiner was divided into two steps. First, its constitutive elements, namely NWG, NWP, and NWM, were described separately. Then followed an in-depth discussion regarding the coordination among these blocks, which was crucial for the joined T-junction combiner.

A. EQUIVALENT CIRCUIT PARAMETER EXTRACTION

With the multi-way circuit model (Fig. 4a) in mind, the details of constituent blocks were separately presented in Fig. 4b, Fig. 4c, and Fig. 4d. The lumped and transmission line components in these blocks allowed for the construction of a flexible framework, which accurately represented the frequency response of waveguide components involved in the fabrication of the WTWPC.

For the quantitative investigation, the relation curves providing the parameter values of the prototype circuit versus the physical dimensions of the WTWPC were extracted for subsequent utilization as the design space for the WTWPC. The quantitative relations were presented in the form of design curves in Fig. 5 and Fig. 6, respectively.

The process for retrieving these relation curves was denoted as the parameter extraction (PE) step. Specifically, the circuit NWG represented the H-plane waveguide iris window (Fig. 3), and its working mechanism of impedance transformation was identical to the shunt inductance impedance inverter developed by Levy. Therefore, its PE process was conducted according to the guidance in [29]. Fig. 7 illustrates a comparison between a typical reflection coefficient obtained from the EM simulation of the iris (ANSYS HFSS) and that from the circuit model. The residual error between the EM-simulated and the circuit-based reflection coefficient ranged between −32 dB to −35dB.

Moreover, the circuit NWP represented the E-plane waveguide probe (Fig. 3). Its PE process was performed according to the method reported by Kishk [27]. Fig. 8 illustrates a comparison between a typical reflection coefficient obtained from the EM simulation of the probe and that from the

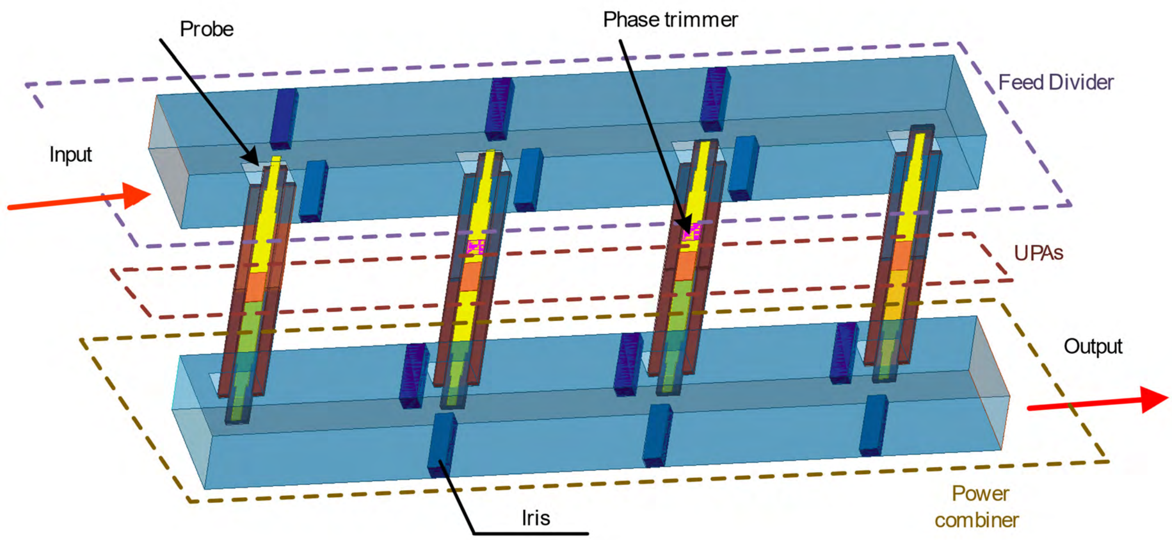

FIGURE 3. **Isometric view of traveling wave spatial power combined amplifier.**

circuit model. The residual error between the two approaches ranged between −29 dB to −33 dB. The impedance transformation mechanism of NWP was almost self-explanatory.

B. SEMI-ANALYTICAL METHOD FOR 3-ELEMENT COMPLEX IMPEDANCE-TRANSFORMING

As demonstrated in Fig. 9, circuit NWG, NWP, and NWM jointly constructed a basic T-junction power combiner displaying an uneven combining ratio. This combiner resembles a resistor-free Wilkinson combiner. The realizations of both combiner types confront a common challenge in that their impedance transformer networks (ITN) aimed for two difficult-to-reconcile goals. First, the operational bandwidth of the ITN was expected to be broader than that of the classical 1/4 λ transmission line. Second, a restriction was imposed on the ITN topology complexity, and its component count due to the non-negligible ohmic loss [33], which manifested more prominently in the mm-Wave band. Moreover, the impedance transformation depended on the input impedance of the combiner. Given that the combiner was connected to external sources and load, which usually exhibited complex input impedance, the ITNs may need additonal readjustment to accommodate these conditions. As examples, several improved solutions for Wilkinson combiner have been developed to address these concerns [34]–[37].

The coordination of NWG, NWP, and NWM were quantified in terms of the normalized admittance of the characteristic impedance of rectangular waveguide (e.g., WR-22 waveguide), which were represented by the equation set in (7) and (8). Notably, the frequency variable was implicitly hidden in the equation set.

$$y_i^P + y_i^G = y_i^{SUM} \tag{7}$$

$$\left|y_i^P\right| \Big/ \left|y_i^G\right| = \chi_i = 1/i \tag{8}$$

A satisfactory solution for the equation set is presented on the Smith chart in Fig. 10. This solution relied on a set of well-chosen parameter values for NWG, NWP, and NWM. The underlying logical relations between the admittances (y_i^G and y_i^P) and the circuit parameter values (C_A, C_P and others) amounted to three points. First, capacitor C_A was minimized to a negligible scale ($< 10^{-5}$ pF) to simplify the wideband impedance transformation of NWP. Second, the transformer turn ratio TF_P and capacitor C_P were highly correlated. C_P was intentionally adjusted to a sufficient magnitude; thereupon the y_i^P trajectories departed from the real axis and moved downward into the capacitive region. Third, the image portion of y_i^G and y_i^P were intended to neutralize each other across the entire bandwidth. This wideband neutralization depended on the additional design freedom offered by circuit NWM, which was represented by Z_i^M (Fig. 9). In the absence of circuit NWM, the inconsistent frequency response of NWG and NWP was irreconcilable.

In general, the complex impedance transformation conformed to the guidance of the classical reactive matching technique [38], which anticipated the patterned trajectories on the Smith chart. The standalone T-junction combiner stage was developed with a fast circuit simulation instead of a purely numerical EM simulation.

C. PHYSICAL DIMENSION DETERMINATION

Following determination of the parameter value set for the equivalent circuit, the acquired parameter mapping curves provided the physical dimensions (Fig. 5 and Fig. 6). Fig. 7 and Fig. 8 provide the residual error of the circuit model used to justify these excellent initial dimensions. Furthermore, while cascading the detached stages to build the WTWPC, the residual error of the circuit model accumulated. Eventually, the physical dimensions of the

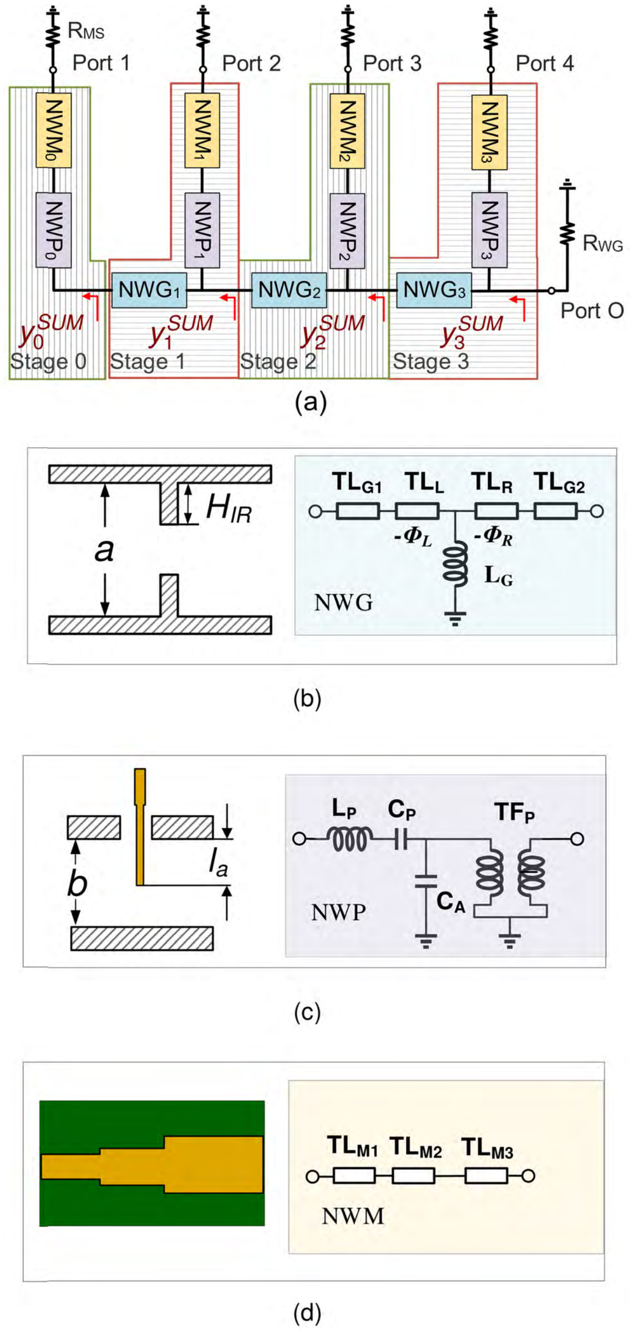

FIGURE 4. (a) Schematic of a WTWPC, (b) Waveguide iris window dimension annotation and its equivalent circuit NWG. (c) Probe dimension annotation and its equivalent circuit NWP (d) Stepped microstrip and its equivalent circuit NWM.

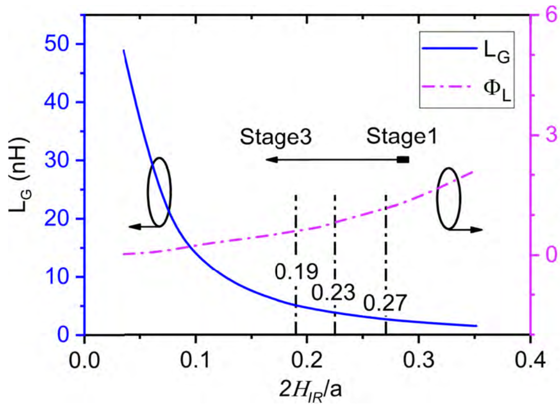

FIGURE 5. NWG circuit parameter values versus normalized iris depth.

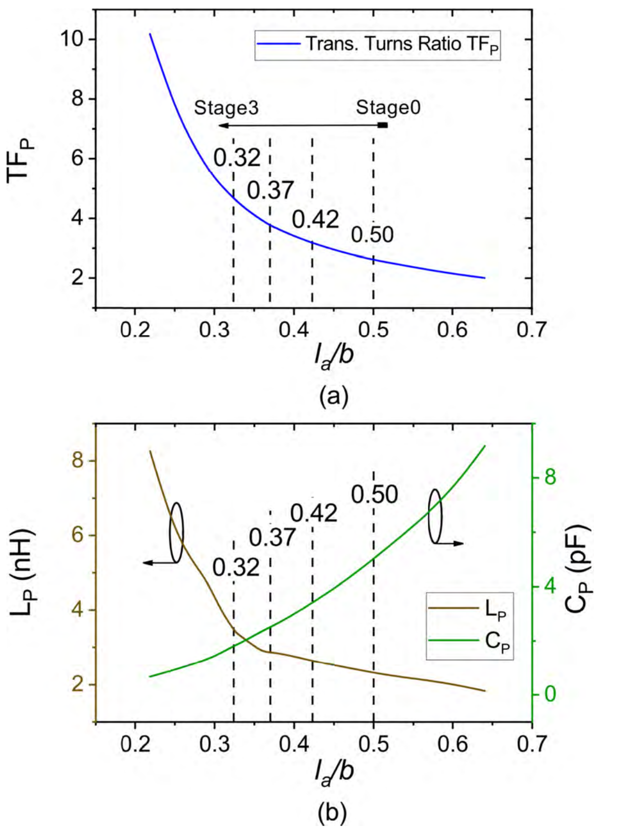

FIGURE 6. NWP circuit parameter values versus normalized probe length.

WTWPC were refined using EM simulation (HFSS). During this step, the refinement only focused on s_{OO}. Fig. 11 presents the ultimate s_{OO}, namely the reflection at port O of the entire combiner while Fig. 12 presents the transmission coefficients s_{Oj} s.

In brief, a versatile prototype equivalent circuit of the WTWPC was established for the first time, which streamlined the physical dimension synthesis of the WTWPC.

IV. REALIZED ESV AND ACTIVE LOAD IMPEDANCE

The implementation of the ESV started from the load modulation solution, in which an ideal ESV $\vec{a}$ is given in (4). The scattering matrix S_C obtained in the previous section is entered into (4). Additionally, the Φ_D value in (4) is provided in (9).

$$\Phi_D = \exp\left\{-j \cdot [phase\,(s_{O1}) + phase\,(s_{O4})]\right\} \tag{9}$$

A simpler serial feeding network, which satisfied the need for concept proof, was utilized to realize the ESV. Admittedly, a more complex reconfigurable feed network similar to one

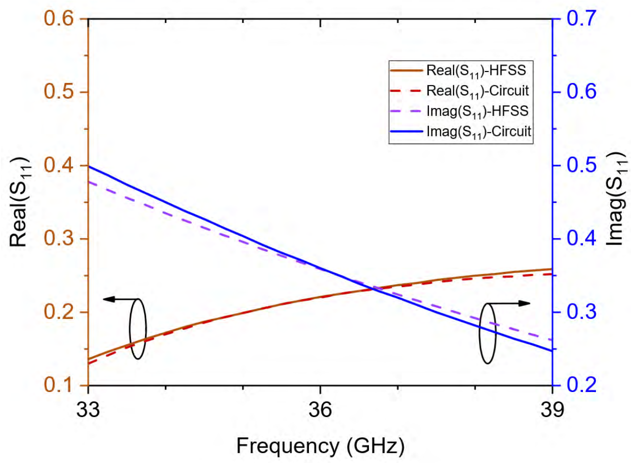

FIGURE 7. Reflection coefficient S_{11} for NWG_1 parameter value extraction ($H_{IR}/a = 0.27$).

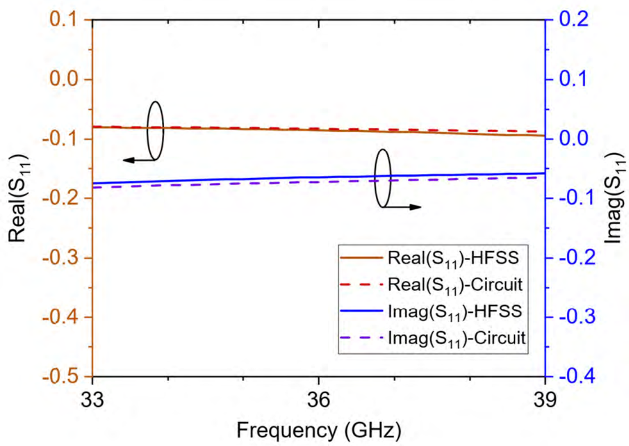

FIGURE 8. Reflection coefficient S_{11} for NWP_1 parameter value extraction ($l_a/b = 0.50$).

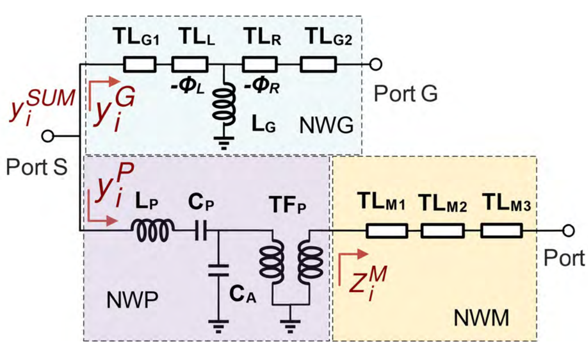

FIGURE 9. Schematic of a general T-junction combiner stage.

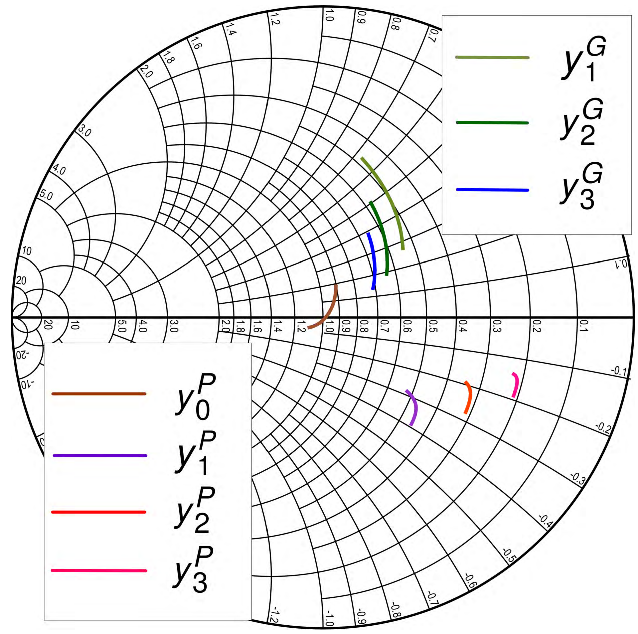

FIGURE 10. The normalized input admittance of the NWG branch, and the NWP branch on a Smith chart.

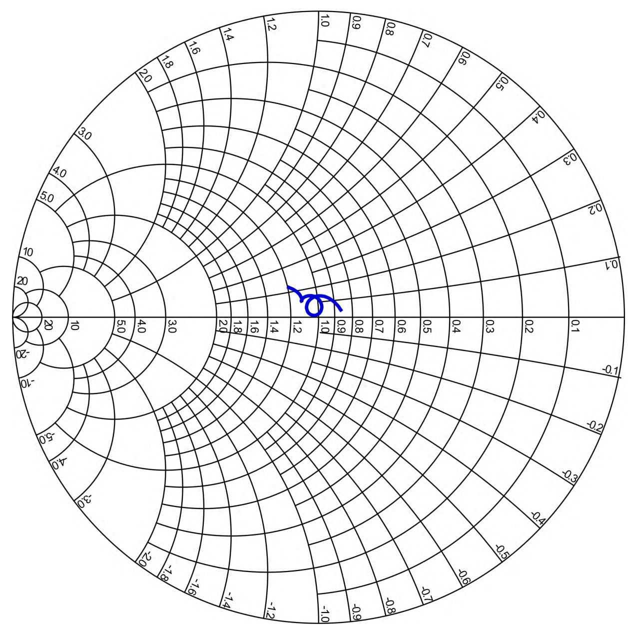

FIGURE 11. Simulated reflection coefficient at port O of the WTWPC (s_{OO}).

presented by Sengupta, provided more flexibility for ESV generation. However, this caused higher hardware complexity, therefore, deserving further study.

The overall ESV generation network was illustrated at the upper side of Fig. 3. The excitation signal entered the input port of the feed network where it connected to the UPAs via the cascaded T-junction dividers. An often-overlooked point is that the ESV realized by a serial feeding network inherently deviates from the ideal ESV. This disturbing problem was discussed, and a countermeasure was provided in [14]. Since the impact of the realized ESV phase deviation exceeded that of the magnitude deviation, only the effect of phase deviation was qualitatively analyzed. Considering the symmetry between the series feed divider and the combiner, the number of s_{oj} s phase deviation terms could be reduced to a roundup (N/2-1). In the case of 4-way power combining, only one

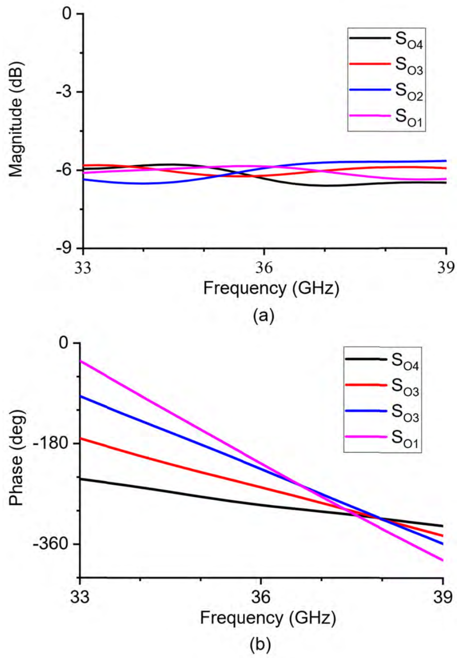

FIGURE 12. (a) Simulated transmission coefficient magnitude of the combiner. (b) Simulated transmission coefficient phase of the combiner.

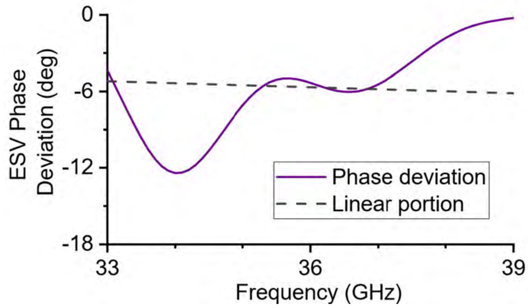

FIGURE 13. Simulated phase deviation between the realized ESV and the ideal ESV.

phase deviation term was evaluated. In line with the countermeasure in [14], the implementation of compensational phase trimmers ensured the reduction of the phase deviation and minimization of its linear portion, both of which are illustrated in Fig. 13. The implantation of the resulting meander microstrip trimmers before UPA_2 and UPA_3 is shown in Fig. 2.

Finally, Fig. 14 presents a comparison between the ARCs under the ideal ESV and under the realized ESV. In particular, the ARCs under the ideal ESV demonstrated the consistency due to γ_C and ψ_j s, while the ARCs under the realized ESV displayed slight distortions. The uneven distortions were more adverse at the side of port 1 than at the port 4 side.

Ultimately, the consequent performance of power combing under the conditions of realized ARCs would be

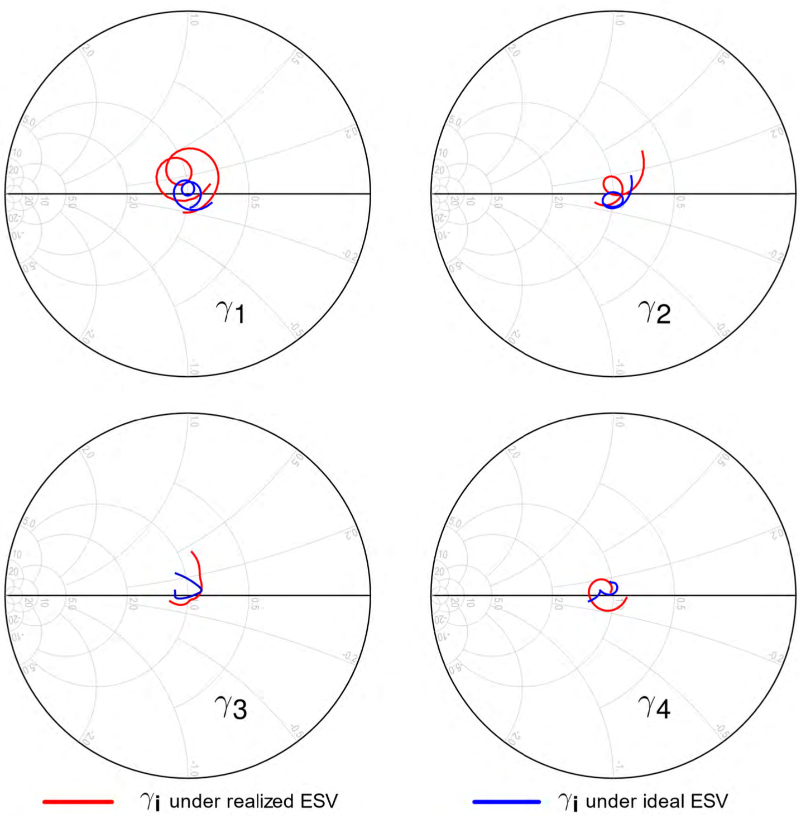

FIGURE 14. Simulated ARCs under excitation of realized ESV and ideal ESV.

TABLE 2. Waveguide probe and Iris dimensions (Units: Millimeter).

Stage	0	1	2	3
H_{IR}	--	0.77	0.64	0.54
T_{IR}	--	0.80	0.80	0.80
d_{IR}	--	0.60	0.60	0.60
l_a	1.42	1.20	1.05	0.92
w_1	0.40	0.38	0.40	0.40
l_1	1.80	1.56	1.53	1.40
w_2	0.60	0.52	0.53	0.52
l_2	1.20	1.22	1.10	1.10

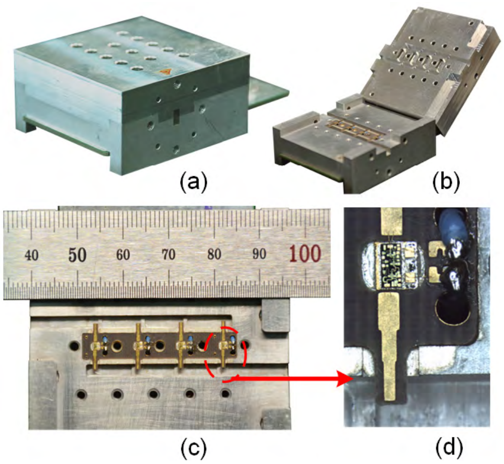

FIGURE 15. Fabricated prototype combined amplifier assembly.

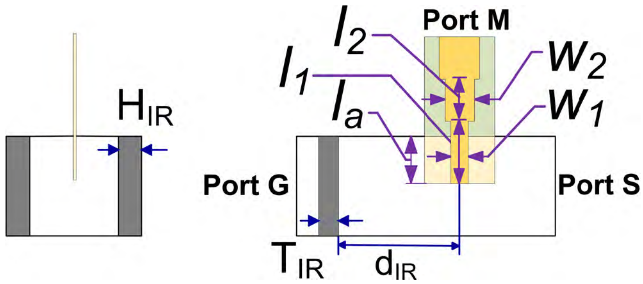

FIGURE 16. Dimension annotation of the E-plane probe and the H-plane iris.

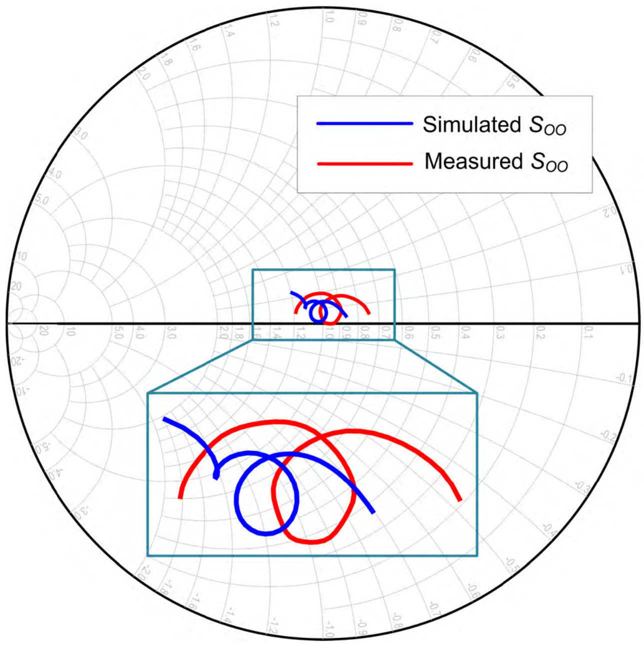

FIGURE 17. Comparison of the simulated and the measured reflection at port.

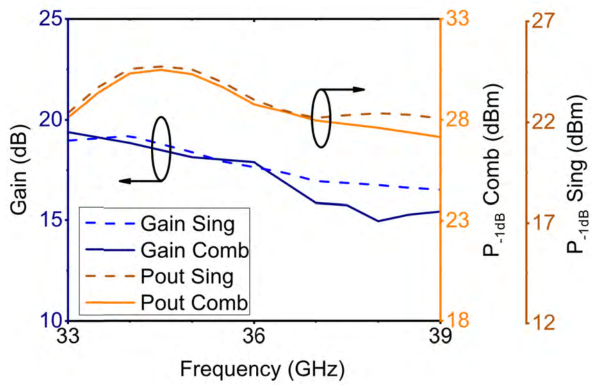

FIGURE 18. Comparison of the measured gain and the P_{1dB} of the combined amplifier with that of a single chip.

codetermined by the superimposition on the specific load-pull curve of the MMIC in the UPAs.

V. EXPERIMENTAL VERIFICATION AND RESULTS

A. COMBINED AMPLIFIER MODULE FABRICATION

The fabrication of a Q-band 4-way travelling-wave power-combining amplifier served as verification of the proposed method. The WTWPC was housed in a WR-22 (5.69x2.845 mm^2) rectangular waveguide. The metal waveguide part was constructed on a 6061 Aluminum alloy (AlMg1SiCu) plate using the computer numerical control (CNC) machining. The microstrip and planar E-plane probes were printed on 10 mil thick TLY-5A laminate (Taconic).

Fig. 15 shows a photograph of the fabricated prototype, while Fig. 16 annotates the geometrical dimensions of the WTWPC, and Table 2 lists their values.

B. MEASURED RESULTS

Fig. 17 presents the measured and the simulated s_{OO}. The measurement was obtained with the assistance of termination by the chip attenuators ATN3580 (Skyworks) mounted at the UPA position, as well as a WR-22 waveguide coaxial adapter SWC-222F-R1 (Sage Millimeter). The deviation between the measured and the simulated results could be ascribed to the superimposed effects of two factors: the impact of the bond wires on the frequency response of the attenuator chips, and the slight misalignment of the planar probes within the prototype

A GaAs MMIC TGA4521 (Qorvo) was used in each UPA. It was biased at 5V drain voltage and a 170mA quiescent current, while the operating frequency ranged between 33 GHz to 39 GHz. Fig. 18 shows the measured gain and output power of the combined PA along with a comparison with that of the single TGA4521 chip. The measured result remained consistent, except for a slight dip in gain at 38 GHz, which was attributed to the response of cavity resonance damping in the UPAs by the RATG-35G microwave absorbers (Dalian Dongshin).

VI. CONCLUSION

This paper ascertains that the WTWPC belongs to the category of asymmetrical non-isolated power combiners. Therefore, suitable load modulation conditions are explored. Specifically, the existing binary load modulation scheme is extended to a nonbinary multi-way case under certain preconditions. The analysis of the active load impedance modulation occurring in a non-isolated combiner reveals a certain consistency among the diverse active impedance trajectories, which is crucial in enabling the coordinated load-pulling of multiple UPAs in the proposed method.

Although full numeric EM simulation provides a static solution for the WTWPC, the indicator for dynamic tuning becomes undistinguishable with the involvement of multi-variable adjustment. To overcome this weakness, a versatile circuit model of the WTWPC is developed based on knowledge obtained from waveguide passive elements. This circuit model provides an effective intermediary between the objective scattering parameters and the physical dimensions of the WTWPC. The appeal of the proposed method lies in its high efficiency and excellent accuracy.

Due to the active load modulation solution, as well as the circuit model for the WTWPC, type-I active load impedance was synthesized. Accordingly, the physical dimensions of the WTWPC are determined directly. Experimental verification of the proposed method was conducted using a Q-band power combined amplifier. Furthermore, the present work lays the foundation for type-II and type-III active load impedance, which enables the operation of UPA producing higher output power.

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