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Design of a Broadband Doherty Power Amplifier Based on Hybrid Continuous Mode

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ABSTRACT Hybrid continuous mode can be utilized to design highly efficient broadband power amplifiers (PAs). In this paper, a broadband Doherty PA (DPA) with enhanced back-off efficiency is realized by using the hybrid continuous mode. Especially, the carrier PA operates under hybrid continuous mode at low-power regions, enhancing the bandwidth and back-off efficiency of the DPAs. For validating the proposed theory, a broadband DPA working over 1.5–2.6 GHz is implemented. The experimental results show that the designed DPA achieves a saturation power of 43.7–45 dBm, a drain efficiency of 41.3%–55.1% at 6-dB output back-off power level, and a drain efficiency of 57%–74.6% at peaking power level.

INDEX TERMS Broadband power amplifier, continuous mode, Doherty, high efficiency.

I. INTRODUCTION

The mobile wireless communications sector has achieved tremendous advances, technology innovations and commercial achievements after years of evolution [1]. However, the explosive proliferation in the number of smart phones and other intelligent devices, coupled with the pursue in much better experience of both users and operators will lead to rapidly growing demands for communication data rates [2]. Rapid transport of signals in next generation communication systems brings about wider signal channels [3]. Thus, the highly-efficient and broadband operation of transmitters is an inevitable progress [3], [4]. Moreover, complex modulation techniques, like orthogonal frequency division multiplexing (OFDM), are expected to continually perform on signals due to the depletable spectrum resources [5]–[7]. In this way, the peak-to-average power ratio (PAPR) of communication signals is ineluctably enhanced [8].

Power amplifiers (PAs) are important elements in wireless communication systems. Due to wireless communication being characterized by high PAPR and broadband operation, broadband PAs with high back-off efficiency are deeply required [5]–[9]. Therefore, how to effectively improve the back-off efficiency of PAs motivates many PA designers [6]–[9]. Compared to other back-off efficiency enhancement techniques, like envelope tracking (ET) and envelope elimination and restoration (EER), Doherty power amplifeir (DPA) is the most popular technique due to its simplified architecture and easy realization [8]. In addition, wideband DPAs are expected to be important components in next generation communication systems [9].

Initially, it was demonstrated in [10] that quarter-wavelength transmission line constrains the bandwidth of DPAs. Nevertheless, the effect of quarter-wavelength transmission line can be deliberately alleviated through reducing transmission ratio [10]. Summarily, the bandwidth of DPAs are affected by combining network. Thus, many innovative combining networks have been adopted for implementing broadband DPAs [11]–[15]. In [11], a grounded quarter wavelength line was added to the output combiner of the traditional DPA architecture for compensating the load impedance of the carrier PA at low power region. Rather than a short circuited stub is added, the authors in [12] inserted a quarter wavelength line into the output of the peaking path for enhancing active load modulation. In [12], the authors presented a 1.7-2.8 GHz DPA based on a modified combining network. The authors in [13] have derived a continuum of DPA solutions with enhanced load modulation for designing broadband DPAs. And a DPA working over an octave was realized in [13]. In [14], a closed form formulation based on an pre-established combiner was presented for designing ultra-wideband DPAs.

The published works indicated that the post-matching DPA is becoming the most popular Doherty architecture,

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especially after 2015 [16], [17]. In [16], the authors demonstrated that low order impedance inverter is more suitable to construct broadband DPAs. As a demonstrator, a 1.7-2.6 GHz DPA was designed by the author in [16]. Moreover, a mutually coupled harmonic post-matching DPA for improving the performances was demonstrated in [17].

It is well known that continuous working mode can be utilized to implement broadband PAs [18], [19]. For extending the working bandwidth and back-off efficiency, applying continuous mode into DPAs appears recently [20]–[22]. In [20], a broadband DPA working across 1.65-2.75 GHz is presented. The measurement results in [20] exhibits a 52%-66% drain efficiency (DE) at a 6 dB back-off power level. Practically, at the low power region, the output impedance of the peaking path locates at the edge of the Smith chart and has some effects on the carrier PA. In [22], a 1.6-2.7 GHz continuous mode DPA (CM-DPA) taking advantage of the non-infinity peaking impedance was implemented.

In [22], at each working frequency, a fixed output impedance of the peaking PA is required by the carrier PA at the low power region. However, at each working frequency, the fixed non-infinity peaking impedance is hard to realized over a wide bandwidth. Thus, in this paper, hybrid continuous mode is applied to Doherty configuration for enhancing the working bandwidth as well as the back-off DE. After introducing hybrid continuous mode into DPA, more impedance space can be derived for the non-infinity peaking impedance at the low power region.

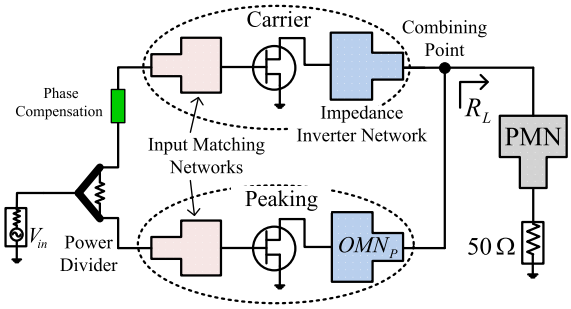


FIGURE 1. The brief architecture of Doherty power amplifiers.

II. HYBRID CONTINUOUS MODE DOHERTY POWER AMPLIFIER

In this contribution, the analysis is based on symmetrical DPA. The brief architecture of DPAs is illustrated in Fig. 1. It includes two PAs, the class-B biased carrier PA and class-C biased peaking PA. The peaking PA is switched-on at 6 dB back-off from saturation power. And it is assumed that the same power ability can be achieved by the carrier and peaking PAs. At the input terminal, two input matching networks are inserted to match the optimal source impedances of two transistors. And a power divider equally splits input signal into carrier and peaking paths. At the output terminal, an impedance inverter network (IIN) after the carrier transistor is utilized to realize active load-modulation. And an output matching network (OMN_P in Fig. 1) after the peaking PA is designed to match the peaking PA. Normally, the load of DPA is R_L, and $R_L = 0.5 \cdot R_{opt}$. Where R_{opt} is the optimal impedance required by a class-B biased transistors [22]. Thus, a post-matching network (PMN) is required to match R_L to 50 Ω. For the whole DPA, a phase compensation line is required to balance the phase difference between the carrier and peaking paths. In the following analysis, all impedances are normalized to R_{opt}.

Hybrid continuous mode is consist of a series continuous modes between class-J and continuous class-F. The detailed theory of the hybrid continuous mode can be derived in [18] and [19]. Hybrid continuous mode is an effective approach to realize broadband PAs [18], [19]. In the following part, the hybrid continuous mode is firstly reviewed. Then, the hybrid continuous mode is introduced into broadband DPAs for enhancing the back-off efficiency.

A. HYBRID CONTINUOUS MODE AT OBO POWER LEVEL

For a symmetrical DPA, at the output back-off (OBO) power level, the current of the carrier PA reaches to half the maximum. Thus the current waveform of the carrier PA at OBO power level can be described as,

$$i_{HB} = \frac{1}{2} \cdot (\frac{1}{\pi} + \frac{1}{2}cos(\theta) + \frac{2}{3\pi}cos(2\theta) + \cdots\cdots) \quad (1)$$

On the other hand, at the back-off power level, the voltage waveform of hybrid continuous mode is [18],

$$v_{HB} = (1 - \mu \cdot cos(\omega t) + \nu \cdot cos(3\omega t)) \cdot (1 - \gamma \cdot sin(\omega t)) \quad (2)$$

where γ, μ and ν are three empirical parameters. And $-1 \le \gamma \le 1$, $1 \le \mu \le 2/\sqrt{3}$. The relationship between μ and ν has been given in [18]. Using (1) and (2), the fundamental impedance of hybrid continuous mode at OBO power level can be derived as,

$$Z_{HB\_1} = 2 \cdot (\mu - j \cdot \gamma) \quad (3)$$

The hybrid continuous mode has two boundaries, class-J and class-F continuums. When $\mu = 1$, the hybrid continuous mode is exactly the class-J continuum. While the hybrid continuous mode is exactly the class-F continuum when $\mu = 2/\sqrt{3}$. Based on (3), the fundamental impedance of the class-J and class-F continuums at OBO power level can be described as,

$$Z_{JB\_1} = 2 \cdot (1 - j \cdot \gamma_J) \quad (4)$$

$$Z_{FB\_1} = 2 \cdot (2/\sqrt{3} - j \cdot \gamma_F) \quad (5)$$

B. BROADBAND DPA UNDER HYBRID CONTINUOUS MODE

For simplicity, the schematic of Fig. 1 can be represented as reported in Fig. 2. Where the carrier and peaking transistors are replaced by current sources I_C and I_P, respectively. In Fig. 2, Z_C is designated as the required load by the carrier PA. Z_{CS} and Z_{CB} are designated as Z_C at maximum power and

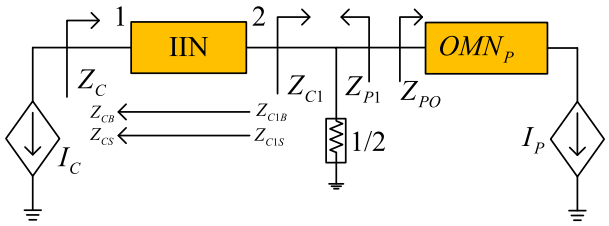


FIGURE 2. The simplified structure of Doherty power amplifiers.

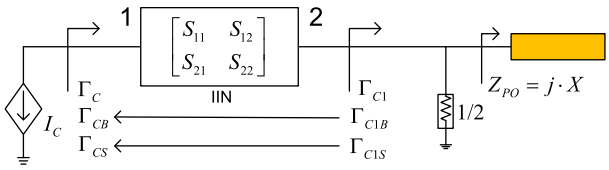


FIGURE 3. The simplified combiner of Doherty power amplifier at the low power region.

output back-off (OBO) power levels, respectively. As shown in Fig. 2, Z_{C1} and Z_{P1} are designated as the load impedances of the carrier and peaking PAs. And Z_{C1B} and Z_{C1S} refer to Z_{C1} at maximum power and OBO power levels, respectively. As stated before, all impedances in this section are normalized to R_{opt}.

At saturation power level, Z_{C1} and Z_{P1} are both equal to 1 due to the active load modulation. The IIN in Fig. 2 maintains matching conditions between 1 and 1 across interested working bandwidth. And OMN_P match the optimal load impedance of the peaking PA to 1 at saturation input power. Traditionally, IIN is a quarter-wave length transmission line. Indeed, IIN can be any passive networks with a phase shift of $-90°$ at the center working frequency. Due to IIN match 1 to 1 across interested working bandwidth, the characteristic impedance at the two terminals of IIN can be set to 1 and 1, respectively. Then, the IIN can be represented by scattering parameter, as shown in Fig. 3. In Fig. 3, the generalized scatter parameters of the IIN can be described as follows [22].

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{j\theta_C} \\ e^{j\theta_C} & 0 \end{bmatrix} \tag{6}$$

where θ_C is the phase delay of the IIN. Normally, θ_C is linearly and periodically. Like in [22], just one period ($-180°$ to $180°$) is considered in this paper.

In Fig. 3, Γ_{C1} is the reflection coefficient looking from port 2 to the combining point. Γ_C is the reflection coefficient looking from carrier transistor to port 1. In Fig. 3, Γ_{C1S} and Γ_{CS} refer respectively to Γ_{C1} and Γ_C at saturation power level. While Γ_{C1B} and Γ_{CB} refer to Γ_{C1} and Γ_C at OBO power level, respectively. The relationship between Γ_{C1} and Γ_C can be represented as [22],

$$\Gamma_C = S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_{C1}}{1 - S_{22} \cdot \Gamma_{C1}}. \tag{7}$$

Based on (6) and (7), the following equation can be deduced.

$$\Gamma_C = \Gamma_{C1} \cdot e^{j2\theta_C}. \tag{8}$$

In equations (8) and (9),

$$\Gamma_{C1} = \frac{Z_{C1} - 1}{Z_{C1} + 1}. \tag{9}$$

At saturation power level, Z_{C1S} equals to 1 due to the active load modulation. Thus, based on (8) and (9), $\Gamma_{C1S} = \Gamma_{CS} = 0$ can be derived. That is, Z_{CS} locates at the center of the Smith chart (A point in Fig. 4). That is, the carrier PA could work very well at saturation power level [21].

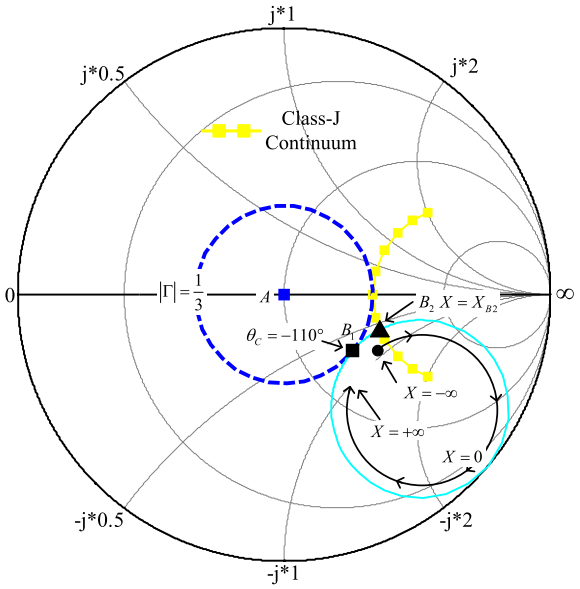


FIGURE 4. The load modulation of the carrier transistor at the low power region.

At the OBO power level, the peaking PA is in the off-sate. Then, the output impedance of the peaking stage locates at the edge of the Smith chart. Therefore, at the OBO power level, the output impedance of the peaking stage can be described as [21],

$$Z_{PO} = (j \cdot X) \tag{10}$$

Then, Z_{C1B} and Γ_{C1B} can be derived as,

$$Z_{C1B} = 0.5//(j \cdot X) \tag{11}$$

$$\Gamma_{C1B} = \frac{0.5//(j \cdot X) - 1}{0.5//(j \cdot X) + 1} = \frac{-1 - j \cdot X}{1 + j \cdot 3 \cdot X} \tag{12}$$

Based on (8), Γ_{CB} and Z_{CB} can be deduced as,

$$\Gamma_{CB} = \Gamma_{C1B} \cdot e^{j \cdot 2 \cdot \theta_C} = \frac{-1 - j \cdot X}{1 + j \cdot 3 \cdot X} \cdot e^{j \cdot 2 \cdot \theta_C} \tag{13}$$

$$Z_{CB} = \frac{1 + \Gamma_{CB}}{1 - \Gamma_{CB}} \tag{14}$$

Equation (14) means that Z_{CB} is determined by X and θ_C simultaneously. On the one hand, when $X = \infty$, Z_{CB} locates

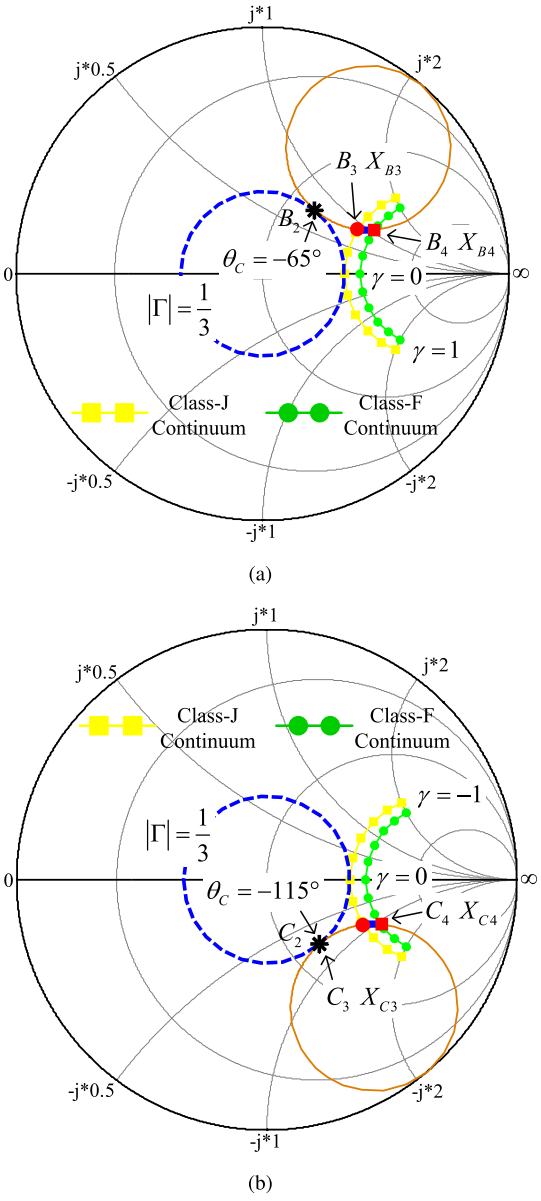


FIGURE 5. The load impedances of the carrier transistors at the low power region with respect to X and θ_C. (a), $\theta_C = -65°$. (b), $\theta_C = -115°$.

on the 1/3 equal reflection coefficient circle with respect to θ_C changes from $-180°$ to $0°$. For example, as shown in Fig. 4, Z_{CB} locates at the B_1 point when θ_C equals to $-110°$. On the other hand, when θ_C is fixed, Z_{CB} forms a circle versus X changes from ∞ to $+\infty$. As shown in Fig. 4, when $\theta_C = -110°$, a circle (the cyan circle in Fig. 4) is formed by Z_{CB} versus X changes from ∞ to $+\infty$. This circle is tangent to the 1/3 equal reflection coefficient circle and the edge of the Smith chart. The cyan circle in Fig. 4 also intersects with the impedance space of the continuous continuum at B_2 point. At the low power region, Z_{CB} can be modulated from B_1 to B_2 when $X = X_{B2}$. The above is the main theory of continuous class-J Doherty PA [22]. Importantly, $|\theta_C|$ should be inside 60°-120°.

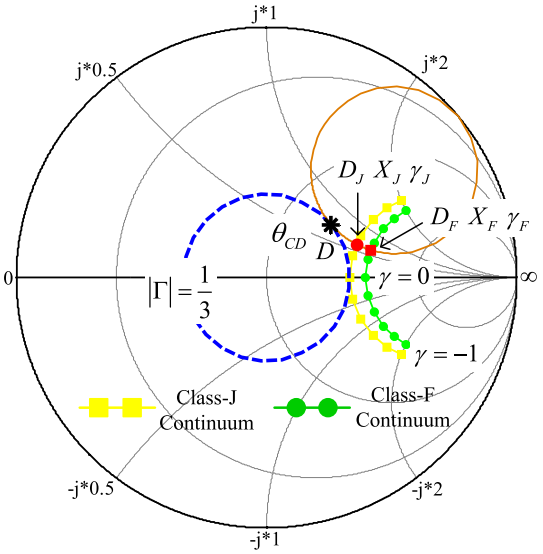


FIGURE 6. The calculation procedure of X when θ_C is fixed.

Like in [22], for deriving hybrid continuous Doherty PA, the following equation should be satisfied.

$$\Gamma_{CB} = \Gamma_{HB\_1} \tag{15}$$

where Γ_{HB_1} is the reflection coefficient of the fundamental impedance of hybrid continuous mode, which can be derived as,

$$\Gamma_{HB\_1} = \frac{Z_{HB\_1} - 1}{Z_{HB\_1} + 1} \tag{16}$$

When $60° \le |\theta_C| \le 120°$, Γ_{CB} will interact with the Γ_{HB_1} by tuning X. For example, when $\theta_C = -65°$, Z_{CB} can be adjusted from B_2 to the impedance space of hybrid continuous mode when X inside X_{B3} and X_{B4}, as shown in Fig. 5(a). And when $\theta_C = -115°$, Z_{CB} can be tuned from C_2 to the impedance space of hybrid continuous mode when X inside X_{C3} and X_{C4}, as shown in Fig. 5(b). Because the circle formed by Γ_{CB} interacts with the boundaries of hybrid continuous mode at B_3 and B_4, or C_3 and C_4. For deriving X_{B3} and X_{C3}, we can set,

$$\Gamma_{CB} = \Gamma_{JB\_1} \tag{17}$$

And for deriving X_{B4} and X_{C4}, we can set,

$$\Gamma_{CB} = \Gamma_{FB\_1} \tag{18}$$

where Γ_{JB_1} and Γ_{FB_1} are the reflection coefficients of the fundamental impedance of class-J and class-F continuums, respectively.

$$\Gamma_{JB\_1} = \frac{Z_{JB\_1} - 1}{Z_{JB\_1} + 1} \tag{19}$$

$$\Gamma_{FB\_1} = \frac{Z_{FB\_1} - 1}{Z_{FB\_1} + 1} \tag{20}$$

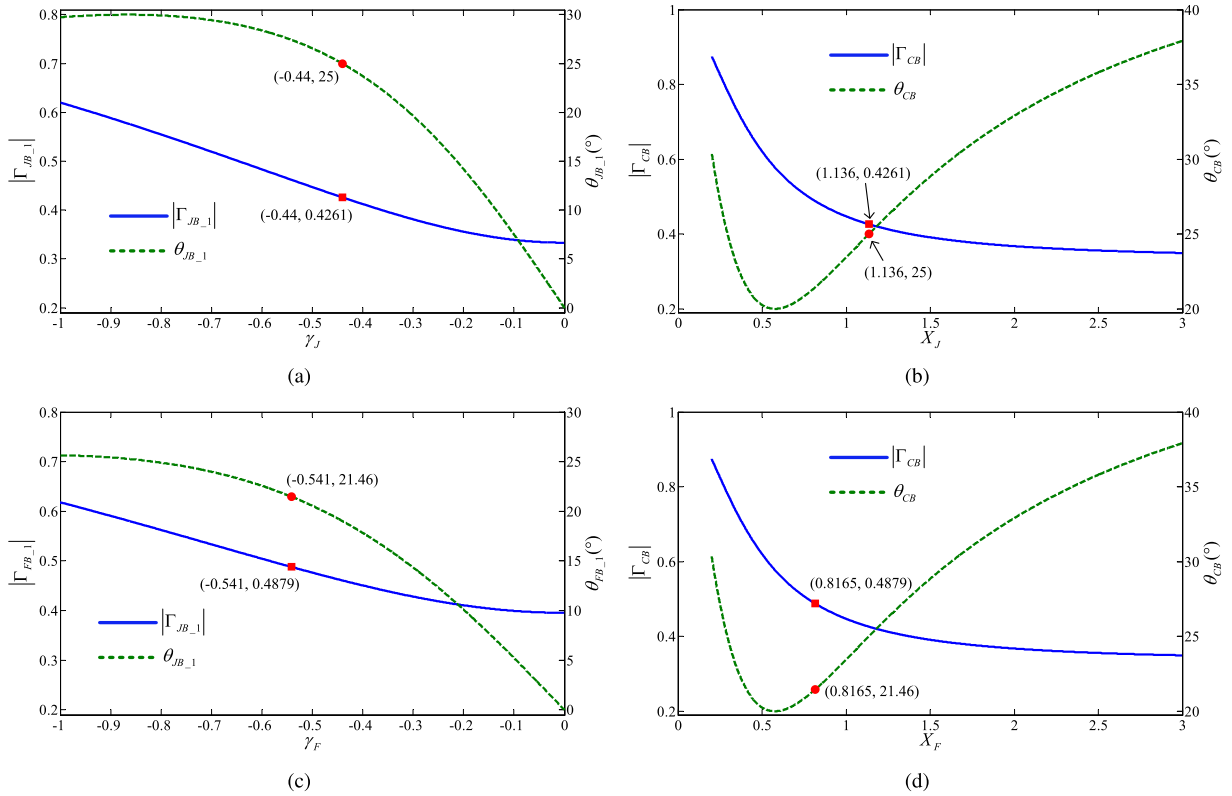


FIGURE 7. An example of the calculation of X when $\theta_C = -65°$. (a) The reflection coefficient of Γ_{JB_1} versus γ_J. (b) The reflection coefficient of Z_{CB} versus X_J. (c) The reflection coefficient of Γ_{FB_1} versus γ_F. (d) The reflection coefficient of Z_{CB} versus X_F.

Combing (4), (13), (17) and (19), X_{B3} and X_{C3} can be obtained. Furthermore, Combing (5), (13), (18) and (20), X_{B4} and X_{C4} can be derived.

Indeed, Both (17) and (18) are include two sub-equations, which can respectively be descried as,

$$\begin{cases} |\Gamma_{CB}| = |\Gamma_{JB\_1}| \\ \theta_{CB} = \theta_{JB\_1} \end{cases} \tag{21}$$

$$\begin{cases} |\Gamma_{CB}| = |\Gamma_{FB\_1}| \\ \theta_{CB} = \theta_{FB\_1} \end{cases} \tag{22}$$

where θ_{CB}, θ_{JB_1} and θ_{FB_1} are the phases of Γ_{CB}, Γ_{JB_1} and Γ_{FB_1}, respectively.

For $\theta_C = -65°$, Z_{CB} can be adjusted from B_2 to the impedance space of hybrid continuous mode after deriving X_{B3} and X_{B4}. When θ_C equals to other values, Z_{CB} can also be tuned to the impedance space of hybrid continuous mode by managing X properly. That is, when $60° \leq |\theta_C| \leq 120°$, the carrier PA could works under hybrid continuous mode by taking advantage of the non-infinity peaking stage.

In continuous class-J DPA, when θ_C is determined, it requires a fixed X to change Z_{CB} to the impedance space of class-J continuum. However, in hybrid continuous mode DPA, there is a impedance space for X when θ_C is fixed, as shown in Fig. 5(a) and (b). Thus, in hybrid continuous mode DPA, more flexibility is derived for the output impedance of the peaking PA at the OBO power level. However, as presented in [22], the phase delay of IIN should be limited by $60° \leq |\theta_C| \leq 120°$. Based on the above theory, a broadband DPA is implemented in the following section.

III. DESIGN AND SIMULATION OF A BROADBAND DPA

This part illustrates the design procedure of a symmetrical DPA based on hybrid continuous mode. The center frequency is assumed to be 2.0 GHz. The active devices utilized in this paper are CGH40010F GaN transistors from Wolfspeed. The optimal impedance of this kind transistor is set to $R_{opt} = 30\ \Omega$ [22]. Thus the load R_L should be 15 Ω.

A. DETERMINATION OF THE NON-INFINITY PEAKING IMPEDANCE

For realizing this broadband DPA, the required X by the carrier PA at different θ_C should be primarily calculated using equations (21) and (22). When θ_C is fixed, two sub-equations of equation (21) has two parameters X and γ_J. Thus, there exist a unique solution for (21). The same conclusion can be derived for equation (22). Indeed, it is a challenge to solve X using (21) or (22) immediately. In this work, a graphical method is presented to determine X, which is presented in the following part.

Firstly, θ_C is fixed at θ_{CD}, which is between $-120°$ and $-60°$. Now, Γ_{CB} locates at the D point in Fig. 6. As shown

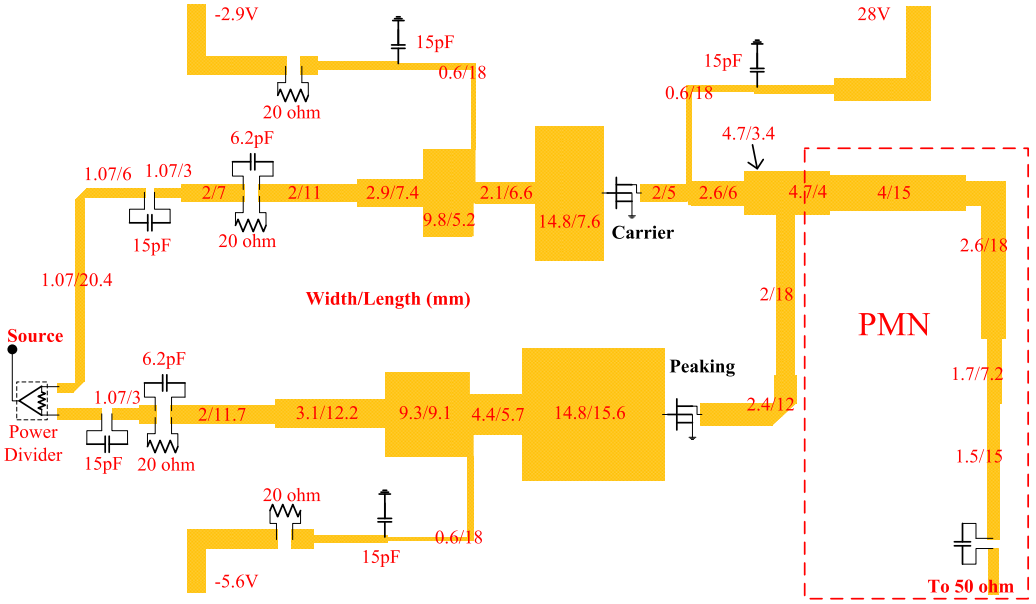


FIGURE 8. The whole schematic of the designed DPA working across 1.4-2.6 GHz.

in Fig. 6, it is assumed that Γ_{CB} interacts with Γ_{JB_1} at D_J point, where two parameters are X_J and γ_J. And it is assumed that Γ_{CB} interacts with Γ_{JB_1} at D_F point, where two parameters are X_F and γ_F. After deriving X_J and X_F, the required X can be determined as $X_F \leq X \leq X_J$ when $\theta_C = \theta_{CD}$.

As an example, $\theta_C = 65°$ is firstly selected. Now, $|\Gamma_{JB\_1}|$ and θ_{JB_1} versus γ_J are illustrated in Fig. 7(a) based on equation (19). Meanwhile, $|\Gamma_{CB}|$ and θ_{CB} versus X_J are illustrated in Fig. 7(b). Then, the unique solution of equation (21) can be obtained from Fig. 7(a) and (b). As shown in Fig. 7(a) and (b), $\gamma_J = -0.44$ and $X_J = 1.136$ is the unique solution of (21). Using the same method, the unique solution of equation (22) can be derived from Fig. 7(c) and (d). As depicted in Fig. 7(c) and (d), $\gamma_F = -0.541$ and $X_F = 0.8165$ is the unique solution of (22) when $\theta_C = 65°$. Using the above method, Table 1 lists the unique solutions of (21) and (22) when θ_C is some fixed values. In Table 1, only θ_C larger than $-90°$ is listed. According to symmetry, the unique solution of (21) and (22) can easily be derived when θ_C is smaller than $-90°$.

TABLE 1. The unique solutions of (21) and (22) when θ_C is some fixed values.

θ_C	-60	-65	-70	-75	-80	-85
γ_J	-0.849	-0.44	-0.307	-0.213	-0.135	-0.0666
X_J	0.589	1.136	1.626	2.35	3.691	7.648
γ_F	N/A	-0.541	-0.3085	-0.1409	0.0345	0.341
X_F	N/A	0.8165	1.108	1.344	1.432	1.06

B. DESIGN OF BROADBAND DPA

In this design, the carrier PA is biased with -2.9 V gate voltage and 28 V drain voltage. While -5.6 V and 28 V are added to the gate and drain of the peaking PA. In this section, all simulation results are derived using Advanced Design System (ADS). Across the simulation, Rogers 4350B substrate with thickness of 20 mil is utilized. The whole schematic of the designed DPA together with the dimensions of utilized elements are depicted in Fig. 8.

Firstly, two input matching networks are realized to match the source impedances of the carrier and peaking PAs. And a two-stage power divider connects the carrier and peaking PAs at the input terminal. The elements of the two-stage power divider has been given in [22]. Thus, the power divider is not detailed here.

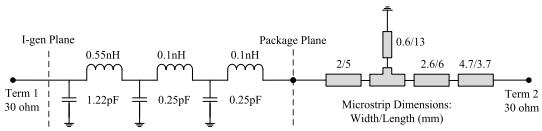


FIGURE 9. The schematic of the designed impedance inverter network.

Then, an IIN is constructed. Due to the utilized transistors possess parasitic and packaged elements, the IIN should include these parasitic and packaged elements. Fig. 9 shows the designed IIN together with the parasitic and packaged elements of the utilized transistors [22]. The simulation results of the IIN are illustrated in Fig. 10. As shown in Fig. 10, the phase delay of the IIN is $-90°$ at 2.0 GHz. And the phase delay of the designed IIN changes from $-60°$ to $-120°$ across 1.5-2.55 GHz. Therefore, the designed IIN satisfies the requirement (where $|\theta_C|$ should be inside 60°-120°) over 1.5-2.55 GHz. Table 2 shows the phase delays of the designed IIN at some working frequencies. At these frequencies, the non-infinity peaking impedances required by the carrier PA at the low power region are also given in Table 2.

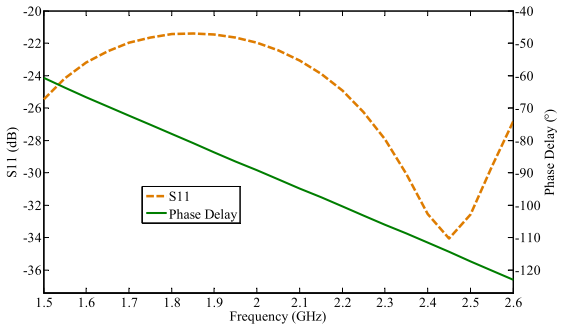


FIGURE 10. The simulation results of the designed impedance inverter network over 1.5-2.6 GHz.

TABLE 2. The phase delays of the designed IIN at some working frequencies.

Frequency (GHz)	1.57	1.75	2.2	2.37
θ_C (°)	-65	-75	-100	-110
X_J	1.136	1.626	-3.691	-1.626
X_F	0.8165	1.108	-1.432	-1.108

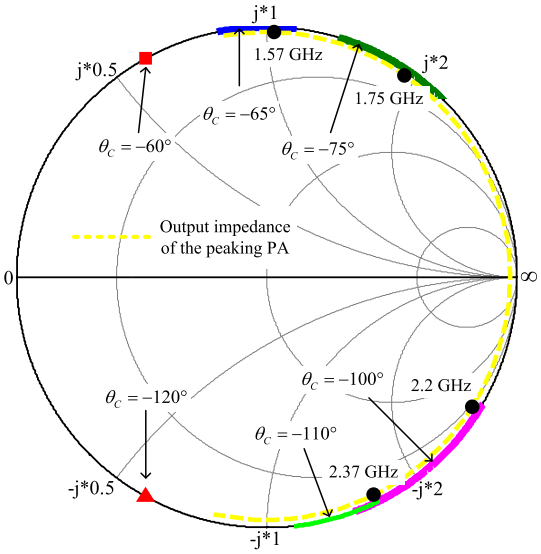
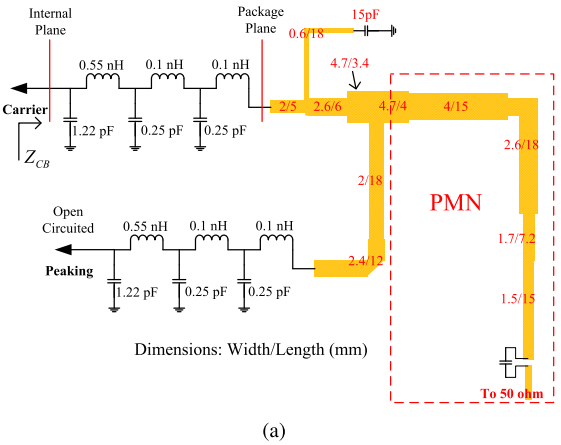
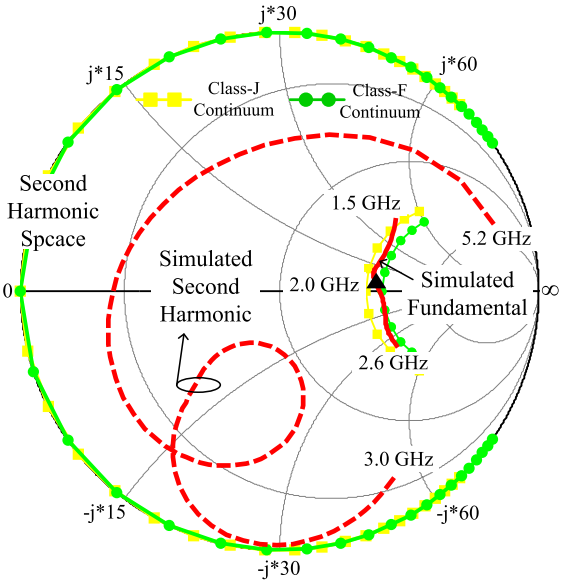


FIGURE 11. The output impedance of the peaking PA at the low power region across 1.5-2.6 GHz.

After completing the design of IIN, an output matching network should be implemented to match the peaking PA. As shown in Fig. 8, the output matching network of the peaking PA (OMN_P) is consist of two transmission lines. The OMN_P not only ensures that the peaking PA possesses high performances at saturation input power level, but also ensures that the peaking PA possesses suitable output impedance at low power region. Fig. 11 shows the output impedance of the peaking at the low power region across 1.5-2.6 GHz. When θ_C equals to $-65°$, $-75°$, $-100°$, and $-110°$, the theoretical output impedances of the peaking PA are given in Fig. 11.



(a)



(b)

FIGURE 12. The simulated load impedance trajectories of the carrier transistors at the low power region. (a) The simulation schematic. (b) The simulated load impedance trajectories.

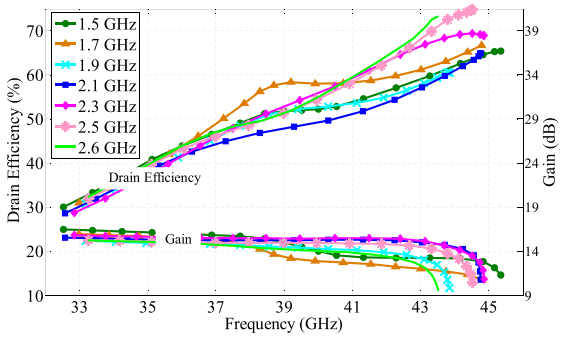


FIGURE 13. The simulated drain efficiency and gain of the fabricated DPA versus output power at some working frequencies.

Based on Table 2, the output impedances of the peaking PA at 1.57, 1.75, 2.2 and 2.37 GHz are also depicted in Fig. 11. Fig. 11 demonstrates that the designed OMN_P ensures the non-infinity peaking PA is suitable across almost the whole interested working bandwidth.

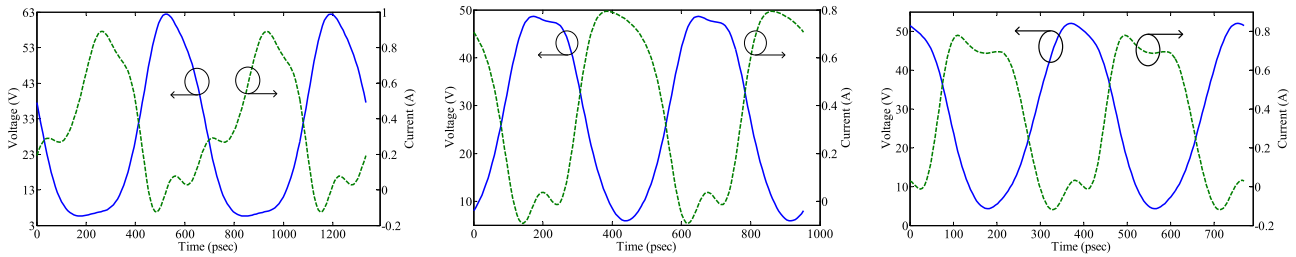


FIGURE 14. The simulated voltage and current waveforms of the carrier transistor at the device intrinsic plane when the output power is 37 dBm. (a) Voltage and current waveforms at 1.5 GHz. (b) Voltage and current waveforms at 2.1 GHz. (c) Voltage and current waveforms at 2.6 GHz.

Undoubtedly, in continuous mode DPA design, the harmonic impedances are very important at the output back-off power level [25]. In the above analysis, the harmonic impedance are ignored. Indeed, the second harmonic impedance plays an important role in hybrid continuous mode PAs. In DPAs, the second harmonic load impedance of the carrier transistor is affected not only by the post-matching network but also by the non-infinity peaking impedance at the low power region.

In our design, the fundamental and second harmonic impedances are considered. After the output matching networks of the carrier and peaking transistors are constructed, the required second harmonic impedance of the Doherty PA at the combining point can be derived though second harmonic load-pull simulation. Then, based on the load-pull data, the harmonic control can be realized by a post-matching network. This harmonic control method has already been presented in [20].

Finally, a post-matching network is constructed to match 15 Ω to 50 Ω across 1.5-2.6 GHz. Meanwhile, the post-matching network should control the second harmonic impedances of the deigned DPA. The designed PMN is shown in Fig. 8 (in the red dashed box).

C. SIMULATION RESULTS

Firstly, the load impedance of the carrier transistor at the low power region (Z_{CB}) is investigated. When evaluating the fundamental and second harmonic impedances of the carrier transistor, the parasitic and package elements of the utilized transistor should be taken into consideration. Fig. 12(a) depicts the simulation schematic which includes the parasitic and package elements of the utilized transistor. Fig. 12(b) shows the simulated fundamental and second harmonic impedance trajectories of the carrier transistor at the low power region. Clearly, the red solid line demonstrates that the fundamental load impedance locates inside the impedance space of the hybrid continuous mode. The red dashed line in Fig. 12(b) indicates that the second harmonic load impedance locates at the edge of the smith chart. And the distribution of the second harmonic load impedance agrees well with the theoretical region of the second harmonic impedance space of the hybrid continuous mode.

Secondly, to validate the hybrid continuous operation mode of the designed DPA at OBO power level, the voltage and current waveforms of the carrier transistor at the device internal plane is simulated when the output power is 37 dBm. The simulated voltage and current waveforms at 1.5, 2.1 and 2.6 GHz are depicted in Fig. 13(a)-(c), respectively. The simulated voltage and current waveforms indicate that the designed DPA operates under hybrid continuous mode at the OBO power level.

Finally, the simulated drain efficiency (DE) and gain of the designed DPA versus output power at some working frequencies are shown in Fig. 14. Clearly, apparent Doherty behavior is derived by the designed DPA over 1.5-2.6 GHz.

IV. EXPERIMENTAL RESULTS

The photograph of the fabricated DPA is shown in Fig. 15. When testing the fabricated DPA, the gate voltages of the carrier and peaking PAs are −2.7 V and −5.9 V, respectively.

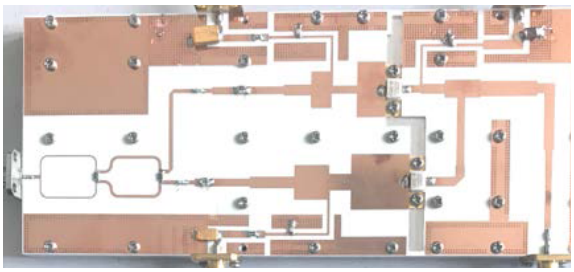
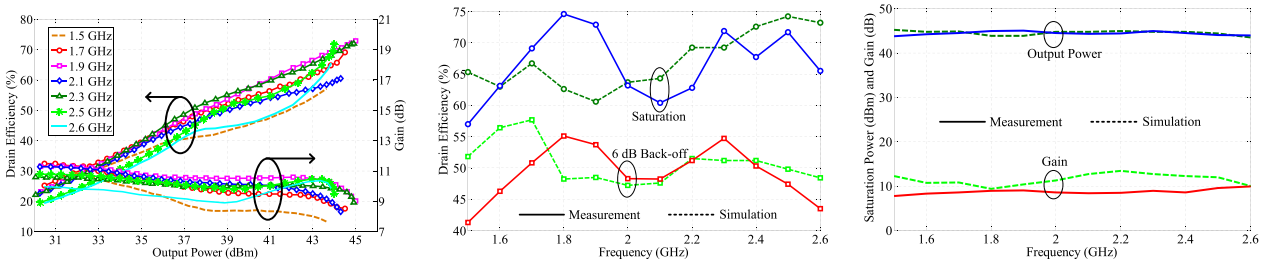


FIGURE 15. The photograph of the fabricated broadband DPA.

A. CONTINUOUS WAVE SIGNAL EXCITATION

Under continuous wave signal excitation, the measured DEs and gains at some working frequencies with respect to output power are indicated in Fig. 16(a). For clearly evaluating the performance of the fabricated DPA, Fig. 16(b) gives the measured DEs versus the entire working band at 6 dB OBO and saturation power levels. It indicates that the fabricated DPA obtains a saturation DE of 57%74.6%, and a 6 dB back-off DE of 41.3%-55.1% over 1.5-2.6 GHz. For comparison, the simulated DEs versus the whole working band are also



(a) (b) (c)

FIGURE 16. The measurement results of the fabricated DPA. (a) The measured drain efficiency and gain of the fabricated DPA versus output power at some working frequencies. (b) The measured and simulated drain efficiency of the fabricated DPA versus the whole working frequency band. (c) The measured and simulated output power and gain of the fabricated DPA over the whole working frequency band.

TABLE 3. Comparison between some recently published symmetrical DPAs and our work.

Year, Ref.	Frequency (GHz)	BW (GHz)	Power (dBm)	Gain (dB)	DE@Sat (%)	DE@OBO (%)
2014, [14]	1.05−2.55 (83%)	1.5	40−42	>7	45−83	35−58
2016, [11]	1.5−2.5 (50%)	1	42−44.5	8−11	55−75	42−53
2016, [12]	1.7−2.8 (49%)	1.1	44−44.5	11−12	57−71	50−55
2016, [20]	1.65−2.75 (50%)	1.1	44−46	7−8	60−75	50−60
2017, [13]	0.55−1.1 (67%)	0.55	42−43.5	N/A	56−72	40−52
2018, [15]	1.5−3.8 (87%)	2.3	42.3−43.4	N/A	42−63	33−55
This Work	1.5−2.6 (53%)	1.1	43.7−45	7.7−9.3	57−74.6	41.3−55.1

illustrated in Fig. 16(b). The simulated DEs of the designed DPA over the whole working band are 60.6%-74.2% and 47.2%-57.7% at saturation and 6 dB OBO power levels, respectively.

Fig. 16(c) shows the saturated output power and gain of the designed DPA. From Fig. 16(c), the measurement results indicate that the designed DPA could deliver an saturation output power of 43.7-45 dBm with a gain of 7.7-9.3 dB over 1.5-2.6 GHz. And the simulation results show that the saturation output power and gain of the designed DPA across 1.5-2.6 GHz are 43.5-45.2 dBm and 9.3-13.4 dB, respectively.

From Fig. 16(b) and (c), small difference between simulation and measurement results can be observed. The difference between simulation and experiment results can be attributed to the following reasons. Firstly, the soldering of transistors, capacitors and other elements could lead to the degradation of the experimental results. secondly, the inaccuracy model of the utilized transistors and other elements is another factor that results in the difference between simulation and experiment. Finally, the process error of printed circuit board (PCB) is an uncontrollable factor.

Under the excitation of CW signal, the experimental results of the fabricated DPA are listed in Table 3. Furthermore, some state-of-the-art works are also given in Table 3 for comparison. Comparable performances are obtained by this work based on Table 3.

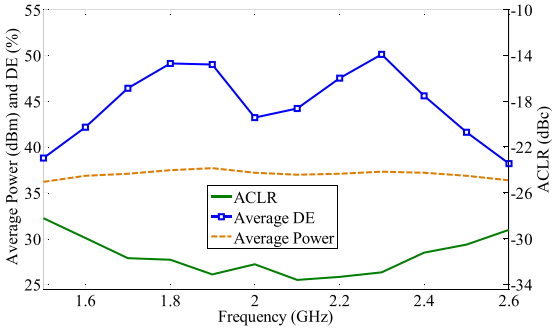


FIGURE 17. The measurement results of the fabricated DPA under the excitation of a 20 MHz LTE modulated signal.

B. MODULATED SIGNAL EXCITATION

To evaluate the linearity of the designed DPA, a 20-MHz LTE signal with a peak to average power ratio (PAPR) of 7.05 dB is adopted to drive the fabricated DPA. The measured adjacent channel leakage ratio (ACLR) with respect to working frequency is shown in Fig. 17. At the average power of 36.2-37.7 dBm, the measured ACLR changes from −33.6 dBc to −28.2 dBc across 1.5-2.6 GHz. Meanwhile, the measured average DE of the fabricated DPA is 38.8%-50.1% over the whole working frequency band.

Furthermore, to further linearize the fabricated DPA, digital pre-distortion (DPD) technique is utilized during the

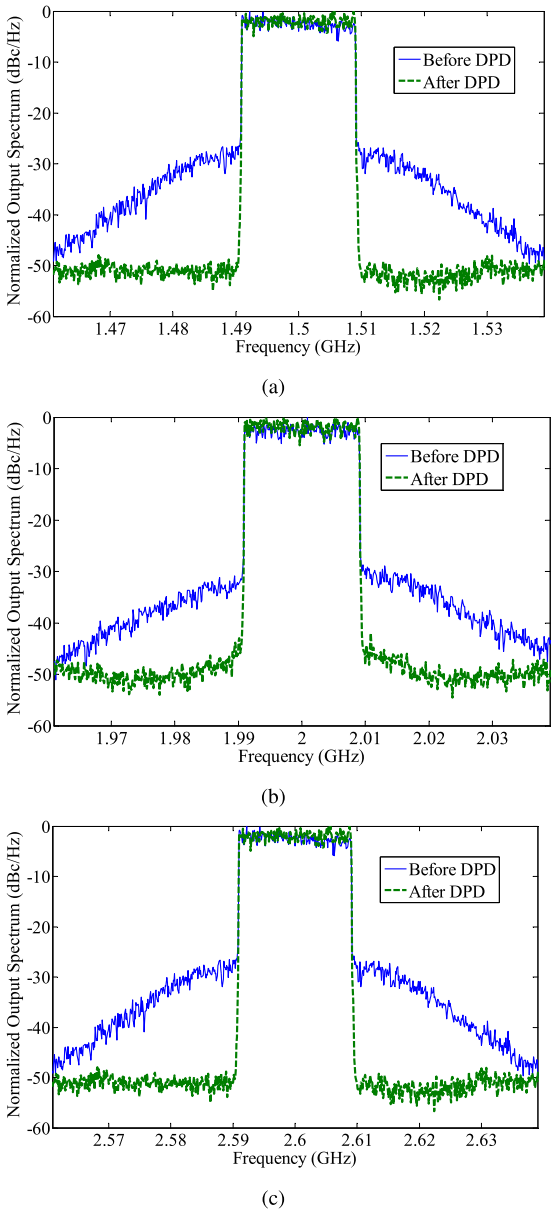


FIGURE 18. The normalized output spectrum of the fabricated DPA before and after DPD. (a) The normalized output spectrum at 1.5 GHz. (b) The normalized output spectrum at 2.0 GHz. (c) The normalized output spectrum at 2.6 GHz.

modulated signal excitation. The testing frequency points are 1.5, 2.0 and 2.6 GHz. As shown in Fig. 17, the measured average power is 36.2, 37.2 and 36.4 dBm with average DEs of 38.8%, 43.2% and 38.2% at 1.5, 2.0 and 2.6 GHz, respectively. The normalized output spectrum of the fabricated DPA at 1.5, 2.0 and 2.6 GHz are depicted in Fig. 18(a)-(c), respectively. The measured ACLRs of the fabricated DPA before DPD are −28.2, −32.1 and −29.2 dBc at 1.5, 2.0 and 2.6 GHz, respectively. While after DPD, the measured ACLRs of the fabricated DPA are −49.7, −48.6 and −49.5 dBc at 1.5, 2.0 and 2.6 GHz, respectively. Clearly, the fabricated DPA can be further linearized by DPD technique.

V. CONCLUSION

Hybrid continuous mode is introduced into broadband DPAs in this contribution. Considering the non-infinity peaking impedance, simulation results validate the designed DPA operates under hybrid continuous mode. A 1.5-2.6 GHz (a relative bandwidth of 53%) DPA is fabricated in this work for validating the proposed theory. Experimental results indicate that the fabricated DPA achieves a 6 dB back-off drain efficiency of 41.3%-55.1% over 1.5-2.6 GHz. The saturation output power of the fabricated DPA is 43.7-45 dBm with a drain efficiency of 57%-74.6% over 1.5-2.6 GHz.

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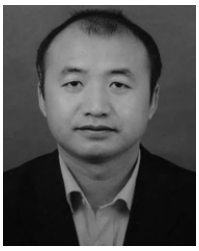

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