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Low Switching Frequency Based Asymmetrical Multilevel Inverter Topology With Reduced Switch Count

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ABSTRACT The inceptions of multilevel inverters (MLI) have caught the attention of researchers for medium and high power applications. However, there has always been a need for a topology with a lower number of device count for higher efficiency and reliability. A new single-phase MLI topology has been proposed in this paper to reduce the number of switches in the circuit and obtain higher voltage level at the output. The basic unit of the proposed topology produces 13 levels at the output with three dc voltage sources and eight switches. Three extentions of the basic unit have been proposed in this paper. A detailed analysis of the proposed topology has been carried out to show the superiority of the proposed converter with respect to the other existing MLI topologies. Power loss analysis has been done using PLECS software, resulting in a maximum efficiency of 98.5%. Nearest level control (NLC) pulse-width modulation technique has been used to produce gate pulses for the switches to achieve better output voltage waveform. The various simulation results have been performed in the PLECS software and a laboratory setup has been used to show the feasibility of the proposed MLI topology.

INDEX TERMS DC–AC converter, multilevel inverter, reduce switch count, nearest level control (NLC).

I. INTRODUCTION

Nowadays, multilevel inverters are getting more attention in many industrial and renewable energy applications. Compare to its two-level counterparts, multilevel inverter have superior power quality feature with low total harmonic distortion (THD). The conventional MLI topologies which include neutral point clamped or diode clamped MLI (NPCMLI), flying capacitor MLI (FCMLI) and cascaded H-bridge MLI (CHBMLI) are being used in industries for varied applications. The high power application include HVDC transmission system, solar PV generation system, wind energy generation system and traction in railways while lower power level MLI is used in grinding mills, pumps, conveyor belts, reactive power compensation, propulsion of marine system and starter of turbines etc. [1]–[4]. But these conventional topologies have some limitations. There is a requirement of large number of isolated DC power supply in CHB topology which increases with the number of levels in the output voltage waveform while FC-MLI requires a complex control mechanism to ensure that the voltage across the capacitor is maintained constant. This control becomes more challenging when the number of capacitor increases exponentially with the higher output voltage level generation. Over the last few years, the research has been focused on developing topologies to overcome the shortcomings of the conventional multilevel inverter [5], [6].

Researchers are trying to further reduce the number of switches for overcoming the cost constraint and improving the quality of output voltage waveform by increasing the

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number of levels at the output voltage. With a higher number of levels, the advantages possessed by the topology includes the increase in efficiency, reliability, power density, reduced filter size, and increased range of applications [7].

Designing newer MLI topology derive its motivation to reduce the count of isolated DC power supply, switch and gate driver requirement. Based on these parameters several topologies have been presented in the literature [6]–[8]. In [9], a topology based on developed H-bridge produces both polarities (negative & positive) in the output voltage waveform. But the requirement of blocking maximum output voltage by two switches in the topology limits its use for high voltage application. The authors of [10] have tried to resolve this problem by modifying circuit topology. Several other MLI topologies have been proposed in [11]–[15] each having some advantages and shortcomings.

The topology proposed in [16] has a structure as a sub multilevel module which can be connected in series. However, the use of backend H-bridge limits its applications for high voltage applications. The work done in [16] has been modified, and a newer topology has been proposed in [17]. In [17], the cascaded topology is based on the half-bridge configured dc voltage sources. The modified single unit structure has switches in one leg instead of the dc voltage sources and every unit has a different H-bridge for obtaining the voltage polarity. The modified structure has lesser voltage stress on the H-bridge switches due to cascade connection but the number of switches increases as compared to [16]. A bidirectional multilevel inverter topology has been proposed in [18] which has asymmetric as well as symmetric configurations having a fewer number of DC power supply and lesser driver circuits and power electronic switches requirement. But, the use of backend H-bridge increases the total standing voltage (TSV) of the topology.

Many topologies incorporating modified H-Bridge (MHB) configuration has been employed by various topologies to enhance the level of voltage generated manifold [10], [19]–[25]. Apart from generating the polarity of voltage level, a MHB also generates voltage level corresponding to the addition of the voltages on the two sides of the MHB. In all of the above topologies, at least two switches need to block the peak of the output voltage. Similarly, a new category of multilevel inverter topologies has been based on the reduced voltage stress across the switches. In this kind of topologies, the maximum voltage stress across any switch is less than the peak output voltage [26]–[30].

In this paper, a novel MLI topology has been proposed with the aim of reduced switch count, reduced TSV and individual voltage stress for the higher number of levels. This paper has been organized as follows: a detailed analysis of the proposed topology is carried out in section II. Section III discusses the nearest level control pulse width modulation techniques for producing pulses for the gate driver circuit. Section IV provided the comparative study for the proposed topology considering various circuit parameters. Section V gives a detailed analysis of the power loss using PLECS software.

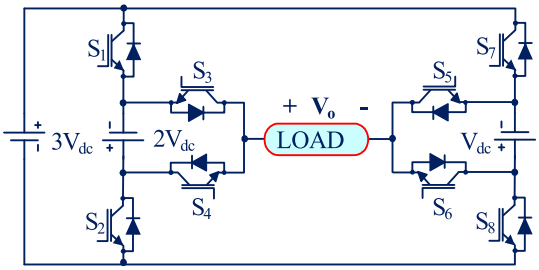

FIGURE 1. Basic unit of the proposed topology.

TABLE 1. Switching table for the basic unit of the proposed topology.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o
0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	1	0	V_{dc}
1	0	0	1	1	0	1	0	$2V_{dc}$
1	0	1	0	0	1	0	1	$3V_{dc}$
1	0	1	0	0	1	1	0	$4V_{dc}$
1	0	0	1	0	1	0	1	$5V_{dc}$
1	0	0	1	0	1	1	0	$6V_{dc}$
1	0	1	0	1	0	1	0	0
1	0	1	0	1	0	0	1	$-V_{dc}$
0	1	1	0	0	1	0	1	$-2V_{dc}$
0	1	0	1	1	0	1	0	$-3V_{dc}$
0	1	0	1	1	0	0	1	$-4V_{dc}$
0	1	1	0	1	0	1	0	$-5V_{dc}$
0	1	1	0	1	0	0	1	$-6V_{dc}$

Simulation results have been presented in section VI which is validated by experiment on a prototype of the MLI. The conclusion is presented in VII.

II. DETAILED ANALYSIS OF THE PROPOSED TOPOLOGY

A. BASIC UNIT

The basic unit of the proposed multilevel inverter topology is shown in Fig 1. The circuit consists of three dc voltage sources of magnitude V_{dc}, $2V_{dc}$ and $3V_{dc}$ and eight power semiconductor switches. The switch pair (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) are connected to the topology such that their conduction at the same time leads to short circuit of dc voltage sources. Therefore these switch pairs need to be operated in complementary mode. Table 1 gives the switching modes of the proposed basic unit. Fig 2. Shows various switching states of the proposed topology as per the switching states shown in Table 1.

One of the important aspect in the designing of MLI topology is the total standing voltage. It is defined as the sum of highest voltage stress appearing across switch for all the levels generated at the output. For the basic unit of the proposed MLI topology, the maximum voltage stress across each switch is given as:

$$\left.\begin{aligned} V_{S1} &= V_{S2} = 3V_{dc} + 2V_{dc} = 5V_{dc} \\ V_{S3} &= V_{S4} = 2V_{dc} \\ V_{S5} &= V_{S6} = V_{dc} \\ V_{S7} &= V_{S8} = V_{dc} + 3V_{dc} = 4V_{dc} \end{aligned}\right\} \quad (1)$$

where V_{S1}, V_{S2}, V_{S3}, V_{S4}, V_{S5}, V_{S6}, V_{S7}, and V_{S8} are the voltage stress of switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8

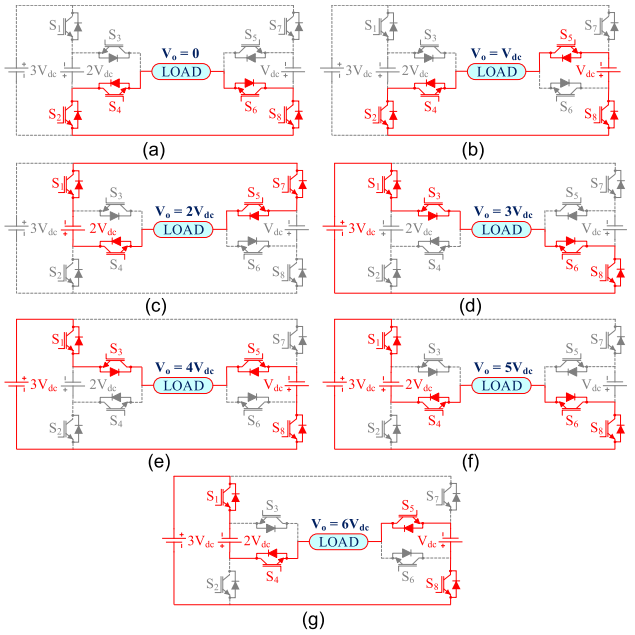

FIGURE 2. Switching states for positive half voltage generation with. (a) $V_o = 0$, (b) $V_o = V_{dc}$, (c) $V_o = 2V_{dc}$, (d) $V_o = 3V_{dc}$, (e) $V_o = 4V_{dc}$, (f) $V_o = 5V_{dc}$, and (g) $V_o = 6V_{dc}$.

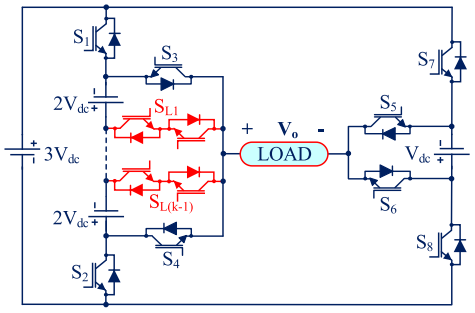

FIGURE 3. Extension I of the basic unit.

respectively. Therefore, the TSV of the basic unit sum to be

$$TSV = 2\left(V_{S1} + V_{S3} + V_{S5} + V_{S7}\right) = 24V_{dc} \tag{2}$$

B. STRUCTURE OF THE PROPOSED TOPOLOGY

The basic unit of the proposed topology as shown in Fig. 1 can be extended in three different approaches which are discussed below.

i. Extension I: In this approach, k number of dc voltage source of magnitude $2V_{dc}$ are included to the basic unit as shown in Fig. 3. The inclusion of a DC power supply increases the output voltage level by four. With each additional dc voltage source, one bidirectional switch is added to the topology.

For k number of such dc power supply, the equations for the number of switches (N_{sw}), gate driver (N_{gd}), the dc power supply (N_{dc}) and the levels (N) for the proposed

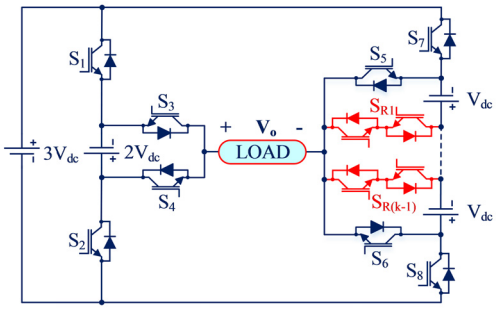

FIGURE 4. Extension II of the basic unit.

MLI topology are given as:

$$\left.\begin{aligned} N_{sw} &= (2k+6) \\ N_{gd} &= (k+7) \\ N_s &= (k+2) \\ N &= (4k+9) \end{aligned}\right\} \tag{3}$$

The TSV of the topology shown in Fig can be calculated as

$$\left.\begin{aligned} V_{S1} &= V_{S2} = 3V_{dc} + k \times 2V_{dc} = (3+2k)\,V_{dc} \\ V_{S3} &= V_{S4} = k \times 2V_{dc} = 2kV_{dc} \\ V_{S5} &= V_{S6} = V_{dc} \\ V_{S7} &= V_{S8} = V_{dc} + 3V_{dc} = 4V_{dc} \end{aligned}\right\} \tag{4}$$

For the voltage stress of the bidirectional switches connected to $2V_{dc}$ (TSV_L) can be calculated as

$$TSV_L = M \times 2V_{dc} \tag{5}$$

where M is given by

$$\left.\begin{aligned} M &= \frac{3k^2+2k-1}{4} \quad \text{for odd number of } k, \quad k > 2 \\ M &= \frac{3k^2+2k}{4} \quad \text{for even number of } k, \quad k > 2 \end{aligned}\right\} \tag{6}$$

Therefore, the TSV of the extension I is given as

$$TSV = (2M + 8k + 16)\,V_{dc} \tag{7}$$

ii. Extension II: In this approach, k number of dc voltage source of magnitude V_{dc} are included in the basic unit as shown in Fig. 4.

There is an increase in two levels at the output voltage level with each addition in DC power supply in this extension. The different equations for the topology shown in Fig. 4 are given as

$$\left.\begin{aligned} N_{sw} &= (2k+6) \\ N_{gd} &= (k+7) \\ N_s &= (k+2) \\ N &= (2k+11) \end{aligned}\right\} \tag{8}$$

Similarly, the TSV of the topology is given as

$$TSV = (M + 4k + 20)\,V_{dc} \tag{9}$$

where M can be calculated using (6).

iii. Extension III: In this extension, both Ext-I and Ext-II are combined together, i.e., there ia an addition of k DC power

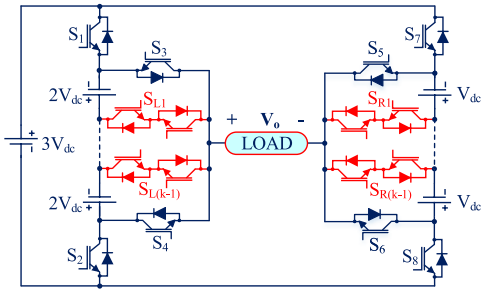

FIGURE 5. Extension III of the basic unit.

TABLE 2. Different equations of the proposed topologies.

Extension	N_{sw}	N_{gd}	N_{dc}
I	$\frac{1}{2}(N+3)$	$\frac{1}{4}(N+19)$	$\frac{1}{4}(N-1)$
II	$(2N-18)$	$(N-5)$	$(N-10)$
III	$\frac{2}{3}(N-1)$	$\frac{1}{3}(N+11)$	$\frac{1}{6}(N+5)$

supply number with magnitudes of $2V_{dc}$ and V_{dc} simultaneously. This arrangement is shown in Fig. 5. The different equations for such kind of extension are given as:

$$\left.\begin{aligned} N_{sw} &= (4k+4) \\ N_{gd} &= (2k+6) \\ N_s &= (2k+1) \\ N &= (6k+7) \end{aligned}\right\} \tag{10}$$

Similarly, the TSV of the topology is given as

$$TSV = (3M + 12k + 12)\, V_{dc} \tag{11}$$

The three extensions of the proposed basic unit has been summarized in Table 2 with equations in terms of the number of levels *N*.

III. NEAREST LEVEL CONTROL

The modulation techniques such as optimal switching technique, selective harmonic elimination (SHE), and nearest level control methods are the most preferred techniques used in high-power applications [31], [32]. In SHE method, nonlinear transcendental equations are used analytically to eliminate lower order harmonics. The trigonometric terms in the equation provide multiple sets of switching angles. The main problem associated with SHE is to solve the transcendental equations due to its complexity. These equations can be solved by using various soft computing techniques for obtaining optimized switching angles in open loop applications. However, it is very difficult to use it in closed loop applications. The nearest level control techniques are used in high voltage applications and can be classified into two types: (i) nearest space vector control and (ii) nearest-level control technique. The drawbacks of SHE can be eliminated

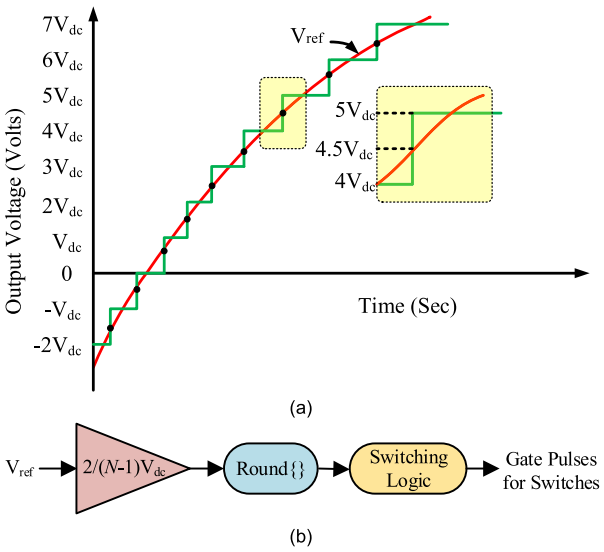

FIGURE 6. Nearest level control with. (a) sampled reference signal and. (b) implementation of NLC.

by using nearest control techniques, in which the switching losses are minimized and lower order harmonics are reduced. The NLC method operates at 50 Hz or 60Hz, and it can be extended to *N* level. The vector control method is more complex in nature for finding the nearest vector and will take more computational time for the operation [33], [34].

In the present work, NLC has been used for controlling the output voltage of the proposed basic unit of the multilevel inverter. The working of the NLC technique is depicted in Fig. 6 (a) and (b). The modulation index (MI) can be varied in NLC by changing the V_{ref} and can be defined in (12).

$$Modulation\ Index = \frac{2V_{ref}}{(N-1)\, V_{dc}} \tag{12}$$

IV. COMPARATIVE STUDY

In order to show the merits of the proposed topology over other structures of the multilevel inverter topologies, a comparative study has been presented in this section for the basic unit and its extended topologies.

A. COMPARISION OF BASIC UNIT

A quantitative comparison has been presented in Table 3, The common aspect of these topology has been that all these topologies have three dc voltage sources. Apart from quantitative comparison, the maximum blocking voltage (MBV) and TSV has also been considered in per unit. For per unit calculation, the actual value of MBV and TSV has been divided by the peak of the output voltage. From Table 3, the topologies proposed in [19] and [27] generates 15 levels. However, the TSV has a higher value compared to the proposed topology. Also, the topology proposed in [28] requires a lower number of switches and gate driver circuit compare to the proposed topology. However, the topology of [28] uses four power diodes which will have an adverse effect on the

TABLE 3. Quantitative comparison of the basic unit of the proposed topology.

Topology	N	N_{sw}	N_{gd}	N_d	MBV	MBV_{pu}	TSV_{pu}
[18]	7	8	7	0	3	1	6
[20]	11	10	9	0	5	1	6.6
[26]	11	8	7	0	4	0.8	5.5
[27]	15	10	9	0	6	0.857	4.857
[28]	9	7	7	4	4	1	5.25
Proposed	**13**	**8**	**8**	**0**	**5**	**0.833**	**4**

efficiency, and the TSV of the topology is higher compared to the proposed topology.

B. COMPARISON OF THE EXTENDED TOPOLOGIES

In this section, a comparison has been carried out with recently proposed reduce switch count based MLI topologies and the proposed topology (extension I). The comparison is based on the switch and driver requirement and the DC power supply as the number of levels increases.

A correlation between the number of switches and the number of levels with similar topologies have been depicted in Fig. 7 (a). The lines shown in Fig. 7 (a) illustrates that the proposed topology requires a lower number of switches compared to all other topologies used for the comparisons. In the same way, Fig. 7 (b) shows the relationship of the number of gate driver circuit required against the number of voltage levels at the output for different topologies along with the proposed topology. The proposed topology requires a lower number of gate driver circuit in contrast to all other topologies.

DC power supply count reduction is an important aspect for design purpose of MLI. Lesser number of DC power supply increases the practical application aspects of the topology. Fig. 7 (c) shows the lower number of dc voltage source requirement of the proposed topology compared to other topologies.

V. POWER LOSS ANALYSIS

For the calculation of power losses of the basic unit of the proposed topologies, PLECS software has been used using the thermal modelling of the power semiconductor devices. The losses in the power semiconductor devices due to switching and conduction loss are accurately calculated using the multi-dimensional lookup tables created by the information provided by the manufacturer in the date sheet. The loss model of turn OFF, turn ON, and conduction losses of the IGBT switch IKW25N120H3 manufactured by Infineon are given in Fig. 8 (a), (b), and (c) respectively up to 25A. With the step voltage of 50V (±300V peak output voltage), the power loss of the proposed topology has been analyzed using different types of load.

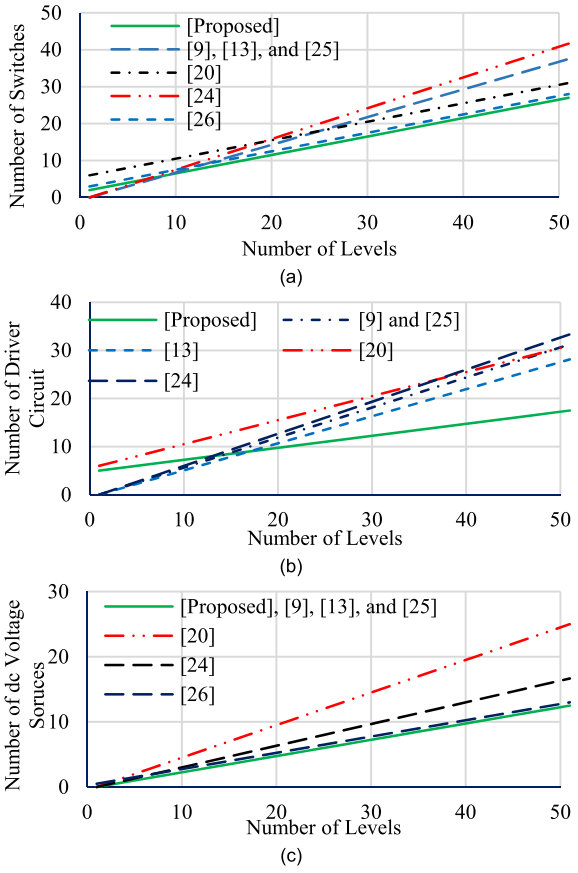

FIGURE 7. Comparison of proposed topology with extension-I for. (a) number of switches. (b) number of gate driver circuit. and (c) number of dc voltage sources against number of levels.

Fig. 9 shows the efficiency vs output power curve for a resistive load. The maximum efficiency achieved using the proposed topology has been 98.5% with an output power of 100W. Furthermore, Fig. 10 (a) - (d) shows the power loss distribution among different switches of the basic unit of the proposed topology. The power loss of switches of complementary switch pair have same value due to same number of turn ON and OFF over a fundamental period.

VI. RESULTS AND DISCUSSION

The basic unit of the proposed topology has been simulated and the simulation results have been verified using the experimental results. In this section, both simulation and experimental results are discussed.

A. SIMULATION RESULTS

The basic unit of the proposed topology has been simulated using PLECS software. For simulation, the V_{dc} is selected as 50V. This results in the magnitude of three input dc voltage sources as 50V, 100V and 150V. The resultant 13 level output voltage has a peak voltage of 300V with a step voltage magnitude of 50V.

Fig. 11 (a) shows the waveforms of output voltage and current of a series connected resistive-inductive load of

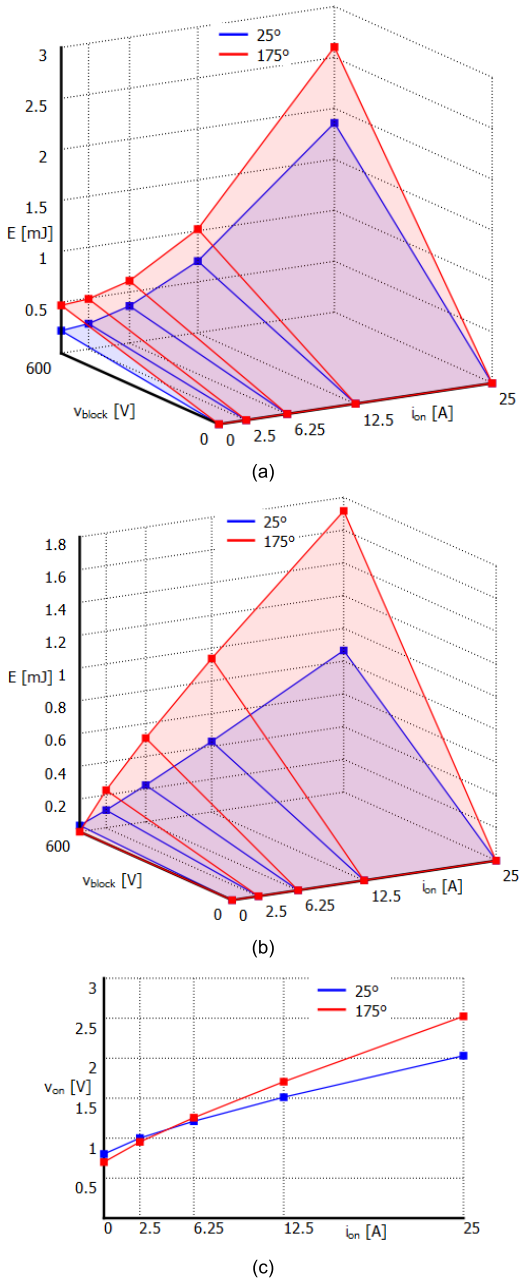

FIGURE 8. Loss model for (a) turn ON losses, (b) turn OFF losses, and (c) conduction losses for IGBT IKW25N120H3 up to 25A, [E = Energy loss (mJ), V_{block} = OFF state blocking voltage (V), i_{on} = ON state current (A), and V_{on} = ON state voltage drop (V)].

Z = 10Ω+ 100mH with a change of modulation index. The different dynamic and steady state response of the output voltage and current waveforms are also depicted in Fig. 11 (a). The harmonic spectrum of the output voltage and current has been depicted in Fig. 11 (b). The THD of voltage and current has a value of 6.3% and 0.35% respectively. Furthermore, a step change of load type from purely resistive load i.e., Z = 50 Ω to a series connected RL load with Z = 50Ω+ 100 mH has been also been depicted in Fig. 11 (c).

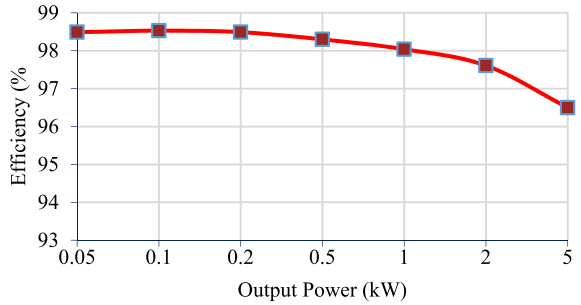

FIGURE 9. Efficiency vs output power curve of the basic unit of the proposed topology.

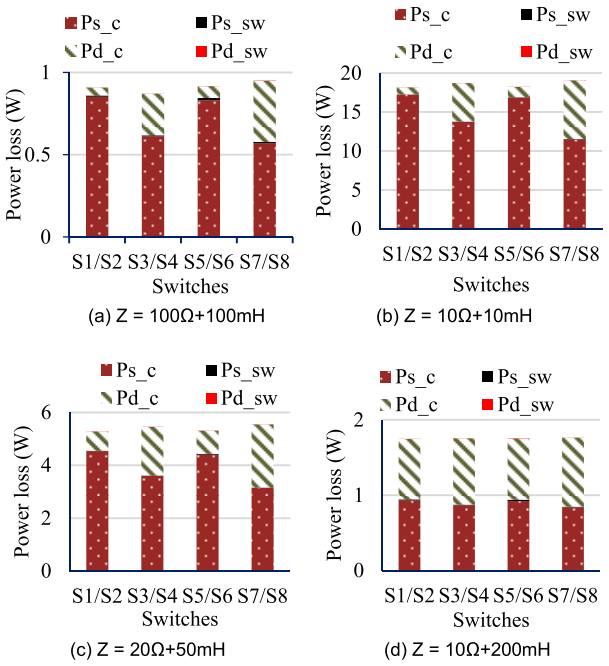

FIGURE 10. Power loss distribution of different switches with different loading conditions [Ps_c, Ps_sw, Pd_c, and Pd_sw represents conduction losses of switch, switching losses of switch, conduction losses of diode, and switching losses of diode respectively.].

B. EXPERIMENTAL RESULTS

The performance of the proposed topology has been verified by developing a laboratory prototype to verify simulation results and is shown in Fig. 12. In the experimental setup, Toshiba IGBT GT50J325 is used as a power switch and dSPACE 1104 controller is used for gate pulse generation for different switches. Nearest level control (NLC) pulse width modulation technique is used due to its ease of implementation.

For the hardware results, the step voltage, i.e., V_{dc} has been selected as 40V. Therefore, the magnitude of dc voltage source used in the basic unit are of 40V, 80V and 120V. This results in a staircase output voltage of 13 levels having a peak voltage of 240V as shown in Fig. 13 (a). Fig. 13 (a) also shows the output voltage and output current when a resistive load of 100Ω is connected at the load. The current waveform will resemble the voltage with different peak. The THD value

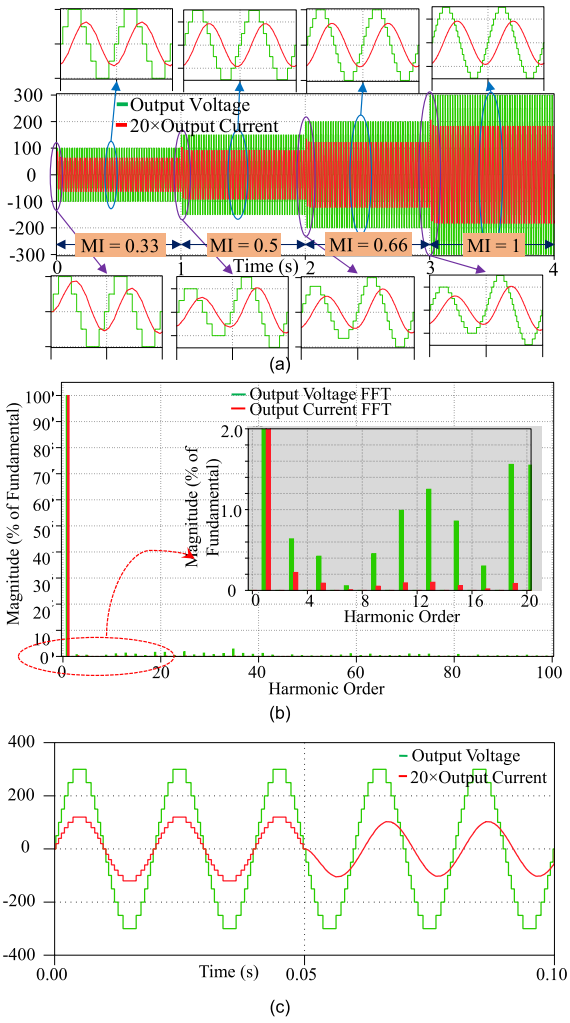

FIGURE 11. Simulation results with (a) dynamic change of modulation index (b) FFT of 13 level output voltage and current with Z=10Ω+100mH and (c) output voltage and current waveforms with change of load from Z=50Ω to Z=50Ω+100mH.

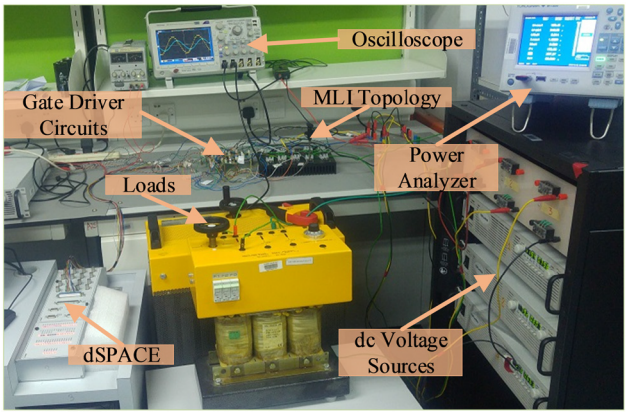

FIGURE 12. Experimental setup.

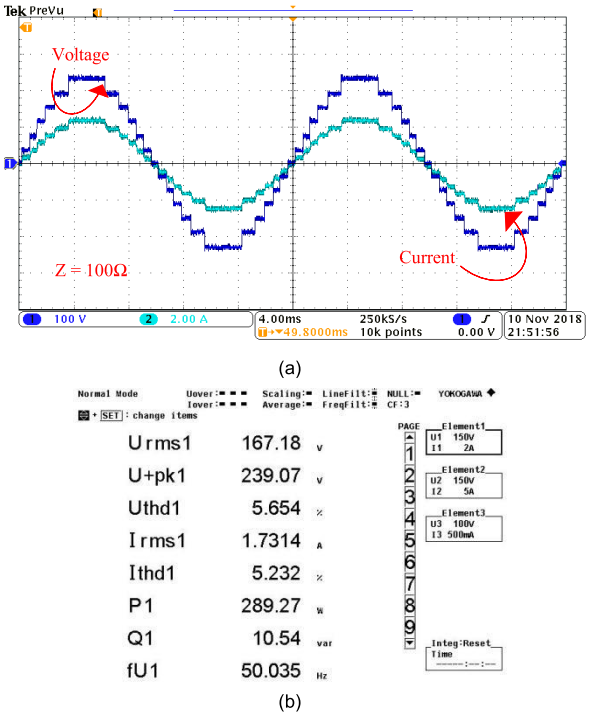

FIGURE 13. Experimental results. (a) voltage and current waveform. and (b) different parameters at the output with resistive load.

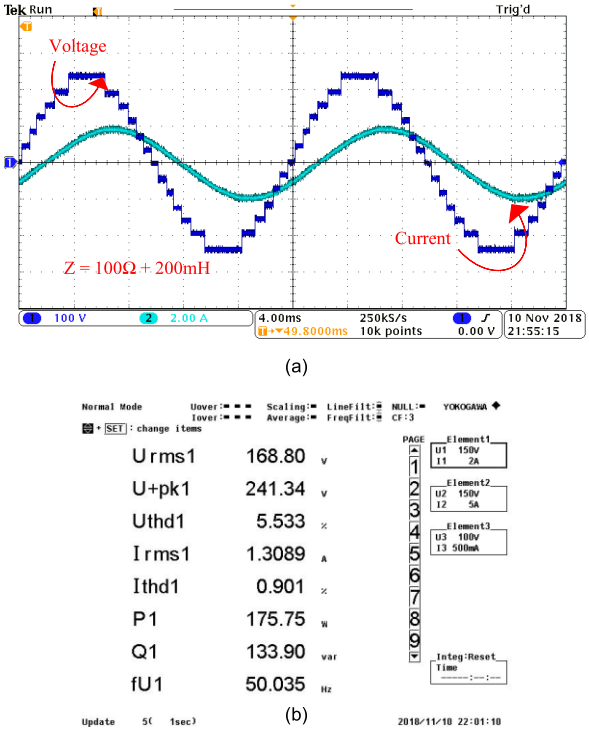

FIGURE 14. Experimental results. (a) voltage and current waveform. and (b) different parameters at the output with resistive-inductive load.

of the output voltage has a value of 5.65%. The different parameter of the output voltage and current have been shown in Fig. 13 (b). Similarly, Fig, 14 (a) and (b) the output voltage with current waveform and output parameters with a series connected resistive-inductive load with Z = 100Ω+ 200mH, respectively.

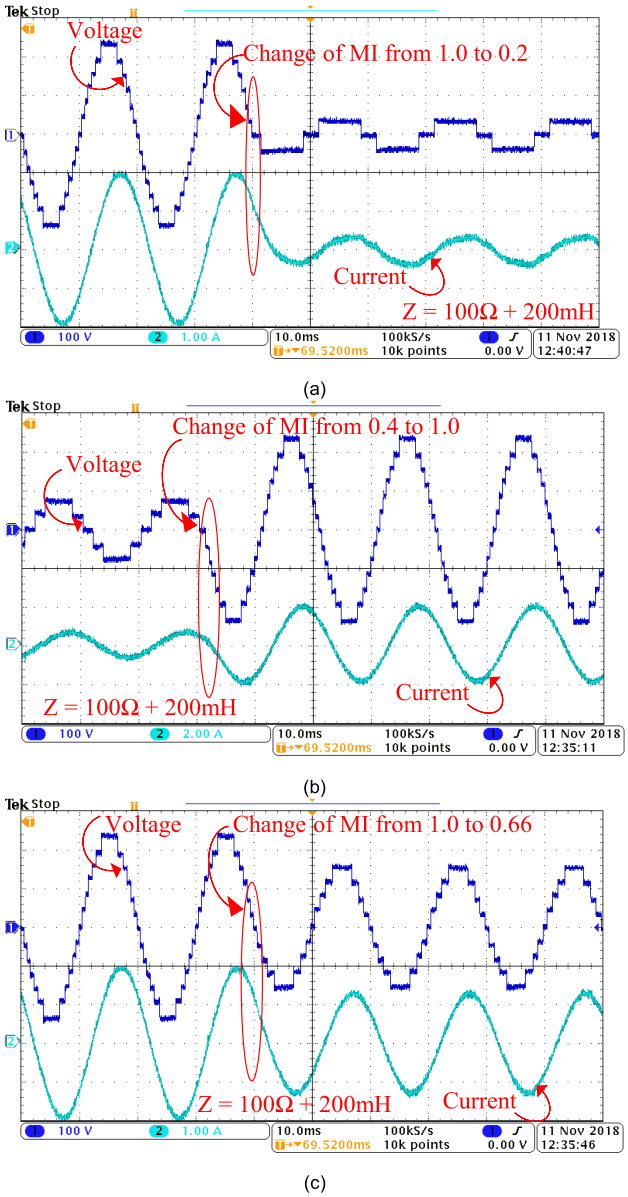

FIGURE 15. Experimental results of basic unit after changing MI values from. (a) 1.0 to 0.2 (b) 0.4 to 1.0. and (c) 1.0 to 0.66.

The circuit is also listed for dynamic change in modulation index as shown in Fig. 15 while it is increases from (1.0-0.2) in Fig.15 (a), (0.4 to 1.0) It decreases from and (1.0-0.66) in Fig.15 (b) and Fig. 15 (c), respectively. Although the number of levels were decreased when decreasing the modulation index, the dynamic performance did not deteriorate. Similarly, increasing the modulation index also have no effect on the dynamic performance of the output voltage. A high concordance is obtained between simulation and experimental results. The harmonic distortion obtained in experimental results is near about same as obtained in simulation as seen by comparing the results of Fig. 15 and Fig. 11 (a). Moreover, results obtained for varying modulation index in both simulation and hardware results are also showing a good performance in both hardware and simulation results.

VII. CONCLUSION

The paper presents a novel MLI topology with multiple extension capabilities. The basic unit of the proposed topology produces 13 levels using eight unidirectional switches and three dc voltage sources. Three different extension of the basic unit has been proposed. The performance analysis of the basic unit of the proposed topology has been done and the comparative results with some recently proposed topologies in literature have been presented in the paper. Further, a power loss analysis of the dynamic losses (switching and conduction) in the MLI has also been presented, which gives the maximum efficicnecy of the basic unit as 98.5%. The power loss distribution in all the switches for different combination of loads have also been demonstrated in the paper. The performance of the proposed topology has been simulated with dynamic modulation indexes and different combination of loads using PLECS sorftware. A prototype of the basic unit has been developed in the laboratory and the simulation results have been validated using the different expriemntal results considering different modulation indexes.

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