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High-Efficiency Single-Input Triple-Outputs DC-DC Converter With Zero-Current Switching

RONG-JONG WAI, (Senior Member, IEEE), AND ZHI-FU ZHANG
Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan
Corresponding author: Rong-Jong Wai (rjwai@mail.ntust.edu.tw)

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ABSTRACT This study mainly develops a high-efficiency single-input triple-outputs dc/dc converter (HSTDC) with a soft-switching technique for high step-up applications. In general, multiple output voltages with only one single input power source is always required for the applications of renewable energy or electric vehicles. At the high step-up operation, the proposed HSTDC has a high voltage conversion ratio to sustain the high-voltage dc bus for the utilization of dc/ac inverter. The proposed HSTDC uses a coupled inductor with lower turn ratios to achieve the high step-up voltage gain and adopts an auxiliary inductor to adjust the voltage of the auxiliary output terminal indirectly. Moreover, the utilization of voltage clamping and zero-current switching (ZCS) in the proposed HSTDC is helpful for accomplishing the goal of high-efficiency power conversion and three output voltage levels. In addition, the effectiveness of the proposed HSTDC is verified by rich experimental results.

INDEX TERMS High-efficiency power conversion, single-input multiple-outputs dc/dc converter, high step-up, coupled inductor, voltage clamping, zero-current switching (ZCS).

I. INTRODUCTION

Multiple-output dc/dc converters have been widely used in many applications, such as hybrid electric vehicles, space crafts, uninterruptible power systems, and so on [1]–[5]. By dealing with the issue of global warning, clean energies, such as fuel cell, photovoltaic, and wind energy, etc., have been rapidly promoted [6]–[8]. For the improvement of the global environmental issue and lack of natural energy, the evolution of electric vehicles with renewable energy as a replacement for the fossil-fuel vehicle has rapidly developed [9]. In order to achieve high voltage-gain applications with a low-voltage power source, the coupled-inductor-based converters in [10]–[14] were investigated in recent years. The requirement of high step-up converter with high-efficiency power conversion, a smaller volume, and a lower manufacturing cost has been increasing in the last decade [10], [15]–[17]. Although a 1kW experimental prototype with a lower input-current ripple for a grid-connected photovoltaic system was designed in [10], it absolutely increased the manufacturing cost and the circuit volume by using two coupled inductors. In spite of an ultra-step-up converter was presented for the high-efficiency application in [11], the corresponding capacitor with a high voltage rating was selected to ensure the safety operation. In [12], the converter was designed with the interleaving technique for achieving a high output voltage 900V. But, the unbalance problem for dividing voltages on series capacitors should be further solved. Although the switched capacitors in [15] were used for obtaining a small and light-weight converter, a large amount of diodes and capacitors were required in this topology. Moreover, a high-efficiency single-input multiple-output converter [17] was presented with the property of zero-current switching (ZCS). But, the clamped capacitor with a higher capacitor value in [17] should be chosen for high power applications. While the utilization of soft switching techniques to minimize switching losses was demonstrated in [18], larger coupled losses and leakages could be produced by the selection of higher turns ratios in a current-fed converter. In addition, the conventional inductor-based boost converters for high voltage-ratios applications are not sufficient to step up the input voltage source because of high switching losses and high voltages across power switches. As a result, power switches with lower turned-on resistors for decreasing conduction losses and voltage stresses are required. Although a 2kW experimental prototype in [19] was built with the property of high-efficiency power conversion, numerous windings for a coupled inductor and power diodes were used

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for only one output terminal. Chen *et al.* [20] designed a CLLC resonant tank to minimize the corresponding switching losses. However, the values of capacitors and inductors should be strictly considered for promising all switches to work with the soft-switching characteristic, and an external control system is required to guarantee the operation stability. Besides, complicated control stages were required for performing precise response behavior in [21]. Even though the properties of coupled-inductor-based converters and soft-switching technique presented in [9]–[21] could be a significant progress, more power switches and passive components are always required so that the corresponding cost and volume will be inevitably increased. For the requirement of single-input multiple-output (SIMO) operation, the design of an auxiliary inductor could be used for dc/dc converters [14], [17], [22], [23]. Although Wang *et al.* [24], [25] and Zheng *et al.* [26] presented multiple-output converters with simple frameworks, complicated control schemes were required for ensuring system stabilization. Wai *et al.* [23] introduced a SIMO dc/dc converter with bidirectional current flow and soft switching behaviors for the high-efficiency power conversion. But, the circuit components in [23] including three power switches, one coupled inductor, two inductors, four diodes, and five capacitors will result in a higher manufacturing cost and a larger volume. Yu *et al.* [27] proposed a high-efficiency bidirectional dc/dc converter constructed by a coupled inductor with the interleaved topology. Although the topology in [27] can achieve high-efficiency power conversion, many battery modules were connected in series to form a high voltage bus because of a low voltage gain. Moreover, the mega-watt level topology was demonstrated in [28] with multilevel outputs and bidirectional operation for a wide power range. Although the topology in [28] was utilized for ultra-high power applications, it had enormous control architecture for supporting the system stabilization, and the hard-switching operation will degenerate the power conversion efficiency. In addition, a high step-up dc/dc converter with the property of high-efficiency power conversion and wide operational range was constructed in [29] with low input-current ripple for renewable energy applications. Because an additional magnetizing inductor should be used for transferring the energy in [29], the corresponding volume will be increased. Ray *et al.* [30] proposed an integrated dual-output converter with synchronous switches for decreasing conduction losses. However, two duty cycles for power switches to be carefully designed will restrict the output voltage range. For decreasing the manufacturing cost of traditional single-input dual-output (SIDO) converters, Chen *et al.* [31] presented a SIDO Ćuk converter. Although the zero-voltage switching (ZVS) technique is designed over a wide load range, the negative output voltage to be considered will complicate the system at the issue of common ground situation. Although Ganjavi *et al.* [32] investigated a simple structure with medium and high output voltages, four power switches were required to increase the manufacturing cost and the converter volume at a low power application.

For accomplishing the objectives of high-efficiency power conversion, low manufacturing cost and multiple output terminals, a high-efficiency single-input triple-outputs dc/dc converter (HSTDC) topology is designed in this study, and an experimental prototype is built to validate the corresponding theoretical analyses. This study is organized into five sections. Following the introduction, the operation principle and steady-state analyses of the proposed HSTDC are presented in Section II. In Section III, the circuit design considerations and the components selection guideline of the proposed converter are explained in detail. In Section IV, experimental results are provided to validate the effectiveness of the proposed converter, and performance comparisons with other converters in previous researches are given to show the superiority of the proposed HSTDC. Finally, conclusions are drawn in Section V.

II. OPERATION PRINCIPLE AND STEADY-STATE ANALYSES

The system configuration for the proposed high-efficiency single-input triple-outputs dc/dc converter (HSTDC) topology is depicted in Fig. 1. The major symbol representations are expressed as follows. In Fig. 1., the low-voltage-side circuit (LVSC) is composed of the low-voltage switch (S_1), the primary-side winding (L_p) of the coupled inductor (T_r), and the low-voltage input terminal (V_{Low}). By turning the low-voltage switch (S_1) on/off to draw/release energy to the secondary-side winding (L_s) of the coupled inductor (T_r). Then, the clamped circuit is composed of the clamped diode (D_1), the clamped capacitor (C_1), the middle-voltage filter capacitor (C_{O3}), and the middle-voltage output terminal (V_{O3}). It mainly absorbs the energy stored in the primary-side leakage inductor (L_k) for protecting the low-voltage switch (S_1) and releasing energy to the middle-voltage capacitor (C_2) and the middle-voltage output terminal (V_{O3}). Moreover, the middle-voltage balanced circuit has the middle-voltage capacitor (C_2), the middle-voltage balanced diode (D_2), and the secondary-side winding (L_s) of the coupled inductor (T_r). It mainly absorbs energy stored in the clamped capacitor (C_1) and the middle-voltage filter capacitor (C_{O3}) for boosting

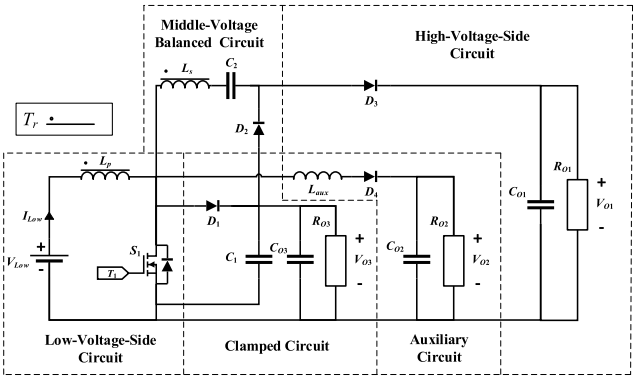

FIGURE 1. System configuration of high-efficiency single-input triple-outputs dc/dc converter.

the voltage conversion ratios and releasing energy to the high-voltage dc bus terminal (V_{O1}). In addition, the high-voltage-side circuit (HVSC) has the high-voltage diode (D_3), the high-voltage filter capacitor (C_{O1}), and the high-voltage dc bus terminal (V_{O1}). It mainly releases energy to the high-voltage dc bus terminal (V_{O1}) through the high-voltage diode (D_3). Furthermore, the auxiliary circuit contains the auxiliary inductor (L_{aux}), the auxiliary diode (D_4), the auxiliary source filter capacitor (C_{O2}), and the auxiliary source output terminal (V_{O2}). It can charge the auxiliary source for peripheral components usage. V_{Low} (I_{Low}) denotes the voltage (current) of the input power source at the LVSC. R_{O1}, R_{O2}, and R_{O3} express the equivalent loads for the high-voltage dc bus terminal (V_{O1}), the auxiliary source output terminal (V_{O2}), and the middle-voltage output terminal (V_{O3}), respectively. T_1 is the driving signal for the low-voltage switch (S_1).

The proposed HSTDC has three output ports with different voltage levels, and only one low-voltage input port. In this study, the output terminals are defined as the high-voltage dc bus (V_{O1}), the auxiliary source (V_{O2}), and the middle-voltage output terminal (V_{O3}), respectively. In order to simplify the description for the output powers of the proposed HSTDC, individual output powers can be denoted as $P_{O1} = V_{O1}^2/R_{O1}$ for the high-voltage dc bus terminal, $P_{O2} = V_{O2}^2/R_{O2}$ for the auxiliary source terminal, and $P_{O3} = V_{O3}^2/R_{O3}$ for the middle-voltage output terminal, respectively. Moreover, the total output power can be expressed as $P_{O1} + P_{O2} + P_{O3} = P_{OT}$.

The proposed HSTDC has two essential characteristics for boosting input voltage and generating different voltage levels. To simplify the mathematic derivations, all of the voltages across a power switch and diodes are ignored. Moreover, it is assumed that the clamped capacitor (C_1) and the middle-voltage capacitor (C_2) are large enough to be considered as constant voltage sources V_{C1} and V_{C2}, respectively. The equivalent circuit, voltage definition, and current definition are illustrated in Fig. 2. For describing the operational modes more clearly, the characteristic waveforms and the operation principle of the proposed HSTDC are depicted in Figs. 3 and 4, respectively.

Figure 2 shows the equivalent circuit of the proposed HSTDC, and the operation of the proposed HSTDC is

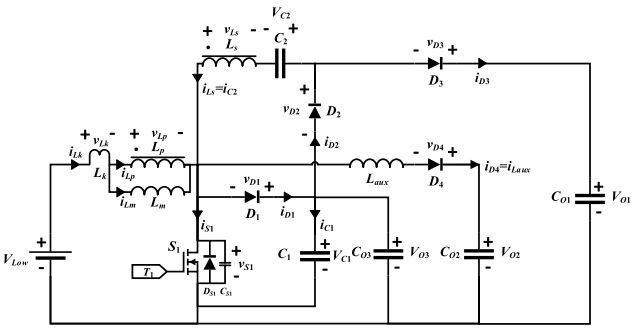

FIGURE 2. Equivalent circuit of HSTDC.

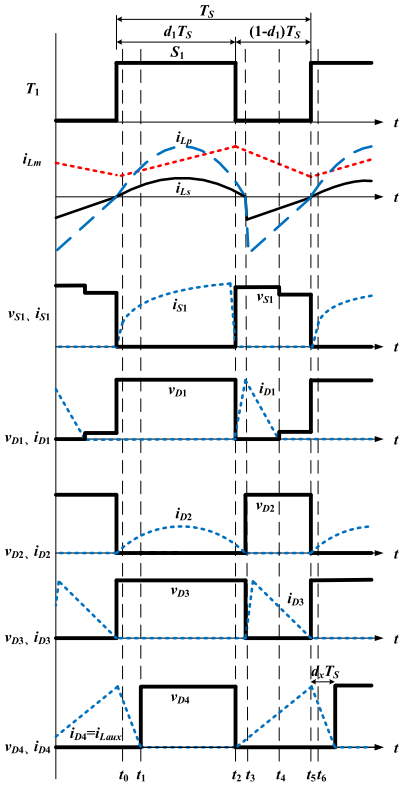

FIGURE 3. Characteristic waveforms of HSTDC.

explained as follows. The equivalent circuit of the coupled inductor (T_r) are composed of the primary-side winding (L_p), the secondary-side winding (L_s), the primary-side magnetizing inductor (L_m), and the primary-side leakage inductor (L_k). By defining the turns ratio (N) to be equal N_s/N_p and labeling the voltage of v_{Lp} and v_{Ls} across the windings L_p and L_s, the turns ratio (N) can be represented as

$$v_{Ls}/v_{Lp} = N \tag{1}$$

Moreover, the coupling coefficient of the coupled inductor (T_r) can be expressed as

$$k = L_m/(L_k + L_m) \tag{2}$$

In Fig. 2, C_{S1} and D_{S1} are the intrinsic capacitance and the body diode of the power switch. In order to simplify theoretical analyses, the power switch and diodes in the proposed converter are considered as ideal components.

Figures 3 and 4 show the characteristic waveforms and the operation principle of the proposed HSTDC. The power flow forwards from the LVSC to the HVSC, the auxiliary circuit, and the clamped circuit, respectively, and one describes the operational modes via the equivalent circuit in Fig. 2. The switch (S_1) is served as the main switch and is controlled for regulating the voltages of the HVSC and the middle-voltage output terminal. Moreover, the diodes (D_1, D_2, D_3, and D_4) are conducted when the voltages of anodes are higher than the voltages of cathodes. The diodes (D_2 and D_3) are conducted complementarily when the switch (S_1) is turned on/off.

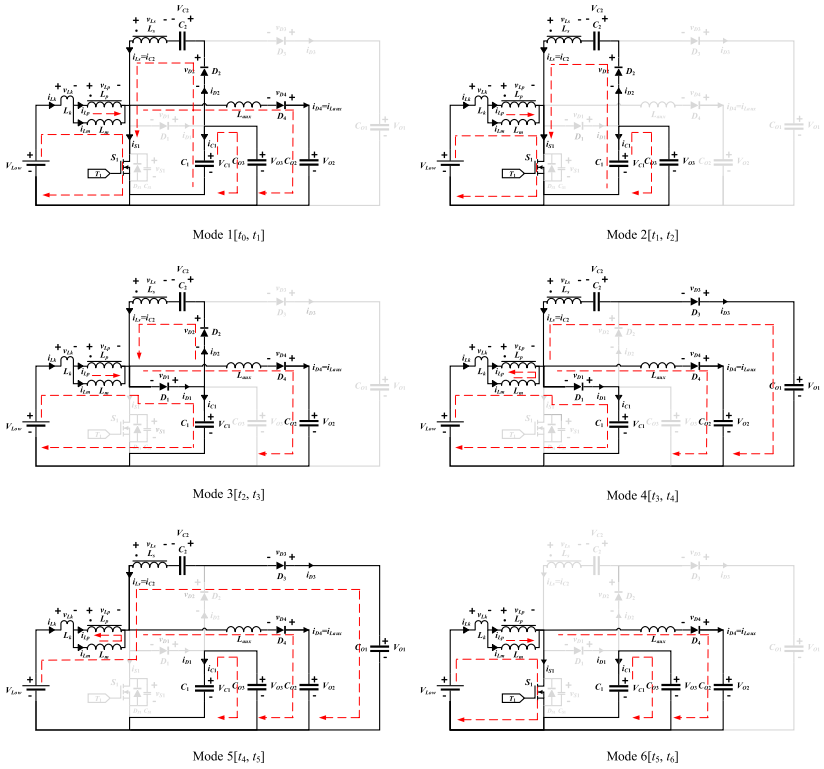

FIGURE 4. Operation principle of HSTDC.

The duty cycle of the power switch (S_1) is defined as d_1, and one switching cycle is denoted as T_S.

1) *Mode 1* [$t_0 \sim t_1$]*:* At the beginning of this mode, the low-voltage switch (S_1) is turned on, and the high-voltage diode (D_3) is reversed bias. The input current magnetizes the primary-side magnetizing inductor (L_m) from the low-voltage input source (V_{Low}). The partial energy of the LVSC transfers to the secondary-side winding (L_s) via magnetic coupling; the energy stored in the clamped capacitor (C_1) transfers to the middle-voltage capacitor (C_2) through the middle-voltage balanced diode (D_2), and the partial energy of the clamped capacitor (C_1) also releases to the middle-voltage output terminal (V_{O3}) simultaneously. Moreover, the energy stored in the auxiliary inductor (L_{aux}) still needs to release energy for charging the auxiliary source continuously. When the current (i_{Laux}) gradually decays to zero, this mode ends.
2) *Mode 2* [$t_1 \sim t_2$]*:* At time $t = t_1$, the current (i_{Laux}) has dropped to zero at mode 2. Except for the path from the auxiliary inductor to the auxiliary source, other operation is similar to the one at mode 1. The low-voltage input source (V_{Low}) magnetizes the primary-side magnetizing inductor (L_m) continuously, and the partial energy of the LVSC still transfers to the secondary-side winding (L_s) via magnetic coupling. The middle-voltage balanced diode (D_2) is conducted to transmit energy into the middle-voltage capacitor (C_2). The energy stored in the clamped capacitor (C_1) releases to the middle-voltage output terminal (V_{O3}) continuously. During modes 1 and 2, the voltage relationship can be expressed as

$$V_{Low} = v_{Lp} + v_{Lk} \tag{3}$$

Because the voltage (v_{Lk}) is equal to $v_{Lk} = v_{Lp}(1-k)/k$, (3) can be rearranged as

$$V_{Low} = v_{Lp}/k \tag{4}$$

Since the voltage across the primary-side magnetizing inductor (L_m) is equal to v_{Lp}, one can obtain

$$v_{Lp} = kV_{Low} \tag{5}$$

According to (5) and $v_{Ls} = Nv_{Lp}$, the voltage across the middle-voltage capacitor can be expressed as

$$V_{C2} = kNV_{Low} + V_{C1} \tag{6}$$

3) *Mode 3* [$t_2 \sim t_3$]*:* At time $t = t_2$, the low-voltage switch (S_1) is turned off. The energy stored in the leakage inductor (L_k) still needs to release energy, the current direction could not be changed immediately. As a result, the clamped diode (D_1) is conducted, and the corresponding energy is absorbed by the clamped capacitor (C_1). The partial energy stored in the leakage inductor (L_k) is delivered to the auxiliary circuit for charging the auxiliary source (V_{O2}) via the L_{aux}-D_4-V_{Low} path. The partial energy stored in the secondary-side winding (L_s) still needs to release

energy to the middle-voltage capacitor (C_2) via the D_1-D_2 path. When the secondary-side current (i_{Ls}) decays to zero and the middle-voltage balanced diode (D_2) is reversed bias, this mode ends.

4) *Mode 4* [$t_3 \sim t_4$]*:* At the beginning of this mode, the energy stored in the primary-side magnetizing inductor (L_m) by way of the flyback energy behavior is transferred to the secondary-side winding (L_s), and the high-voltage diode (D_3) is forward bias to transmit the energy to the HVSC via the V_{Low} - L_p - L_s - C_2 path. The leakage inductor (L_k) still needs to release energy to the clamped capacitor (C_1), the middle-voltage output terminal (V_{O3}), and the auxiliary source (V_{O2}) continuously. At this mode, the voltages across L_p and L_s can be given by

$$v_{Lp} = k(V_{Low} - V_{C1}) \tag{7}$$
$$v_{Ls} = Nv_{Lp} \tag{8}$$

5) *Mode 5* [$t_4 \sim t_5$]*:* At time $t = t_4$, the energy stored in the leakage inductor (L_k) has dropped to zero, and the clamped diode (D_1) is reversed bias because the voltage (V_{C1}) is higher than the voltage across the low-voltage switch (v_{S1}). The situation of the HVSC is the same as the one at mode 4 for delivering the energy to the high-voltage dc bus (V_{O1}) via the high-voltage diode (D_3). Moreover, the low-voltage input source (V_{Low}) and the partial energy of the primary-side magnetizing inductor (L_m) transmit to the auxiliary source (V_{O2}) through the auxiliary diode (D_4). In addition, the clamped capacitor (C_1) begins to release energy to the middle-voltage output terminal (V_{O3}) directly. When the secondary-side current (i_{Ls}) converts to zero, this mode ends.

6) *Mode 6* [$t_5 \sim t_6$]*:* At the beginning of this mode, the low-voltage switch (S_1) is turned on, and the energy stored in the auxiliary inductor (L_{aux}) still needs to release to the auxiliary source (V_{O2}) via the auxiliary diode (D_4). The situation of the clamped capacitor (C_1) is the same as the one at mode 5 to transmit the energy to the middle-voltage output terminal (V_{O3}). The current ascendant slope of i_{Lk} is limited by the leakage inductor (L_k), and no current is available in the HVSC, the middle-voltage balanced circuit, and the clamped circuit. As a result, the low-voltage switch (S_1) is turned on under the condition of zero-current switching (ZCS) to alleviate the switching loss. Moreover, the current in the high-voltage diode (i_{D3}) decays to zero, and the current direction of the secondary-side winding (i_{Ls}) changes to conduct the middle-voltage balanced diode (D_2). After that, the primary-side magnetizing inductor (L_m) will be magnetized again by the low-voltage input source (V_{Low}), and one switching cycle is completed.

Due to the coupled inductor with a good coupling effect, the leakage energy is much smaller than the energy of a ferrites powder core. Because the proposed circuit topology has excellent voltage clamping property, the leakage energy can be fully absorbed. For simplifying mathematical derivations, the coupling coefficient is assumed to be $k = 1$. To derive the voltage gains of the proposed HSTDC, the voltages of V_{C1} and V_{C2} should be obtained in advance. Applying the principle of the volt-second balance [33] for the primary-side magnetizing inductor (L_m) and the secondary-side winding (L_s) can obtain

$$V_{Low}d_1T_S + (V_{Low} - V_{C1})(1 - d_1)T_S = 0 \tag{9}$$
$$(V_{C2} - V_{C1})d_1T_S + N\left(\frac{V_{Low} - V_{O1} + V_{C2}}{N+1}\right)(1 - d_1)T_S = 0 \tag{10}$$

According to (9) and (10), the voltages of V_{C1} and V_{C2} can be calculated as

$$V_{C1} = \frac{V_{Low}}{1 - d_1} \tag{11}$$
$$V_{C2} = NV_{Low} + V_{C1} = \frac{1 + N(1 - d_1)}{1 - d_1}V_{Low} \tag{12}$$

At modes 3 and 4, the voltage across the primary-side magnetizing inductor (L_m) and the voltage of the high-voltage dc bus (V_{O1}) can be respectively expressed as

$$v_{Lm} = V_{Low} - V_{C1} = -V_{Low}[d_1/(1 - d_1)] \tag{13}$$
$$V_{O1} = V_{Low} - V_{Lp} - V_{Ls} + V_{C2} \tag{14}$$

By substituting (6) and (7) into (14), and using the voltage relation of $v_{Ls} = Nv_{Lp}$, the voltage gain (G_{V1}) of the proposed HSTDC from the LVSC to the HVSC can be represented as

$$G_{V1} = \frac{V_{O1}}{V_{Low}} = \frac{N + 2}{1 - d_1} \tag{15}$$

Moreover, the clamped diode (D_1) is conducted to transmit the energy to the clamped capacitor (C_1) at mode 4, and the clamped capacitor (C_1) has released energy to the middle-voltage output terminal (V_{O3}) at mode 5. As a result, the middle-voltage output terminal (V_{O3}) can be represented as

$$V_{O3} = V_{C1} = \frac{V_{Low}}{1 - d_1} \tag{16}$$

According to (16), the voltage gain (G_{V3}) of the proposed HSTDC from the LVSC to the middle-voltage output terminal (V_{O3}) can be calculated as

$$G_{V3} = \frac{V_{O3}}{V_{Low}} = \frac{1}{1 - d_1} \tag{17}$$

For calculating the discharge time of the auxiliary inductor between modes 1 and 6, the time interval can be denoted as $d_xT_s = [(t_6 - t_5) + (t_1 - t_0)]$. By using the volt-second balance theorem [33], the average voltage of the auxiliary inductor (L_{aux}) should be equal to zero during one complete switching cycle (T_S), and one can obtain

$$(V_{Low} - v_{Lm} - V_{O2})(1 - d_1)T_S + (-V_{O2})d_xT_S = 0 \tag{18}$$

By substituting (13) into (18), the auxiliary voltage gain (G_{V2}) of the proposed HSTDC from the LVSC to the auxiliary source (V_{O2}) can be expressed as

$$G_{V2} = \frac{V_{O2}}{V_{Low}} = \frac{1}{1 - d_1 + d_x} \tag{19}$$

Then, the average current ($i_{D4(\text{avg})}$) of the auxiliary diode (D_4) can be represented as

$$i_{D4(\text{avg})} = \frac{1}{T_S}[\frac{1}{2} i_{Laux(\max)}(1 - d_1)T_S + \frac{1}{2} i_{Laux(\max)} d_x T_S] \tag{20}$$

where the maximum current ($i_{Laux(\max)}$) of the auxiliary inductor (L_{aux}) can be expressed as

$$i_{Laux(\max)} = (V_{O2}/L_{aux}) d_x T_S \tag{21}$$

By substituting (21) into (20), the average current ($i_{D4(\text{avg})}$) of the auxiliary diode (D_4) can be calculated as

$$i_{D4(\text{avg})} = \frac{V_{O2} d_x T_S}{2L_{aux}}(1 - d_1 + d_x) \tag{22}$$

By assuming that the average current ($i_{D4(\text{avg})}$) is equal to the auxiliary source current, one can obtain

$$i_{D4(\text{avg})} = (V_{O2}/R_{O2}) \tag{23}$$

where R_{O2} is the equivalent load at the auxiliary circuit. From (22) and (23), the duty cycle (d_x) can be given by

$$d_x = \frac{-(1 - d_1) + \sqrt{(1 - d_1)^2 + [8L_{aux}/(R_{O2}T_S)]}}{2} \tag{24}$$

By substituting (24) into (19), the voltage gain (G_{V2}) of the proposed HSTDC from the LVSC to the auxiliary source (V_{O2}) can be rearranged as

$$G_{V2} = \frac{V_{O2}}{V_{Low}} = \frac{2}{(1 - d_1) + \sqrt{(1 - d_1)^2 + [8L_{aux}/(R_{O2}T_S)]}} \tag{25}$$

III. DESIGN GUIDELINE OF CIRCUIT COMPONENTS

In this study, the proposed high-efficiency single-input triple-outputs dc/dc converter (HSTDC) is assumed to be operated with one input power source 12V±10% and has three different voltage levels for three specific utilizations. For this case, a 12V power supply is utilized for the low-voltage input source in the low-voltage-side circuit (LVSC). Moreover, the output terminals have three different voltage levels, including the high-voltage dc bus 200V, the middle voltage 40V, and the auxiliary source voltage 25V $\sim$ 30V. To demonstrate the proposed HSTDC in practical applications, the maximum power at the high-voltage-side circuit (HVSC) is set at 800W (i.e., the equivalent load $R_{O1} = 50\Omega$); the maximum power at the auxiliary circuit is set at 100W (i.e., the equivalent load $R_{O2} = 6.25\Omega$), and the maximum power at the middle-voltage output terminal is also set at 100W (i.e., the equivalent load $R_{O3} = 16\Omega$) for validating the experimental prototype. In addition, this converter is operated with a 50kHz switching frequency ($f_S = 50\text{kHz}$),

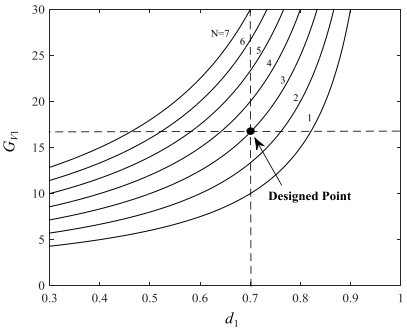

FIGURE 5. Voltage gain G_{V1} with respect to duty cycle d_1 under different turns ratios N.

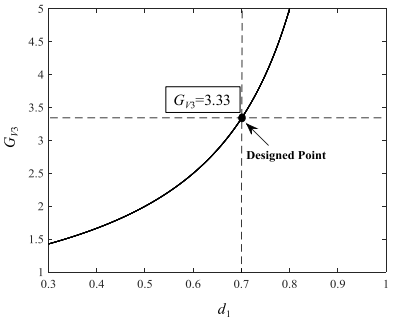

FIGURE 6. Voltage gain G_{V3} with respect to duty cycle d_1.

and the coupling coefficient could be simplified as $k = 1$ because the proposed topology has a good voltage-clamping performance.

The voltage gain (G_{V1}) from the LVSC to the HVSC in (15) with respect to the duty cycle (d_1) under different turns ratios (N) is depicted in Fig. 5. Moreover, the voltage gain (G_{V3}) from the LVSC to the middle-voltage output terminal in (16) with respect to the duty cycle (d_1) is depicted in Fig. 6. According to Figs. 5 and 6, the turns ratios of the coupled inductor (T_r) and the duty cycle (d_1) for the power switch (S_1) can be determined. By considering the voltages $V_{O1} = 200V$ and $V_{O3} = 40V$, the voltage gain $G_{V1} = 16.67$ and the voltage gain $G_{V3} = 3.33$ can be respectively obtained because of the input low-voltage source $V_{Low} = 12V$. By substituting the voltage gain $G_{V1} = 16.67$ into Fig. 5, and considering $V_{Low} = 12V$ and $N = 3$, the duty cycle (d_1) for the power switch (S_1) is 0.7. By substituting the voltage gain $G_{V3} = 3.33$ into Fig. 6, and considering the input voltage source $V_{Low} = 12V$, the duty cycle (d_1) of the power switch (S_1) is also 0.7. Basically, the value of $d_1 = 0.7$ is exactly obtained from the calculation results of G_{V1} and G_{V3}, and is reasonable for the proposed HSTDC in practical applications.

The voltage gain (G_{V2}) in (25) and the auxiliary source power (P_{O2}) with respect to the auxiliary inductors (L_{aux}) at the duty cycle $d_1 = 0.7$ under different values of R_{O2} are depicted in Fig. 7(a) and (b), respectively. By considering the range of $V_{O2} = 25V \sim 30V$ (i.e., the minimum value of V_{O2} is set 25V), the minimum voltage gain from the LVSC to the auxiliary source is about $G_{V2} = 2.083$, and the corresponding maximum power is about $P_{O2} = 104W$. As a result, the value

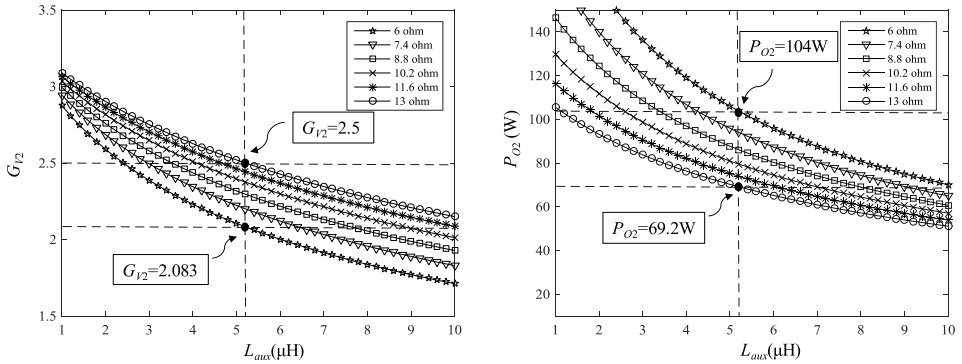

FIGURE 7. Relationship for different values of R_{O2}: (a) G_{V2} with respect to L_{aux}; (b) P_{O2} with respect to L_{aux}.

of the auxiliary inductor (L_{aux}) can be obtained as $L_{aux} = 5.2\mu$H at this specific condition. Moreover, substituting the value of the auxiliary inductor $L_{aux} = 5.2\mu$H into Fig. 7(b), the maximum voltage gain (G_{V2}) and the corresponding power (P_{O2}) are 2.5 and 69.2W, respectively, and the voltage of the auxiliary source is 30V. In order to achieve the preset voltage range of V_{O2}, the value of the auxiliary inductor (L_{aux}) can be selected as $L_{aux} = 5.2\mu$H for the voltage gain range (G_{V2}) during $2.083 \sim 2.5$ and the power range (P_{O2}) during 69.2W $\sim$ 104W. Regardless of the variations of the power (P_{O2}) between 69.2W $\sim$ 104W, it will produce the output voltage range from 25V to 30V for charging the auxiliary source (e.g., battery module). Although the voltage of the auxiliary source (V_{O2}) cannot be regulated freely, the predetermined voltage range by the design of the auxiliary inductor (L_{aux}) is appropriate to provide the floating charge voltage for an energy storage device (e.g., battery module) as the load in the auxiliary circuit. Even though it is easy to realize multiple dc outputs with a coupled-inductor-based converter by adding more transfer windings, the magnetic core of the coupled inductor will be selected carefully to hold up the transferring energy. By regulating the power switch (S_1), the proposed HSTDC with the turns ratio of $N = 3$ can control two output voltages (V_{O1} and V_{O3}), and the compromised choice of the auxiliary inductor $L_{aux} = 5.2\mu$H can manipulate the output voltage (V_{O2}) for the auxiliary source in this study.

In order to select appropriate power switch and diodes, the corresponding voltage and current stresses should be considered. The proposed topology in this study has favorable voltage-clamping performance to absorb the leakage energy for effectively transmitting to output terminals. Therefore, the broken phenomena of the power switch (S_1) because of the voltage spike on the leakage inductor (i.e., L_k) can be prevented by the designed clamped capacitor (C_1). From Fig. 4, the maximum voltage stresses of the power switch (S_1) and the diode (D_2) are $v_{S1} = V_{C1} = V_{Low}/(1-d_1)$ and $v_{D2} = V_{O1} - V_{O3} = V_{Low}(N+1)/(1-d_1)$ at mode 4, respectively; the maximum voltages across the diodes (D_1 and D_3) are $v_{D1} = V_{C1} = V_{Low}/(1-d_1)$ and $v_{D3} = V_{O1} - V_{O3} = V_{Low}(N+1)/(1-d_1)$ at modes 1 and 2, respectively. According to above analyses, the maximum voltage stresses of S_1 and D_1 are $V_{Low}/(1-d_1)$, and the maximum voltages across D_2 and D_3 are $V_{Low}(N+1)/(1-d_1)$. By considering $V_{Low} = 12$V, $N = 3$ and $d_1 = 0.7$, the maximum voltages across circuit components (v_{S1}, v_{D1}) and (v_{D2}, v_{D3}) are 40V and 160V, respectively. If the ringing phenomena caused by stray inductances and the intrinsic capacitances are further considered, the schottky diode with 100V voltage rating for the diode (D_1), and the schottky diodes with 200V voltage rating for the diodes (D_2 and D_3) can be selected.

By analyzing mode 2 in Fig. 4, the relation of $v_{D4} = V_{O2} + [(L_{aux}(di_{D4}/dt)]$ holds, and the diode (D_4) is reversed bias at this time interval. Since no current flow is passed through the diode (D_4), the ascendant slope of this diode current (di_{D4}/dt) is equal to zero. Thus, the relation of $v_{D4} = V_{O2}$ can be obtained. Because the voltage level of the auxiliary source is preset at 25V $\sim$ 30V, and the stray inductances effect is considered, a schottky diode with 100V voltage rating can be selected for the diode (D_4) so that the corresponding reverse-recovery current can be further reduced. For ensuring the proposed HSTDC to be operated at the continuous conduction mode (CCM), the minimum value of the primary-side magnetizing inductor (L_m) inside the coupled inductor (T_r) should be designed as $L_{m(\min)} = d_1^2 V_{Low}/(2f_S I_{Low})$ from mode 3 to mode 5. Moreover, the LVSC to the middle-voltage output terminal is a conventional boost topology, and the minimum value of the primary-side magnetizing inductor (L_m) operated at CCM should be designed as $L_{m(\min)} = V_{Low}d_1T_S/\Delta i_{Lm}$ from mode 1 to mode 2. In addition, it is assumed the maximum current of the high-voltage dc bus $I_{O1(\max)} = 4$A ($V_{O1} = 200$V and $P_{O1(\max)} = 800$W); the maximum current of the auxiliary source $I_{O2(\max)} = 4$A ($V_{O2} = 25$V and $P_{O2(\max)} = 100$W); the maximum current of the middle-voltage output terminal $I_{O3(\max)} = 2.5$A ($V_{O3} = 40$V and $P_{O3(\max)} = 100$W). By considering the maximum total power $P_{OT(\max)} = 1$kW and the input voltage $V_{Low} = 12$V, the average magnetizing inductor

current ($i_{Lm(\text{avg})}$) equal to the input current (I_{Low}) can be approximated as $i_{Lm(\text{avg})} = I_{Low} = 83.3\text{A}$. Thus, the ripple current $\Delta i_{Lm} = 2i_{Lm(\text{avg})} = 166.6\text{A}$ can be obtained when the proposed converter is assumed to be operated at the boundary between the CCM and the DCM (i.e., the minimum magnetizing inductor current $i_{Lm(\min)} = 0\text{A}$). Increasing the switching frequency of a power converter will bring a number of benefits. For example, passive component size can be reduced as the requirements for stored energy decrease, and increasing control loop bandwidths will enhance dynamic performance. In order to lower the conduction loss compared with commonly switching frequency $10 \sim 20\text{kHz}$, a higher switching frequency 50kHz is selected in the proposed converter, and the corresponding switching loss can be alleviated with the property of ZCS feature. By considering the switching frequency ($f_S = 50\text{kHz}$), the input current at the full-load condition (i.e., maximum total power $P_{OT(\max)} = 1\text{kW}$) and the ripple current, the values of $L_{m(\min)} = 0.7\mu\text{H}$ from mode 3 to mode 5 and $L_{m(\min)} = 1\mu\text{H}$ from mode 1 to mode 2 can be calculated. In order to ensure the CCM operation for the proposed converter, the value of $L_m = 1\mu\text{H}$ can be chosen as the primary-side magnetizing inductor of the coupled inductor (T_r). Furthermore, the maximum current of the power switch (S_1) can be represented as $i_{S1(\max)} = i_{Lm(\max)} = i_{Lm(avg)} + 0.5\Delta i_{Lm} = 166.6\text{A}$. Thus, the power MOSFET with the voltage rating 75V and the minimum current stress to be larger than 166.6A for the power switch (S_1) can be selected.

According to the magnetic field principle, the relation of the magnetic motive force (F), the winding turns (N), and the winding current (i) can be represented as $F = Ni$. Moreover, the relation of the magnetic flux (ϕ), the total magnetic resistance (R_T), and the magnetic motive force (F) can be given by

$$\phi = F/R_T = Ni/R_T \tag{26}$$

where the total magnetic resistance (R_T) can be expressed as $R_T = R_g + R_l$, in which R_l is the core magnetic resistance, and R_g is the air magnetic resistance. By the law of conservation of energy, and the electromagnetic principle, the relation of the current (i) and the magnetic flux (ϕ) can be given as

$$V = L(\frac{di}{dt}) = N(\frac{d\phi}{dt}) \tag{27}$$

By comparing (26) and (27), the total magnetic resistance (R_T) can be rearranged as

$$R_T = N^2/L \tag{28}$$

Substituting (28) into (26), the magnetic flux (ϕ) can be given by

$$\phi = Li/N \tag{29}$$

In addition, the magnetic flux density (B) can be expressed as

$$B = \phi/A \tag{30}$$

where A is the cross-section area of the magnetic core. The air magnetic resistance (R_g) can be represented as

$$R_g = l/(u_0 A) \tag{31}$$

where l is the length of the air gap, and u_0 is the air permeability coefficient ($4\pi \times 10^{-7}$). In this study, a ferrite powder core (i.e., EPCOSB66344 EE-55) with the maximum magnetic flux density $B = 390\text{mT}$, the cross-section area $A = 354\text{mm}^2$, and the maximum magnetic flux $\phi = 138\mu\text{weber}$ is selected as the magnetic core of the coupled inductor, and the corresponding air gap is designed as 0.8mm. According to (31), the air magnetic resistance (R_g) can be calculated as $1.8\text{M}\Omega$. Because the value of R_g is much larger than the value of R_l, the relation of $R_T \doteq R_g$ holds. By substituting the primary-side magnetizing inductor (L_m) and the air magnetic resistance (R_g) into (28), the primary-side winding turns (N_p) can be obtained as 1.34 turns. For compromising the winding turns between the theoretical analyses and the practical fabrication, the primary-side winding turns (N_p) can be selected as 2 turns, and the primary-side inductor (L_p) can be designed as $2.23\mu\text{H}$. On the other hand, the secondary-side turns (N_s) can be selected as 6 turns, and the corresponding value of the secondary-side inductor (L_s) can be obtained as $20.1\mu\text{H}$. By substituting the air magnetic resistance (R_g), the maximum power conversion efficiency 95%, and the maximum input current 87.7A into (26), the magnetic flux (ϕ) can be calculated as 97.4μ weber. Because the actual magnetic flux (ϕ) is smaller than the maximum magnetic flux of the adopted EE-55 ferrite powder core, it can promise that the EE-55 core does not enter the magnetic saturation area.

Because V_{C1} and V_{C2} can be approximately considered as constant voltage sources, the maximum allowable voltage variation percentage of the clamped capacitor (C_1) and the middle-voltage capacitor (C_2) are assumed to be 1%. The clamped capacitor (C_1) mainly absorbs the energy stored in the leakage inductor (L_k). It is assumed that the coupling coefficient is equal to 0.98, and the fall time (t_f) of the power switch (S_1) is 260ns. From the relation of $i_{Lk} = v_{Lk} t_f / L_k$ with $v_{Lk} = 12 \times 0.02 = 0.24\text{V}$ and $L_k = 2.23 \times 0.02 = 0.0446\mu\text{H}$, the current ($i_{Lk}$) passed though the leakage inductor (L_k) can be calculated as 1.4A. Moreover, the relations of $C_1 = i_{Lk}(1 - d_1)/(\Delta V_{C1} f_S)$ and $C_2 = I_{O1}(1-d_1)/(\Delta V_{C2} f_S d_1)$ can be obtained from the Gauss' low [33]. According to $I_{O1} = 4\text{A}$, $d_1 = 0.7$, $f_S = 50\text{kHz}$, and 1% voltage variation in (11) and (12), the clamped capacitor (C_1) and the middle-voltage capacitor (C_2) should be larger than $21\mu\text{F}$ and $45.1\mu\text{F}$, respectively. In order to cope with unpredictable effect in practical applications, the practical values of C_1 and C_2 are selected $24\mu\text{F}$ and $51\mu\text{F}$, respectively. The metalized-polyester film capacitors are adopted in this study because they have many distinguishing characteristics, such as low equivalent series resistance, fast dynamic response, and fast charging and discharging. To select the high-voltage filter capacitor (C_{O1}), the auxiliary source filter capacitor (C_{O2}), and the middle-voltage filter capacitor (C_{O3}) for reducing the output ripple voltage, the value of

the capacitors should be exactly designed. By substituting $I_{O1(\max)} = 4\text{A}$ and $I_{O2(\max)} = 4\text{A}$ into $C_{O1} = I_{O1}/(\Delta V_{O1} f_S)$ and $C_{O2} = I_{O2}/(\Delta V_{O2} f_S)$, the values of C_{O1} and C_{O2} should be respectively larger than $40\mu\text{F}$ and $320\mu\text{F}$ for promising the output voltage variation under 1%. In addition, the partial energy stored in the middle-voltage filter capacitor (C_{O3}) should be delivered to the middle-voltage capacitor (C_2). By substituting $I_{O1(\max)} = 4\text{A}$ and $I_{O3(\max)} = 2.5\text{A}$ into $C_{O3} = (I_{O1} + I_{O3})/(\Delta V_{O3} f_S)$, the value of C_{O3} should be larger than $325\mu\text{F}$. In order to cope with unpredictable effect and lower ripple voltage variation in practical applications, the practical values of electrolytic capacitors (C_{O1}, C_{O2} and C_{O3}) are selected as $100\mu\text{F}$, $680\mu\text{F}$, and $680\mu\text{F}$, respectively.

For the stable operation of the proposed HSTDC, the feedback control is used to solve the problem of the output voltage varied with load variations, and a digital signal processor (DSP) TMS320F28335 manufactured by Texas Instruments is adopted to satisfy the requirement of feedback control and stable operation. In this control scheme, a conventional proportional-integral (PI) controller without complex mathematical dynamic models is utilized. In this study, the output voltages (i.e., the high-voltage dc bus (V_{O1}) and the middle-voltage output terminal (V_{O3})) of the proposed HSTDC are controllable via the conventional PI control framework, and the voltage level of the auxiliary source (V_{O2}) is regulated by the design of the auxiliary inductor (L_{aux}). Although the voltage of the auxiliary source (V_{O2}) is incontrollable real time, the predetermined voltage range by the design of the auxiliary inductor (L_{aux}) is appropriate to provide the floating charge voltage for an energy storage device (e.g., a battery module) as the load in the auxiliary circuit.

IV. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed high-efficiency single-input triple-outputs dc/dc converter (HSTDC) in practical applications, the experimentations of the proposed HSTDC are provided in this section. According to the circuit analyses in Section II and the design considerations in Section III, the circuit components and the preset electrical specifications of the proposed HSTDC are summarized in Tables 1 and 2, respectively. The practical photographs of the proposed HSTDC and the experimental equipment are depicted in Fig. 8(a) and 8(b), respectively. The PI control methodology and the analog/digital (A/D) sampling action are carried out in a 32-bit floating point DSP TMS320F28335 with a sampling frequency of 20kHz. The PWM duty cycle is produced by up-and-down counters and comparators in the DSP. Then, the corresponding PWM duty cycle is sent to gate driver for driving the power switch.

The measured waveforms of the power switch (S_1), diodes (D_1, D_2, D_3 and D_4), and the coupled inductor (T_r) of the proposed HSTDC under the total output power $P_{OT} = 500\text{W}$ ($P_{O1} = 330\text{W}$, $P_{O2} = 70\text{W}$ and $P_{O3} = 100\text{W}$) are depicted in Fig. 9, where the input voltage at low-voltage-side circuit (LVSC) is considered as $V_{Low} = 12\text{V}$.

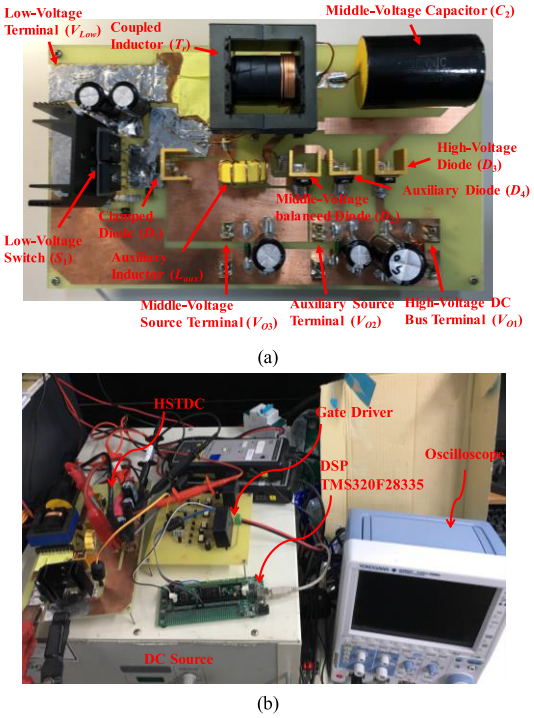

FIGURE 8. Practical photograph: (a) Converter prototype; (b) Experimental equipment.

TABLE 1. Circuit components of HSTDC.

Circuit Components	Symbol	Values and Types
Coupled inductor	T_r	N=3, L_p=2.23μH, L_s=20.1μH
Switching frequency	f_S	50kHz
Auxiliary inductor	L_{aux}	5.2μH
Low-voltage switch	S_1	IRFP4368*2
Clamped diode	D_1	SR20100
Middle-voltage balanced diode	D_2	SR20200
High-voltage diode	D_3	SR20200
Auxiliary diode	D_4	SR20100
Clamped capacitor	C_1	24μF
Middle-voltage capacitor	C_2	51μF
High-voltage filter capacitor	C_{O1}	100μF
Auxiliary source filter capacitor	C_{O2}	680μF
Middle-voltage filter capacitor	C_{O3}	680μF

TABLE 2. Preset electrical specifications of HSTDC.

Specifications	HSTDC
Full-load output power	P_{O1}=1kW (P_{O1}=800W, P_{O2}=100W, P_{O3}=100W)
Input voltage	V_{Low}=12V±10%
Output voltages	V_{O1}=200V, V_{O2}=25V~30V, V_{O3}=40V
Voltage ripple percentage	$V_{O1\text{ripple}} \leqq 1\%$, $V_{O2\text{ripple}} \leqq 1\%$, $V_{O3\text{ripple}} \leqq 1\%$

From Fig. 9(a), the leakage inductor restricts the instantaneous current change, and the current direction could not be changed immediately in the auxiliary inductor. It is obvious that power switch (S_1) is turned on under the property of

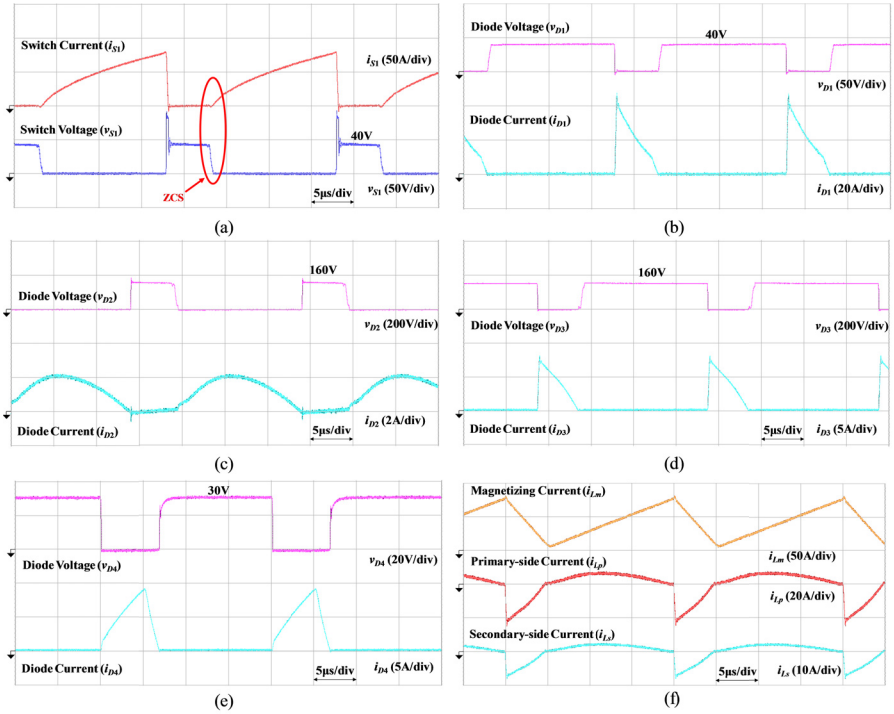

FIGURE 9. Experimental waveforms of switch, diodes, and coupled inductor at $P_{OT} = 500$W: (a) S_1; (b) D_1; (c) D_2; (d) D_3; (e) D_4; (f) T_r.

zero-current switching (ZCS) so that the corresponding switching loss can be reduced. Moreover, the voltage across the power switch (S_1) is clamped at 40V. As can be seen from Fig. 9(b), when the power switch (S_1) is turned off, the clamped diode (D_1) is conducted to transfer the energy stored in the leakage inductor to the clamped capacitor (C_1), and the reverse-recovery current inside the clamped diode (D_1) is approximately zero due to the selection of a schottky diode. From Fig. 9(c), the middle-voltage balanced diode (D_2) is conducted to transfer the energy to the middle-voltage capacitor (C_2) from the secondary-side winding (L_s), the clamped capacitor (C_1), and the middle-voltage filter capacitor (C_{O3}). Due to the selection of a schottky diode, the reverse-recovery current inside the middle-voltage balanced diode (D_2) is also approximately zero. As can be seen from Fig. 9(d)- Fig. 9(e), the high-voltage diode (D_3) and the auxiliary diode (D_4) are conducted when the diodes are forward bias, and the energy is delivered to the high-voltage dc bus (V_{O1}) and the auxiliary source (V_{O2}), respectively. Because there is no reverse-recovery current inside the high-voltage diode (D_3) and the auxiliary diode (D_4), the effect of the electromagnetic interference (EMI) can be alleviated, and the power consumption on the diodes can be decreased for the high power conversion. In addition, the current waveforms of the primary-side magnetizing inductor (i_{Lm}), the primary-side winding (i_{Lp}), and the secondary-side winding (i_{Ls}) inside the coupled inductor (T_r) are depicted in Fig. 9(f). It is obvious that the proposed HSTDC is operated at CCM owing to the minimum value of i_{Lm} to be larger

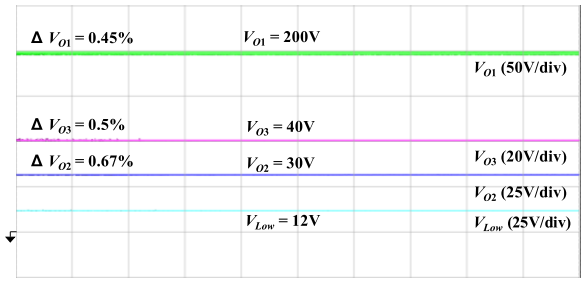

FIGURE 10. Experimental waveforms of input and output voltages at $P_{OT} = 500$W.

than zero. The corresponding waveforms of the input voltage (V_{Low}) and three output voltages (V_{O1}, V_{O2} and V_{O3}) are depicted in Fig. 10. From Fig. 10, the output voltages can be stably controlled to achieve the desired values via the feedback control. The voltage ripple percentages of V_{O1}, V_{O2} and V_{O3} are 0.45%, 0.67%, and 0.5%, respectively.

When the output power is increased to the maximum power P_{OT} = 1kW (P_{O1} = 800W, P_{O2} = 100W and P_{O3} = 100W), the measured waveforms of the power switch (S_1), diodes (D_1, D_2, D_3 and D_4), and the coupled inductor (T_r) of the proposed HSTDC are depicted in Fig. 11, where the input voltage at the LVSC is considered as V_{Low} = 12V. As can be seen from Fig. 11(a), the switching loss also can be alleviated because the power switch (S_1) is also operated under the property of ZCS condition, and the voltage across the power switch (S_1) is also clamped at 40V. By observing Fig. 11(b)-Fig. 11(e), the clamped diode (D_1), the

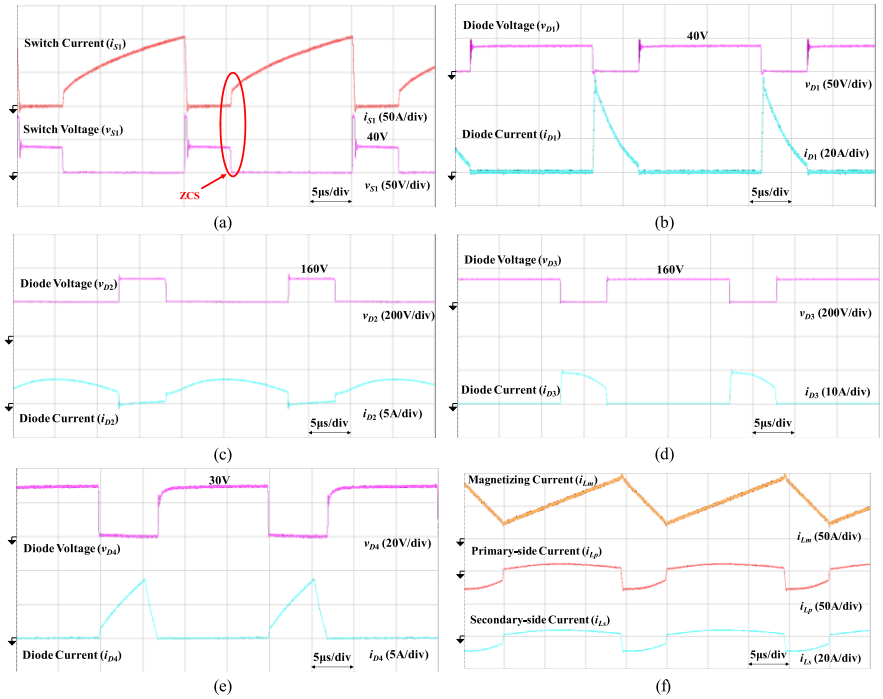

FIGURE 11. Experimental waveforms of switch, diodes, and coupled inductor at P_{OT} = 1kW: (a) S_1; (b) D_1; (c) D_2; (d) D_3; (e) D_4; (f) T_r.

middle-voltage balanced diode (D_2), the high-voltage diode (D_3), and the auxiliary diode (D_4) are conducted for transferring the energy to the output terminals, and the reverse-recovery currents inside the diodes (D_1, D_2, D_3 and D_4) are almost equal to zero. As can be seen from Fig. 11(f), the energy transmission between the primary side and the secondary side of the coupled inductor (T_r) is obvious. As a result, the correctness of the designed air gap can be verified to prevent the coupled inductor from entering the magnetic saturation area. From Fig. 11(f), it can conclude that less copper loss is produced inside the coupled inductor because there are lower ripple currents (i_{Lp} and i_{Ls}) at the full-load operation, and the power conversion efficiency can be significantly improved. In addition, the corresponding waveforms of the input voltage (V_{Low}) and three output voltages (V_{O1}, V_{O2} and V_{O3}) are depicted in Fig. 12. As can be seen from Fig. 12, the output voltages also can be stably controlled to the predetermined levels via the feedback control. The voltage ripple percentages of V_{O1}, V_{O2} and V_{O3} are 0.56%, 0.73%, and 0.61%, respectively.

In spite of operating at half-load (P_{OT} = 500W) or full-load (P_{OT} = 1kW) conditions, the power switch (S_1) in the proposed HSTDC is operated under the ZCS condition to reduce the switching loss, and stable output voltage levels can be exactly regulated by the feedback control and the design of the auxiliary inductor. By observing Fig. 10 and Fig. 12, the output voltage 200V for the high-voltage dc bus, the output voltage 40V for the middle-voltage output terminal, and the output voltage 25V $\sim$ 30V for the auxiliary source are ensured to stably supply power for various voltage-level applications.

The transient responses of the proposed HSTDC under step output-power changes between P_{OT} = 500W and P_{OT} = 1kW are depicted in Fig. 13. Although there are little voltage variations under step output-power changes, the voltage levels for the high-voltage dc bus terminal, the middle-voltage output terminal, and the auxiliary source terminal can be stably adjusted. Moreover, the output voltage responses of the proposed HSTDC under the corresponding nominal input voltage 12V to be varied $\pm$10% are depicted in Fig. 14. Although there are little voltage variations under input voltage change from 12V to 13.2V, three output voltages (V_{O1}, V_{O2} and V_{O3}) can be stably adjusted at desired values. As for input voltage change from 13.2V to 10.8V, three output voltages (V_{O1}, V_{O2} and V_{O3}) also can be stably adjusted at desired values. Although V_{O1} and V_{O3} are controlled by the same duty cycle of the power switch in Figs. 13 and 14, the output voltages can be stably controlled under the occurrence of load variations by the closed-loop control methodology. Although the output voltage of the auxiliary circuit only can be adjusted at the setting range 25V $\sim$ 30V via the design of the auxiliary inductor, the output voltages of the high-voltage dc bus and the middle-voltage output terminal can be precisely controlled to be 200V and 40V, respectively.

The waveforms including the power conversion efficiency and three output powers of the proposed HSTDC are depicted in Fig. 15(a). In the experiments, the converter efficiency is evaluated via Power Analyzer WT500 equipment, manufactured by the Yokogawa Electric Corporation. The bandwidth of the WT500 is 0.5Hz to 100kHz, and the accuracy of the measured power is within $\pm$0.1%. The experimental results reveal that the maximum efficiency is measured to

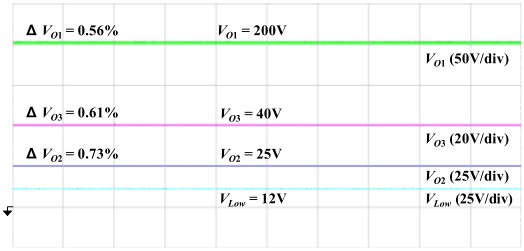

FIGURE 12. Experimental waveforms of input and output voltages at P_{OT} = 1kW.

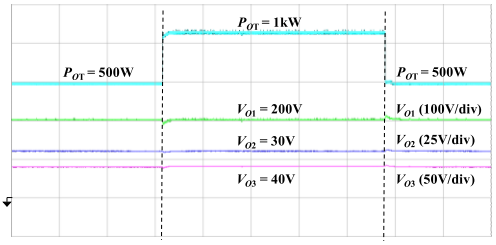

FIGURE 13. Measured transient responses of HSTDC under step output-power changes.

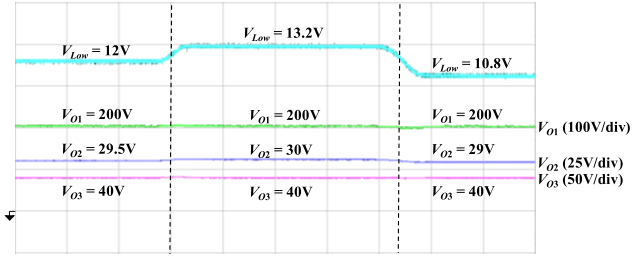

FIGURE 14. Measured transient responses of HSTDC under input voltage variations.

be 96.5% under the output power about 250W (P_{O1} = 120W, P_{O2} = 70W and P_{O3} = 60W) in Fig. 15(a). Moreover, the efficiency is also measured to be 90.4% under the maximum output power P_{OT} = 1kW.

In order to explain the power conversion efficiency of the proposed HSTDC, the power losses caused by main circuit components [34] are introduced. The power consumptions on power switch and diodes are denoted as P_{S1} for switch S_1; P_{D1}, P_{D2}, P_{D3} and P_{D4} for diodes D_1, D_2, D_3 and D_4, respectively. Moreover, the power consumptions in the coupled inductor contain the copper loss (P_{cu}) and the core loss (P_{fe}). Because metalized-polyester film capacitors are used, the corresponding power consumptions can be neglected in power loss analyses. In addition, the turn-on resistance of power switch and the forward voltages of diodes can be represented as R_{ds} and V_F, respectively. By the amp-second balance theory [33], the charging currents are equal to the discharging currents on the capacitors (C_1 and C_2), and the diode currents can be expressed as $I_{D1(rms)} = I_{O3(rms)}$ and $I_{D2(rms)} = I_{O1(rms)}$, respectively. Thus, one can obtain the following relations:

$$P_{S1} = I^2_{S1(rms)} R_{ds(S1)} = (P_{Low}/V_{Low})^2 R_{ds(S1)} \quad (32)$$

$$P_{D1} = I_{D1(rms)} V_{F(D1)} = (P_{O3}/V_{O3}) V_{F(D1)} \quad (33)$$

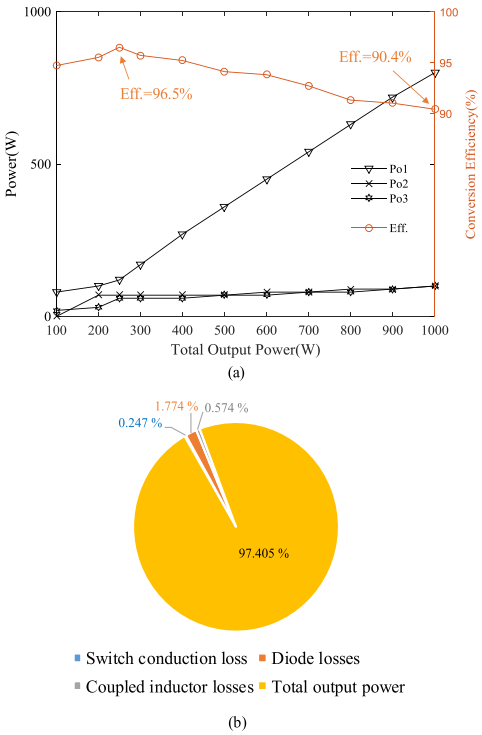

FIGURE 15. Experimental power analyses of HSTDC: (a) Power conversion efficiency; (b) Power loss ratio.

$$P_{D2} = I_{D2(rms)} V_{F(D2)} = (P_{O1}/V_{O1}) V_{F(D2)} \quad (34)$$

$$P_{D3} = I_{D3(rms)} V_{F(D3)} = (P_{O1}/V_{O1}) V_{F(D3)} \quad (35)$$

$$P_{D4} = I_{D4(rms)} V_{F(D4)} = (P_{O2}/V_{O2}) V_{F(D4)} \quad (36)$$

$$P_{cu} = I^2_{Low(rms)} R_{(L_p)} + I^2_{O1(rms)} R_{(L_s)} = (P_{Low}/V_{Low})^2 R_{(L_p)} + (P_{O1}/V_{O1})^2 R_{(L_s)} \quad (37)$$

According to the relation of $P_{fe} = C_m f_{eq}^{\alpha} B^{\beta} f_S$ in [35], the maximum core loss can be calculated as $P_{fe(\max)} = 8W$ via the datasheet of EE-55 ferrite core, and the practical core loss in the proposed converter with the typical value of $\beta = 2.5$ can be rearranged as

$$P_{fe} = P_{fe(\max)} (B^{2.5}_{practical} f_S / B^{2.5}_{test} f_{test}) \quad (38)$$

Because the small current pass through the auxiliary inductor (L_{aux}) with low resistance, the power loss of the auxiliary inductor can be neglected. Meanwhile, the parasitic parameters are summarized in Table 3. As a result, the total power loss in the proposed HSTDC can be represented as

$$P_{loss} = P_{S1} + P_{D1} + P_{D2} + P_{D3} + P_{D4} + P_{cu} + P_{fe} \quad (39)$$

From (39), the calculation of the power conversion efficiency with parasitic parameters can be expressed as

$$\eta = \frac{P_{O1} + P_{O2} + P_{O3}}{P_{O1} + P_{O2} + P_{O3} + P_{loss}} \quad (40)$$

As can be seen from Fig. 15(a), the calculated maximum efficiency is 97.405% by substituting the powers (P_{O1} = 120W, P_{O2} = 70W and P_{O3} = 60W) at

TABLE 3. Parasitic parameters of components.

Parasitic Parameters	Symbol	Values
Turn-on resistance of S_1	$R_{ds(S1)}$	1.46mΩ
Forward voltage of D_1	$V_{F(D_1)}$	0.9V
Forward voltage of D_2	$V_{F(D_2)}$	0.92V
Forward voltage of D_3	$V_{F(D_3)}$	0.92V
Forward voltage of D_4	$V_{F(D_4)}$	0.9V
Primary-side winding resistance	$R_{(L_p)}$	1.13mΩ
Secondary-side winding resistance	$R_{(L_s)}$	12.99mΩ
Maximum EE-55 ferrite core loss ($B_{test}=200\,\text{mT}$, $f_{test}=25\,\text{kHz}$)	$P_{fe(\max)}$	8W

the maximum power conversion efficiency into (40). The corresponding power loss ratio of the proposed HSTDC is depicted in Fig. 15(b). The above experimental results agree well with those obtained from theoretical analyses given in Section II and the prototype manufacturing considerations given in Section III. According to the experimental verification, the proposed HSTDC can achieve the objectives of three different voltage levels and high power conversion efficiency.

In order to exhibit the advantages of the proposed HSTDC, comprehensive comparisons of step-up dc/dc converters in previous literatures are summarized in Table 4. As can be seen from the tabular data, the circuit frameworks in [12], [13] belong to single-input single-output (SISO) dc/dc converters without the function of multiple output voltages. Moreover, the topologies in previous works [14], [17], [23], [30]–[32] belong to single-input multiple-output (SIMO) dc/dc converters to be similar to the proposed one in this study. As high step-up behaviors obviously can be demonstrated by electrical specifications in [14], [17] and [23], the design similar to the one in the proposed HSTDC has been reported. Although the power conversion efficiency of the framework in [14] is slightly larger than the one in the proposed HSTDC, the amount of power switches in [14] is four times the requirement in this study, so that the manufacturing cost in [14] is inevitably increased. In addition, the third output port is constructed in the proposed HSTDC with a controllable voltage level, and the required capacitor value of the clamped capacitor is lower than the one in the converter [17]. Moreover, the voltage gain and the power conversion efficiency of the proposed HSTDC are higher than the ones in [17]. In addition, the converters without coupled inductors may be operated with narrow voltage-gain ranges for dual outputs applications in [30]–[32]. Owing to hard switching conditions in these topologies, the power consumptions on power switches will degenerate the power conversion efficiency. Although a ripple-free single-input three-output converter without a coupled inductor was introduced in [36], large amount passive components including diodes, capacitors and inductors were adopted, and the corresponding voltage gain was sensitive to parasitic parameters. In this study, the soft-switching technique is adopted for improving the power

TABLE 4. Performance comparisons of Step-Up converters with other literatures.

References	Input voltage	Output voltage	Output power	Maximum conversion efficiency	Amount of power switches
[12]	59V	V_1:900V	415W	96.8%	4
[13]	30V	V_1:200V	200W	93.9%	2
[14]	24V	V_1:200V V_2:58V	1kW	97%	4
[17]	12V	V_1:200V V_2:28V V_3:14V	1kW	95.3%	1
[23]	12V	V_1:200V V_2:28V	1kW	95.55%	3
[30]	12V	V_1:18V V_2:6V	120W	90%	2
[31]	48V	V_1:156V V_2:24V	252W	91.3%	2
[32]	60V	V_1:125V V_2:36V	300W	95.9%	4
[36]	40V	V_1:200V V_2:100V V_3:360V	600W	95.8%	2
This study	**12V**	**V_1:200V V_2:30V V_3:40V**	**1kW**	**96.5%**	**1**

conversion efficiency. As can been seen from comprehensive comparisons with other literatures in Table 4, the proposed HSTDC indeed performs high power conversion efficiency and fewer manufacturing cost under a kW-level experimental prototype.

V. CONCLUSION

This study has successfully developed a high-efficiency single-input triple-outputs dc/dc converter (HSTDC) for high step-up applications, and this coupled-inductor-based converter has been applied well for the application with high voltage ratios and multiple output terminals. The proposed HSTDC has an excellent stabilization under various experimental conditions and input voltage variations. From the experimental verification, the maximum power conversion efficiency is over 96% due to the soft-switching technique. In this study, the proposed HSTDC incorporates a coupled inductor, a power switch, four schottky diodes, two metalized-polyester film capacitors, and one auxiliary inductor to achieve the objectives of high-efficiency power conversion, zero-current-switching (ZCS) turned-on, and single-input triple-outputs feature. A kW-level experimental prototype has built and verified the theoretical analyses with the practical behaviors. Due to the distinguishing characteristics of the single-input multiple-outputs operation, the proposed HSTDC also can be easily used for other high step-up applications.

The major advantages of this study are summarized as follows: 1) The proposed converter via only one power switch achieves the goals of a high step-up ratio, the high-efficiency power conversion, and different output voltage levels. 2) Since the voltage stress of the power switch can be clamped to be a specific voltage level, the power switch with a lower turned-on resistor can be selected to decrease the

conduction loss, and the switching loss will be alleviated via the soft-switching technique. 3) A feedback control system can be implemented by a digital signal processor instead of a traditional analog control circuit. 4) The closed-loop control method is designed to stabilize the output voltage for load variations. 5) The auxiliary source supplies energy for peripheral equipment instead of another power subsystems, and benefits as saving the manufacturing cost and simplifying complicated control systems.

In order to further regulate the output voltage levels independently, an active switch and a three-winding coupled inductor can be introduced to manipulate the output voltage levels with different duty cycles. By this case, the new circuit framework can be referred to [31], and multiple-input multiple-output (MIMO) dc/dc converter used in power systems also can be further investigated in the future research.

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RONG-JONG WAI (M'99–SM'05) was born in Tainan, Taiwan, in 1974. He received the B.S. degree in electrical engineering and the Ph.D. degree in electronic engineering from Chung Yuan Christian University, Chung Li, Taiwan, in 1996 and 1999, respectively.

From 1998 to 2015, he was with Yuan Ze University, Chung Li, where he was the Dean of General Affairs, from 2008 to 2013, and the Chairman of the Department of Electrical Engineering, from 2014 to 2015. Since 2015, he has been with the National Taiwan University of Science and Technology, Taipei, Taiwan, where he is currently a Distinguished Professor, the Dean of General Affairs, and the Director of the Energy Technology and Mechatronics Laboratory. He is a chapter-author of the *Intelligent Adaptive Control: Industrial Applications in the Applied Computational Intelligence Set* (Boca Raton, FL: CRC Press, 1998) and the coauthor of the *Drive and Intelligent Control of Ultrasonic Motor* (Taichung, Taiwan, R.O.C.: Tsang-Hai, 1999), the *Electric Control* (Tai-chung, Taiwan, R.O.C.: Tsang-Hai, 2002), and the *Fuel Cell: New Generation Energy* (Tai-chung, Taiwan, R.O.C.: Tsang-Hai, 2004). He has authored more than 170 conference papers, over 180 international journal papers, and 57 inventive patents. His research interests include power electronics, motor servo drives, mechatronics, energy technology, and control theory applications. The outstanding achievement of his research is for contributions to real-time intelligent control in practical applications and high-efficiency power converters in energy technology.

Dr. Wai is a Fellow of the Institution of Engineering and Technology (U.K.) and a Senior Member of the Institute of Electrical and Electronics Engineers (USA). He received the Excellent Research Award, in 2000, and the Wu Ta-You Medal and Young Researcher Award from the National Science Council, R.O.C., in 2003. In addition, he was a recipient of the Outstanding Research Award from the Yuan Ze University, R.O.C., in 2003 and 2007, respectively; the Excellent Young Electrical Engineering Award and the Outstanding Electrical Engineering Professor Award from the Chinese Electrical Engineering Society, R.O.C., in 2004 and 2010, respectively; the Outstanding Professor Award from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, R.O.C., in 2004 and 2008, respectively; the International Professional of the Year Award from the International Biographical Centre, U.K., in 2005, respectively; the Young Automatic Control Engineering Award from the Chinese Automatic Control Society, R.O.C., in 2005; the Yuan-Ze Chair Professor Award from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, R.O.C., in 2007, 2010, and 2013, respectively; the Electric Category-Invent Silver Medal Award, in 2007, the Electronic Category-Invent Gold and Silver Medal Awards, in 2008, the Environmental Protection Category-Invent Gold Medal Award, in 2008, the Most Environmental Friendly Award, in 2008, the Power Category-Invent Bronze Medal Award, in 2012, and the Electronic Category-Invent Gold and Silver Medal Awards from the International Invention Show and Technomart, Taipei, R.O.C., in 2015; the University Industrial Economic Contribution Award from the Ministry of Economic Affairs, R.O.C., in 2010; the Ten Outstanding Young Award from the Ten Outstanding Young Person's Foundation, R.O.C., in 2012; the Taiwan Top 100 MVP Managers Award from MANAGER today magazine, R.O.C., in 2012; the Outstanding Engineering Professor Award from the Chinese Institute of Engineers, R.O.C., in 2013; the Green Technology Category-Scientific Paper Award from the Far Eastern Y. Z. Hsu-Science and Technology Memorial Foundation, R.O.C., in 2014; the Scopus Young Researcher Lead Award-Computer Science from Taiwan Elsevier, in 2014; the Outstanding Research Award from the National Taiwan University of Science and Technology, R.O.C., in 2016 and 2018, respectively; and the Most Cited Researchers Award (2016) (Field: Electrical & Electronics Engineering).

ZHI-FU ZHANG was born in Taichung, Taiwan, in 1994. He received the B.S. and M.S. degrees in electronic and computer engineering from the National Taiwan University of Science and Technology, Taiwan, in 2017 and 2019, respectively. His research interests include power electronics and dc–dc converter.