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Technology Computer Aided Design Study of GaN MISFET With Double P-Buried Layers

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ABSTRACT In this paper, a performance-improved AlGaN-/GaN-Based metal-insulator-semiconductor field effect transistor (MISFET) with double P-buried layers MISFET (DP-MISFET) is proposed. The proposed structure is simulated, and its characteristics are analyzed by the Sentaurus TCAD tool; the results show that with a gate-drain spacing of 6 μm, the optimized DP-MISFET can achieve high Baliga's figure of merit of 3.23 GW $\cdot$ cm^{-2} due to the modulation of the electric field distribution. Compared with the conventional MISFET (C-MISFET) with the breakdown voltage (BV) of 503.9 V and specific on-resistance ($R_{on,sp}$) of 0.63 m$\Omega \cdot$ cm^2, the proposed structure can achieve a better trade-off between the breakdown voltage and specific on-resistance achieving $R_{on,sp}$ and BV of 0.63 m$\Omega \cdot$ cm^2 and 1427 V, respectively.

INDEX TERMS P-buried layers, GaN, MISFET, Sentaurus TCAD, figure of merit.

I. INTRODUCTION

Over the past decades, the AlGaN/GaN-Based metal-insulator-semiconductor field effect transistors (MISFETs) have been attracting much attention [1]–[8] due to their excellent features, such as great properties of gallium nitride materials [9] and high electron density of a two-dimensional electron gas (2DEG) from the polarization effect [10]. Moreover, GaN HEMTs have been recognized as excellent devices for the fabrication of high efficiency power converters, since they can have very low ON- resistance, high switching speed, and high breakdown voltage [11]. However, achieving a high breakdown voltage (BV) at a low on-resistance (R_{on}) is still challenging. Over the years, many scholars and researchers have done a lot of researches to improve the characteristics of the MISFETs. For example, the field plate (FP) devices such as uniform field plates [12], multiple field plates [13], source-drain field plates [14], and floating field plates [15] were proposed to reduce the electric field peak at the gate edge and achieve the multiple electric field peaks between the gate and drain. Karmalkar *et al.* [16] and Duan and Yang [17] adopted the reduced surface field (RESURF) concept [18] to achieve a high breakdown voltage. The Fe-doped [19]–[21] and C-doped [22]–[24] technologies were also proposed to reduce the buffer leakage current.

Luo et al. used the P-buried layer technology to improve the breakdown voltage [25]. In the proposed SC-PBL FPs MISFET structure, the P-buried layer could fully deplete the 2DEG in channel and improve the breakdown voltage significantly. However, the P-buried layer also increased the specific on-resistance ($R_{on,sp}$) and reduced the maximum saturation current due to the decrease in 2DEG density of the channel, which degraded the forward characteristic of the device.

Hence, this paper introduces an AlGaN/GaN based MISFET with the double P-buried layers (DP-MISFET). The source-connected bottom P-buried layer (BP) can deplete the 2DEG and improve the breakdown voltage without affecting the forward characteristic due to the large distance between the BP and channel layer. The floating top P-buried (TP) layer can further improve the breakdown voltage by absorbing the lateral electric field from the drain and blocking current flowing from the source to the drain as a current blocking layer (CBL) [26] while the forward characteristic of the device is almost unchanged because the 2DEG density is not affected by the P-buried layers; meanwhile, the TP is formed by Magnesium (Mg) ion implantation in this paper.

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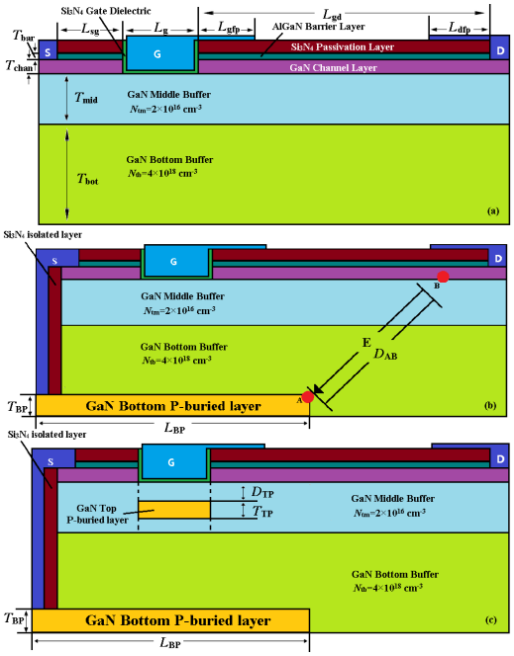

FIGURE 1. The cross-section of: (a) C-MISFET (b) BP-MISFET, and (c) DP-MISFET.

II. STRUCTURES AND SIMULATION

The cross-section of a MISFET with the double P-buried layers (DP-MISFET) is illustrated in Fig. 1(c). To show the difference in structure between the MISFET we proposed and the conventional MISFET (C-MISFET) and the MISFET with only one bottom P-buried layer (BP-MISFET), the cross-sections of the C-MISFET and BP-MISFET are also proposed in Fig 1(a) and (b).

All these structures include an unintentionally doped $Al_{0.15}Ga_{0.75}N$ barrier layer, an unintentionally doped GaN channel layer, a 0.4-μm-thick GaN middle buffer layer and a 1.6-μm-thick GaN bottom buffer layer that form the buffer layer of the MISFET, and the donor concentration is set to 1×10^{16} cm^{-3} in the buffer layers as background carriers induced by fabrication process. Besides, in middle buffer layer and bottom buffer layer, we sets an acceptor type traps at concentrations of 2e16 cm^{-3} and 4e18 cm^{-3}, respectively, and its trap level is 1.0 eV from intrinsic fermi level. On the Si_3N_4/AlGaN interface, we also sets a donor type traps at concentrations of 5e13 cm^{-2}, and its trap level is 0.4 eV from intrinsic fermi level. Moreover, the silicon nitride (Si_3N_4) material is used as a gate dielectric and the passivation layers with the thicknesses of 20 nm and 100 nm, and which are also used as an isolated layer with the length of 0.1 μm. Furthermore, the lengths of the gate field plate and drain field plate are 0.5 μm and 0.8 μm at first, respectively [25].

The values of the key parameters of the proposed structure are summarized in Table 1. As shown in Fig. 1(b), L_{BP} and T_{BP} are the length and thickness of the bottom P-buried layer (BP), respectively, and N_{aBP} is the hole concentration of the BP. In Fig. 1(c), D_{TP} is the spacing between the top P-buried layer (TP) and the channel layer, and N_{aTP} is the hole concentration of the TP. The whole concentration of both P-buried layers is set in the range from 1×10^{17} cm^{-3} to 5×10^{17} cm^{-3} [25], [27]. The thickness of the TP (T_{TP}) is set to 0.1 μm [28]. The work function of the gate metal is set to 5.15eV [29].

TABLE 1. Simulation parameters used for device simulation.

PARAMETERS	ALIASES	VALUES
Gate-source spacing	L_{sg}	0.5 μm
Gate Length	L_g	0.5 μm
Gate-drain spacing	L_{gd}	6 μm
Gate field plate length	L_{gfp}	0.5 μm
Drain field plate length	L_{dfp}	0.8 μm
Thickness of TP	T_{TP}	0.1 μm
TP and channel layer spacing	D_{TP}	0.2 μm
Thickness of BP	T_{BP}	0.4 μm
Length of BP	L_{BP}	4 μm
TP hole concentration	N_{aTP}	5×10^{17} cm^{-3}
BP hole concentration	N_{aBP}	2×10^{17} cm^{-3}
Barrier layer thickness	T_{bar}	25 nm
Channel layer thickness	T_{chan}	50 nm
Middle buffer layer thickness	T_{mid}	0.4 μm
Bottom buffer layer thickness	T_{bot}	1.6 μm

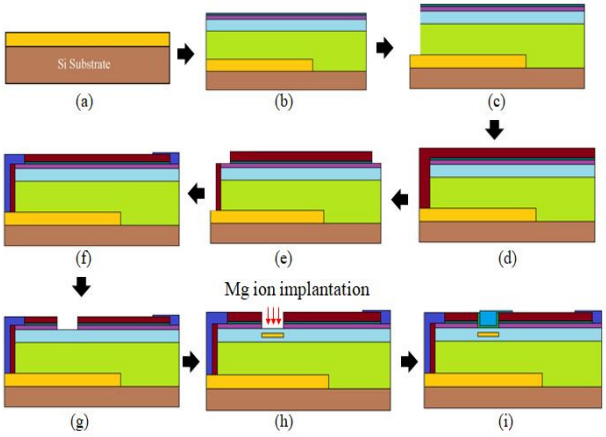

FIGURE 2. Schematic of fabrication process steps for proposed structure.

The schematic of the fabrication process of the proposed structure is presented in Fig. 2.

(a) Growing an epitaxial p-type layer on a Si substrate, this can be realized by the metal-organic chemical vapor deposition (MOCVD) using Mg as a P-type impurity [30]–[32].
(b) Etching the right part of p-type layer through the inductively coupled plasma (ICP) process [30], [33] and then growing the bottom buffer layer, middle buffer layer, channel layer and barrier layer.
(c) Etching the left part of the device.
(d) Si_3N_4 is used to fill the trench and form the passivation layer.
(e) Etching the source and drain contact.
(f) Forming the ohmic contact of the source and drain electrode.
(g) Etching the gate contact.

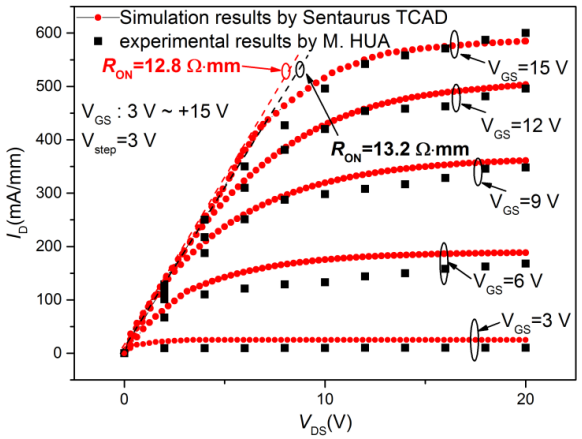

FIGURE 3. The I_D-V_{DS} characteristics from simulation and experiment validate the effectiveness of models in simulation.

(h) Forming the p-type region by using Mg ion implantation, which can simplify the fabrication procedures by accomplishing the gate at the same time, and the depth or hole concentration are decided by the energy and dose of ion implantation [34]–[36].

(i) Growing epitaxial Si_3N_4 as a gate dielectric and forming the gate electrode.

The TCAD Sentaurus software from the Synopsys Inc was used to simulate and optimize three different MISFETs based on the Baliga's figure of merit (*BFOM*), defined as $BFOM = V_{BK}^2/R_{on,sp}$ [37]. To get more accurate results, the physical models such as the SRH, Auger, DopingDep, high field saturation and polarization model including the Gate Dependent strain were used in the simulation. Besides, the substrate is removed for the suppression of the vertical leakage current [38]–[41]. In Fig 3, the effectiveness of these models has been proved by Luo *et al.* [29] with the experimental results [42], in which the gate-drain spacing took the value of 15 μm. It can be seen that the simulation results as 12.8Ω•mm of R_{ON} is fit well with the experimental results as 13.2Ω•mm of R_{ON}.

When the breakdown performance was simulated, the Avalanche model with a dependent electric field was adopted in the simulation. The impact ionization rate was defined by [25]:

$$G = \alpha_n n v_n + \alpha_p p v_p \tag{1}$$

where n and p refer to the concentration of electrons and holes, respectively, v_n and v_p refer to the saturation velocity of the electrons and the holes, respectively, and α_n and α_p are the values of the impact-ionization coefficient which relates to the electric field, and they are defined by Equation (2). The temperature dependence of the phonon gas against which carriers are accelerated is expressed by parameters γ_n and γ_p. In (2), coefficients a_n, a_p, b_n, and b_p are fitting parameters, and their values are listed in Table 2 [25], [43].

$$\alpha_{n,p} = \gamma_{n,p} a_{n,p} \exp(-b_{n,p}\gamma_{n,p}/E) \tag{2}$$

TABLE 2. Fitting parameters used in equation (2).

PARAMETERS	VALUES
a_n	2.9×10^8 cm^{-1}
a_p	3.4×10^7 V/cm
b_n	1.34×10^8 cm^{-1}
b_p	2.03×10^7 V/cm

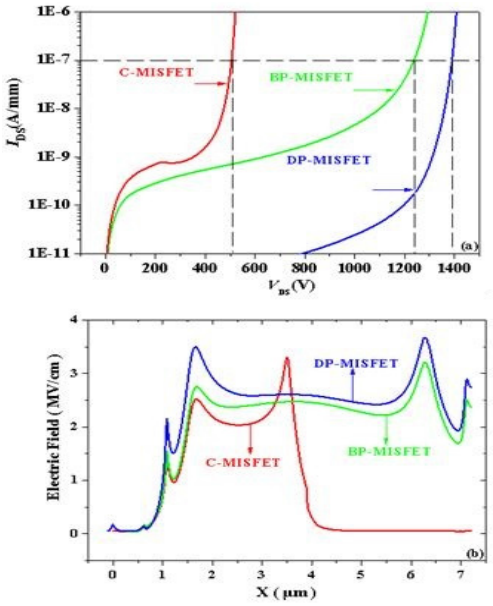

FIGURE 4. (a) Breakdown characteristics of C-MISFET, BP-MISFET and DP-MISFET. (b) the corresponding horizontal electric field distribution in channel 1nm below heterojunction.

III. RESULTS AND DISCUSSION

A. BASIC CHARACTERISTICS

The comparison of the breakdown characteristics and the electric field distribution of the C-MISFET, BP-MISFET, and DP-MISFET is presented in Fig. 4. The *BV* values of the C-MISFET, BP-MISFET, and DP-MISFET extracted at $I_D = 0.1$ μA/mm and $V_{GS} = 0$ V are 503.9 V, 1237 V, and 1389 V, respectively. In the C-MISFET, the 2DEG is not completely depleted, so the electric field peak appears between the gate and drain, which limited the breakdown voltage of the device. In contrast to the C-MISFET, the bottom P-buried layer could deplete the 2DEG completely and improve *BV* of the BP-MISFET, which could flat the electric field distribution and extend the electric field distribution to the drain. In the DP-MISFET, a floating top P-buried layer was added to further improve *BV* at the cost of slight forward characteristics degradation.

As presented in Figs. 5(a)-(b), the on-resistance (R_{ON}) increased only from 8.72 Ω•mm in the C-MISFET to 8.77Ω•mm in the optimized DP-MISFET, which was lower than 9.18 Ω•mm presented in [25], and V_{TH} increased only from 2.21 V to 2.98 V. The shift of V_{TH} was due to the higher-band energy level under the gate induced by the floating top P-buried layer [29], which also increased R_{ON} because the

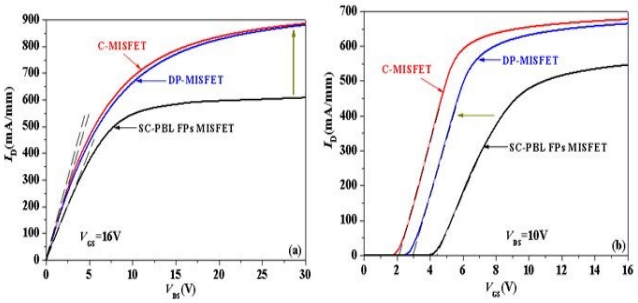

FIGURE 5. (a). I_D-V_{DS} characteristics at V_{GS} = 16 V and (b) I_D-V_{GS} characteristics at V_{DS} = 10 V.

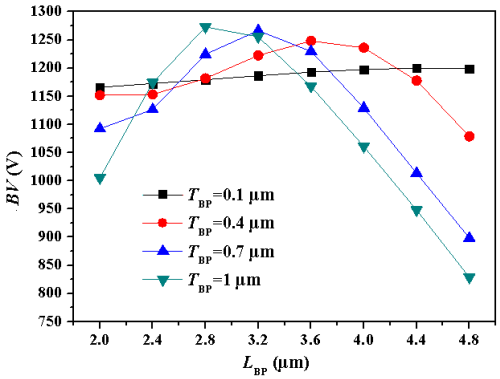

FIGURE 6. The relationship between *BV*, L_{BP} and T_{BP} while $N_{aBP} = 3 \times 10^{17}$ cm^{-3}.

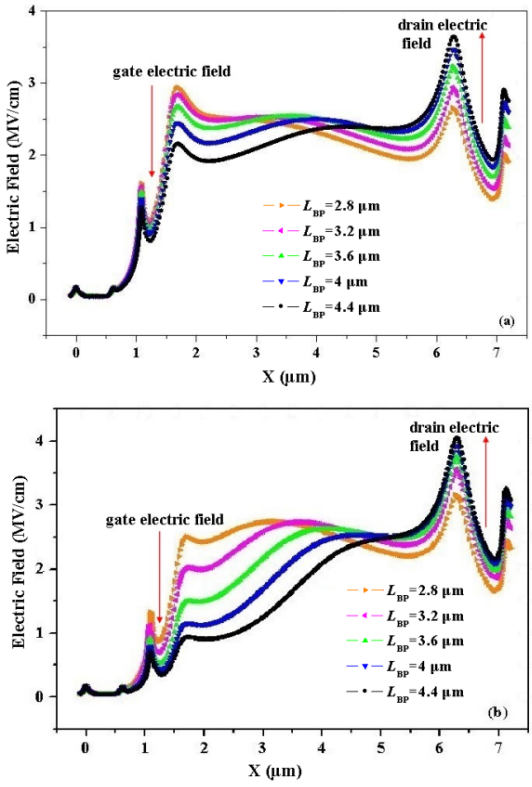

FIGURE 7. The relationship between Electric Field and L_{BP} while $N_{aBP} = 3 \times 10^{17}$ cm^{-3} with (a) T_{BP} = 0.4 μm (b) T_{BP} = 1 μm.

eDensity under the gate was decreased from 2.79×10^{13} cm^{-2} to 2.71×10^{13} cm^{-2} at $V_{GS} = 16$ V. Besides, the eDensity of the 2DEG was almost unaffected because the gate and the top P-buried layer were aligned, thus, the maximum saturation current of the device is increased form 609mA/mm presented in [25] to 881mA/mm in the optimized DP-MISFET, increased by 45%, which can ensure that the device has a strong current drive capability.

B. EFFECT OF BOTTOM P-BURIED LAYER (BP)

As shown in Fig. 1(b), the P-buried layer was added to the bottom buffer. The influence on the breakdown characteristic of three key parameters, i.e., N_{aBP}, L_{BP}, and T_{BP}, were analyzed through the simulations. Initially, N_{aBP} was set to 3×10^{17} cm^{-3}.

The relationship between *BV*, L_{BP}, and T_{BP} is presented in Fig. 6, and these relationships also can be summarized as the relationship between *BV* and the distance of point A and point B (D_{AB}) in Fig. 1(b). At $T_{BP} = 0.4$ μm, when L_{BP} increased, *BV* also increased until the *BV* peak occurred at $L_{BP} = 3.6$ μm. Due to the absorbing of the electric field by the BP, the electric field line from the drain to the point A was directed, which enhanced the electric field in the body of MISFET, decreased the concentration of the electric field under the gate and modulated the electric field distribution between the gate and drain.

The results presented in Fig. 7(a) also prove that with the increase in L_{BP}, i.e. decrease in D_{AB}, the value of the drain electric field peak was getting higher and higher; at the same time, the value of the gate electric field peak was getting lower and lower, and the high drain electric field peak would cause avalanche breakdown to occur in advance, so the *BV* decrease when L_{BP} was larger than 3.6 μm (Fig.7). On the other hand, Fig. 6 also shows that with the increase in the thickness of BP (T_{BP}), the *BV* peak shifted to the left and the value of maximum *BV* increased only a little; however, the *BV* curves declined rapidly after the peak point. This phenomenon is related to the change of D_{AB}. When T_{BP} was small, about 0.1 μm, with the increase in L_{BP}, the change of D_{AB} was not obvious. On the other hand, when T_{BP} was larger than 0.4 μm, the changes of D_{AB} were particularly significant as L_{BP} increased. Both situations are presented in Fig.6, where one curve is almost flat, and the other curves have a distinct rise and fall.

The results presented in Fig. 7(b) also show that the peak of the gate electric field droped more rapidly at T_{BP} of 1 μm than at T_{BP} of 0.4 μm, which is displayed in Fig. 7(a), causing a rapid drop in the breakdown voltage. Also, if the BP layer is too thick, it would be more difficult to control the length of the BP in semiconductor fabrication procedure. In this work, the T_{BP} was set to 0.4 μm. Besides, the reason for the changes of the drain electric field and gate electric field was not only related to D_{AB} but also to N_{aBP}. With the aim to

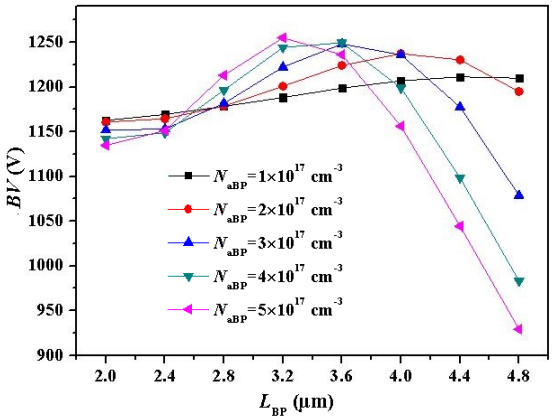

FIGURE 8. The relationship between BV, L_{BP} and N_{aBP} while $T_{BP} = 0.4$ μm.

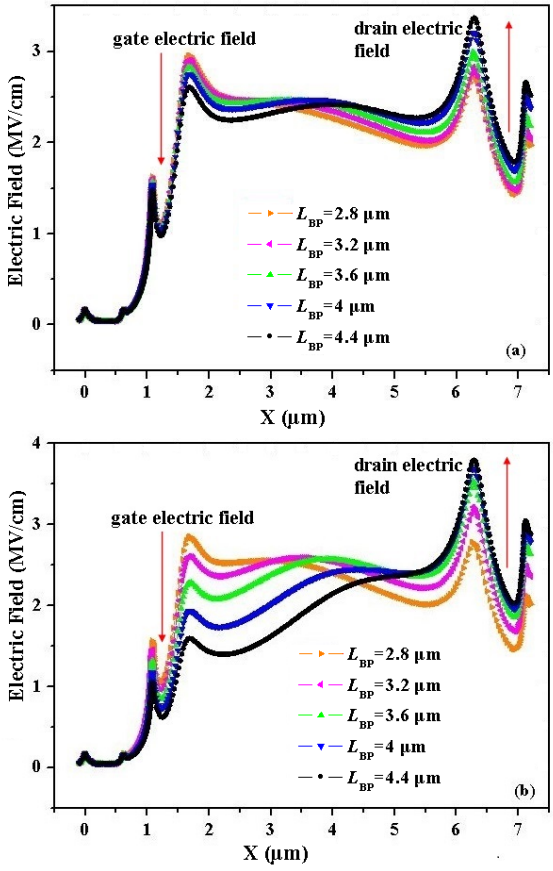

FIGURE 9. The relationship between electric field and L_{BP} while $T_{BP} = 0.4$ μm with (a) $N_{aBP} = 2 \times 10^{17}$ cm^{-3} (b) $N_{aBP} = 5 \times 10^{17}$ cm^{-3}.

study the influence of N_{aBP} and L_{BP} on BV, more simulations were performed to provide the results necessary for further discussion; while the relationship between BV and L_{BP} was investigated in the previous work at $N_{aBP} = 3 \times 10^{17}$ cm^{-3}.

In Fig. 8, it is shown that the maximum BV was almost unchanged, but the curves declined more rapidly when N_{aBP} was large than 2×10^{17} cm^{-3}. As N_{aBP} increased, the ability

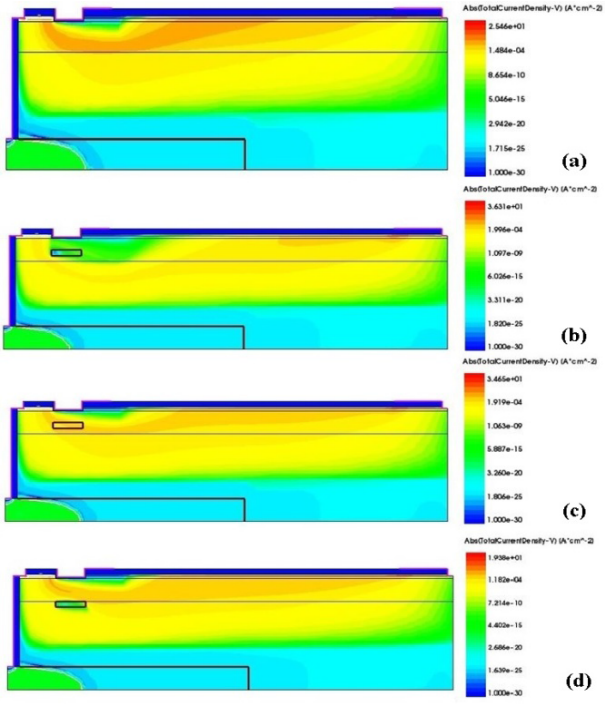

FIGURE 10. The path of the leakage current of: (a) BP-MISFET (b) DP-MISFET with $N_{aTP} = 5 \times 10^{17}$ cm^{-3} and $D_{TP} = 0.2$ μm (c) DP-MISFET with $N_{aTP} = 1 \times 10^{17}$ cm^{-3} and $D_{TP} = 0.2$ μm (d) DP-MISFET with $N_{aTP} = 5 \times 10^{17}$ cm^{-3} and $D_{TP} = 0.4$ μm.

of BP to absorb the electric field was also getting stronger, which decreased the concentration of the electric field under the gate and caused a rapid drop in the breakdown voltage. The results presented in Fig. 9(b) prove that the peak of the gate electric field dropped more rapidly at N_{aBP} of 5×10^{17} cm^{-3} than at N_{aBP} of 2×10^{17} cm^{-3} in Fig. 9(a). Considering that BV dropped rapidly after the peak point at a higher N_{aBP}, which made it difficult to control L_{BP} in semiconductor fabrication procedure, N_{aBP} and L_{BP} were set to 2×10^{17} cm^{-3} and 4 μm, respectively.

C. EFFECT OF FLOATING TOP P-BURIED LAYER (TP)

The BP is discussed in the previous section, where it is stated that breakdown voltage can fully deplete 2DEG and enhance the electric field in the body of the MISFET; however, the electric field lines points not only to the BP but also to the source, which causes the current leakage as shown in Fig 10(a), and limiting the breakdown voltage.

Therefore, a floating top P-buried layer was added to further improve the breakdown voltage without increasing $R_{on,sp}$ or complicating the fabrication process presented in Fig. 1(c).

It can be seen that the TP not only could absorb more lateral electric field but also could block the current flowing through the middle buffer layer, acting as a current blocking layer (CBL) as shown in Fig. 10(b) unlike the BP-MISFET shown in Fig. 10(a). So the leakage current could only pass through the bottom buffer layer which could suppress the

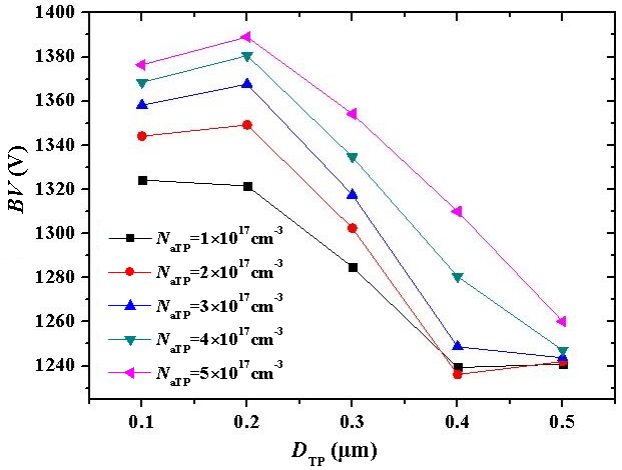

FIGURE 11. The relationship between *BV*, $R_{on,sp}$ and D_{TP}.

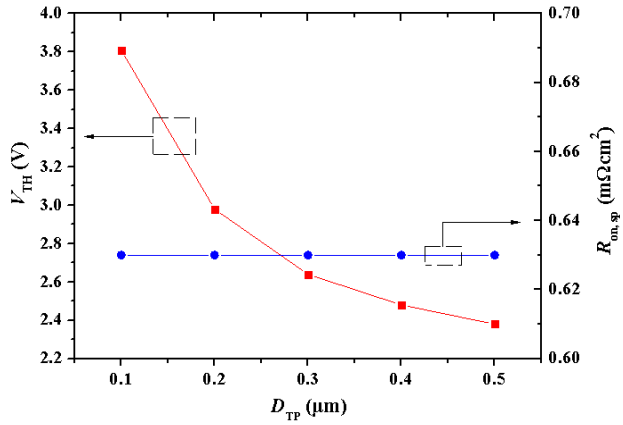

FIGURE 12. The relationship between V_{TH}, $R_{on,sp}$ and D_{TP} while $N_{aTP} = 5 \times 10^{17}$ cm^{-3}.

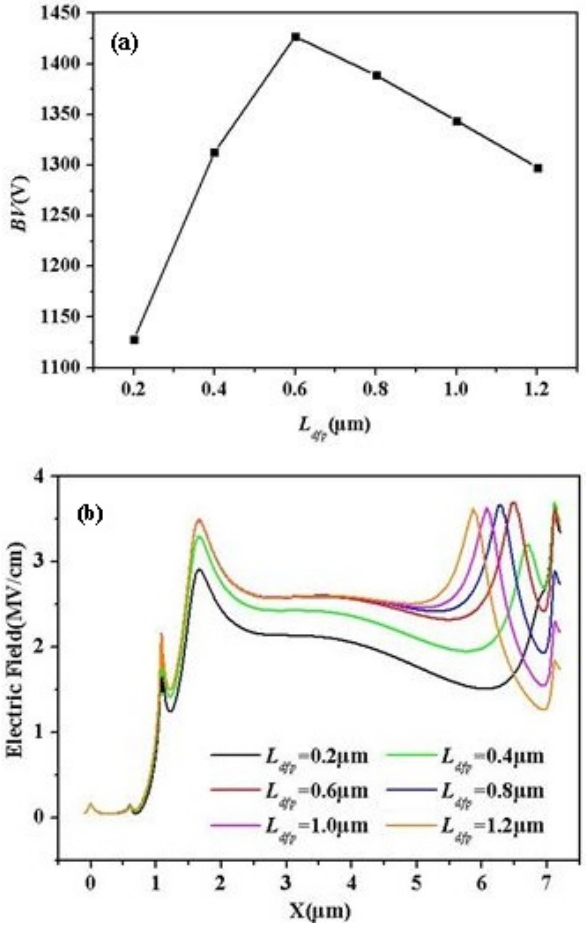

FIGURE 13. (a) The relationship between L_{dfp} and *BV* (b) The relationship between L_{dfp} and the surface electric field distribution.

leakage current by a higher acceptor trap. Consequently, as shown in Fig. 4, the electric field distribution and breakdown voltage were improved.

The results presented in Fig. 11 show that *BV* increased with the increase in N_{aTP}, Also, as it can be seen in Fig 10(c), the TP at lower N_{aTP} could not act as a current blocking layer, so the leakage current still could pass through the middle buffer layer; meanwhile, when the TP was far away from the channel layer, i.e., it was getting closer to the BP, the ability to block the leakage current in the middle buffer layer decreased as displayed in Fig 10(d); then, the device breakdown occurs in advance. Furthermore, the results in Fig. 11 also indicate that the highest value of *BV* was 1389 V while D_{TP} was 0.2 μm and N_{aTP} was 5×10^{17} cm^{-3}, which was higher than 1312 V in [25].

As shown in Fig. 12, the change of D_{TP} almost did not affect $R_{on,sp}$, which could guarantee good conduction characteristics, but in the other hand, V_{TH} increased when the TP got close to the gate.

Finally, we discusses and corrects the length of the drain plate, which can be seen in Fig 13(a). It shows that when L_{dfp} is equal to 0.6 μm, the breakdown voltage and *BFOM* of the device can reach the maximum of 1427V and 3.23 GW•cm^{-2}. And Fig 13(b) shows the relationship between the length of the drain field plate and the surface electric field distribution.

IV. CONCLUSION

In this paper, we presented a high *BFOM* normally-off AlGaN/GaN MISFET with the double P-buried layers. To shows the improvement in the MISFET characteristics, we compared three different MISFETs, i.e., the C-MISFET, the BP-MISFET and the DP-MISFET, and simulated the properties of these devices using the common physical models. Moreover, we analyzed the influence of the BP and the TP by discussing and optimizing their values. The optimized MISFET exhibited a strong current drive capability, a high-power *BFOM* of 3.23 GW• cm^{-2}, *BV* of 1427 V, and $R_{on,sp}$ of 0.63 mΩ• cm^2, thus, the proposed structure showed good performance.

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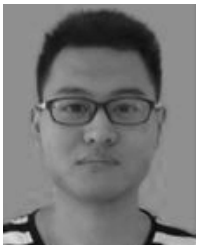

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